Pergamon

Scand. J. Mgmt, Vol. 12, No. 4, pp. 437–461, 1996

0956–5221/96 $15.00 + 0.00

S0956-5221(96)00001-2

STRATEGIC INTERACTIONS IN DRAM AND RISC TECHNOLOGY: A NETWORK APPROACH

GEERT DUYSTERS and WIM VANHAVERBEKE

Department of Management Sciences, University of Limburg, Maastricht, The Netherlands

(*First received August* 1994; *accepted in revised form September* 1995)

Abstract — Interorganizational cooperation in some high-tech industries is no longer confined to two-company alliances, but entails industry-wide alliance networks. This article examines how industry analysis and network analysis can be combined to provide a thorough understanding of how network positions, and the overall network structure, may play a part in cooperative strategies. Industry analysis can indicate which properties of the network structure and network positions are congruent with the firms' cooperative strategies, but tells us little about how these network characteristics can be measured. Network analysis provides such measures, which can then be used as feedback in the industry analysis. The article illustrates this approach by comparing the alliance networks associated with the DRAM and RISC microprocessor technologies.

Key words: Strategic allowances networks, technological cooperation, microelectronics, network analysis.

1. INTRODUCTION

Cooperative agreements have long been disregarded in business literature. Only recently have organizational theorists devoted more attention to interorganizational relationships as part of corporate strategies. The concept of interorganizational relationships was introduced in organizational literature as far back as the late 1960s by Evan (1966) and Warren (1967) among others, but it was the rocketing numbers of cooperative agreements in the 1980s that made way for a growing body of literature on the development, structure and use of such agreements (Contractor and Lorange, 1988; Hagedoorn, 1990; Haklisch, 1986, 1989; Harrigan, 1985; Mowery, 1988; Parkhe, 1991; Ring and Van de Ven, 1994). In this paper we will use the term cooperation to denote cooperative agreements between partners who are not connected through (majority) ownership. A cooperative agreement can be seen as an agreement which is positioned between two extremes: arm's length transactions on the one hand and the merger of two firms on the other (Ring and Van de Ven, 1992).

With a few notable exceptions (see, e.g. Forsgren and Johanson, 1992; Gomes-Casseres, 1994; Hagedoorn and Schakenraad, 1990, 1992, 1993; Håkansson, 1989; Johanson *et al.*, 1994; Nohria and Garcia-Pont, 1991; Nohria and Eccles, 1992) agreements among companies have been studied on a dyadic or firm level. However, in high-tech industries where almost all incumbents are linked to each other by means of a network of cooperative agreements, an analysis at the level of the individual players or alliances is not appropriate to understand the strategic value of cooperative strategies. In an environment which is characterized by a mix of cooperation and

competition and in which firms are embedded in a set of relationships, strategic action cannot be analysed properly at the individual-firm or dyadic level. Rather, such an analysis involves part or even the whole network to which the firm is linked. Competition no longer occurs between individual companies, but between groups of allies, and the strategic position of the company within and among alliance groups is a source of competitive advantage alongside the traditional company-based competencies. The evaluation of the power of organizations in a network thus requires an analysis of their position in the network, their links with other players and their ability to "control" flows of information.

The paper combines industry analysis and network analysis in order to achieve a thorough understanding of how network positions and the overall network structure can play a part in cooperative strategies in industries characterized by industry-wide strategic alliance (SA) networks. The combination is an obvious choice because the two analyses are complementary. Industry analysis analyses the underlying corporate strategies behind the cooperation between firms and unravels the reasons why there are competitive advantages to be gained from cooperation and group-based competition. All this means that companies' positions within networks, and the overall network structure, are important strategic variables. Industry analysis consequently indicates which properties of the network structure and of the network positions of the allies are congruent with these cooperative strategies, but it leaves us in the dark about how to measure these variables. We therefore require an additional framework which specifically addresses these issues. One of the most promising statistical techniques to analyse the structure of SA networks is network analysis.* Network analytical tools provide reliable quantitative measures about network structures and network positions, and should thus be a valuable instrument to test whether inter-industry differences in competitive and cooperative strategies result in differences between network structures and network positions. In this way, network analysis enriches and complements the results of the industry analysis. Hence, industry analysis and network analysis have to be used jointly when networks of SAs are important as part of the strategy of the collaborating firms.

Values for network-analytic measures are not always readily interpretable within a strategic context. The relevance of network analysis within this context is thus best illustrated by a comparison between two networks with different characteristics. For this purpose, this paper focuses on the network-analytical similarities and differences between two networks of strategic alliances related to integrated circuits (IC) technologies — the DRAM chip and the RISC microprocessor. We limited ourselves to these two SA networks for three reasons. First, they can be clearly defined as technologies which lead to an identifiable product (DRAM memory chips and RISC microprocessors).† Second, these markets are among the few which have a dense network of cooperative agreements among a limited number of players — there are 43 firms in the RISC network and 72 in the DRAM network.‡ Third, firms in the RISC market establish cooperative agreements for *different reasons* from those applying in the DRAM market. DRAM manufac-

*Network analysis has only recently been applied to industrial networks. For an example, see Nohria and Garcia-Pont (1991). For more detailed accounts of interorganizational industrial networks, see Håkansson (1989) and Axelsson and Easton (1992).

†Most studies on strategic alliance networks focus on industries or markets, but we prefer to highlight networks around a particular technology because technology-based strategic alliances cut across industry boundaries.

‡The restriction on the number of players is dictated by the calculation capabilities of software packages for network analysis, and by the need to restrict the number of players in order to work out a credible industry analysis that copes with cooperative strategies.

turers are well known for teaming up in order to deal with their enormous R&D costs, short life cycles and steep learning curves.

RISC manufacturers, on the other hand, have been found to engage in cooperative agreements and group-based competition in order to establish a new industry standard. Differences between industries as regards competitive and cooperative strategies lead to differences in network structure and in the relative network positions of the allies. By comparing the network-analytical statistics of both networks, we could perhaps learn something about the way different competitive drivers and cooperative strategies are translated into differences in the network structure and the network positions of the focal partners.

This paper is organized as follows. The second section describes the two technologies and the role of competitive and cooperative strategies in both cases. In the third section we describe the data and present the networks in a graphic form. The network analysis is displayed in the fourth section. We focus on various measures of centrality, and apply them to both technologies. The use of these centrality measures provides us with a better understanding of the position of individual companies in the overall network. Finally, the fifth section offers a summary and some conclusions.

2. DRAM AND RISC TECHNOLOGIES

Before proceeding with the network analysis it is important to understand the role of technology-related strategic alliances in a particular industry. In this section we therefore provide a short description of the two technologies, followed by an analysis of their role in different segments of the electronics industry, and the reasons why companies set up strategic alliance networks.

2.1. Strategic alliances in the DRAM market

The DRAM (Dynamic Random Access Memory) is a particular general-purpose kind of memory chip, which continues to be the product that turns the IC industry and which accounts for as much as a fifth of the IC industry as a whole. Furthermore, DRAMs are generally considered as a process-technology driver from which innovations can be readily diffused into other segments of the IC industry such as the microcontroller, microprocessor and ASIC markets. Their strategic value is thus much greater than their market share in the IC industry would suggest. The production of DRAMs has been used as an example to highlight the dynamic relationship between innovative leads, economies of scale, learning by doing, oligopolistic exploitation of these advantages, and international competition (Krugman, 1990; Bowen, 1991). Strategic alliances are frequently used as a tool in achieving one of these competitive advantages.

One of the key characteristics of the semiconductor industry is its *extremely rapid pace of technological change*. The trend towards ever-increasing integration levels puts continuous pressure on processing technology requirements at the different stages in the manufacturing process. As a result, DRAM manufacturers have to spend huge amounts of money on R&D to realize these technological developments, or even just to keep up with the rapid pace of technological advances in the memory chips market. R&D budgets typically fluctuate around 15% of company sales. Forecasts predict that R&D costs (and manufacturing plant costs) will soar with each introduction of a new DRAM generation. The escalating R&D and investment costs are one of the main reasons why DRAM manufacturers — even the largest ones — are teaming up to develop and produce future DRAM generations.

DRAMs are mass-produced chips used in many electronic products, which have to be compatible with the industry standards demanded by consumers and software suppliers. Consequently, DRAMs are commodity items for which pricing strategies are extremely important as a competitive factor. The pricing of DRAMs is a complex process depending on a set of key features of the semiconductor industry, which determine the cost structure.

First, the DRAM market is characterized by the *succession of different families* of DRAMs with ever-increasing reliability and performance. The shortness of the production cycle makes *dynamic-scale economies* important in two ways. First, the continually rising R&D and capital costs cannot be amortized by cumulative production over many years.* Second, the DRAM manufacturing processes are characterized by significant *learning* effects, which are the result of potential improvements in the yield rate.† Since the product cycles are short, DRAM manufacturers always find themselves at the early, steep stage of the learning curve.

In memory chips the highest profits come in the first year of the new chip generation, when supply is tight and demand high. "Time to market" is thus an important element for a successful strategy in this industry: it has become the driving force after the recent international technological cooperative agreements between major DRAM producers. Although the product life cycle of DRAMs is short, their development cycle is long.‡ Consequently, *processing technology* has been a major source of technology transfer agreements between technological leaders and laggards in the DRAM market. Leading Japanese DRAM manufacturers have also shared their competence in CMOS manufacturing technology in exchange for design capabilities regarding microprocessors and other logic devices, in which U.S. firms usually excel (Haklisch, 1986; Chesnais, 1988; ICE, 1993).

The race between competitors to be first in the market with the next generation of DRAMs causes periods of over-production. The cyclical nature of the industry in combination with the enormous sunk costs which prevent incumbents from exiting, makes the DRAM market a very risky business. Dumping practices are very likely to occur during slumps, as increasing volumes make it possible to retrieve part of the sunk costs and to move down along the learning curve.

Many of the vertically-integrated companies in the electronics industry invest in DRAMs not because it is a profitable business but for strategic reasons:§ the volume of production required by DRAMs propels them into the position of technology driver, stimulating (and funding the huge depreciation costs of) the advances in IC manufacturing technologies, which can in turn be applied to the production of other ICs. The volume production of DRAMs allows a chip manufacturer to use the latest DRAM technology for the production of other ICs, while at the same time reducing the unit cost of the latter (Methé, 1991).

Market transactions between DRAM suppliers and system producers have often been tense. Problems in the market for standard DRAMs have been alleviated by means of *(mutual) second-sourcing agreements*, with a view to improving market transactions between IC manufacturers and electronic system companies. The *raison d'être* of second-sourcing agreements in the DRAM

*R&D and capital costs range from 30 to 45% of DRAM sales (Mouline and Santucci, 1992, p. 25).
†On the introduction of new DRAM family, average yield does not exceed 15%, whereas most manufacturers achieve an 85% yield after 24 months (Mouline and Santucci, 1992, p. 26).
‡It can take 10 years to move a generation of chips from the development stage through to volume production.
§The Nomura Research Institute (1992) calculated that return on investment in semiconductor operations had been less than 1% in the last 4 years.

market is to avoid market power being exercised by one or a few DRAM suppliers which could control industry output (Collins and Doorley, 1991). They are an interesting instrument for industry leaders who want to free their human and financial resources for newer and more specialized ICs, while assuring themselves of a reliable second source.

In brief, we can conclude that strategic alliances in the field of DRAM technology do *not directly* influence the competitive position of DRAM manufacturers. The link is *indirect*: strategic alliances are established in order to improve the *technological position* of the partners, which is likely in turn to improve their *competitive position*. Technological progress is so fast and R&D costs are so huge, that even the biggest partners are teaming up and sharing technological skills, although technological collaboration is usually followed by fierce competition once the new DRAM generation is commercialized. Consequently, we expect to find an SA network which is relatively open, i.e. one in which important companies cannot occupy network positions which allow them to get "control" over the network. In the next section, we focus on the SA network associated with the RISC microprocessor technology, in which companies try to improve their competitive position *directly* by means of cooperative agreements.

2.2. Strategic alliances in the RISC microprocessor market

RISC (Reduced Instruction Set Computer) microprocessors are relatively new and are used mainly in workstations. Recently they have become a rising threat to established industry standards in the PC market as well; Intel-based CISC (Complex Instruction Set Computer) chip designs are said to be slower than the new RISC architectures and the MS-DOS operating system may face competition from the Unix operating system (OS), which up to now has been a common OS for RISC-based workstations.* The quest to establish new standards is one of the main reasons why RISC-designing companies are teaming up with other companies (Khazam and Mowery, 1994). Ever since the RISC microprocessor technology became popular in the late eighties, a thickening web of strategic alliances, joint ventures, technology-licensing deals and consortiums has been established between IC manufacturers, computer makers and software writers.

In order to evaluate RISC microprocessor technology, we first specify RISC architectures and their role in microprocessor and computer markets. We then investigate the impact of an industry standard for RISC technology on the microprocessor and computer markets.† Special attention will be paid to the interaction between these markets, and to the relation between the search for a new industry standard and the establishment of SAs. Finally, some conclusions will be drawn and hypotheses formulated regarding the emergence of the SA network in connection with the RISC technology.

In order to understand why computer manufacturers, software writers and companies with a proprietary RISC architecture are eager to get control over the RISC-based computer markets, we have to look at the conditions for competitive success in the information technology industry

*RISC microprocessors offer significant cost/performance advantages over computers based on the traditional CISC microprocessors. The technical characteristics of RISC designs translate themselves into economic benefits compared with CISC designs. Reduced and simplified instructions mean simpler circuits that need fewer transistors. Besides the fact that the relatively small and simple control unit in the RISC design makes the microprocessor faster, it also implies a reduction in the overall design costs and design time, reducing the probability that the end product will be obsolete by the time the design is completed. At the same time, the number of design errors is reduced, thus improving reliability. Moreover, it is easier to locate and correct errors.

†We omitted the implications of the introduction of RISC-microprocessors on the software market in order to keep the article to a reasonable length.

in general and the computer industry in particular. In almost all cases, architectures in open systems are proprietary,* and they generate huge profits for a handful of companies which supply components defining and controlling the critical functions of the computer or electronic system. Typical architectural standard-setters are microprocessor designers (Sun and MIPS in RISC, Intel in CISC), and operating system vendors (Sun's or IBM's version of UNIX and Microsoft's DOS or Windows NT). While most microprocessor and computer manufacturers have a hard time, firms which command such critical architectural control points as the system software and the microprocessor design, have generous after-tax margins.

Many IT companies are developing (cooperative) strategies in face of the emergence of RISC technology. We discuss these strategies in several steps. First, we focus on the microprocessor market and then look at the implications for the computer industry. After this, we turn to the battle for dominance between different operating systems. Finally, conclusions will be drawn with respect to the cooperative strategies and the SA network associated with RISC technology.

Commercial RISC designs began to appear in the late eighties and RISC chips are still used primarily in workstations, which represent only a fraction of the computer industry.† But RISC chips have an excellent growth potential because workstations are the fastest growing sector of the computer market. Moreover, RISC-based computers tend to penetrate a whole range of submarkets in the computer industry. On the one hand, flexible workstation networks based on multiple microprocessors are making inroads into minicomputers and mainframes, as workstations built from RISC chips can perform the same computation work for a fraction of the cost when using a mainframe computer. On the other hand, further price reductions for RISC chips will open up the huge PC market.

Consequently, it is not surprising that players from outside the workstation and RISC chip markets are interested in RISC architectures. In 1992 several RISC designs were competing for market shares (see table in Appendix B). Since RISC chips have the potential for use in a wide range of computers, the emergence of an industry standard for RISC microprocessors could eventually supplant the aging PC standard, which is based on Intel Corp CISC chips. The establishment of a new industry standard creates positive network externalities and generates benefits for computer users, RISC manufacturers, and RISC-based computer makers. Thus, firms with a proprietary RISC architecture are now aggressively promoting their architecture by means of *free licensing and other cooperative agreements* (see also Kukalis and Kanazawa, 1993; Garud and Kumaraswamy, 1993).

Two early movers in the RISC market were the workstation sellers MIPS Computer Systems Inc and its larger rival Sun Microsystems Inc. They pushed hard for clones, to get their architecture as the basis for a new industry standard. Sun's strategy is to license freely the design of its SPARC microprocessor, inviting other companies to clone its machines. Such licensing agreements are interesting to all the agents involved. They increase the probability of SPARC becoming an industry standard, which creates a larger market share and thus offsets the negative effects of increased competition between Sun and its clone makers.‡ The latter gain access to the

*It is wrong to think that in open systems proprietary architecture control is no longer possible or desirable. Morris and Ferguson (1993, p. 89) argue that the opposite is true, as architectural coherence becomes even more important in an open systems era and non-proprietary system architectures have proved to be static and unable to keep up with rapid technological changes. Proprietary architectures, in contrast, are under constant competitive attack and must be vigorously defended. This dynamic engenders a very rapid rate of technological improvement.

†According to Dataquest Inc. 387,000 RISC chips were sold in 1990 by all manufacturers, whereas Intel Corp's 386 and 486 CISC chips, used in the PC market, totalled 7.5 million in unit sales.

‡Other industry experts, however, note that Sun and MIPS could be eclipsed by clone-makers such as Fujitsu, Mitsubishi and Matsushita, which could eventually undercut prices. These clone-makers are large diversified firms, which can easily cross-subsidize their RISC-based computers (see Ruhl, 1988).

technology, while multiple licence agreements operate at the same time as second sourcing agreements, which avoids single-supplier domination and reduces the risk of chip shortages when demand suddenly rises. In order to slow down acceptance of Sun's SPARC architecture, MIPS and Compaq spearheaded the formation of a group of 21 companies called ACE (Advanced Computer Environment).* The ACE systems would use the MIPS 64-bit RISC microprocessor (R4000) as the heart of their systems. But many things have gone wrong since ACE began in late 1990 and the ACE consortium lost its cohesiveness. In the end, MIPS abandoned its neutrality when it agreed to a buy-out by workstation maker Silicon Graphic Inc (ICE, 1993; Hof, 1992b).

These aggressive strategies on the part of both companies triggered reactions from the other players with a proprietary RISC design. Hewlett–Packard formed PRO, the Precision RISC Organization, to promote and coordinate the use of its PA-RISC architecture by developing standards for hardware and software. IBM and Motorola, who both have their own RISC architecture, joined forces to develop the PowerPC which will power a range of products from notebooks to supercomputers. The venture between Apple, IBM, and Motorola is a hedging strategy by Apple and IBM against the growing threat of RISC chips for the PC market. DEC was late in developing its own Alpha RISC chip, and it still has to look for partners to promote and coordinate the use of its architecture.

The growth of the workstation market and the attempts to standardize RISC architectures are threatening the comfortable position of Intel Corp in the CISC-based microprocessor market. If RISC-based workstations become more popular and penetrate the PC market, RISC chip producers may become serious challengers of Intel. Although Intel produces its own i860 RISC chips, its main answer to the growing RISC-chip threat consisted of speeding up the introduction of new families of CISC-based microprocessors. The workstation market is only about one-tenth the size of the PC market and is thus not important to Intel's sales figures. However, it is an important market in the strategic sense, because there is always the threat that RISC chips could make incursions into the PC market. The future market position of Intel Corp depends on the performance of its future CISC families in relation to that of future RISC microprocessors (Rice, 1992; Hof, 1992a; Port, 1992a, b).

Up until now, no RISC chip has established itself as a new standard. The fact that there is no industry leader which could impose its own design as an industry standard, implies that firms with proprietary RISC architectures have licensed their technology freely in order to develop an "installed base", which can in turn give them a competitive advantage over their rivals. As a result, the competition for market share in the computer industry is a *direct* consequence of the competition for dominance in the RISC chip market. This competition for market share appeared first in the workstation market, but it is shifting towards other segments of the computer industry as the popularity and capabilities of RISC microprocessors are growing. The table in Appendix C shows how different microprocessor manufacturers have to win the commitment of a number of workstation manufacturers in order to have a substantial market share.

Strategic alliances in the young RISC technology are largely determined by the search for compatible RISC architectures. Since there is no industry leader to impose its RISC architecture as an industry standard, different companies with competing architectures establish a network of strategic alliances (mainly (cross-)licensing agreements and consortiums) with IC manu-

*ACE members included MIPS, Compaq, DEC, NEC, Microsoft, Acer, CDC, Olivetti, Prime, Pyramid, Siemens/Nixdorf, Bull, Silicon Graphics, Sony, Sumitomo, Tandem, Wang, Zenith Data Systems and numerous other companies.

facturers, computer makers and software writers to ensure their customer base. The result is that the firms involved in RISC technology are grouped into "strategic blocks" around the different proprietary RISC architectures. The block with the largest (combined) consumer base has the best chance of imposing its RISC architecture as the industry standard of the future.

Since the relation between strategic alliances and competition for market share in the workstation market is a *direct* one, we expect that focal partners in the SA network in the RISC market will have a relatively tight grip on the SA network. This is in contrast to the DRAM network where the link between SAs and market share is only an *indirect* one and the search for a dominant position in the network is thus less compelling.

The authors expect that the nature of the linkage between cooperative agreements and market share competition will have implications for the structure of the strategic alliance network. This topic is addressed in the Sections 3 and 4.

3. DATA AND GRAPHICAL REPRESENTATION

3.1. The data

The data about cooperative agreements related to the RISC and the DRAM technologies are extracted from the MERIT-CATI database. This database contains information on almost 10,000 cooperative agreements involving some 5000 different parent companies active in biotechnology, information technology, new materials or other "non-core" technologies.

The cooperative agreements included in this network analysis all started between 1980 and 1989.* The eighties were a turbulent period for cooperative agreements in the DRAM market, and the RISC technology took off only after 1985. At the time this paper was written, the CATI data bank had not been systematically upgraded for alliances that were established after 1989. The study does not thus pretend to describe the actual situation in either of the markets. The data sets for the following network analysis are valued graphs, where the cells of the matrices represent the frequency of a (specified kind) of cooperative agreement between two actors. However, this data may have been transformed, since some network procedures require binary and/or symmetric data.

3.2. A graphical representation of the networks

The best way to get an overview of the two cooperative networks is to plot them as in Figs 1 and 2. The full company name and nationality of each firm are given in Appendix D.

The two graphs reveal both similarities and differences. Both show that all firms — with the exception of a few pairwise isolates — are linked to each other in a direct or indirect way. As a result, the network positions of the individual firms change all the time, not only because of their own actions, but also because of changes in their counterparts' positions and in those of third parties with

*Alliances in the networks under study are composed of different forms of cooperation. In the CATI database we discriminate between seven basic forms of cooperative agreement: (a) The category "Joint R&D" which embraces both joint research pacts and joint development agreements. (b) "Customer–supplier relationships" which include R&D contracts, co-production contracts, co-makership contracts and customer–supplier partnerships. (c) "Technical exchange agreements" (two-directional) which include technology sharing, mutual second-sourcing and cross-licensing. (d) "One-directional technology flow" agreements which consists of licensing and second sourcing agreements. (e) "Standardization and bidding consortia." Equity agreements include (f) "equity joint ventures" which enclose both the classical joint ventures as well as the research corporations, and finally (g) "equity ownership."

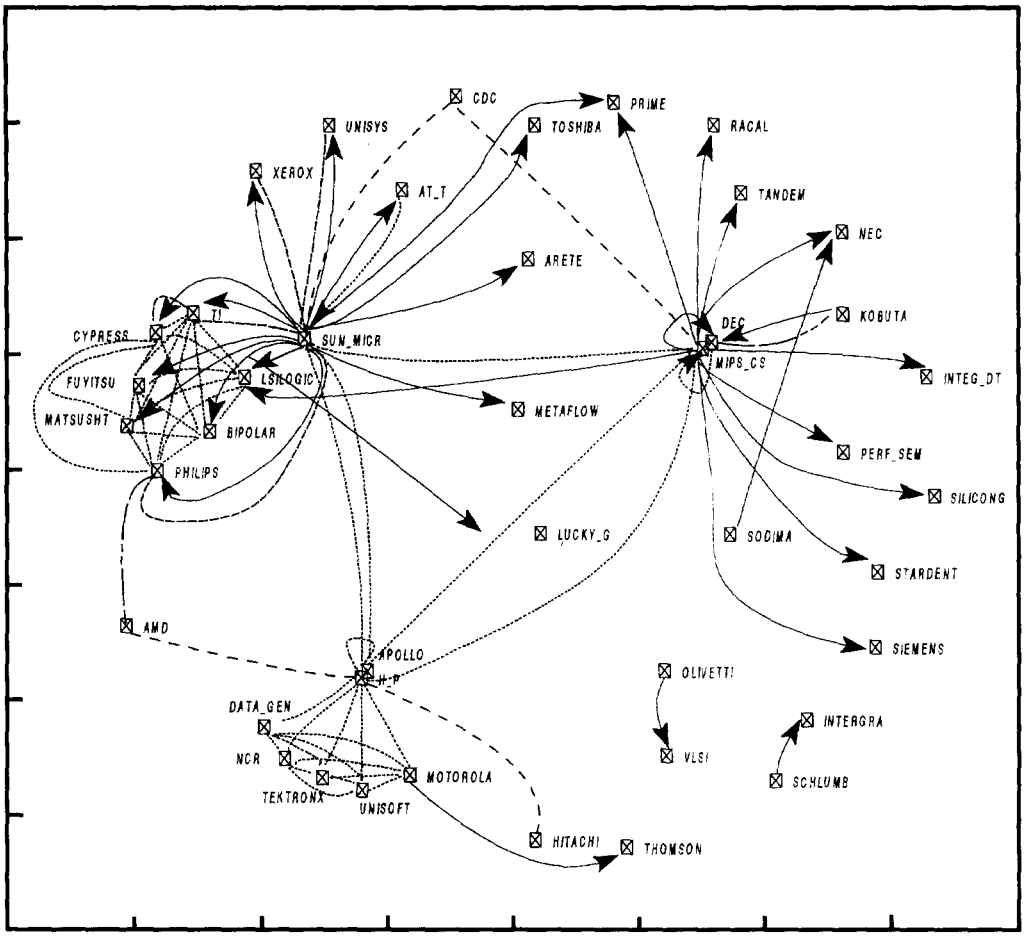

Fig. 1. Cooperative agreements in RISC technology: 1980–1989. ..., Consortia; – –, joint R&D; ---, technology exchange; — - -, customer–supplier relationship; —>, one-directional technology flow; and ··>, direct investment.

whom they have no direct relationships (Axelsson and Easton, 1992, p. 213).* The positions of the companies in a network form the base for their competitive and cooperative strategies.

The two networks are also structured differently. Figure 1 shows that the RISC network is built around three focal players. The two major players are the arch-rivals, MIPS Computer Systems and Sun Microsystems. Hewlett–Packard seems to represent the focal actor of a third but smaller cluster of firms. The DRAM network is more like a "chain", in which most companies are linked one to one. Although less obviously than in the RISC market, there are a number of subgroups in this network too: the group around the European big three, Siemens, Philips and SGS-Thomson; the U.S. Memories Consortium including the major American companies; Texas Instruments (and AT&T) with its South Korean and Japanese partners; and, finally the group including

*Although the two cooperative networks are industry-wide, they are still sparse: the density of the adjacency matrix that simultaneously accounts for all ties among the actors is 0.087 for the RISC technology and 0.043 for the DRAM technology. This is a general characteristic of industrial networks and can be partly explained by the exclusiveness of many cooperation deals and the relative inefficiency — at least in the micro-electronics industry — of industry-wide consortia (Boulton *et al.*, 1992; Burrows, 1992; OECD, 1991; Vickery, 1992).

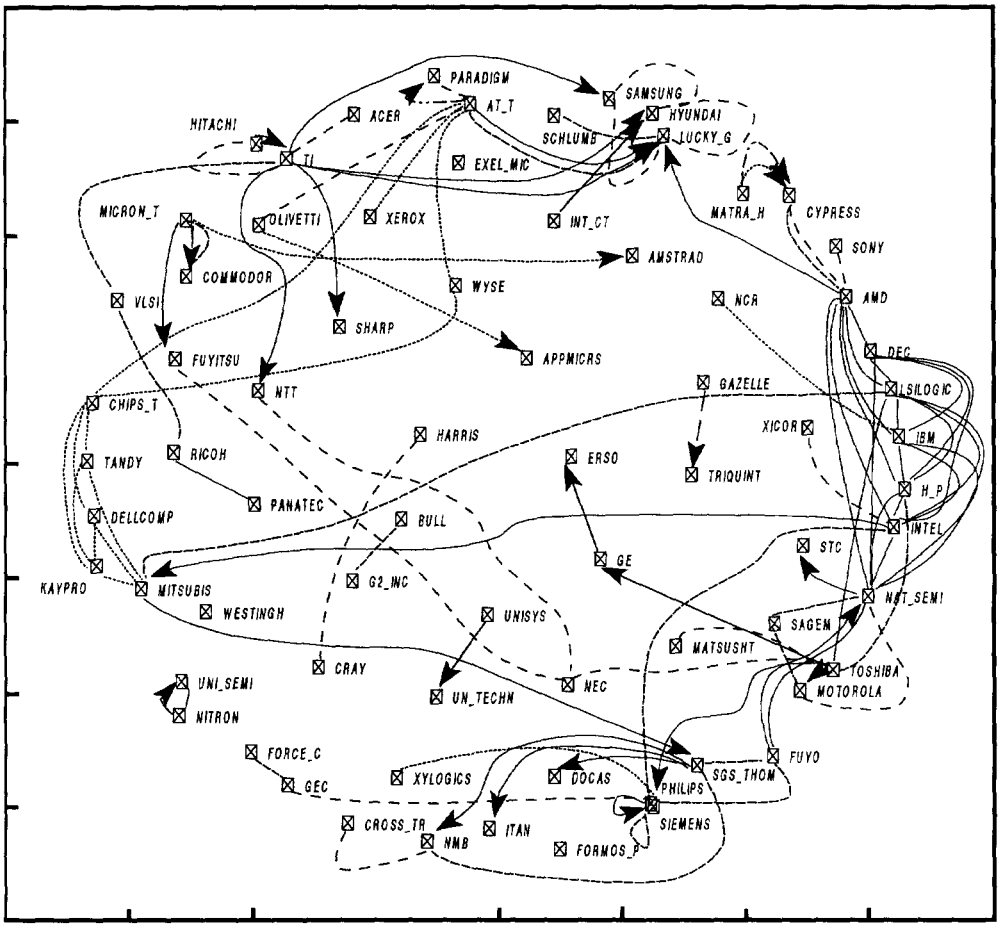

Fig. 2. Cooperative agreements in DRAM technology: 1980–1989.——, Equity JV; – – –, joint R&D; - - -, technology exchange; . . ., customer–supplier relationship; —>, one-directional technology flow; and ··>, direct investment.

Mitsubishi. Mitsubishi and Intel developed cooperative agreements that cut across the whole network, which gives them freedom of action since they are not locked into any one of the subgroups.

It is also important to mention the existence of several consortiums which determine to a considerable extent the shape of the network in both markets. There were three consortia in the RISC market during the late eighties: (a) the Sparc Vendor Council,* (b) the Systems Performance Evaluation Cooperation (SPEC),† and the 88-Open.‡ They were started in order to establish industry standards and to increase compatibility primarily between allies, but also between rivals. The consortia in the DRAM market are mostly joint development agreements. In the early

*The Sparc Vendor Council includes Bipolar, Fujitsu, LSI Logic, Texas Instruments, Cypress, Matsushia and Philips. All these firms have licensing agreements with Sun Microsystems for its SPARC technology.

†SPEC intended to develop industry-wide standard benchmarks for (32-bits) RISC architecture computers. It includes the major companies — Sun Microsystems, MIPS Computer Systems, Apollo and Hewlett–Packard.

‡The 88-Open Consortium is a consortium of computer suppliers supporting Motorola's 88000 RISC processors. It includes Motorola, Unisoft, Apollo, Hewlett–Packard, NCR, Tektronix and Data General, and it intends to foster source compatibility for the 88000 RISC processors.

eighties NTT, Fujitsu and NEC had agreements to develop the 128 Kb and the 256 Kb DRAM chip. Similar agreements existed between Samsung, Hyundai and Lucky Goldstar in the late eighties in order to develop the 4 Mb and 16 Mb DRAM chip. There were also consortia between American DRAM producers. One of them was US Memories* which was established in 1989, but was broken up a year later. Another U.S. consortium in Sematech which tries to improve semiconductor manufacturing technologies. Since Sematech's interest is directed towards the semiconductor equipment industry rather than the DRAM market itself, it is not included in the DRAM SA network.

4. CENTRALITY MEASURES

In this section different measures of point centrality and graph centrality are shown and discussed for both markets. Examining the point centralities is one way of getting reliable and quantified measures of the position of each partner with respect to the overall structure of the network.† A comparison of centrality measures between the RISC and the DRAM SA networks will indicate possible differences in the value and strategic use of alliances in both networks.

4.1. Point centrality and graph centrality measures

Point centrality can be measured in several ways.‡ A first indicator (C_D) measures point centrality as a function of the degree of a point§ — the mathematical formulae for the centrality measures are shown in Appendix A. A second indicator, closeness-based point centrality (C_C), measures the centrality of a point by summing the geodesic distances from that point to all other points in the graph.¶ Another centrality measure, the so-called betweenness centrality (C_B), is based upon the frequency with which a point falls between pairs of other points on geodesic paths connecting them.‖

In the case of valued graphs there is also a centrality measure based upon maximal flow betweenness (C_P): the information flow between two points is not the direct flow between adjacent points, but the overall flow between pairs of points along all the paths that connect them. The information flow between two points thus depends on the capacity of all the channels of communication on all the paths that connect them. A channel is defined in turn as the value of the connection linking two points, and it determines the capacity or maximum amount of information that can be passed between them.**

Graph centralization, or the centrality of an entire network, measures the tendency of a single point to be more central than all other points in the network. Consequently, graph centrality measures are based on differences in point centralities and, more precisely, on the difference

*US Memories included IBM, Hewlett–Packard, DEC, Intel, National Semiconductor, AMD and LSI Logic.

†Depending on the research questions, other network analytical tools can also be used.

‡We confine our attention to a few centrality measures. Centrality measures based on eigenvectors, as developed by Bonacich (1972), and the Stephenson and Zelen (1989) information centrality measure have been left out of the following analysis.

§The degree of a point, p_i, is the count of the number of other points, p_j $(i \neq j)$, to which it is adjacent and with which it is therefore in direct contact (Freeman, 1979, p. 219).

¶The geodesic is the shortest path linking a given pair of points.

‖Degree centrality can handle both symmetric and asymmetric valued graphs. In this section we treat a matrix in a symmetric way, but this will change when we examine in- and out-degrees. Closeness centrality is always based on symmetric binary graphs, while betweenness centrality can handle both symmetric and asymmetric binary graphs.

**Flow betweenness works with valued graphs. (These indicators are explained in the following paragraphs.) For further details on this centrality measure, see Freeman *et al.* (1991).

between the centrality of the most central point and that of all others (Freeman, 1979, p. 227) — see formula equation A9 in Appendix A. In other words, graph centralization measures the average difference between the network positions of focal and peripheral players.

4.2. Centrality in the RISC network

The point and graph centrality measures of the strategic alliances network in the RISC technology are shown in Table 1. These measures are relative or normalized measures, so that comparison between the RISC and DRAM SA networks is straightforward.

The simplest conception of point centrality is C_D, i.e. centrality as a function of the degree of a point. A point with a high C_D value is considered to be "in the thick of things", so that in some sense it is a focal point playing an essential role in the network. A point with a low degree is isolated from most other actors in the network and will play only a marginal role. The two firms with a high degree centrality are MIPS Computer Systems Inc and Sun Microsystems Inc. Their focal position is the result of their active policy of RISC-architecture licensing. Other firms with a relatively high C_D-value are Hewlett–Packard, who acquired Apollo in 1990, Texas Instruments, LSI Logic and Philips. The last three companies belong to the "cluster" of firms that have a licensing agreement with Sun Microsystems. The high ranking of these firms is an indication of the network density of that "cluster". Hewlett–Packard/Apollo, on the other hand, is the focal partner of a group of firms that constitute a third cluster beside those of MIPS Computer Systems and Sun Microsystems. Most licensees are located at the lower part of Table 2 and play only a marginal role in the network.

The second column in Table 1 represents the closeness-based index: the centrality of a point is measured by summing the geodesic distances from that point to all other points in a graph. Again, MIPS Computer Systems, Sun Microsystems, and Hewlett–Packard have the highest closeness centralities, but their value is of the same order of that of other companies. This implies that the RISC alliance network exhibits a number of loops or circles; the central loop is the triangle between Sun, MIPS and Hewlett–Packard, but other companies also have direct links with companies in another cluster. The result is that the variance of the distance of the geodesics across the firms is relatively small. Exceptions are Olivetti, Schlumberger, VLSI and Intergraph, which have an extremely low value for this indicator, as their alliances are isolated from the main network. The low variance in the C_C values are mainly the result of the SPEC consortium which intended to develop industry-wide standard benchmarks for (32-bits) RISC architecture computers. It involves an agreement between the major companies — Sun Microsystems, MIPS Computer Systems, Apollo and Hewlett–Packard — and in this way it transforms the three strategic blocks into a connected network.

The betweenness centrality index is based on the frequency with which a company lands between pairs of other companies on the geodesic path between them. A firm that lands on the shortest path between two other firms, has a potential for control. Sun Microsystems, MIPS Computer Systems and Hewlett–Packard have a clear potential for such control. Their value is even higher for C_F, i.e. when we take all paths into account, which confirms in turn the presence of cycles in the network.* Some firms have bridge functions, such as CDC and LSI-Logic

*"Connected graphs without cycles have only one path — a single geodesic — linking any pair of points. When there are no alternative paths, the counts tabulated by the betweenness measures must equal the flows of the flow-based measures. However, when cycles are present, C_F and C_B will differ. This is because the C_B measures record flow only along geodesics, while the C_F measures are responsive to *all* paths along which information can flow. The two kinds of measures will therefore produce different results for any graph that contains any cycles." (Freeman *et al.*, 1991, pp. 150–151).

Table 1. Point and network centrality measures for the RISC microprocessor technology

Company*	C_D	C_C	C_B	C_F
SUN-MICR	61.90	18.10	25.53	30.90
MIPS-CS	42.86	18.03	18.35	36.58
H-P	26.19	17.57	12.22	24.22
TI	23.81	16.15	2.57	6.19
APOLLO	21.43	17.43	6.51	11.86
LSILOGIC	21.43	16.87	1.63	2.15
PHILIPS	21.43	16.15	2.45	9.92
BIPOLAR	19.05	16.09	1.12	1.99
CYPRESS	19.05	16.09	0.02	1.52
FUJITSU	19.05	16.09	0.02	1.14
MATSUSHT	19.05	16.09	0.02	1.40
MOTOROLA	16.67	15.61	1.34	2.46
DATA GEN	14.29	15.56	0.00	1.42
NCR	14.29	15.56	0.00	1.42
TEKTRONX	14.29	15.56	0.00	1.42
UNISOFT	14.29	15.56	0.00	1.42
PRIME	4.76	16.41	0.00	0.00
CDC	4.76	15.97	0.76	2.98
AMD	4.76	15.67	0.51	6.78
NEC	4.76	15.67	0.00	0.00
UNISYS	4.76	15.61	0.00	0.00
XEROX	4.76	15.61	0.00	0.00
DEC	4.76	15.56	0.00	0.00
KOBUTA	4.76	15.56	0.00	0.00
ARETE	2.38	15.61	0.00	0.00
AT T	2.38	15.61	0.00	0.00
LUCKY G	2.38	15.61	0.00	0.00
METAFLOW	2.38	15.61	0.00	0.00
TOSHIBA	2.38	15.61	0.00	0.00
INTEG DT	2.38	15.56	0.00	0.00
PERF SEM	2.38	15.56	0.00	0.00
RACAL	2.38	15.56	0.00	0.00
SIEMENS	2.38	15.56	0.00	0.00
SILICONG	2.38	15.56	0.00	0.00
STARDENT	2.38	15.56	0.00	0.00
TANDEM	2.38	15.56	0.00	0.00
HITACHI	2.38	15.22	0.00	0.00
SODIMA	2.38	13.77	0.00	0.00
SGS/THOMS	2.38	13.73	0.00	0.00
INTERGRA	2.38	2.38	0.00	0.00
OLIVETTI	2.38	2.38	0.00	0.00
SCHLUMB	2.38	2.38	0.00	0.00
VLSI	2.38	2.38	0.00	0.00
Mean	10.52	14.60	1.70	3.39
S.D.	12.18	4.00	5.00	7.99
Network centralization	53.89	7.26	24.40	33.98

*See Appendix D for full company names.

between MIPS Computer Systems and Sun Microsystems, AMD and Philips between Sun Microsystems and Hewlett–Packard, or Motorola between Hewlett–Packard and Thomson.

4.3. Centrality in the DRAM network

The same centrality indices are calculated for the DRAM technology. They are shown in Table 2 and will be discussed in a comparison with the data in Table 1.

Table 2. Point and network centrality measures for the DRAM technology

Company*	C_D	C_C	C_B	C_F
AMD	18.31	8.05	11.31	33.52
TI	18.31	8.04	8.76	8.18
NAT_SEMI	16.90	7.92	10.08	12.16
LUCKY_G	15.49	8.00	12.49	16.49
AT&T	14.08	7.73	13.38	26.37
SIEMENS	14.08	7.73	6.79	10.71
LSILOGIC	12.68	8.05	14.61	9.79
SGS THOM	12.68	8.03	11.89	15.11
INTEL	12.68	7.87	4.81	5.66
MITSUBIS	11.27	8.17	20.11	25.53
IBM	11.27	7.82	2.03	3.51
TOSHIBA	11.27	7.80	10.00	12.40
PHILIPS	11.17	7.73	3.47	4.70
H/P	9.86	7.91	2.31	1.37
SAMSUNG	9.86	7.77	2.30	2.74
DEC	8.45	7.81	0.00	0.82
HYUNDAI	8.45	7.74	1.01	2.26
MICRON_T	8.45	7.58	2.47	3.24
TANDY	7.04	7.79	3.82	0.43
CHIPS_T	7.04	7.79	5.09	5.77
FUYO	5.63	7.73	1.25	2.12
KAYPRO	5.63	7.72	0.00	0.32
DELLCOMP	5.63	7.72	0.00	0.32
MOTOROLA	5.63	7.58	0.71	2.54
CYPRESS	5.63	7.55	2.03	3.17
FUJITSU	4.23	7.69	2.62	2.28
NMB	4.23	7.54	2.03	2.79
HITACHI	4.23	7.53	0.00	0.00
NEC	2.82	7.63	4.03	4.61
VLSI	2.82	7.56	2.54	4.62
SONY	2.82	7.54	0.00	0.00
SAGEM	2.82	7.49	0.00	1.18
GE	2.82	7.33	1.09	0.57
GEC	2.82	7.27	2.03	2.59
OLIVETTI	2.82	7.27	1.07	0.74
PARADIGM	2.82	7.26	0.00	0.00
RICOH	2.82	7.12	1.31	2.38
COMMODOR	2.82	7.12	0.00	0.00
MATRA_MHS	2.82	7.10	0.00	0.00
NITRON	2.82	1.41	0.00	0.00
UNI_SEMI	2.82	1.41	0.00	0.00
WESTINGH	1.41	7.64	0.00	0.00
ACER	1.41	7.53	0.00	0.00
SHARP	1.41	7.53	0.00	0.00
ITAN	1.41	7.52	0.00	0.00
DOCAS	1.41	7.52	0.00	0.00
SCHLUMB	1.41	7.50	0.00	0.00
STC	1.41	7.43	0.00	0.00
XICOR	1.41	7.38	0.00	0.00
NCR	1.41	7.33	0.00	0.00
MATSUSHT	1.41	7.32	0.00	0.00
EXEL_MIC	1.41	7.29	0.00	0.00
INT_CT	1.41	7.27	0.00	0.00
WYSE	1.41	7.26	0.00	0.00
XEROX	1.41	7.26	0.00	0.00
FORMOS_P	1.41	7.26	0.00	0.00

—continued opposite

Table 2. *continued*

Company*	C_D	C_C	C_B	C_F
XYLOGICS	1.41	7.26	0.00	0.00
NTT	1.41	7.22	0.00	0.00
AMSTRAD	1.41	7.12	0.00	0.00
CROSS_TR	1.41	7.09	0.00	0.00
ERSO	1.41	6.91	0.00	0.00
FORCE_C	1.41	6.85	0.00	0.00
APPMICRS	1.41	6.85	0.00	0.00
PANATEC	1.41	6.72	0.00	0.00
BULL	1.41	1.41	0.00	0.00
CRAY	1.41	1.41	0.00	0.00
G2_INC	1.41	1.41	0.00	0.00
HARRIS	1.41	1.41	0.00	0.00
UNISYS	1.41	1.41	0.00	0.00
GAZELLE	1.41	1.41	0.00	0.00
TRIQUINT	1.41	1.41	0.00	0.00
UN_TECHN	1.41	1.41	0.00	0.00
Mean	5.01	6.67	2.33	3.21
S.D.	4.80	2.13	4.25	6.48
Network centralization	13.68	3.06	252.58	30.74

*See Appendix D for full company names.

In contrast with the RISC network where a few focal firms have an extremely high C_D value, the distribution of degree-based centrality values among companies in the DRAM market is more evenly spread.* The degree centrality of Sun Microsystems is 5.9 times the mean, and that of MIPS Computer Systems is 4.1 times the mean, while this figure for AMD and Texas Instruments, the two firms with the highest degree centrality in the DRAM network, is only 3.7. Hence, it can be argued that the DRAM SA network has a more "open" character than the RISC network: while 12 firms play a central role in the DRAM network, we have only two or three central players in the RISC case.

The closeness-based centrality index, C_C, shows values much lower on average than those in the RISC network.† The focal firms do not have the same potential for control as in the RISC network. The structure of the network is such that many firms are interconnected with each other, but there is no hub–spoke structure as in the RISC network, giving some companies a strong potential for control over the others. The abundance of cycles in the DRAM alliance network implies that most companies can avoid the potential control of another company to which they are linked.

The betweenness centrality of some firms in the DRAM market reaches the same level as the three focal companies in the RISC network. Companies such as Mitsubishi, AMD, AT&T, LSI Logic, Lucky-Goldstar and SGS-Thomson have high values for C_B and their value for C_F is even higher, with the exception of LSI Logic. These high values indicate strategic alliances that cut across the whole network, improving significantly their centrality in terms of betweenness.

The difference in network structure and the network positions of focal partners in both SA networks can be partly explained by the different goals of the cooperative strategies behind the technology alliances. In the RISC network the search for a new industry standard and the resulting

*The ratio of the mean over the standard deviation is 0.86 for the RISC market and 1.04 for the DRAM market.
†The mean in the RISC network is 2.19 times higher.

group-based competition are the drivers behind most SAs, such as the licensing of RISC architectures: this economic drive almost by definition implies the clustering of firms around a few focal actors who have a fairly strong grip on the other players. The result is that competition is no longer company-based but is group-based. Strategic alliances in the DRAM case, on the other hand, are to a large extent linked to process technologies and manufacturing capabilities, with R&D joint ventures and cross-licensing for second-sourcing as the main SA modes. Such agreements do not have a direct impact on the competitive position of the partners on the DRAM market, and in most cases allies are free to cooperate with third parties on other technological issues.

In short, the centrality measures show that the DRAM network is much more "open" than the RISC network. In the latter each firm is linked to a focal partner which is the central player in the group-based market share competition. Consequently, the RISC network can be neatly divided into three strategic blocks.* Within each of these, relations are abundant, but relations across them are scarce because of their exclusivity. In the DRAM network, agreements are not exclusive or they involve only a few partners, with the result that many strategic alliances cut across the network. The DRAM network is loosely structured and does not divide the set of companies into clearly identifiable strategic blocks.

This is exactly what we would expect from the industry analysis in Section 3. The competition between different RISC architectures leads to clearly identifiable strategic blocks, and among these cooperation is excluded (almost) by definition. Most cooperative agreements concerning DRAM chips are process technology-based and have no direct relationship with market share competition. Usually, the agreements relate to two or three companies only, and often concern several distinct spheres of exchange. The DRAM network can therefore be expected to consist of a criss-cross of SAs without well-defined strategic blocks.

5. CONCLUSION

In this paper we have argued that our present understanding of cooperative agreements could be substantially improved by adopting a network approach, instead of using the traditional way of analysing cooperative agreements on a dyadic level or by focusing on the set of SAs of a focal firm. In a growing number of industries interorganizational collaboration is no longer confined to two-company alliances; rather, groups of companies link themselves together into networks of alliances in order to command competitive advantages which individual companies or two-company alliances cannot achieve. The result is the emergence of group-based competition between "blocks" of allied companies. Focusing only on company-based advantages or on the set of SAs of only one focal company is not adequate for analysing the competitive position of firms in industries with industry-wide SA networks. The competitive positions of companies in such industries are also largely determined by the whole SA network structure, and by their position within it.

Industry analysis can unravel group-based advantages and the reasons why companies are teaming up in strategic alliances. It can also focus on the role that SAs play in corporate strategies and on the consequences of this for the network positions of the focal firms and for the structure of the industry-wide network. However, industry analysis says nothing about how companies' positions within networks or the overall network structure within particular industries can

*"Strategic blocks" are based on similarities in the strategic linkages between companies (see Nohria and Garcia-Pont, 1991).

be measured. This article has illustrated how network analytical tools can be used in order to find reliable measures. Network analysis is thus a valuable tool that enriches and complements the results of the industry analysis.

A comparison has been made here between the two networks associated with RISC microprocessor technology and DRAM chip technology. These two networks were chosen because cooperative strategies regarding both technologies are based on completely different economic drivers, so that network positions and the overall network structure could be expected to differ significantly between the two networks.

The network analysis shows that significant differences do exist between the two SA networks, not only in terms of network structure but also as regards the role played by specific companies within the networks. The network associated with RISC technology is clearly structured around focal players, who in turn have consortia-like agreements among themselves as regards industry standards. Most agreements in the DRAM network are not exclusive, or they involve only a few partners. The result is that the DRAM network, unlike RISC, is basically loosely structured and can be described as a criss-cross of SAs without any well-defined strategic blocks. These differences between the structures of the two SA networks reflect the different roles SAs play in corporate strategies in the two technologies. The various centrality measures have shown that network positions and overall network structure can be measured in a reliable and quantitative way, so that the results can be used as feedback in the industry analysis. Naturally, centrality measures represent only one of several possible tools for analysing networks, but the use of simple centrality measures has already revealed a picture which goes beyond that which an analysis on a dyadic or individual firm level can give. Industry analysis and network analysis thus complement each other, increasing our understanding of cooperative strategies in high-tech industries characterized by industry-wide SA networks.

REFERENCES

Axelsson, B. and Easton, G., *Industrial Networks: A New View of Reality* (London: Routledge, 1992).

Bonacich, P., Factoring and weighting approaches to status scores and clique identification, *Journal of Mathematical Sociology* (1972), Vol. 2, pp. 113–120.

Bonacich, P., Power and centrality: a family of measures, *American Journal of Sociology* (1987), pp. 1170–1182.

Boulton, W. R., Dowling, M. J. and Lohmeyer, J., Technology development strategies in Japan, Europe and the United States, *Technovation* (1992), Vol. 12, No. 2, pp. 99–118.

Bowen, H. P., Electronic components and semiconductors. In: *The European Challenge: Industry's Response to the 1992 Programme* (New York: Harvester/Wheatsheaf, 1991).

Burrows, P., Consortia: are they getting better?, *Electronic Business* (1992), 18 May, pp. 47–79.

Chesnais, F., *Technical Cooperation Agreements Between Firms* (1988), STI review, No. 4, December, pp. 52–119.

Collins, T. M. and Doorley, T. L., *Teaming up for the 90s* (Paris: Deloitte & Touche, 1991).

Contractor, F. J. and Lorange, P., *Cooperative Strategies International Business* (Lexington: D.C. Heath and Company, 1988).

Dinneen, G. P., R&D consortia: are they working?, *Research & Development* (1988), June, pp. 63–66.

Evan, M. W., The organization-set: toward a theory of interorganizational relations. In: J. D. Thompson (Ed.), *Approaches to Organizational Design* (Pittsburgh: University of Pittsburgh Press, 1966).

Flamm, K., Semiconductors. In: G. C. Hufbauer (Ed.), *Europe 1992: An American Perspective* (Washington, D.C.: The Brookling Institution, 1990).

Forsgren, M. and Johanson, J. (Eds), *Managing Networks in International Business* (Philadelphia: Gordon and Breach, 1992).

Freeman, L. C., Centrality in social networks: conceptual clarification, *Social Networks* (1979), Vol. 1, pp. 215–239.

Freeman, L. C., Borgatti, S. P. and White, D. R., Centrality in valued graphs: a measure of betweenness based on network flow, *Social Networks* (1991), Vol. 13, pp. 141–145.

Garud, R. and Kumaraswamy, A., Changing competitive dynamics in network industries: an exploration of Sun Microsystems' open systems strategy, *Strategic Management Journal* (1993), Vol. 14, pp. 351–369.

Gomez-Casseres, B., Group versus group: how alliance networks compete, *Harvard Business Review* (1994), July–August, pp. 62–74.
Hagedoorn, J., Organizational modes of inter-firm cooperation and technology transfer, *Technovation* (1990), Vol. 10, pp. 17–30.
Hagedoorn, J. and Schakenraad, J., Inter-firm partnerships and cooperative strategies in core technologies. In: C. Freeman and L. Soete (Eds), *New Explorations in the Economics of Technical Change* (London: Pinter, 1990).
Hagedoorn, J. and Schakenraad, J., Leading companies and networks of strategic alliances in information technologies, *Research Policy* (1992), Vol. 21, pp. 163–190.
Hagedoorn, J. and Schakenraad, J., Strategic technology partnering and international corporate strategies. In: K. Hughes (Ed.), *European Competitiveness* (Cambridge: Cambridge University Press, 1993).
Håkansson, H. (Ed.), *Industrial Technological Development: a Network Approach* (London: Routledge, 1989).
Haklisch, C. S., *Technical Alliances in the Semiconductor Industry*, Center for Science and Technology Policy, New York University, unpublished paper (1986).
Haklisch, C. S., Technical alliances in the semiconductor industry: effects on corporate strategy and R&D. In: *Background Papers for Conference on Changing Global Patterns of Industrial R&D*, Stockholm, 20–22 June (1989).
Harrigan, K. R., *Strategies for Joint Ventures* (Lexington Books, Lexington, 1985).
Hof, R. D., Inside Intel: It's moving at double-time to head off competitors, *Business Week* (1992a), 1 June, pp. 48–54.
Hof, R. D., Why ACE may be in the hole, *Business Week* (1992b), 17 February, p. 86.
Integrated Circuit Engineering Corporation, *Status 1993: A Report on the Integrated Circuit Industry*, W. J. McClean (Ed.), (Scottsdale: Arizona, 1993).
Johanson, J. *et al.*, *Internationalization, Relationships and Networks* (Uppsala, Uppsala University, 1994).
Johnstone, B., RISC and its rewards, *Far Eastern Economic Review* (1991), 3 October, p. 66.
Khazam, J. and Mowery, D., The commercialization of RISC: strategies for the creation of dominant designs, *Research Policy* (1994), Vol. 23, pp. 89–102.
Krugman, P. R., *Rethinking International Trade* (Cambridge, MA: The MIT Press, 1990).
Kukalis, S. and Kanazawa, B., Sun Microsystems reorganizes for growth, *Long Range Planning* (1993), Vol. 26, No. 5, pp. 42–48.
Methe, D. T., *Technological Competition in Global Industries: Marketing and Planning Strategies for American Industry* (Westport, CT: Quorum Books, 1991).
Morris, C. and Ferguson, C. H., How architecture wins technology wars: inventing — and reinventing — the proprietary architectures for open systems is critical to competitive success, *Harvard Business Review* (1993), March–April, pp. 86–96.
Mouline, A. and Santucci, G., *La filière micro-électronique dans la monde: Les semi-conducteurs au coeur des mutations technologiques*, Collection "Analyses des secteurs", 2ième trimestre 1992 (Paris: Eurostaf, 1992).
Mowery, D. C., *International Collaborative Ventures in U.S. Manufacturing* (Cambridge: Ballinger, 1988).
Neff, R., The costly race chipmakers can't afford to lose, *Business Week* (1990), 10 December, pp. 56–58.
Nohria, N. and Garcia-Pont, C., Global strategic linkages and industry structure, *Strategic Management Journal* (1991), Vol. 12, pp. 105–124.
Nohria, N. and Eccles, R. G. (Eds), *Networks and Organizations: Structure, Form and Action* (Boston: Harvard Business School Press, 1992).
Nomura Research Institute, Cross currents in the Japanese Semiconductor Industry, *NRI Electronics Industry Review* (1992), Spring.
OECD, *Strategic industries in a global economy: Policy issues for the 1990s* (Paris, 1991).
Parkhe, A., Interfirm diversity, organizational learning and longevity in global strategic alliances, *Journal of International Business Studies* (1991), Vol. 22, pp. 579–601.
Port, O., Talk about your dream team, *Business Week* (1992a), 27 July, pp. 33–34.
Port, O., Intel braces for a chorus of 'send in the clones', *Business Week* (1992b), 3 February, pp. 40–41.
Rice, V., Intel's 586 strategy: It's always been US versus THEM, *Electronic Business* (1992), November, pp. 53–58.
Ring, P. S. and Van de Ven, A. H., Structuring cooperative relationships between organizations, *Strategic Management Journal* (1992), Vol. 13, pp. 483–498.
Ring, P. S. and Van de Ven, A. H., Developmental processes of cooperative interorganizational relationships, *Academy of Management Review* (1994), Vol. 19, No. 1, pp. 90–118.
Ruhl, M., Sun Microsystems could get eclipsed by its satellites, *Electronic Business* (1988), p. 78.
Stephenson, K. and Zelen, M., Rethinking centrality: methods and applications, *Social Networks* (1989), Vol. 11, pp. 1–37.
Verity, J. W., The Japanese juggernaut that isn't, *Business Week* (1992), 31 August, pp. 62–64.
Vickery, G., *The European Experience in Advanced Electronics*, STI Review (Paris: OECD, 1992).
Warren, R. L., The interorganizational field as a focus for investigation, *Administrative Science Quarterly* (1967), Vol. 30, pp. 103–130.

APPENDIX A: DEFINITIONS OF CENTRALITY MEASURES*

Point centrality measures

Freeman's (1979) measure of degree centrality (C_D) is defined as the count of number of adjacencies for a point p_k:

$$C_D(p_k) = \sum_{i=1}^{n} a(p_i, p_k), \tag{A1}$$

where $a(p_i, p_k) = 1$ if and only if p_i and p_k are connected by a line; otherwise, $a(p_i, p_k) = 0$.

A relative measure of degree-based point centrality for a given point p_k is defined as follows:

$$C_D^{l}(p_k) = \frac{\sum_{i=1}^{n} a(p_i, p_k)}{n-1}, \tag{A2}$$

where $n - 1$ is the maximum number of points to which a point p_k can be connected.

A closeness-based measure of centrality varies inversely with $d(p_i, p_k)$, the number of edges in the geodesic linking p_i and p_k

$$C_C(p_k) = \{1/\sum_{i=1}^{n} d(p_i, p_k)\}. \tag{A3}$$

However, C_C is only meaningful for a connected graph. In an unconnected graph every point is at infinite distance from at least one other point. The relative centrality of point p_k can be defined as:

$$C_C^{l}(p_k) = \{(n-1)/\sum_{i=1}^{n} d(p_i, p_k)\}. \tag{A4}$$

Betweenness-based centrality can be measured as follows:

$$C_B(p_k) = \sum_{i}^{n} \sum_{<j}^{n} \frac{g_{ij}(p_k)}{g_{ij}}, \tag{A5}$$

where n is the number of points in the graph, g_{ij} the number of geodesics linking p_{ij} and p_j and $g_{ij}(p_k)$ is the number of geodesics linking p_i and p_j that contain p_k. The relative measure of betweenness centrality is:

$$C_B^{l}(p_k) = \{2 \sum_{i}^{n} \sum_{<j}^{n} \frac{g_{ij}(p_k)}{g_{ij}} / (n^2 - 3n + 2)\}. \tag{A6}$$

A centrality measure for valued graphs based on a maximum amount of information flow between two points was developed by Freeman *et al.* (1991). Let m_{ij} be the maximum flow from a point p_i to another p_j. And let $m_{ij}(p_k)$ be the maximum flow from p_i to p_j that passes through point p_k. Then the degree to which the maximum flow between all unordered pair of points depends on p_k, where $i < j$ and $i \neq j \neq k$ is:

$$C_F(p_k) = \sum_{i}^{n} \sum_{<j}^{n} m_{ij}(p_k). \tag{A7}$$

*For a more detailed discussion of centrality measures, we refer the reader to Bonacich (1987), Freeman (1979) and Freeman *et al.* (1991).

If the previous formula is divided by the total flow between all pairs of points where p_k is neither a source nor a sink, we can define a relative measure of flow betweenness as follows:

$$C_F^I(p_k) = \frac{\sum_{i}^{n} \sum_{<j}^{n} m_{ij}(p_k)}{\sum_{i}^{n} \sum_{<j}^{n} m_{ij}} . \tag{A8}$$

Connected graphs without cycles have only one path — a single geodesic — linking any pair of points, and thus have the same values for C_B and C_F. When cycles are present these two centrality measures differ because C_B measures record flow only along the geodesics, while the C_F measures are responsive to all paths along which information can flow.

Graph centrality measures

When the concept of "centrality" is applied to whole networks, it refers to differences in point centrality. If n is the number of points, $C_x(p_i)$ one of the point centralities defined above, and $C_x(p_i)$ the largest of $C_x(p_i)$ for any point in the network, then:

$$C_x = \frac{\sum_{i=1}^{n} (C_x(p^*) - C_x(p_i))}{\max \sum_{i=1}^{n} (C_x(p^*) - C_x(p_i))} \tag{A9}$$

is Freeman's (1979) index for graph centrality. The denominator represents the maximum possible sum of differences in point centrality for a graph with n points. This maximum usually coincides with the point centrality of a star.

When (A9) is applied to the point centralities, as we have defined them above, we get the following formulas for network centrality.

The degree-based network centrality measure can be formulated as follows:

$$C_D = \frac{\sum_{i=1}^{n} (C_D(p^*) - C_D(p_i))}{n^2 - 3n + 2} . \tag{A10}$$

Similarly, we can write the closeness-based network centrality measure as follows:

$$C_C = \frac{\sum_{i=1}^{n} (C_C(p^*) - C_C(p_i))}{(n^2 - 3n + 2)/(2n - 3)} . \tag{A11}$$

The betweenness-based graph centrality measure can be written as follows:

$$C_B = \frac{\sum_{i=1}^{n} (C_B(p^*) - C_B(p_i))}{n^3 - 4n^2 + 5n - 2} . \tag{A12}$$

Finally, the flow betweenness graph centrality measure can be expressed in the following way:

$$C_F = \frac{\sum_{i=1}^{n} (C_F(p^*) - C_F(p_i))}{n - 1} . \tag{A13}$$

APPENDIX B: RISC CHIPS AND MANUFACTURING FIRMS

Company	Architecture	Chip	Manufacturers*
Hewlett–Packard Co (U.S.)	PA	PA-4	Hitachi (J)
			Samsung (S.K.)
		PA-7100	HP (U.S.) (captive)
			Oki (J)
			Mitsubishi (J) (captive)
			Winbond (Taiwan)
Intel Corp (U.S.)	i860	860XP	Intel (U.S.)
Apple/IBM/Motorola (U.S.)	Power PC	Power PC 601	IBM (U.S.)
			Motorola (U.S.)
Motorola	88000		Motorola (U.S.)
MIPS Computer Systems (U.S.)	R3000	IDT (U.S.)	
		R4000	Q.E.D. (U.S.)
		R4400	LSI Logic (U.S.)
			Performance Semiconductors (U.S.)
			Siemens (G)
			NEC (J)
			BIT (U.S.)
			Sony (J)
			Toshiba (J)
			Macronix (Taiwan)
Sun Microsystems (U.S.)	SPARC	HyperSPARC	Cypress (U.S.)
		Viking	Fujitsu (J)
			LSI Logic (U.S.)
		SuperSPARC	TI (U.S.)
		microSPARC	TI (U.S.)
			Philips (NL)
			Matsushita (J) (captive)
			Toshiba (J) (captive)
			Weitek (U.S.)
DEC Corp. (U.S.)	Alpha		DEC (U.S.)
			Cypress (U.S.)
Intergraph (U.S.)	Clipper		Samsung (S.K.)
			Motorola (U.S.) (foundry)
			Fujitsu (J) (foundry)
Acorn Computers (U.S.)	ARM		Sanyo (J)
		ARM60	VLSI Technology (U.S.)
			GEC Plessey (U.K.)
			Hitachi (J)
AT&T (U.S.)	Hobbit		NEC (J)
National Semiconductors (U.S.)	Swordfish		National Semiconductors (U.S.)

Sources: IEEE Spectrum (April 1991, p. 61), (July 1992, p. 28); ICE (1992, pp. 6–33), (1993, pp. 6–34).
*J, Japan; S.K., South Korea; G. Germany; NL, The Netherlands.

APPENDIX C: REPRESENTATIVE SAMPLE OF COMMERCIALLY AVAILABLE WORKSTATIONS IN THE U.S.A. IN 1991

Central processing unit	Workstation manufacturer	
CISC		
Cypress	Cypress CY7C601	Mars Microsystems Inc.
		Solarix Systems
		Star Technologies Inc.
SGS-Thomson	Inmos T800	EE International Computer Corp.
Intel	Intel 80386	Mars Microsystems Inc.
	Intel 80486	Acer America Corp.
		American Mitac Corp.
		Arche Technologies Inc.
		AT&T Computer Systems
		Compaq Computer Corp.
		Copam USA Inc.
		Dell Computer Corp.
		Dolch Computer Systems
		EE International Computer Corp.
		Fortron/Source Corp.
		Laser Digital Inc.
		Microway Inc.
		Micro Express
		Mobius Computer Corp.
		NCR Corp.
		Polywell Computers Inc.
		Tangent Computer Inc.
		TeleCAD
		TeleVideo Systems Inc.
		Wyse Technology Inc.
Motorola	Motorola 68030	Apple Computer Inc.
		Commodore Business Machines Inc.
	Motorola 68040	Concurrent Computer Corp.
		Hewlett–Packard Co.
RISC		
	Custom	International Business Machines Corp.
	Custom	Visual Information Technologies Inc.
Intel	Intel i860	EE International Computer Corp.
Intergraph	Intergraph C300	Intergraph Corp.
LSI Logic	LSI Logic Sparkit 20	CompuAdd Corp.
	LSI Logic 64801	Tatung Science and Technology Inc.
	LSI Logic L64084	Twinhead International Corp.
MIPS	MIPS R3000	Control Data Corp.
		Digital Equipment Corp.
		Evans & Sutherland Design Systems Division
		MIPS Computer Systems Inc.
		Silicon Graphics Inc.
		Sony Microsystems Co.
		Stardent Computer Inc.
Sun	Panasonic MN 10501	Solbourne Computer Inc.
	Sparc Engine	Ramtek Corp.
	Sun Sparc	RDI Inc.
		Sun Microsystems Inc.

Source: Adapted from IEEE Spectrum, April 1991, pp. 40–46.

APPENDIX D: COMPANIES INCLUDED IN THE RISC AND DRAM SA NETWORK

	Name	Code	Country
DRAM network			
1	Acer	ACER	Taiwan
2	Advanced Micro Devices Inc.	AMD	U.S.A.
3	American Telephone & Telegraph Co.	AT&T	U.S.A.
4	Amstrad Plc.	AMSTRAD	U.K.
5	Applied Micro Systems Corp.	APPMICRS	U.S.A.
6	Groupe Bull	BULL	France
7	Chips and Technologies	CHIPS_T	U.S.A.
8	Commodore	COMMODOR	U.S.A.
9	Cray Research Inc.	CRAY	U.S.A.
10	Cross & Trecker Corp.	CROSS_TR	U.S.A.
11	Cypress Semiconductor	CYPRESS	U.S.A.
12	Dell Computer	DELLCOMP	U.S.A.
13	Docas	DOCAS	Brazil
14	Erso	ERSO	Republic of China
15	Exel microelectronics	EXEL_MIC	U.S.A.
16	Force Computers Inc.	FORCE_C	U.S.A.
17	Fujitsu Ltd.	FUJITSU	Japan
18	Fuyo Group	FUYO	Japan
19	Digital Equipment Corp. (DEC)	DEC	U.S.A.
20	Formosa Plastic Corp.	FORMOS_P	U.S.A.
21	Gazelle microcircuits	GAZELLE	U.S.A.
22	General Electric	GE	U.S.A.
23	General Electric Company	GEC	U.K.
24	G-2 Inc.	G2_INC	U.S.A.
25	Harris Corp.	HARRIS	U.S.A.
26	Hewlett–Packard Co.	H-P	U.S.A.
27	Hitachi Ltd.	HITACHI	Japan
28	Hyundai	HYUNDAI	South Korea
29	Int. CMOS Technology	INT_CT	U.S.A.
30	Integrated Device Technology	INTEG-DT	U.S.A.
31	International Business Machines	IBM	U.S.A.
32	Intel Corp.	INTEL	U.S.A.
33	Itan	ITAN	Brazil
34	Kaypro Corp.	KAYPRO	U.S.A.
35	LSI Logic	LSILOGIC	U.S.A.
36	Lucky Goldstar Ltd.	LUCKY_G	South Korea
37	Matra MHS	MATRA_MHS	France
38	Matsushita Elect. Industrial Co. Ltd.	MATSUSHT	Japan
39	Micron Technology Inc.	MICRON_T	U.S.A.
40	Mitsubishi Electric Corp.	MITSUBIS	Japan
41	Motorola Inc.	MOTOROLA	U.S.A.
42	National Cash Register Corp. (NCR)	NCR	U.S.A.
43	National Semiconductor Corp.	NAT_SEMI	U.S.A.
44	NEC Corp.	NEC	Japan
45	NMB Semiconductor	NMB	Japan
46	Nitron	NITRON	U.S.A.
47	NTT	NTT	Japan
48	Olivetti SpA.	OLIVETTI	Italy
49	Panatec R&D Corp.	PANATEC	U.S.A.
50	Paradigm Technologies Inc.	PARADIGM	U.S.A.
51	Philips N.V.	PHILIPS	Netherlands
52	Ricoh	RICOH	Japan
53	Sagem	SAGEM	France
54	Samsung	SAMSUNG	South Korea

— *continued overleaf*

Appendix D. *Continued*

Name		Code	Country
55	Schlumberger N.V.	SCHLUMB	U.S.A.
56	Sharp	SHARP	Japan
57	Siemens A.G.	SIEMENS	Germany
58	Sony	SONY	Japan
59	STC	STC	U.K.
60	Tandy	TANDY	U.S.A.
61	Texas Instruments Inc.	TI	U.S.A.
62	Thomson S.A. (SGS-Thomson)	THOMSON	France/Italy
DRAM network			
63	Toshiba Corp.	TOSHIBA	Japan
64	Triquint	TRIQUINT	U.S.A.
65	Unisys Corp.	UNISYS	U.S.A.
66	Universal Semiconductor	UNI_SEMI	U.S.A.
67	United Technologies Corp. (UTV)	UN_TECHN	U.S.A.
68	VLSI Technology Inc.	VLSI	U.S.A.
69	Westinghouse	WESTINGH	U.S.A.
70	Wyse	WYSE	U.S.A.
71	Xerox Corp.	XEROX	U.S.A.
72	Xicor	XICOR	U.S.A.
73	Xylogics	XYLOGICS	U.S.A.
RISC network			
1	Advanced Micro Devices Inc.	AMD	U.S.A.
2	American Telephone & Telegraph Co.	AT&T	U.S.A.
3	Apollo Computer	APOLLO	U.S.A.
4	Arete Systems Corp.	ARETE	U.S.A.
5	Bipolar Integrated Technology	BIPOLAR	U.S.A.
6	Control Data Corp.	CDC	U.S.A.
7	Cypress Semiconductor	CYPRESS	U.S.A.
8	Fujitsu Ltd.	FUJITSU	Japan
9	Data General Corp.	DATA-GEN	U.S.A.
10	Digital Equipment Corp. (DEC)	DEC	U.S.A.
11	Hewlett–Packard Co.	H-P	U.S.A.
12	Hitachi Ltd.	HITACHI	Japan
13	Integrated Device Technology	INTEG-DT	U.S.A.
14	Intergraph	INTERGRA	U.S.A.
15	Kubota Corp.	KUBOTA	Japan
16	LSI Logic	LSILOGIC	U.S.A.
17	Lucky Goldstar Ltd.	LUCKY-G	South Korea
18	Matsushita Elect. Industrial Co. Ltd.	MATSUSHT	Japan
19	Metaflow Technologies	METAFLOW	U.S.A.
20	Mips Consumer Systems	MIPS-CS	U.S.A.
21	Motorola Inc.	MOTOROLA	U.S.A.
22	National Cash Register Corp. (NCR)	NCR	U.S.A.
23	Olivetti SpA.	OLIVETTI	Italy
24	Performance Semiconductor	PERF-SEM	U.S.A.
25	Philips N.V.	PHILIPS	Netherlands
26	Prime Computer Inc.	PRIME	U.S.A.
27	Racal	RACAL	U.K.
28	Schlumberger N.V.	SCHLUMB	U.S.A.
29	Siemens A.G.	SIEMENS	Germany
30	Silicon Graphics	SILICONG	U.S.A.
31	Stardent Inc.	STARDENT	U.S.A.
32	Sté.de Dév.Ind.de Matériel & d'Ass.	SODIMA	France
33	NEC Corp.	NEC	Japan

— continued opposite

Appendix D. *Continued*

Name		Code	Country
34	Sun Microsystems	SUN-MICR	U.S.A.
35	Tandem Computers Corp.	TANDEM	U.S.A.
36	Tektronix Inc.	TEKTRONX	U.S.A.
37	Texas Instruments Inc.	TI	U.S.A.
38	Thomson S.A. (SGS-Thomson)	THOMSON	France/Italy
39	Toshiba Corp.	TOSHIBA	Japan
40	UniSoft	UNISOFT	U.K.
41	Unisys Corp.	UNISYS	U.S.A.
42	VLSI Technology Inc.	VLSI	U.S.A.
43	Xerox Corp.	XEROX	U.S.A.