LOAD DISTRIBUTION AND RESOURCE SHARING

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This paper will discuss about the system structure and system design philosophy for the large scale control systems. The design philosophy, the main theme of this article, is "load distribution and resource sharing", but also the following items will be discussed:
- *three level hierarchy control system philosophy;*
- *coupling and optimal load sharing among SCC/DDC computers;*
- *sharing of the process resources among computers.*

1. Introduction

In order to meet the control system requirements, and to achieve the large-scale control system design, there are established new basic concepts:
a) To determine the number of levels of total control system hierarchy;
b) To optimally allocate the functional blocks among the computers, which build-up multi-computer system ar chitecture;
c) To distribute the jobs of computers to programmable controllers (PC);
d) To make the process input/output resources to be shared among computers and programmable controllers (PC).

Up to now, two-level hierarchy control systems seem to be very common. These two levels are:
a) Supervisory Control Computer level, SCC; at this level there are used process control computers or industrial system computers;
b) Direct Digital Control level, DDC; at this level there are used microcomputers, or programmable controllers.

We will show an evaluation chart, fig.1, to review the differences in performance between SCC computers and programmable controllers.
Investigating the application range of SCC computers and PC's, the following points may be pointed out:
- they cover almost all the required application ranges of total control system hierarchy; but relatively quick (30 ms¸ 1 sec.) and small (1K¸ 4Kwords) applications are not covered enough;
- it seems better if we have one more level between SCC level and PC level (the DDC2 level), named DDC1 level, which uses advanced DDC.

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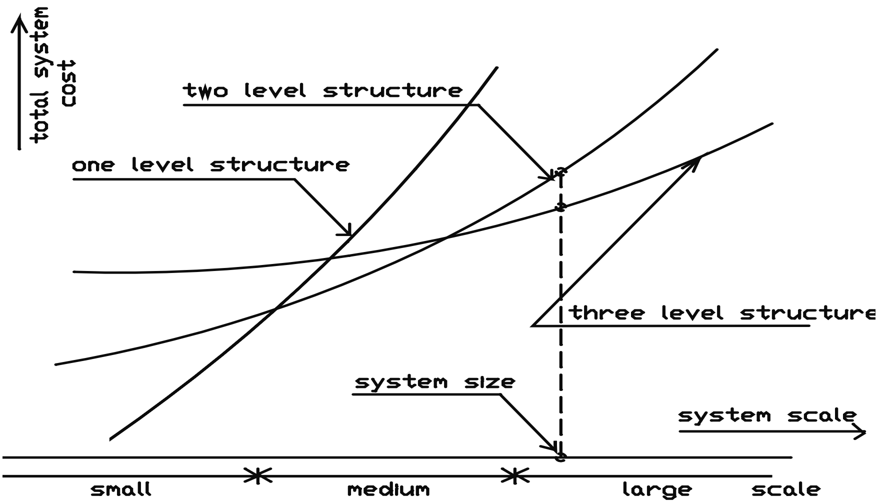


Fig. 1 - Evaluation of computers and controllers

In fig.2 are shown three curves which represent total system cost versus system scale for the three structure types: one level control system may be applicable in case of small scale control system; for medium scale control system, two level control system may be suitable, and even this one may be extended to large-scale control; but for a large-scale control system is optimal a three-level structure.

Reviewing these two figures, it may be concluded that three level control system may be optimal in case of a total control large-scale system.

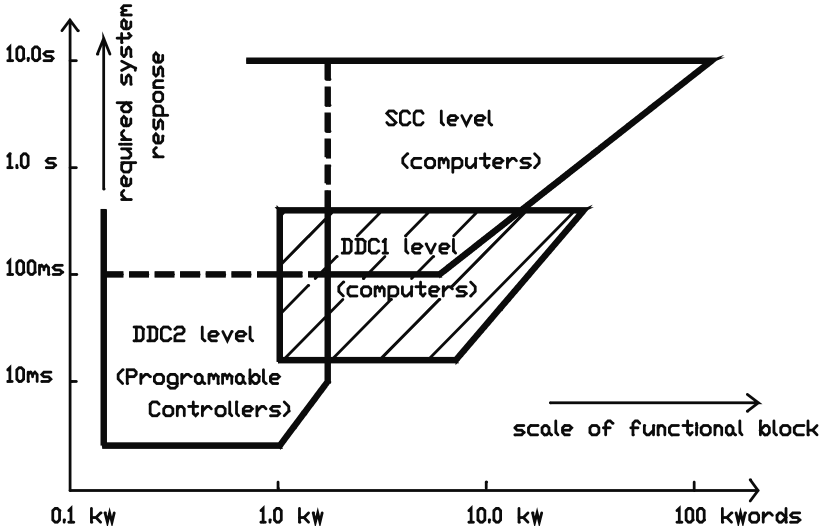


Fig. 2 - Total system cost estimation

2. Optimal Functional Allocation

The next problem would be how to allocate the required functional blocks among the computers and controllers within the level. This is a kind of multi-computer system design problem.

There are two major categories of interconnecting processors and memories, which are called multiprocessor systems (tightly coupled) and multicomputer systems (loosely coupled).

We will select, from these two categories, in this case (large systems), the multi-computer system, on the following reasons:
- control functions are relatively independent, one of the others;
- processing data and process signals may be the information mostly used in common, between computers;
- the interactions between functions are not so frequent and require relatively slow response time.

Tacking into account by these reasons, the muti-computer system could be for the two levels (SCC and DDC1) structured as in fig.3.

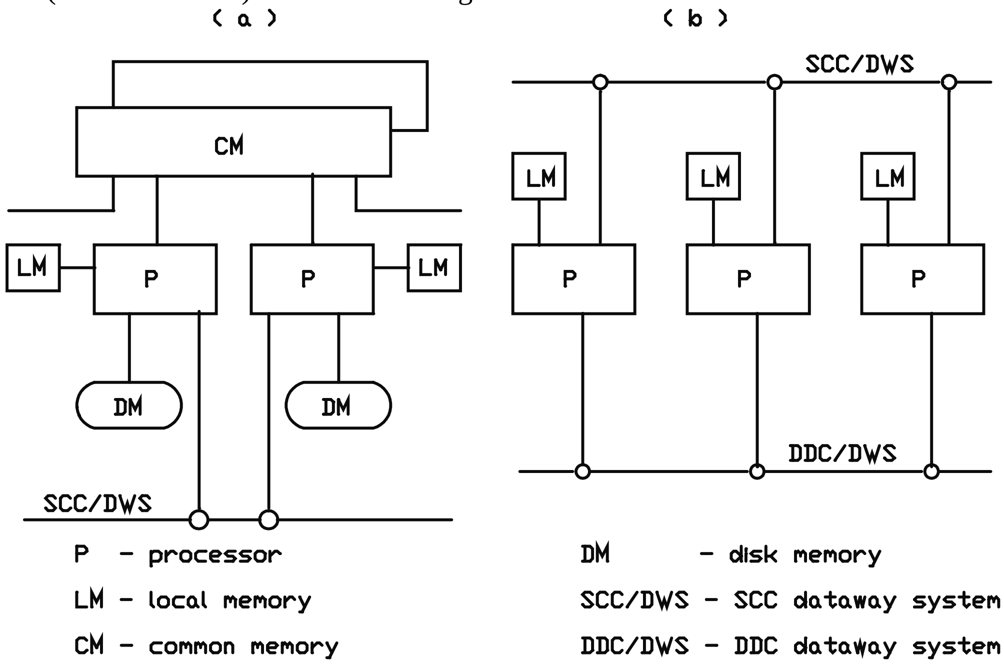


Fig. 3 - Multicomputer system architecture at SCC and DDC1 levels

The optimal design criteria, applied for SCC level and DDC1 level are as follows:
- minimizing the processor load shared for inter-computer data communication, so that the total system performance may not be reduced;
- each of system computers should be well-balanced with respect to
    (1) - average processor load;
    (2) - required local memory size;

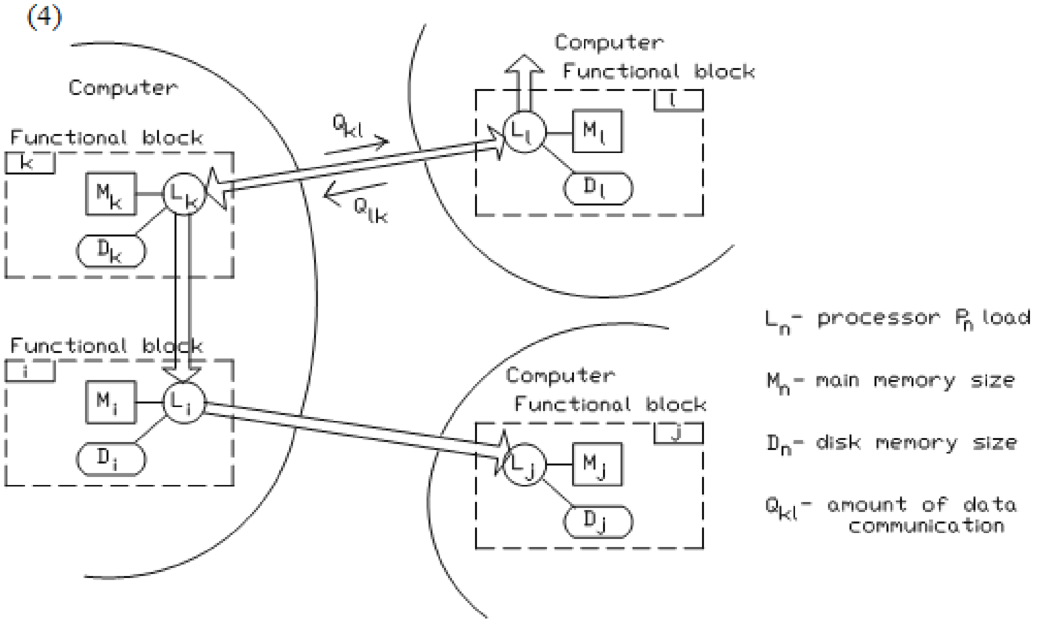
(3) - required disk memory.

In order to formulate the above-mentioned optimal design criteria, we have to introduce a model on the functional structure (fig.4). We assume that the total control function can be divided into a number of functional blocks;and each of these blocks require so much amount of processor load, local memory size and disk memory.

In order to obtain an optimal task allocation, firstly we have to construct data tables, which contain, for every task, processor load and the local and disk memory requirements. In order to solve this optimal problem we have to use non-linear integer programming techniques. However we can obtain suitable solutions by trial and error method, starting from the conventional functional allocation.

(1) The optimal problem is to determine a set of assignment variables, which minimizes the total sum of inter-computer data communication:

(4)



$$Q = \sum_{i=1}^{m} \sum_{j=1}^{m} \sum_{k=1}^{n} \sum_{l=1}^{n} [Q_{kl} * x_{ik} * x_{jl}]$$

$$\overline{M} = \frac{1}{m}\sum_{k=1}^{n} M_k ; \overline{D} = \frac{1}{m}\sum_{k=1}^{n} D_k ; \overline{L} = \frac{1}{m}\sum_{k=1}^{n} L_k$$

Fig. 4 - Model for functional structure

$$\left| \sum_{k=1}^{n} [M_k * X_{ik}] - \overline{M} \right| \leq \Delta M, i = 1 \div m \quad (1)$$

$$\left| \sum_{k=1}^{n} [D_k * X_{i,k}] - \overline{D} \right| \leq \Delta D, i = 1 \div m \quad (2)$$

$$\left| \sum_{k=1}^{n} [L_k * X_{i,k}] - \overline{L} \right| \leq \Delta L, i = 1 \div m \quad (3)$$

Where:

Restrictions on inter-computer balance may be expressed as:
The variables are defined as :
X_{ik} , assignment variable , which is 1 if the functional block k is assigned on processor P_i;
Q_{kl} , amount of data communication from functional block k to functional block l;
M_k, D_k , required local/disk memory size, associated with functional block k;
L_k , occupied processor load, associated with functional block k.

3. Processor Load Distribution

On designing the system configuration, the basic objectives of introducing the distributed system architecture with SCC data way system and PC's are as follows:
- to reduce cabling cost associated with peripheral devices,
while the process I/O cabling reduction is realized by the introduction of DDC data way system;
- to distribute tasks of SCC computers among PS's, for reduction of the processor load of SCC computers.

Taking as an example the data handling at the SCC level, it will be shown how the data processing cost is reduced by introducing the distributed system. The analysis below is comparison of two system configurations on process I/O which is built on DDC dataway system:
- SCC computers have direct coupling with DDC data way system, so that the data handling on process I/O may be done in SCC computers;
- PC's are to be prepared, so that the primary parts of process data handling may be done at PC's.
The data processing cost is one of the major factors, in choosing either one of these two configurations; for estimating the data-processing cost the following premises are needed:
(1) If they are direct coupled, the data processing cost is proportional with the number of process I/O points;
(2) The system total cost is estimated according to the following equation:

$$C_t = \sum_{i} \alpha_i * P_i + \sum_{i,j} Q_{i,j} \qquad (4)$$

where C_t = *total data processing cost;*

a_i = *cost coefficient for computer i;*

P_i = *number of process I/O points, to be processed at computer i;*

$Q_{i,j}$ = *data communication cost, if there exist communication between i and j computers, else* $Q_{i,j}=0$.

(3) The cost coefficient for SCC computers is much higher than at PC's, i.e. :

a_i » a_j , *i - SCC computer, j* - PC.

The total data processing cost, both direct coupling case and distributed case, are shown in fig.5, with the parameterization of the SCC computers number.

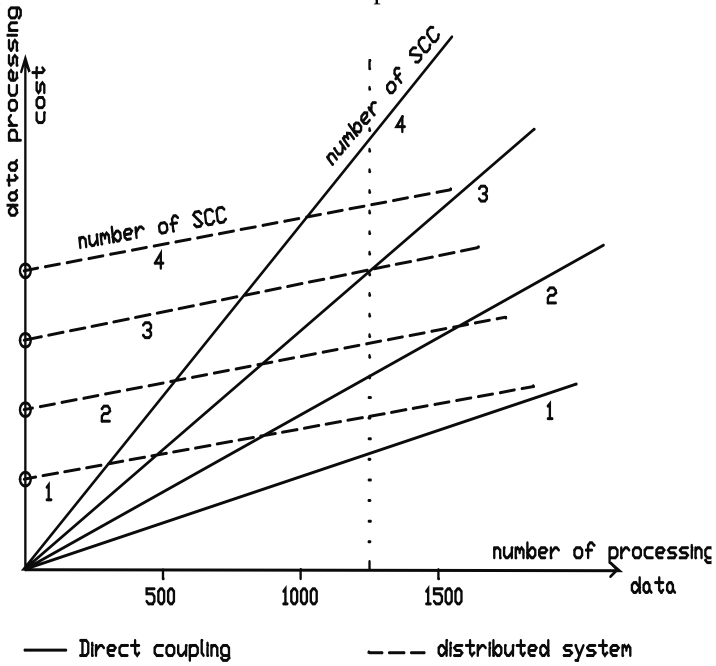


Fig. 5 - Data processing cost diagram

Starting from this diagram, considering the processing data number and between certain cost limits, we can choose the system architecture and the I/O connecting system structure.

By using two data-ways, separately, SCC and DDC, it is permitted a high throughput, of application-application type, and a good response time, for sensor based application.

One of the objectives of introduction of DDC data-way system is to process I/O resources be shared among SCC, DDc2 computers and DDC2 controllers.

4. Conclusions

Taking in account the above-mentioned criteria, we have implemented a hierarchical system; the lower lever of this system is shown in fig.6.

This system has, at the lower level, a distributed structure, which realizes: the data gathering and validation, the distribution of the commands and the process control tasks.
The computer from the higher hierarchical level satisfies the information requirements of a variety of users (operators, engineers, technicians and managers) by providing tools for:
- monitoring and controlling the process and the system;
- configuring control strategies and creating the system data base;
- history and archive of the process data;
- evaluating plant and operator performance.

The system has several multi-channel regulators that are connected by a star communicating network to a central computer.

The multi-channel regulator is a multiprocessor system, with four processors, which can access to a common data base, by a MULTIBUS, and to the same set of interfaces with the process. The first of them, P_1 (80x86), transmits the command values to controlled process, beginning from data acquisition to regulatory and advanced control (discrete PID algorithms, horizon predictive control, etc.), and also updates the common data base. It has 48 slots, which half of them are to analogue variables, and the others are to binary variables.

The second processor provides: the communication between the regulator computer and local equipments, direct and real-time access to process data needed by the operator. At the P1 processor failure, the P2 processor takes over the P2 tasks.

The third functional unit it is a sequential machine which assures the communication interface to higher level computer.

The last one assures the regulator's communication to automatic reservation system for fault-regulators, i.e. the communication with reservation regulator. Thus the system is fault-tolerant: the loss of the communication with higher level is compensated by manual control facility of the process, by the local operators. Also, the local console task can be compensated by the central operator.

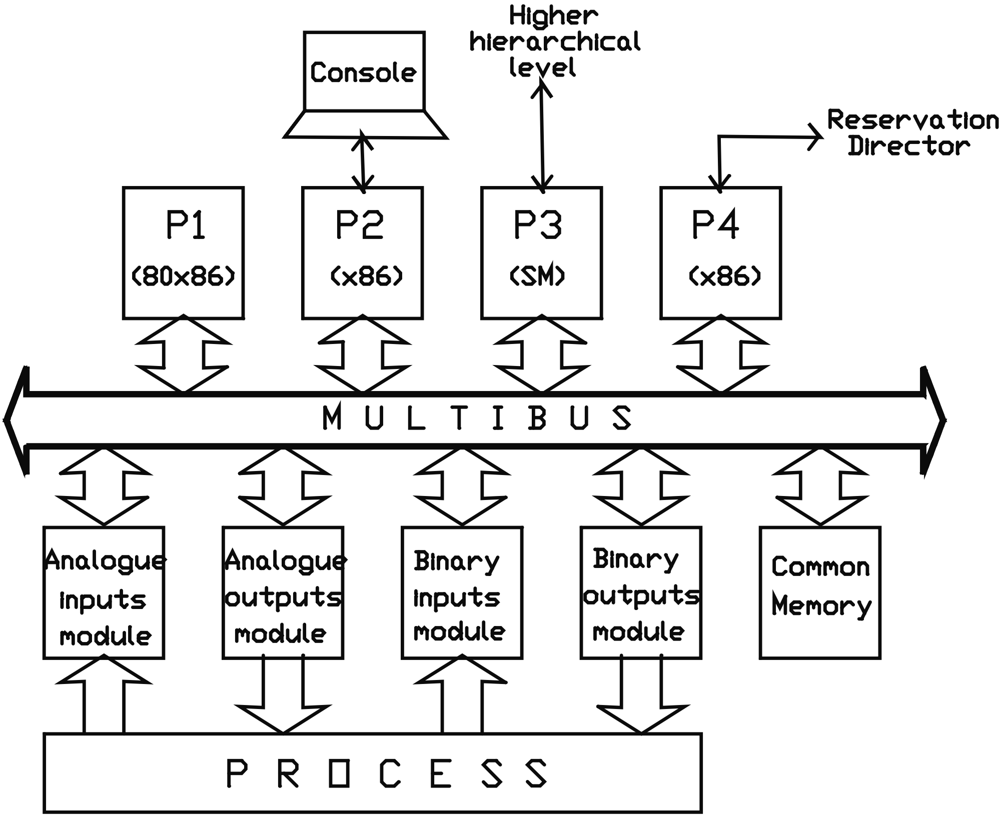


Fig. 6 - Lower level of a three level hierarchy structure

5. References

1. *V.Lungu, Gh. Petrescu*, Algoritmi si strucuri de date Editura Printech, 2011
2. *V. Lungu, Gh. Petrescu*, Programarea in C/C++, Ed. Printach,, 2010
3. *J. Zhao, C.H. Wang*, "Control system of the BEPCII", 8th International Conference on Accelerator & Large Experimental Physics Control Systems, 2001, San Jose, California
4. *J. Zhao et al*, "Preliminary Design of the Control System for SSRF and BTCF", ICALEPCS, 1997, Beijing, China.
5. *G. Palade, Gh. Petrescu*, " Logical design of an operator interface for a hierarchical management system", CSCS- Buc.,1989
6. *B.W. Arden, H. Lee*, "A regular network for multi-computer system" IEEE Trans. Comput ., C-31 , 1982.