ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE ENGINEERING AND TECHNOLOGY

ANALOG CIRCUIT DESIGN WITH NEW ACTIVE CIRCUIT COMPONENTS

M.Sc. THESIS

Ersin ALAYBEYOĞLU
(504111234)

Department of Electronics & Communications Engineering

Electronic Engineering Programme

Thesis Advisor: Prof. Dr. Hakan Kuntman

JUNE 2013

İSTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ

YENİ AKTİF DEVRE ELEMANLARIYLA ANALOG DEVRE TASARIMI

YÜKSEK LİSANS TEZİ

Ersin ALAYBEYOĞLU
(504111234)

Elektronik ve Haberleşme Mühendisliği Anabilim Dalı

Elektronik Mühendisliği Programı

Tez Danışmanı: Prof. Dr. Hakan KUNTMAN

HAZİRAN 2013

Ersin Alaybeyoğlu, a **M.Sc.** student of ITU **Graduate School of Science Engineering and Technology** student ID 504111234 , successfully defended the **thesis** entitled "**Analog Circuit Design With New Active Circuit Components**", which he prepared after fulfilling the requirements specified in the associated legislations, before the jury whose signatures are below.

Thesis Advisor :	**Prof. Dr. Hakan KUNTMAN** Istanbul Technical University	.....
Jury Members :	**Doç. Dr. Nil TARIM** Istanbul Technical University	.....
	Doç. Dr. Fırat Kaçar Istanbul University	.....

Date of Submission : 3 May 2013
Date of Defense : 6 June 2013

To my wife and my sons,

FOREWORD

First of all, I am grateful for directing all aspects of me in the preparation of the thesis study to my advisor, Prof. Dr. Hakan Kuntman.

New active elements CMOS realizations and their current-mode applications is presented in this thesis. The proposed CMOS realization and applications circuits were investigated with computer aided simulators. Advantages and weaknesses of the applications and CMOS circuits are discussed.

June 2013 Ersin ALAYBEYOĞLU

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ABBREVIATIONS

CDU	**:** Current Differencing Unit
CCII	**:** Second Generation Current Conveyor
CCIII	**:** Third Generation Current Conveyor
ECCII	**:** Electronically Controllable Second Generation Current Conveyor
OTA	**:** Operational Transconductance Amplifier
ZC-CDTA	**:** Z-Copy Current Differencing Transconductance Amplifier
ZC-CDBA	**:** Z-Copy Current Differencing Buffered Amplifier
ZC-CG-CDBA	**:** Z-Copy Controlled Gain Current Differencing Buffered Amplifier

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ANALOG CIRCUIT DESIGN WITH NEW ACTIVE CIRCUIT COMPONENTS

SUMMARY

The design of electronics which are indispensable for every area of our lives is mainly studied in two groups as analog circuit design and digital circuit design. The use of digital circuits compared to analog circuits is increasing day by day. Due to the creation of man and the universe, analog signal processing circuits and systems is inevitable. This inevitability shows us analog signal processing and analog signal processing circuits and systems are unavoidable despite the increase in the prevalence of digital systems and circuits.

Analog signal processing systems can be examined in two main groups as voltage-mode or current-mode circuits, in terms of operating principles. The voltage-mode circuits' input signal and the output signal is voltage. The input signal and the output signal are current in current mode circuits. Designs of this work have been tested with current-mode applications.

The design of electronic circuits facilitated with the discovery of the transistors. Nowadays, the sizes of electronic circuits are much smaller. CMOS 20nm gate length production can do as of 2013. However, the small size integrated circuit technologies that can be used easily in digital circuit design are not widely available in analog circuit design. The main reason for this is that analog processing blocks with small sized MOS transistors working with low supply voltages, does not allow all the transistors to operate in saturation mode. For this reason, the existing analog signal processing building blocks must be adapted to small size technologies. In this work, the simulations have been performed using 0.18μm AMS parameters.

In this work, the CMOS internal structure is proposed for ZC-CDTA (Z-Copy Current Differencing Transconductance Amplifier), ZC-CDBA (Z-Copy Current Differencing Buffered Amplifier) and ZC-CG-CDBA (Z-Copy Controlled Gain

Current Differencing Buffered Amplifier) which recently recommended as analog building blocks. Input stage of the ZC-CDTA, ZC-CDBA and the ZC-CG-CDBA consist of current differencing unit. Different current differencing unit CMOS structures are used in this work. Ideally, these elements of ZC-CDTA, ZC-CDBA and ZC-CG-CDBA input resistance were reduced with the help of positive feedback structure close to ideal. Application circuits designed by exploiting smaller value resistors allow the design of integrated circuit structures occupying less area.

CDU (current differencing unit), CCIII (third generation current conveyor), ECCII (electronically controllable second generation current conveyor), OTA (operational transconductance amplifier) and voltage buffer which form the structure of the proposed ZC-CDTA, ZC-CDBA and ZC-CG-CDBA analog building blocks' performances has been tested using CADENCE environment and the performances of these sub-circuits were presented in Chapter 2.

In Chapter 3, negative and positive feedbacks were discussed. The effect of positive and negative feedback to the input resistance were also examined. The structure of the ZC-CDTA, ZC-CDBA and ZC-CG-CDBA was proposed by putting together the analog sub-circuits in Chapter 4. The CCIII (third generation current conveyor) recommended by Alain Fabre was used for obtaining the Z copy terminal current which exists in the structures of ZC-CDTA, ZC-CDBA and ZC-CG-CDBA. The layout of the ZC-CDBA, the ZC-CDTA and the post-layout simulations are given in Chapter 5. A second order KHN filter structure realized with ZC-CDBA, a biquad filter structure realized with ZC-CDTA and frequency agile filter realized with ZC-CG-CDBA were presented in Chapter 6. Also, a frequency agile filter structure realized with ZC-CDTA and ECCII is given in Chapter 6. All works were concluded in Chapter 7.

YENİ AKTİF DEVRE ELEMANLARIYLA ANALOG DEVRE TASARIMI

ÖZET

Hayatımızın her alanının vazgeçilmezi olan elektronik düzenlerin tasarımı temel olarak sayısal devre tasarımı ve analog devre tasarımı olarak iki grupta incelenir. Sayısal devrelerin kullanımı analog devrelere kıyasla gün geçtikçe daha da artmaktadır. İnsanın ve kainatın yaratılışı gereği analog işaret işleyen devre ve sistemler kaçınılmazdır. Bu kaçınılmazlığın sebebi evrende var olan tüm varlıkların ve insanın duyularının analog işaretleri algılayabilmeleridir. Bu da bize sayısal sistem ve devrelerin yaygınlığının artmasına rağmen analog işaret işlemenin ve analog işaret işleyen devre ve sistemlerin tasarlanmasının kaçınılmaz olduğunu göstermektedir.

Analog işaret işleyen sistemler çalışma prensibi bakımından gerilim modlu veya akım modlu devreler olarak iki ana grupta incelenebilir. Gerilim modlu devrelerde giriş işareti ve çıkış işareti gerilimdir. Akım modlu devrelerde ise giriş işareti ve çıkış işareti akımdır. Akım modlu çalışma denilince devrede sadece akım bağıntılarının var olduğu akla gelmemelidir. Elbetteki akım modlu devrelerde gerilim, gerilim modlu devrelerde de ise akımdan söz edilebilir. Temel olarak akım modlu devrelerde işaret akım ile taşındığı için düşük empedanslı düğümler vardır. Düşük empedanaslı düğümler zaman sabitini küçülttüğü için işaret daha hızlı taşınabilmektedir. Temel olarak bu sebepden dolayı akım modlu devreler gerilim modlu devrelere kıyasla daha yüksek bir performans ile çalışmaktadır. Bu çalışmadaki tasarımlar akım modlu uygulamalar ile test edilmiştir.

Transistorun keşfedilmesiyle elektronik devrelerin tasarlanması kolaylaşmış bir o kadar da elektronik devrelerin boyutu küçülmüştür. 2013 yılı itibariyle 20nm geçit uzunluğunda CMOS üretimi yapılabilmektedir. Ancak sayısal devre tasarımında kolaylıkla kullanılabilen küçük boyutlu tüm devre teknolojileri analog devre tasarımlarında yaygın olarak kullanılamamaktadır. Bunun temel sebebi düşük

besleme gerilimleri ile çalışan küçük boyutlu MOS transistorlar ile tasarlanan analog işlem bloklarında besleme gerilimi bütün transistorların doymada çalışmasına olanak sağlamamasıdır. Oysa analog işaret işleyen devrelerde bütün transistorların doymada çalışması gerekmektedir. Bu sebeple mevcut analog işlem bloklarının yeniden düzenlenilerek küçük boyutlu teknolojilere uygun hale getirimesi gerekmektedir. Biz çalışmalarımızda 0.18µm AMS parametrelerinden yararlanarak benzetimlerimizi gerçekleştirdik.

Çalışmada temel olarak yakın zamanda önerilmiş analog işlem blokları olan ZC-CDTA (Z kopyalı akım farkı alan geçiş iletkenliği kuvvetlendiricisi) ve ZC-CDBA (Z kopyalı akım farkı alan tamponlanmış kuvvetlendirici) ve ZC-CG-CDBA (Z kopyalı kazancı kontrol edilebilir akım farkı alan tamponlanmış kuvvetlendirici) elemanları için CMOS iç yapısı önerildi ve önerilen iç yapılar uygulama devreleri ile test edildi. ZC-CDTA, ZC-CDBA ve ZC-CG-CDBA aktif elemanları CDTA (akım farkı alan geçiş iletkenliği kuvvetlendiricisi) ve CDBA (akım farkı alan tamponlanmış kuvvetlendirici) yapılarından geliştirilmişlerdir ve CDTA ile CDBA'nın evrenselliğini artırmaktadırlar.

Önerilen ZC-CDTA, ZC-CDBA ve ZC-CG-CDBA analog işlem bloklarının yapısını oluşturan CDU (farksal akım bloğu), CCIII (üçüncü nesil akım taşıyıcı), ECCII (elektronik olarak kontrol edilebilen ikinci nesil akım taşıyıcı), OTA (geçiş iletkenliği kuvvetlendiricisi) ve gerilim tamponunun başarımları CADENCE ortamında denemiş ve başarımları çalışmanın ikinci kısmında sunulmuştur. ZC-CDTA, ZC-CDBA ve ZC-CG-CDBA'nın giriş katı akım farkı alan blokdan oluşur. Bu kısımda iki farklı akım farkı alan CMOS iç yapı ve başarımları verildi. OTA yapısı olarak kullanılan yüzen akım kaynağı ZC-CDTA'nın çıkış katında, gerilim tamponu ZC-CDBA ve ZC-CG-CDBA'nın çıkış katında kullanıldı. ZC-CDTA, ZC-CDBA ve ZC-CG-CDBA analog işlem bloklarının yapısındaki Z kopyayı elde etmek için Alain Fabre tarafından önerilen CCIII (üçüncü nesil akım taşıyıcı) kullanılmıştır. ECCII ise akım kazancını kontrol etmek için kullanıldı.

Üçüncü kısımda ise negatif ve pozitif geribeslemeden bahsedilmiştir. Pozitif ve negatif geri beslemenin giriş direncine etkisi incelenmiştir. İdealde giriş direnci sıfır olan bu elemanların giriş direnci pozitif geri besleme yardımıyla ideale yakın azaltıldı. Tasarlanan uygulama devrelerini daha küçük değerli dirençler ile

gerçekleyerek daha az alan kaplayan tüm devre yapılarının tasarlanabilmesine olanak sağlanmış oldu. Bu kısımda ikinci kısımda verilen akım farkı alan bloklar ile pozitif geri besleme ile gerçeklenen CMOS yapıların başarımları kıyaslandı.

Çalışmanın dördüncü bölümünde analog alt bloklar bir araya getirilerek ZC-CDTA, ZC-CDBA ve ZC-CG-CDBA analog işlem bloklarının yapısı oluşturulmuştur.

Çalışmanın beşinci bölümde ZC-CDBA ve ZC-CDTA CMOS yapılarının serimi verişmiştir. Bu kısımda ZC-CDBA CMOS gerçeklemesinde Z akımını kopyalamak için üçüncü nesil akım taşıyıcı yerine klasik akım aynası kullanılmıştır.

Çalışmanın son kısmında uygulama devreleri ile yeni analog işlem bloklarının başarımı test edimiştir. ZC-CDTA (Z kopyalı akım farkı alan geçiş iletkenliği kuvvetlendiricisi) ile iki tane ikinci derecede süzgeç yapısının ardarda bağlanılmasıyla dördüncü derece süzgeç yapısı elde edilmiştir. ZC-CDBA (Z kopyalı akım farkı alan tamponlanmış kuvvetlendirici) CMOS iç yapısı performansı ikinci derece KHN süzgeç yapısı ile test edilmiştir. Yine ZC-CDBA CMOS iç yapısı elektronik olarak kontrol edilebilen ikinci nesil akım taşıyıcı yardımıyla ZC-CG-CDBA (Z kopyalı kazancı kontrol edilebilir akım farkı alan tamponlanmış kuvvetlendirici) yapısına dönüştürülmüştür. ZC-CDBA için tasarlanan ikinci derece KHN süzgeç yapısı ZC-CG-CDBA ile tekrar gerçeklenmiştir. Bu şekilde kutuplama akımı ile kesim frekansı değişebilen frekans atik süzgeç yapısı elde edilmiştir. Aynı kısımda ZC-CG-CDBA ile elde edilen frekans atik süzgeç yapısının eksik yönleri değerlendirilmiştir.

Son bir uygulama olarak ZC-CDTA ikinci derece süzgeç yapısı geri besleme kullanılarak frekans atik süzgeç yapısına dönüştürülmüştür. Alain Fabre ve ekibi tarafından önerilen gerilim modlu geri besleme yapısı akım modlu yapıya dönüştürülmüştür. Akım modlu olarak tasalanan kurgulanabilir süzgeç yapısı merkez frekansı ECCII yardımıyla akım ile kontrol edilebilmektedir. Tasarlanan frekans atik süzgeç yapılarının kavramsal radyo, şifreli haberleşme, geniş kapsamlı konumlandırma sistemleri gibi uygulama alanlarında kullanılabileceği öngörülmüştür.

Tasarım kütüphanesi tarafından önerilen tüm testler ve benzetim setleri serim sırasında ve serim sonrası benzetimlerde uygulanmıştır. Önerilen yapıların analog tasarımcılar için alternatif oluşturacağı düşünülmektedir.

1. INTRODUCTION

Operational amplifiers have been used as fundamental circuit components in analog circuit design since the emergence of integrated circuits. After the emergence of new analog circuit applications, the voltage-mode operational amplifiers performance characteristics are not enough for analog signal processing requirements. The compensation capacitance which provides the stability of the OP-AMP reduces the bandwidth of the operational amplifier due to expected excessive voltage gain from the OP-AMP [1, 2, 3].

Those voltage mode circuits that have high-impedance nodes draw large time constants of the circuit help to reduce the operation frequency with parasitic capacitance. Current-mode circuits that have low impedance nodes do not have these type of problems. As a result, the suitability of current-mode applications operating on wide-band is higher than voltage mode counterpart.

Nowadays, power consumption is the most important design criteria for analog applications. Especially the portable cell phone, laptop, mp3 player production that operates with low power is necessary for long time using. In particular, the low supply voltage of digital applications significantly reduces the power consumption. In the case of the design of analog and digital structures in the same chip, digital blocks and analog blocks are obliged to align. Current mode approach is the biggest advantages of easier design of circuits in accordance with the low supply voltages [4].

1.1 Purpose of Thesis

Nowadays, although digital circuits and systems became prominent in electronic applications, analog circuit structures and systems are continuing to be important. The main reason is the signals in the nature are continuous-time analog signals. Human senses and the brain process only continuous-time analog signals. Thus, analog structures are inevitable considering the human factor. In addition, some of

the signals sometimes become difficult and expensive to process digitally and analog electronic circuits and systems are required anyway. For example, a speaker can be considered. Such a practice, the function realized with digital building block is very difficult and expensive, or even impossible to implement digitally. That in many applications, such as the need for analog circuit structures today's modern electronic devices are produced as a combination of analog and digital circuits. For the realization of such a mixed system which successfully adapts to high-performance digital blocks, analog circuit structures must be designed.

In this work, different type of current mode filter structure and its CMOS realization for narrow band pass tuned amplifiers such as video signal processing, TV receivers, cognitive communication, encrypted communication and wireless communications stages is proposed.

1.2 Literature Review

CCI (first generation current conveyor) is proposed by Sedra A. and Smith K. C. in 1968 is known as the beginning of the current mode application [5]. After a short time CCII (second generation current conveyor) is proposed by Sedra A. and Smith K. C. in 1970 [6]. Today, when it is said current conveyor second generation current conveyor is understood. The third generation current conveyor is presented by Fabre A. in 1995 [7].

CDBA (current differencing buffered amplifier) is proposed by Acar C. and Ozoğuz S. as a current mode building block in 1999 [8]. CDTA (current differencing transconductance amplifier) is submitted by Biolek D. in 2003 [9]. ZC-CDBA (Z-copy current differencing buffered amplifier) and ZC-CDTA (Z-copy current differencing transconductance amplifier) is also proposed by Biolek D in 2008 [10]. The ZC-CDBA, ZC-ZDTA and ZC-CG-CDTA increase the universality of the CDBA and CDTA.

2. THE BUILDING BLOCKS

The basic building blocks CDU (Current Differencing Unit), CCIII (Third Generation Current Conveyor), OTA (Operational Transconductance Amplifier), Voltage Buffer, ECCII (Electronically Controllable Second Generation Current Conveyor) simulation results, CMOS realization and performance parameters will be given in this chapter. The performances of these building blocks are investigated in CADENCE 0.18µm AMS parameters.

2.1 CDU(Current Differencing Unit)

In current mode analog design, the unity gain current differencing block is widely used at the input stage. For example, Current Differencing Buffered Amplifier, Current Differencing Transconductance Amplifier, Current Operational Amplifier, etc. input stage consist of unity gain current differencing unit. The current differencing unit has ideally two zero impedance input impedances and one infinite output impedance.

The current differencing unit can be realized with two positive second generation current conveyors as seen Figure 2.1. But, this structure contains lots of transistors and the parasitics narrow the available frequency region. Two alternative current differencing structures are presented in this chapter. Also, another low impedance current differencing unit realized with positive feedback is presented in the Chapter 3.

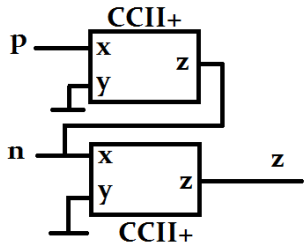

Figure 2.1 : Current differencing unit realized with CCII+ [3].

2.1.1 The First Current Differencing Unit Structure

The first current differencing unit CMOS structure schematic view is shown in Figure 2.2. This structure also is known as "Differential Current Controlled Current Source" (DCCCS). In Table 2.1, the performance parameters of the first current differencing unit CMOS structure are seen. The size of the transistors is shown in Table 2.2. The bias currents I_{b1} and I_{b2} are selected 100µA. The bias voltages are selected as V_{b1}=-600mV and V_{b2}=600mV.

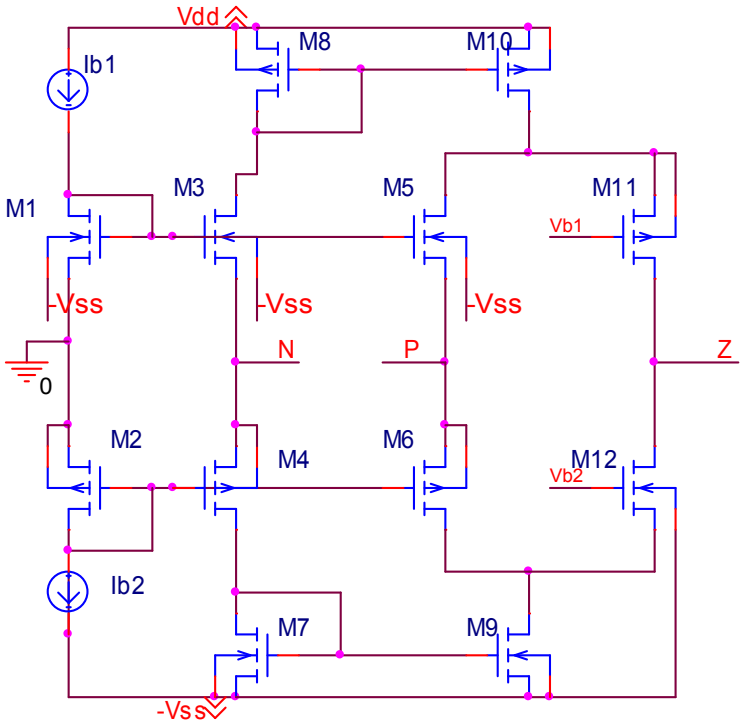

Figure 2.2 : The first current differencing unit CMOS structure [11].

The defining equation of the current differencing unit is given in Equation 2.1.

$$I_z = I_p - I_n \tag{2.1}$$

The change of the output terminal current according to P terminal input current and N terminal input current are given in Figure 2.3 and Figure 2.4. The Z terminal current dynamic range was found between -100µA, 100µA. The frequency responses of the input impedances at P and N terminals and the output impedance at Z terminal are given in Figure 2.5, 2.6, 2.7, respectively.

The input impedances for proposed current differencing unit at P and N input terminal were found 600.248Ω, 233.798Ω, respectively. The output impedance at Z terminal was found 129.529kΩ. The bandwidth ratio of the Z terminal current respect to P and N terminal currents are given in Figure 2.8, 2.9, respectively.

Table 2.1 : Simulation results of the first current differencing unit structure.

Power Supply	±0.9V
Z terminal current dynamic range	-100µA ≤ Iz ≤ 100µA
Iz/In (-3dB) bandwidth	540.335MHz
Iz/Ip (-3dB) bandwidth	692.879MHz
P terminal input impedance	600.248Ω
N terminal input impedance	233.798Ω
Z terminal output impedance	129.529kΩ
Current tracking error (%)	1,04
Power Consumption	256.45µW

Table 2.2 : Transistors size of the first current differencing unit structure.

Transistors	(W/L)
M1,M2	72µ/0.36µ
M3,M4	144µ/0.36µ
M5,M6,M7,M8,M9,M10,M11,M12	72µ/0.36µ

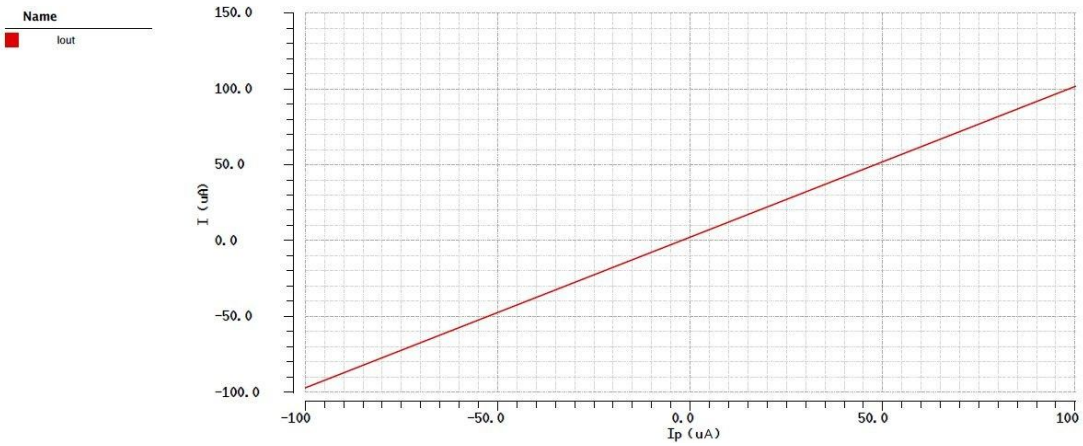

Figure 2.3 : The output terminal current according to the P terminal input current.

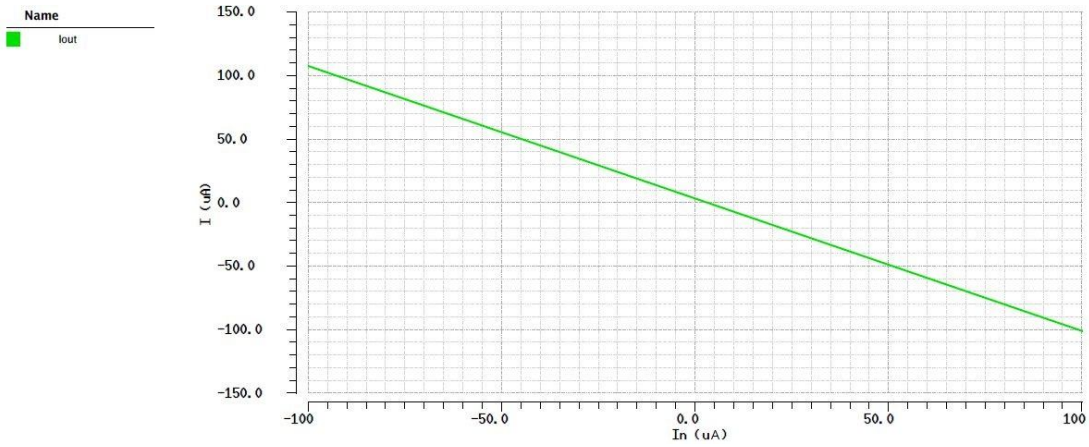

Figure 2.4 : The output terminal current according to the N terminal input current.

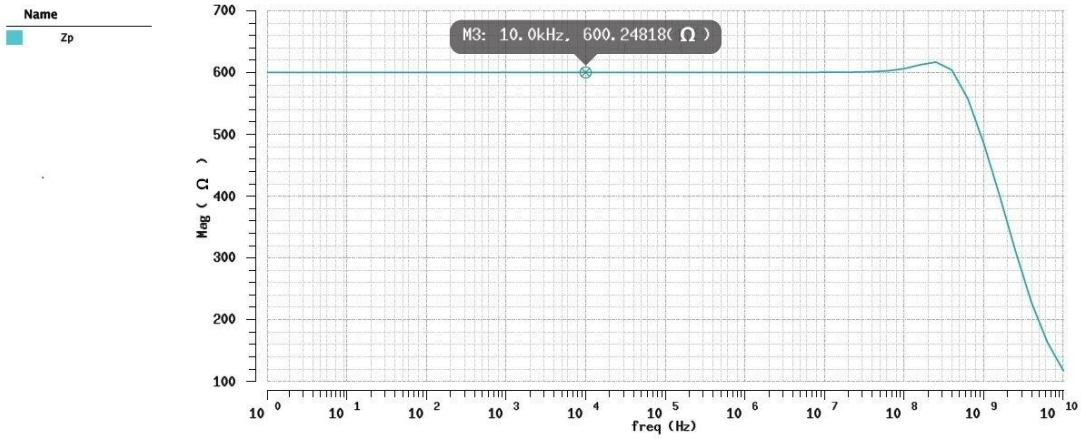

Figure 2.5 : The frequency response of the input impedance at P.

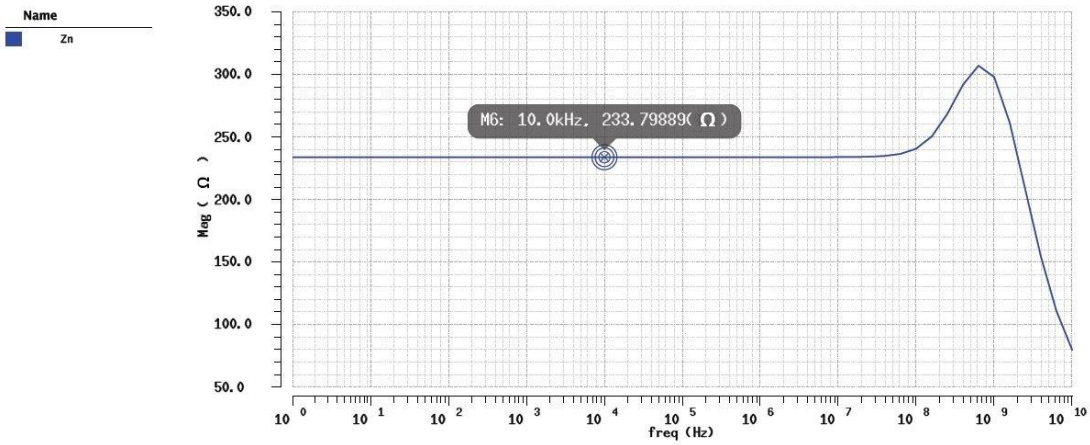

Figure 2.6 : The frequency response of the input impedance at N.

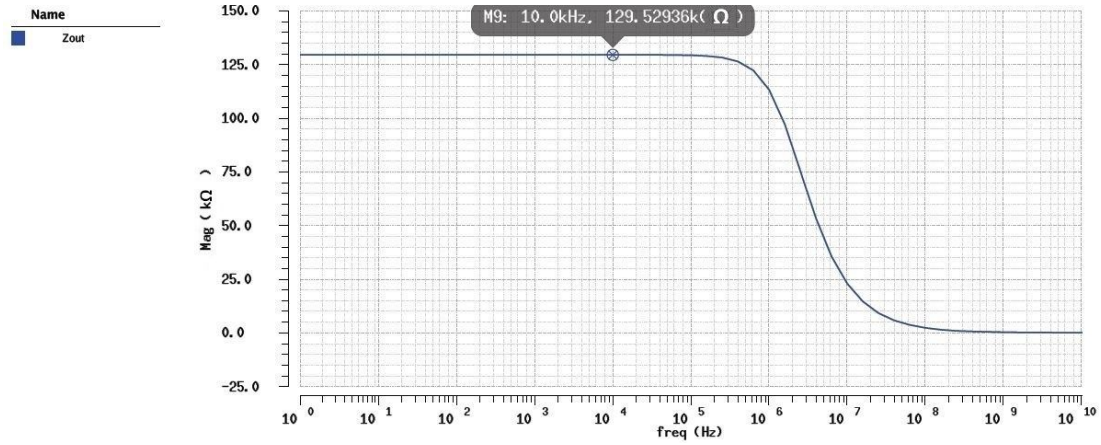

Figure 2.7 : The frequency response of the output impedance at Z.

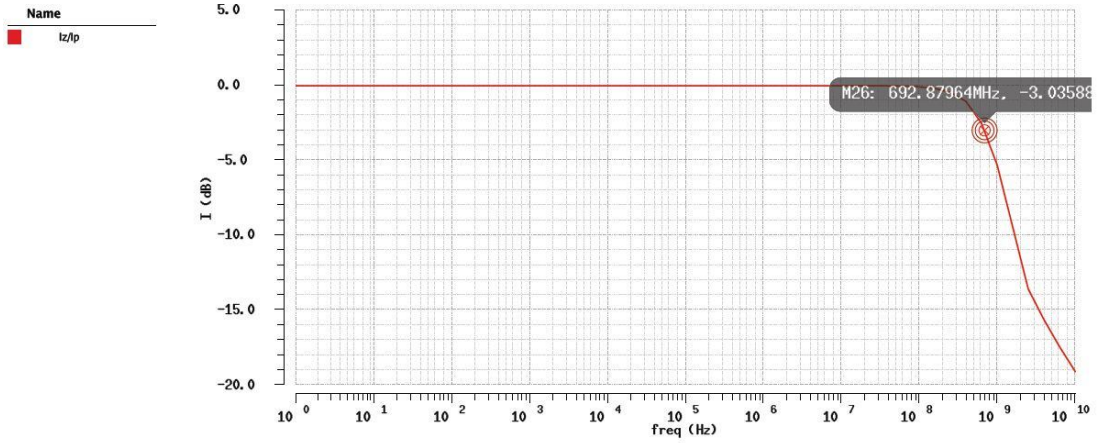

Figure 2.8 : The bandwidth ratio of the Z terminal current respect to P.

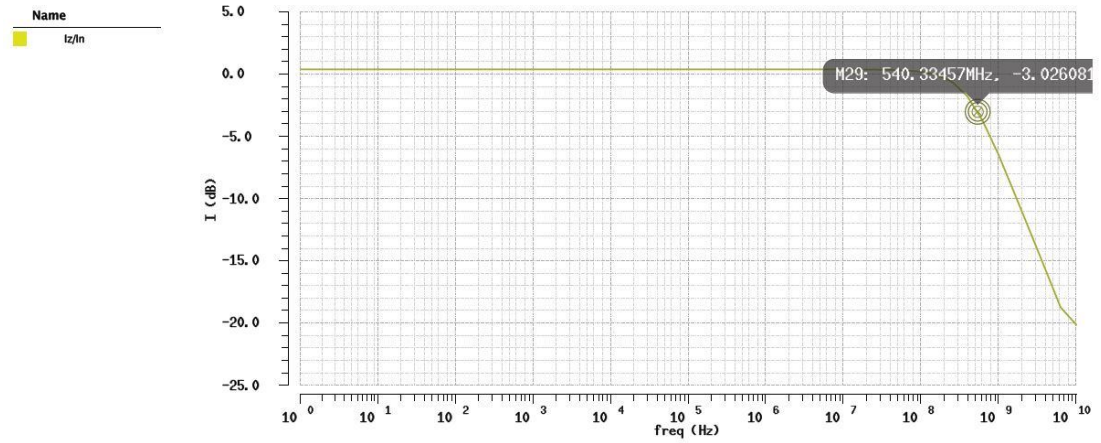

Figure 2.9 : The bandwidth ratio of the Z terminal current respect to N.

2.2 The Second Current Differencing Unit Structure

The current differencing unit CMOS realization used in ZC-CDTA, ZC-CDBA and ZC-CG-CDBA is given in Figure 2.10. In Table 2.3 the performance parameters of the circuit is seen. The size of transistors is shown in Table 2.4. The bias currents of I_{b1} and I_{b2} are 100µA. The defining equation of the CMOS structure is given in Equation 2.2.

$$I_z = I_p - I_n \tag{2.2}$$

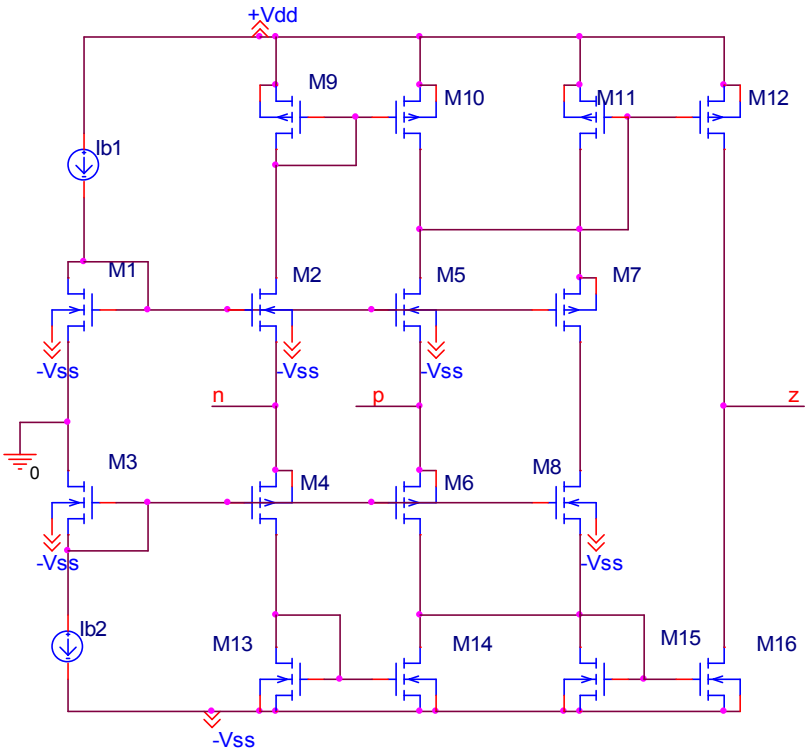

Figure 2.10 : The second current differencing unit CMOS structure [12].

Table 2.3 : Simulation results of the second current differencing unit structure.

Power Supply	±0.9V
Z terminal current dynamic range	-28µA ≤ Iz ≤ 28µA
Iz/In (-3dB) bandwidth	354,774MHz
Iz/Ip (-3dB) bandwidth	417.224MHz
P terminal input impedance	6.206kΩ
N terminal input impedance	4.273kΩ
Z terminal output impedance	295.682kΩ
Current tracking error (%)	1,86
Power Consumption	189.35µW

Table 2.4 : Transistors size of the second current differencing unit structure.

Transistors	(W/L)
M1,M2,M5,M7	0.36µ/0.36µ
M3,M4,M6	1.4µ/0.36µ
M8,M15,M16	3.5µ/0.36µ
M9,M10,M11,M12,M13,M14	14µ/0.36µ

The change of output terminal current according to the P terminal input current and N terminal input current are given in Figure 2.11 and Figure 2.12. The Z terminal current dynamic range was found between -28µA, 28µA. The frequency responses of the input impedances at P and N terminals and the output impedances at Z terminal are given in Figure 2.13, 2.14, 2.15, respectively.

The input resistances for proposed current differencing unit at P and N input terminal were found 6.206kΩ, 4.273kΩ, respectively. The output resistance at Z terminal was found 295.682kΩ. The bandwidth of the ratio Z terminal current respect to P and N terminal current are given in Figure 2.16, 2.17, respectively.

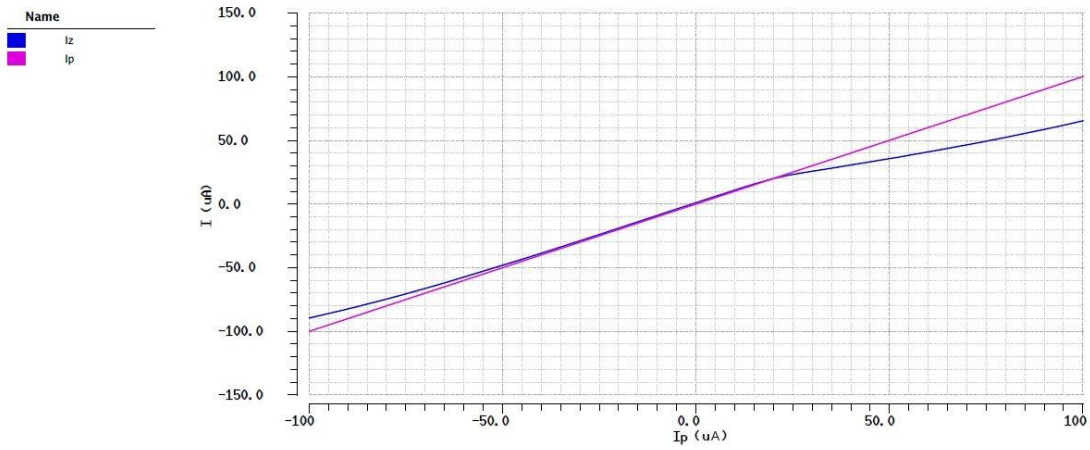

Figure 2.11 : The output terminal current according to the P terminal input current.

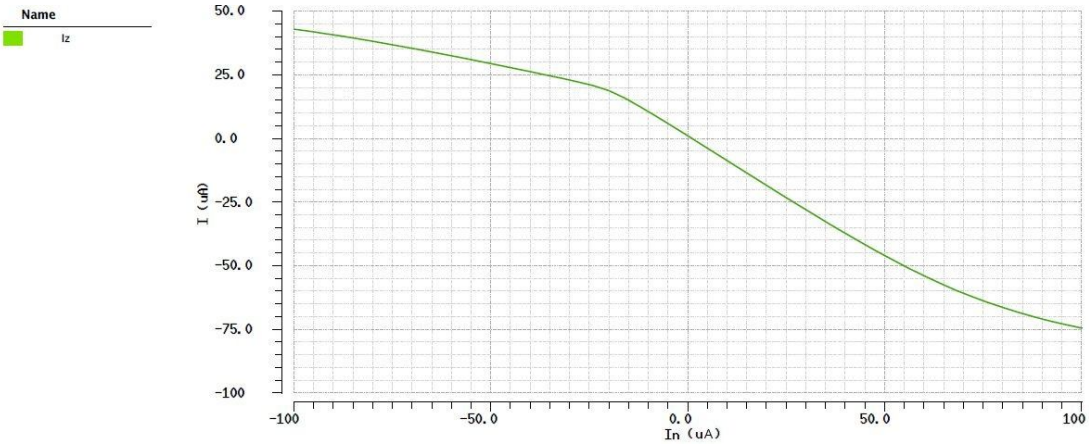

Figure 2.12 : The output terminal current according to N terminal input current.

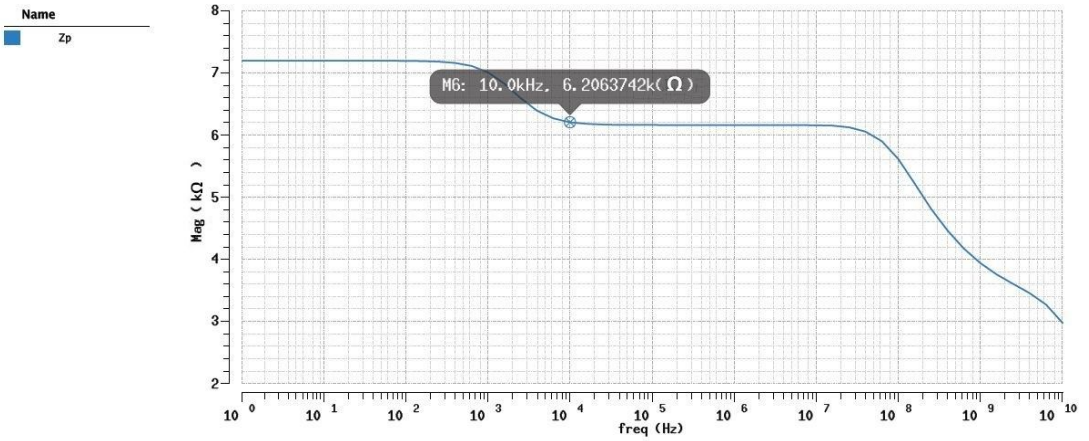

Figure 2.13 : The frequency response of the input impedance at P.

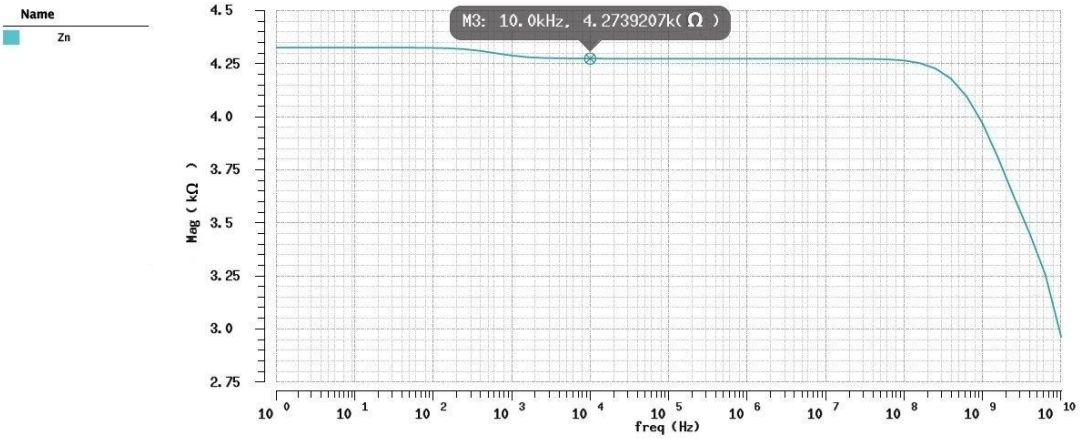

Figure 2.14 : The frequency response of the input impedance at N.

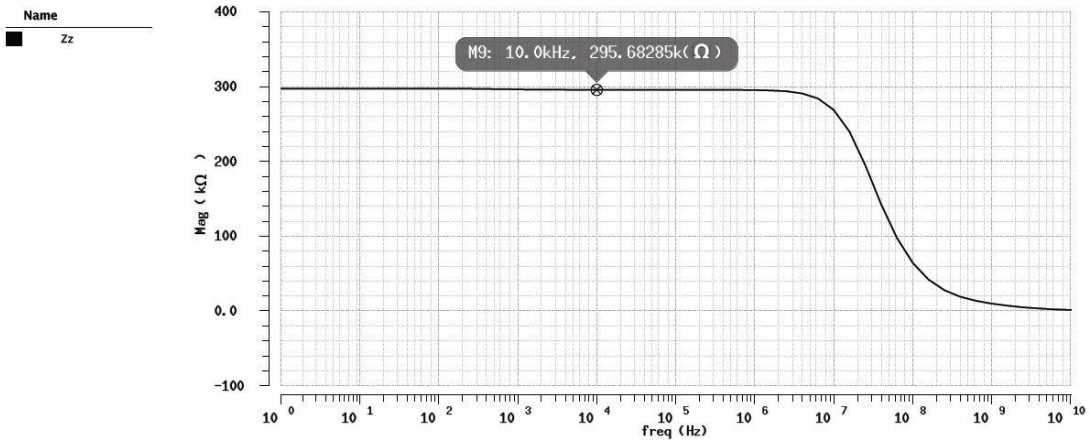

Figure 2.15 : The frequency response of the output impedance at Z.

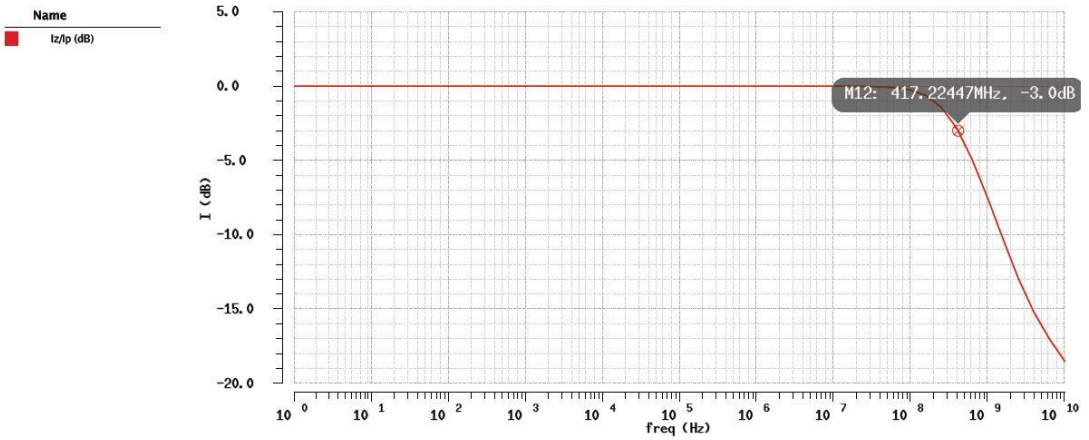

Figure 2.16 : The bandwidth of the ratio Z terminal current respect to P.

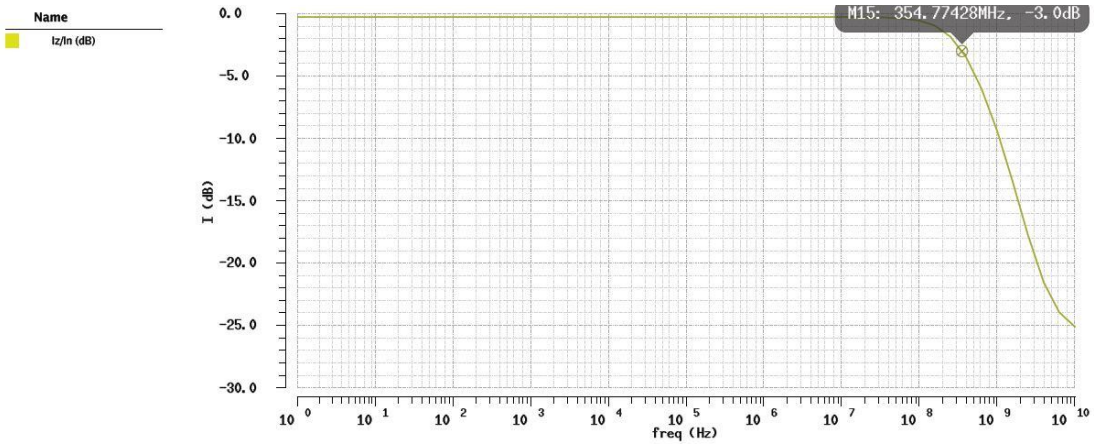

Figure 2.17 : The bandwidth of the ratio Z terminal current respect to N.

2.3 CCIII(Third Generation Current Conveyor)

An ideal third generation current conveyor is shown in Figure 2.18. The defining equation matrix is given in Equation 2.3. The basic formulas of the CCIII are given in Equation 2.4, 2.5, 2.6, respectively.

Only two classes of output currents can be found; some flows directly to ground through two port elements and the others flow through floating branches. To be usable, these output signals have to be taken out of the circuit, so they must be available at high impedance to drive. It is not very easy to copy the current flowing through floating branches. For these purpose the third generation current conveyor is used to copying the z terminal current.

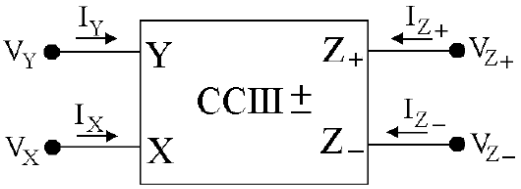

Figure 2.18 : CCIII (The third generation current conveyor) [7].

$$\begin{pmatrix} I_Y \\ V_X \\ I_{Z+} \\ I_{Z-} \end{pmatrix} = \begin{pmatrix} 0 & -1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & -1 & 0 & 0 \end{pmatrix} \begin{pmatrix} V_Y \\ I_x \\ V_{Z+} \\ V_{z-} \end{pmatrix} \quad \textbf{(2.3)}$$

$$V_X = V_Y \quad \textbf{(2.4)}$$

$$I_Y = -I_X \quad \textbf{(2.5)}$$

$$I_{Z+} = -I_{Z-} = I_X \quad \textbf{(2.6)}$$

The third generation current conveyor CMOS structure is shown in Figure 2.19. The simulation results of the CCIII and the transistors size are given in Table 2.5 and 2.6, respectively.

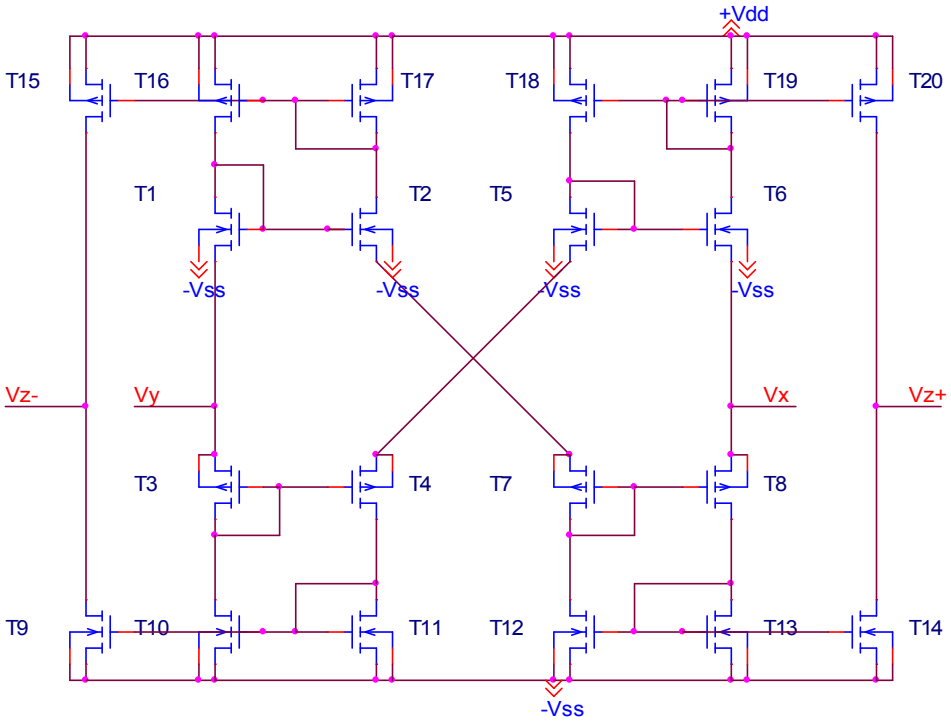

Figure 2.19 : The third generation current conveyor CMOS structure [13].

The change of Z+, Z- terminal currents according to the X terminal current is given in Figure 2.20 and Figure 2.21, respectively. Z+,Z- terminal currents dynamic range are found between -97µA and 97µA. The change of X terminal voltage respect to the Y terminal voltage is shown in Figure 2.22. X terminal voltage dynamic range is found between -230mV and 230mV. The X terminal input impedance, the Y terminal input impedance and Z output terminal impedances are given in Figure 2.23, 2.24, 2.25, 2.26, respectively.

The bandwidth of the Vx/Vy, the X terminal input impedance, Y terminal input impedance, the Z+ output terminal impedance and the Z- output terminal impedance of the third generation current conveyor were found 648.816MHz, 131.772Ω, 539.613Ω, 62.285kΩ, 82.339kΩ, respectively. The X and Y terminal input impedance is appropriate for current copying. The bandwidth of the ratio Z+, Z- terminal current respect to X terminal current are given in Figure 2.27, 2.28, respectively.

Table 2.5 : Third generation current conveyor simulation results.

Power Supply	±0.9V
Z+,Z- terminal currents dynamic range	-97µA ≤ Iz ≤ 97µA
Vx/Vy (-3dB) Bandwidth	648.816MHz
X terminal voltage dynamic range	-230mV ≤ Iz ≤ 230mV
Y terminal input impedance	539.613Ω
X terminal input impedance	131.772Ω
Z- terminal output impedance	82.339kΩ
Z+ terminal output impedance	62.285kΩ
Current tracking error (%)	0,84
Power Consumption	240.56µW
Z+ terminal bandwidth	65.934MHz
Z- terminal bandwidth	41.283MHz

Table 2.6 : Third generation current conveyor transistors sizes.

Transistors	**(W/L)**
T1,T2,T5,T6,T9,T10	36µ/0.36µ
T11,T12,T13,T14	36µ/0.36µ
T3,T4,T7,T8,T15,T16	12µ/0.36µ
T17,T18,T19,T20	12µ/0.36µ

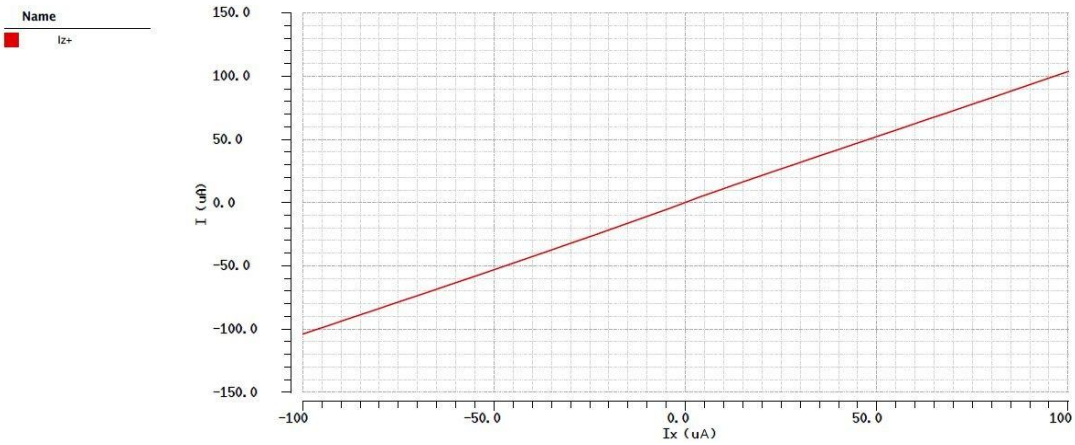

Figure 2.20 : The change of Z+ terminal current according to X terminal current.

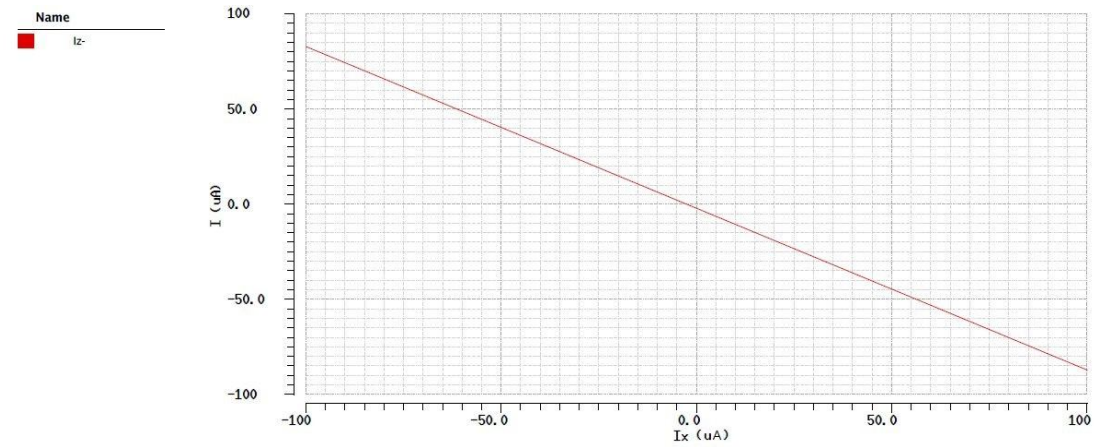

Figure 2.21 : The change of Z- terminal current according to X terminal current.

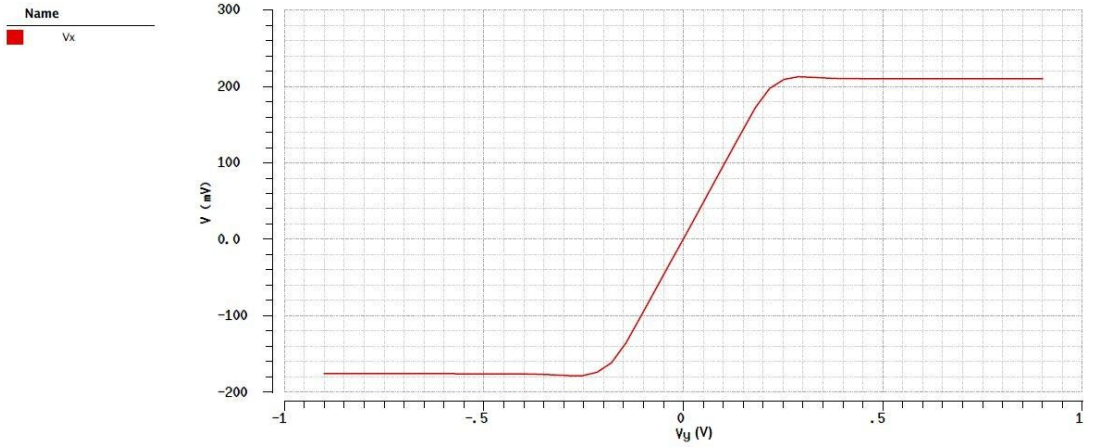

Figure 2.22 : The change of X terminal voltage respect to the Y terminal voltage.

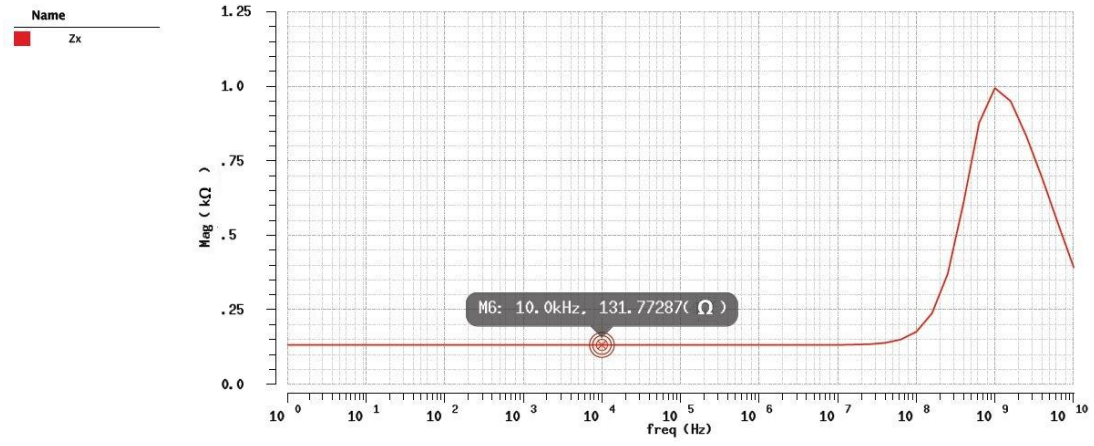

Figure 2.23 : The frequency response of the input impedance at X.

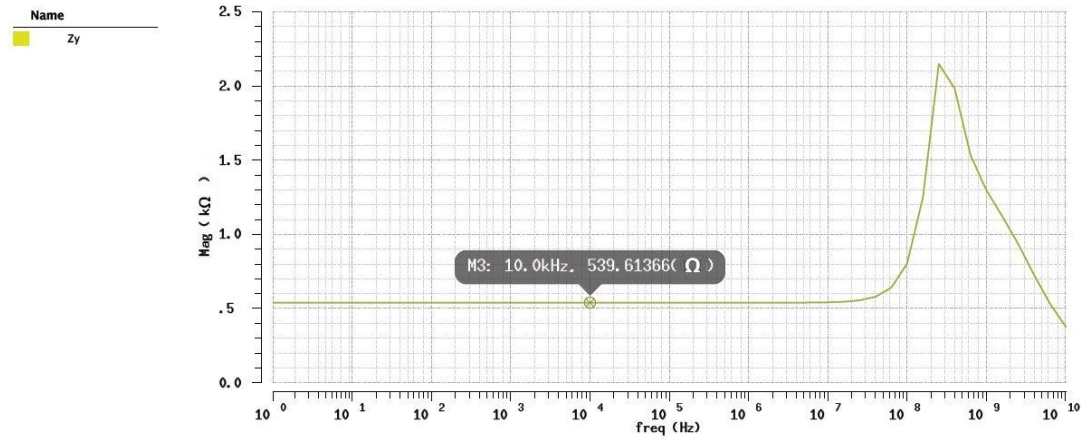

Figure 2.24 : The frequency response of the input impedance at Y.

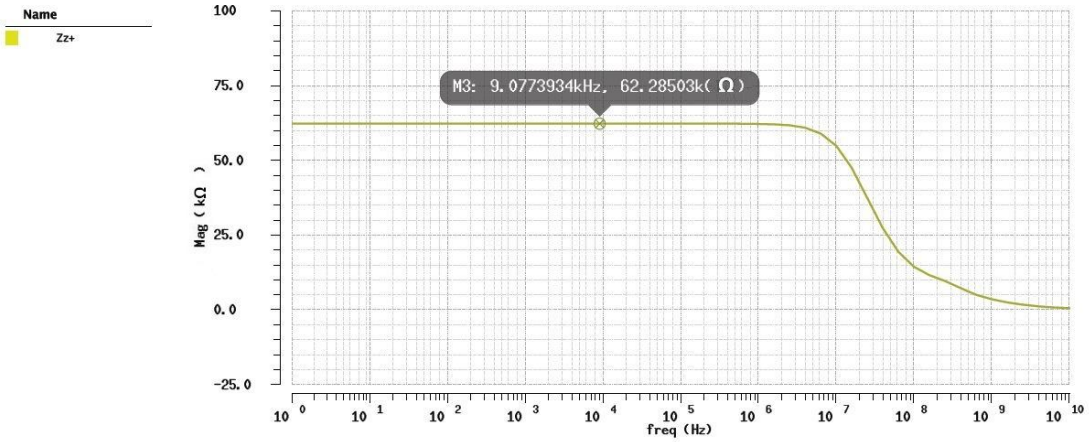

Figure 2.25 : The frequency response of the output impedance at Z+.

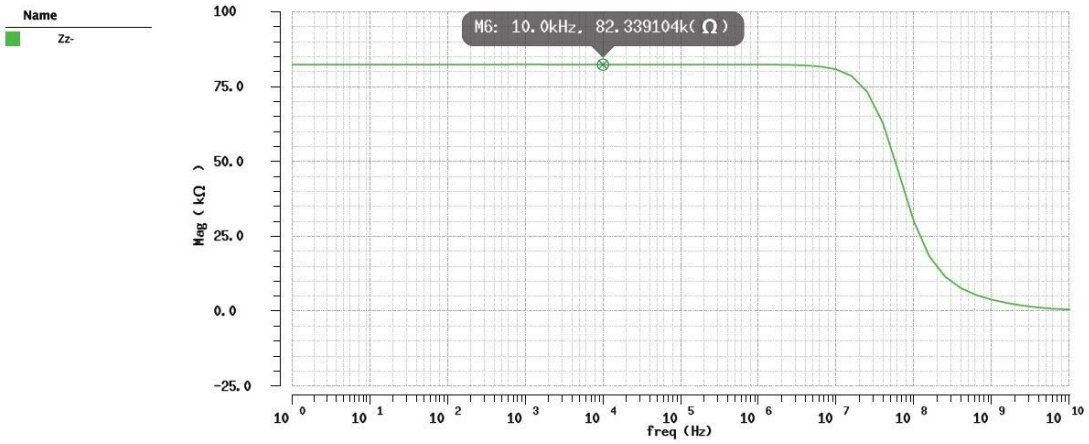

Figure 2.26 : The bandwidth of the ratio Z terminal current respect to N.

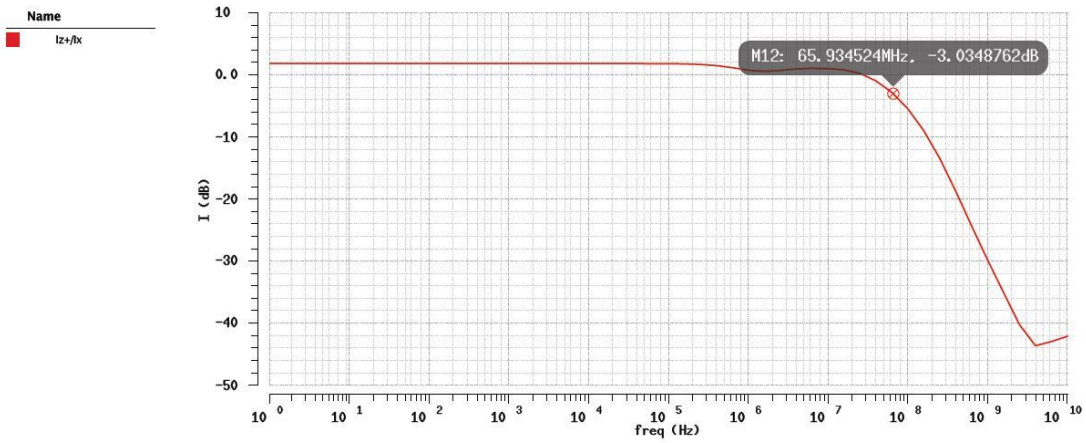

Figure 2.27 : The bandwidth of the ratio Z+ terminal current respect to X terminal current.

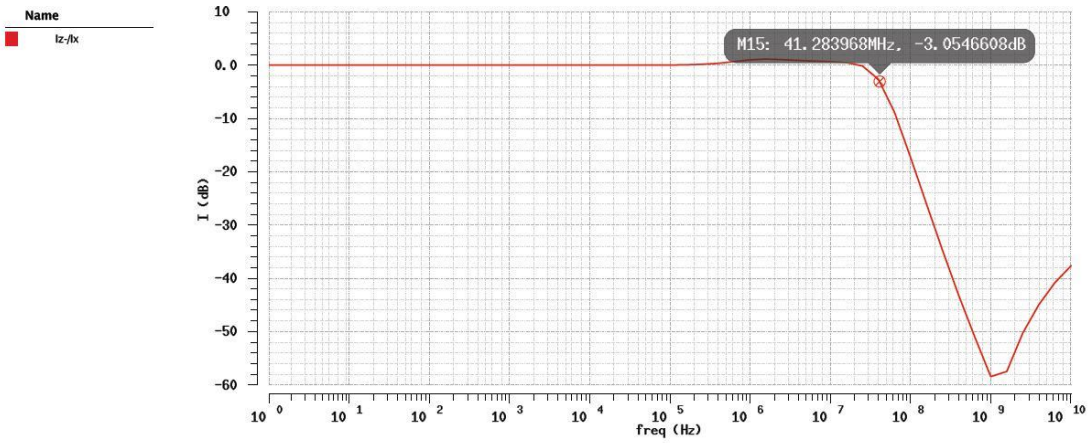

Figure 2.28 : The bandwidth of the ratio Z- terminal current respect to X terminal current.

2.3 OTA(Operational Transconductance Amplifier)

The input of an operational transconductance amplifier is voltage and the output is current. Hence the input impedance must be high (ideally infinite) and the output impedance must be low (ideally zero). Floating current source proposed by Arbel and Goldminz is used as a dual output operation transconductance amplifier in this work [14].

The CMOS structure of the floating current source is shown in Figure 2.29. The simulation results of the floating current source and the transistors size are given in Table 2.7 and 2.8, respectively. The bias currents I_{b1} and I_{b2} are selected 100µA.

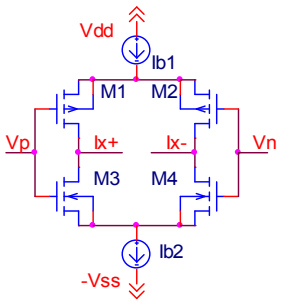

Figure 2.29 : The floating current source CMOS structure [14].

The transconductance simulations, g_m value and the output terminal impedances are given in Figure 2.30, 2.31, 2.32, 2.33, respectively. The defining equation of the CMOS structure is given in Equation 2.7.

$$I_{Z+} = g_m(V_p - V_n)\,,\; I_{Z-} = -g_m(V_p - V_n) \qquad \textbf{(2.7)}$$

Table 2.7 : Floating current source simulation results.

Power Supply	±0.9V
g_m	51.773µA/V
The input voltage dynamic range	±210mV
Z- terminal output impedance	256.480kΩ
Z+ terminal output impedance	256.480kΩ
g_m bandwidth	9.917GHz

Table 2.8 : Transistors sizes of the floating current source.

Transistors	(W/L)
M1,M2,M3,M4	16µ/0.36µ

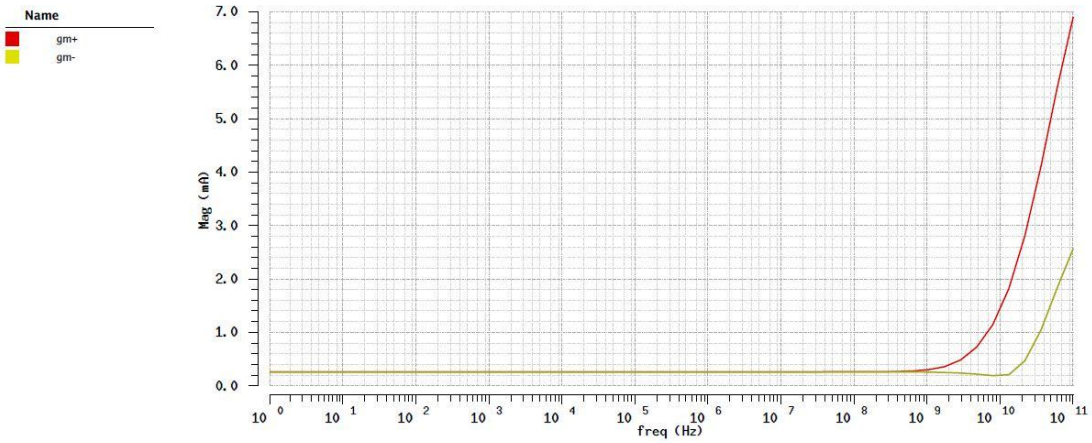

Figure 2.30 : The transconductance (g_m) value.

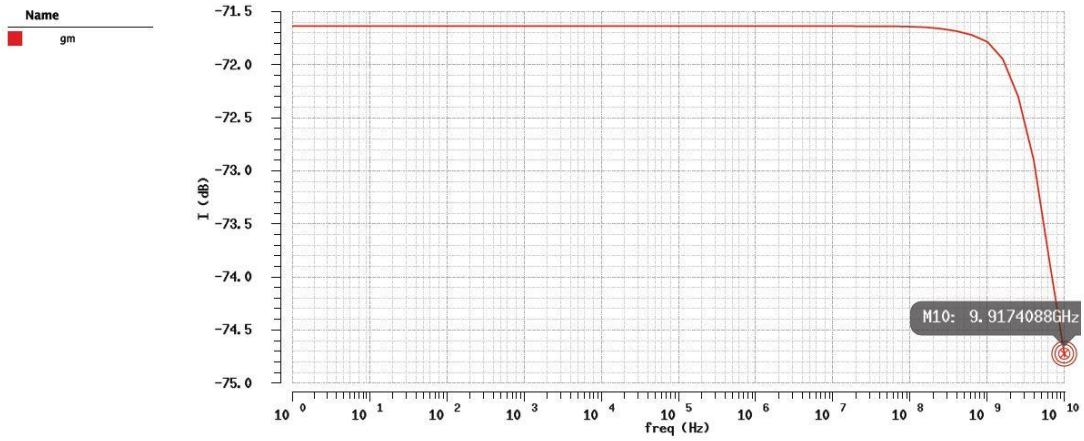

Figure 2.31 : The transconductance (g_m) bandwidth.

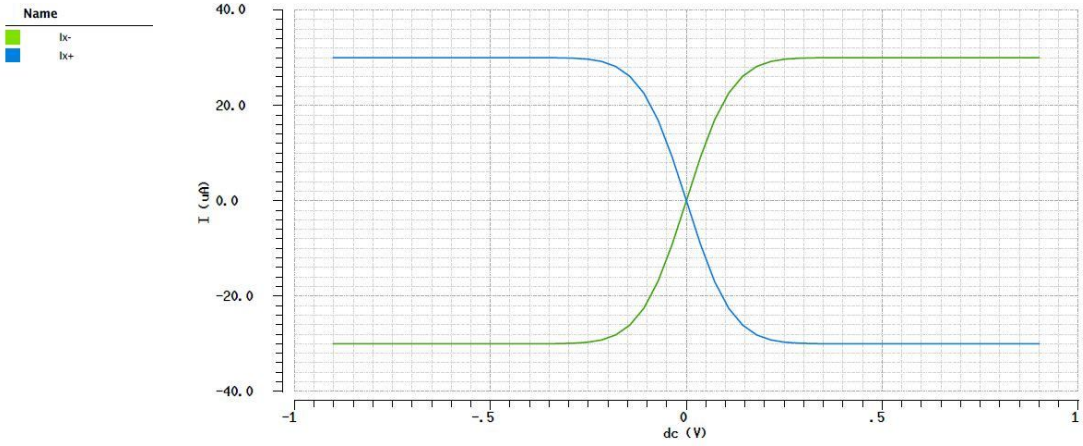

Figure 2.32 : The input voltage dynamic range.

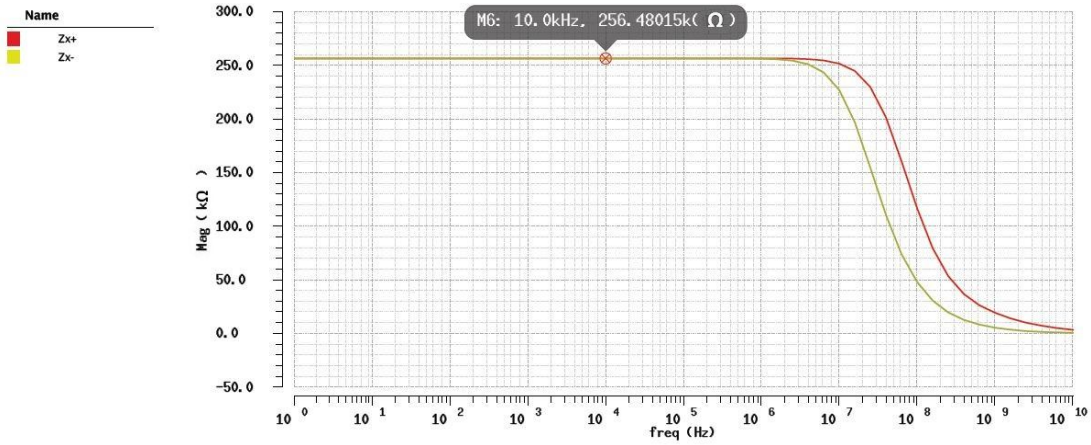

Figure 2.33 : The output impedances.

2.4 Voltage Buffer

The classical voltage buffer has one high impedance input and one low impedance output. The CMOS structure of the voltage buffer is shown in Figure 2.34. The simulation results of the buffer and the transistors size are given in Table 2.9 and 2.10, respectively. The bias current I_b is selected 50µA.

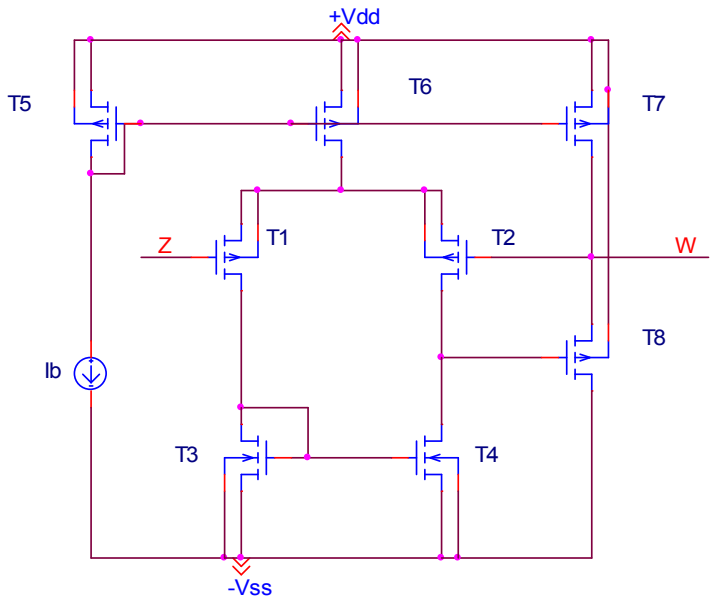

Figure 2.34 : The voltage buffer CMOS structure [15].

It is shown the DC transfer characteristic of buffer in Figure 2.35. The Z terminal voltage dynamic range was found between -240mV, 240mV. The AC transfer characteristic of buffer is given in Figure 2.36. The frequency response of the output terminal is given in Figure 2.37. The Z terminal resistance of the voltage buffer is found 5.4582kΩ. The defining equation of the CMOS structure is given in Equation 2.8.

$$V_w = V_z \qquad \textbf{(2.8)}$$

Table 2.9 : The voltage buffer simulation results.

Power Supply	±0.9V
W terminal voltage dynamic range	-180mV ≤ Iz ≤ 180mV
Vw/Vz (-3dB) bandwidth	382.830MHz
Vw/Vz phase margin	117.731°
W terminal output impedance	3.231kΩ
Voltage tracking error (%)	1,48
Power Consumption	69.46µW

Table 2.10 : Transistors sizes of the voltage buffer.

Transistors	(W/L)
T1,T2,T3,T4,T6,T7	24µ/0.36µ
T8	72µ/0.36µ

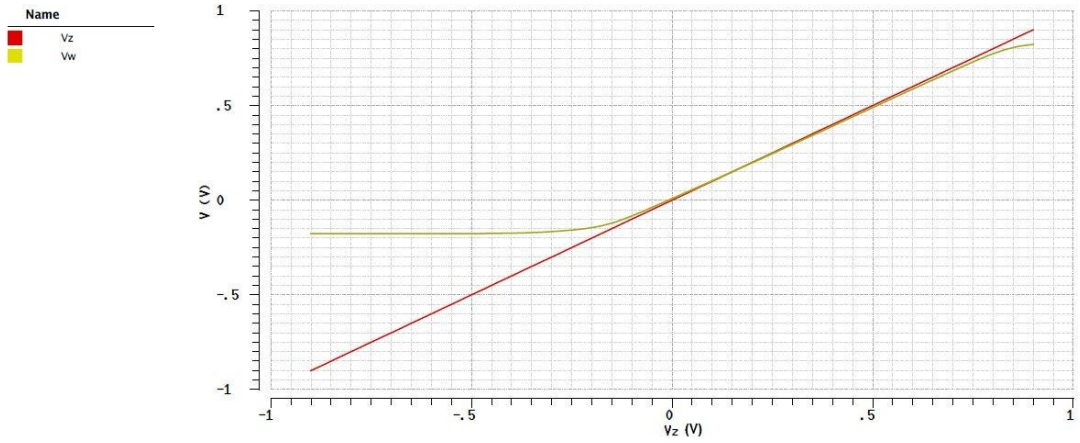

Figure 2.35 : The DC transfer characteristic of voltage buffer.

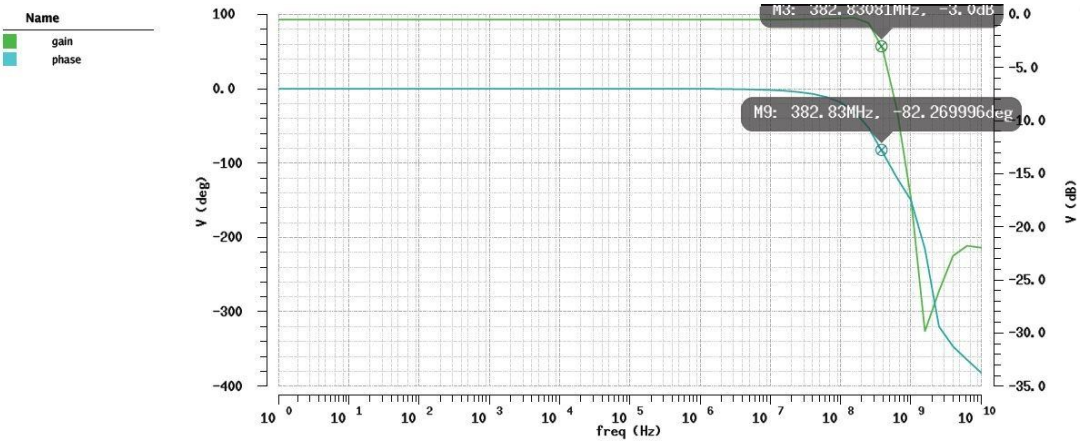

Figure 2.36 : The AC transfer characteristic of voltage buffer.

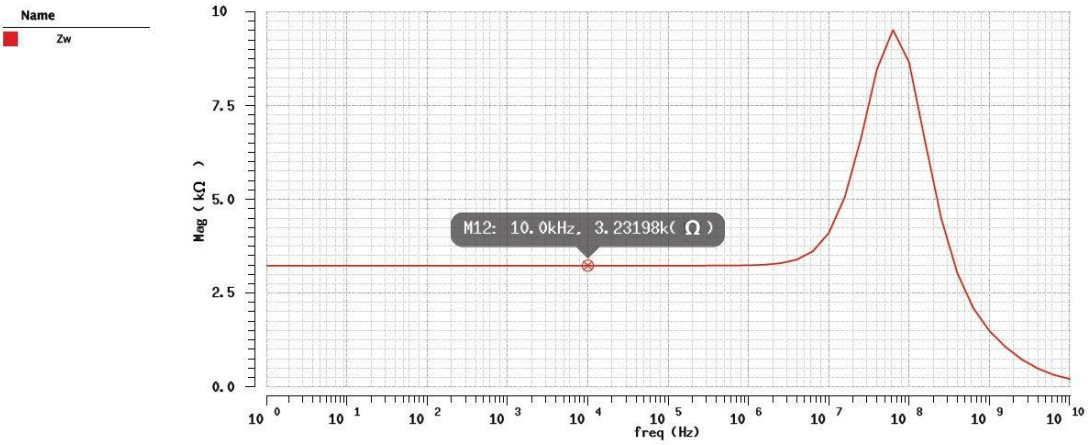

Figure 2.37 : The frequency response of the output terminal.

2.5 ECCII (Electronically Controllable Second Generation Current Conveyor)

The electronically controllable second generation current conveyor has one high impedance input terminal, one low impedance input terminal and one high impedance output terminal. The CMOS structure of the electronically controllable second generation current conveyor is shown in Figure 2.38. The bias current I_C is 60µA. The bias current of the I_B is 30µA.

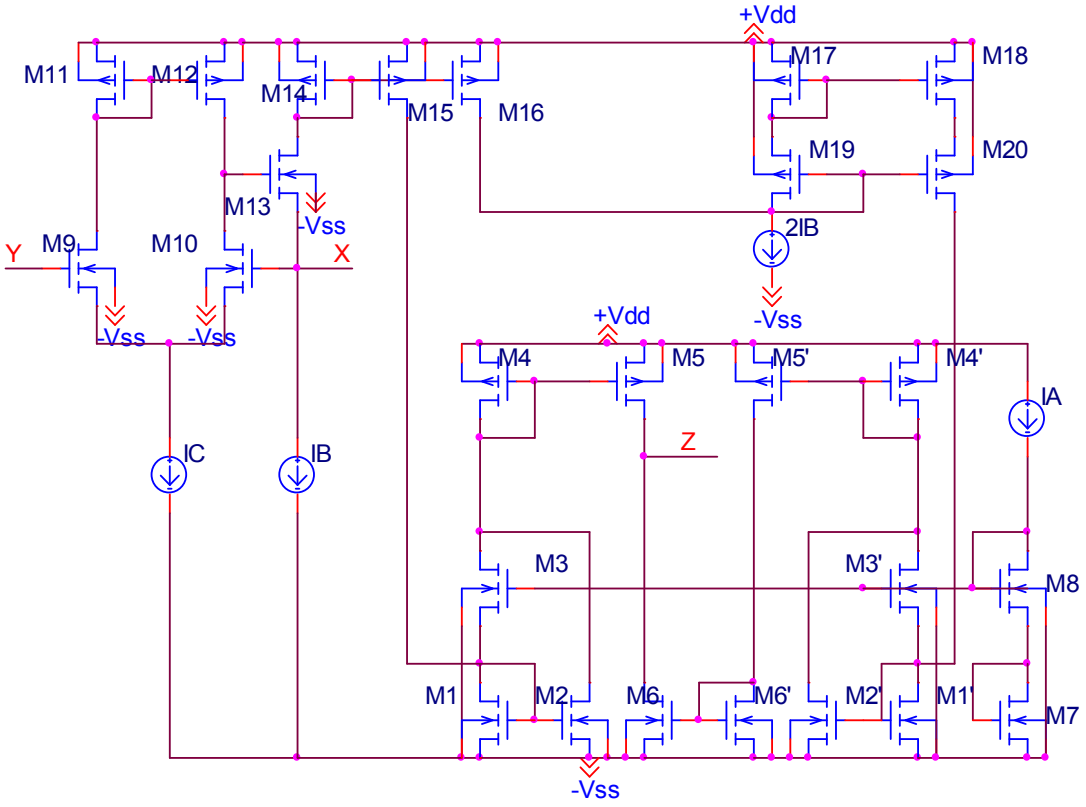

Figure 2.38 : The electronically controllable second generation current conveyor CMOS structure [16].

The current transfer ratio is controlled by the ratio of I_B / I_A bias currents. The simulation results of the ECCII and the transistors size of the circuit are given in Table 2.11 and 2.12, respectively.

The change of Z terminal current according to the X terminal current is given in Figure 2.39. Z terminal current dynamic range are found between -42µA and 42µA. The change of X terminal voltage respect to the Y terminal voltage is shown in Figure 2.40. X terminal voltage dynamic range is found between -214mV and 214mV. The frequency response of the Vx/Vy, the X terminal input impedance, the

Y terminal input impedance and Z output terminals impedance are given in Figure 2.41, 2.42, 2.43, respectively. The bandwidth of the Vx/Vy, the X terminal input impedance, the bandwidth of the Iz/Ix and the Z output terminal impedance of the third generation current conveyor were found1.3GHz, 7.691kΩ, 114.484MHz, 45.049kΩ, respectively. The X and Y terminal input impedance is appropriate for current copying. The bandwidth of the ratio Z terminal current respect to X terminal current is given in Figure 2.44.

The defining equations of the CMOS structure ECCII are given in Equation 2.9, 2.10, respectively.

$$V_x = V_y \quad \textbf{(2.9)}$$

$$I_z = \alpha I_x \quad \textbf{(2.10)}$$

Table 2.11 : The electronically controllable second generation current conveyor simulation results.

Power supply	±0.9V
Iz/Ix (-3dB) Bandwidth	114.484MHz
Vx/Vy (-3dB) Bandwidth	1.3GHz
X terminal input impedance	7.691kΩ
X terminal dynamic voltage range	-214mV ≤ Iz ≤ 214mV
Z terminal output impedance	45.049kΩ
Z terminal current dynamic range	-42µA ≤ Iz ≤ 42µA
Current tracking error (%)	1.62
Power dissipation	346.76µW

Table 2.12 : Transistors sizes of the electronically controllable second generation current conveyor.

Transistors	**(W/L)**
M1, M2, M3, M4, M5, M6, M1', M2', M3', M4', M5', M6', M7, M8, M9, M10, M11, M12, M13, M14, M15, M16, M17, M18, M19, M20	16µ/0.36µ

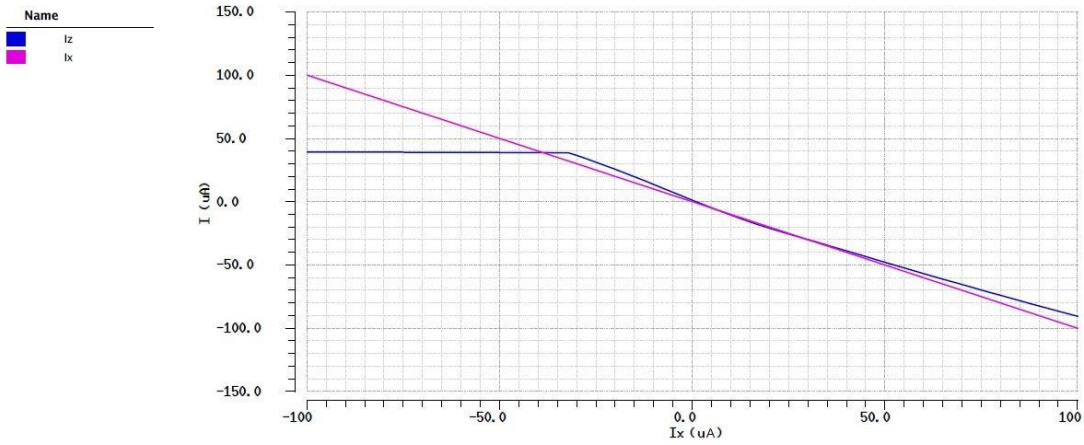

Figure 2.39 : The change of Z terminal current according to X terminal current.

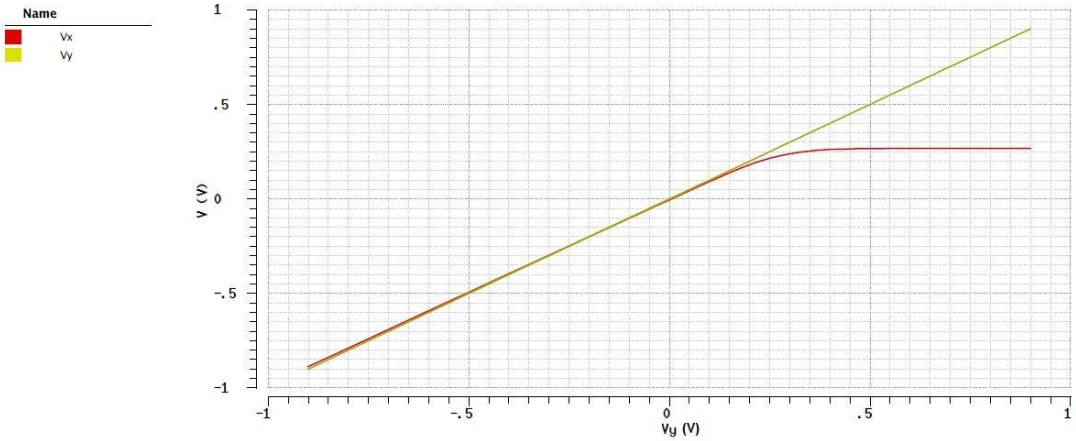

Figure 2.40 : The change of X terminal voltage respect to the Y terminal voltage.

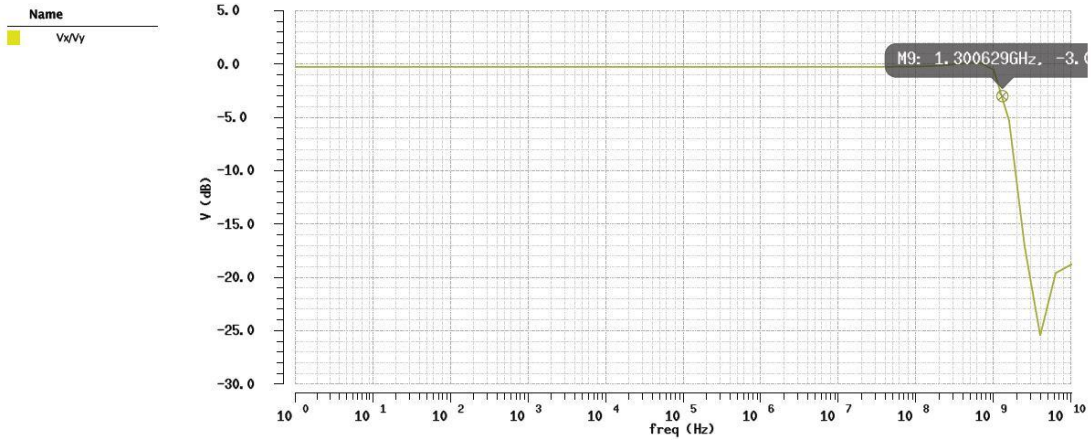

Figure 2.41 : The frequency response of the Vx/Vy.

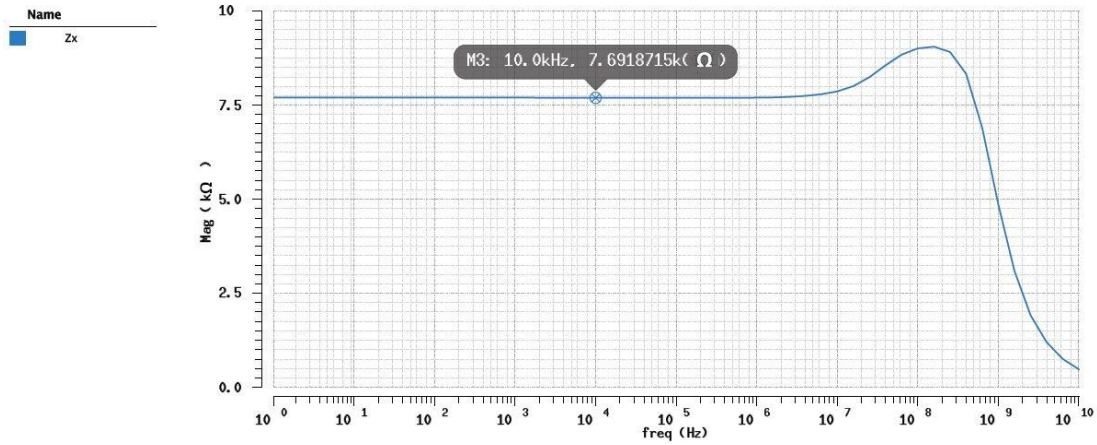

Figure 2.42 : The X terminal input impedance.

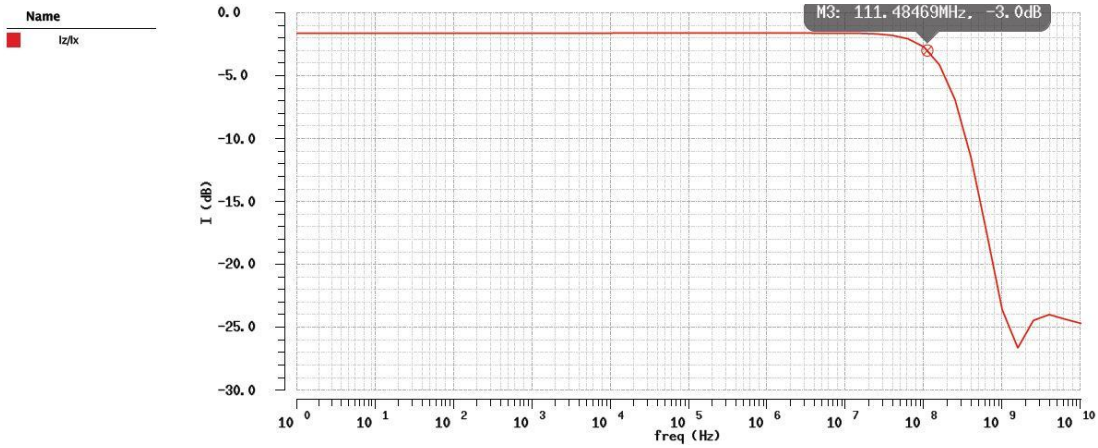

Figure 2.43 : The bandwidth of the Iz/Ix.

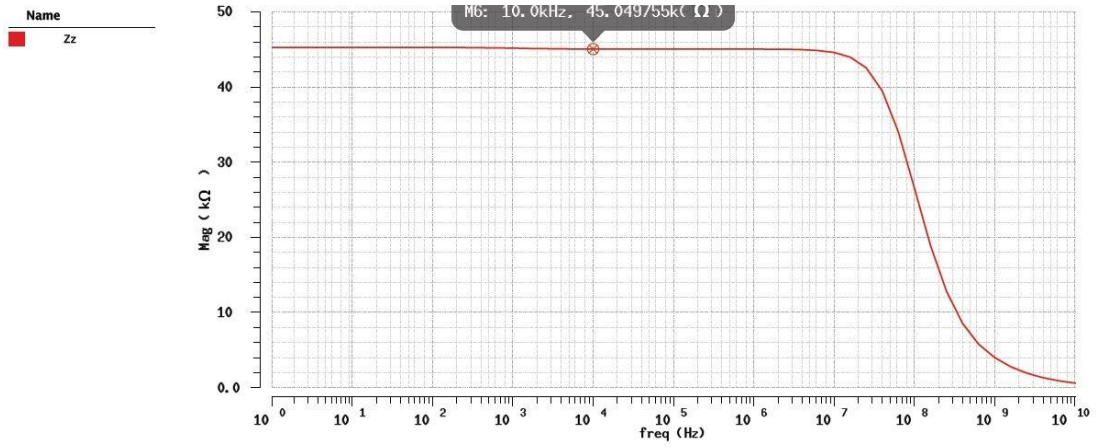

Figure 2.44 : The Z output terminal impedance.

3. POSITIVE FEEDBACK

The engineer solves problems with the most accurate approach. In electronic circuits, the voltage source input impedance is ideally zero and the current source input impedance is ideally infinite. In reality, it is impossible to realize infinite output impedance for current sources.

Designers who use building blocks in order to obtain impedance values close to ideal, benefit from negative or positive feedback. In this work, positive feedback is used to reduce the input impedance of the current differencing unit. Also, comparison of negative and positive feedback is given.

3.1 General Information and Purpose

Figure 3.1 shows a system without feedback. The impedance seen from the input of a system is the ratio of the input voltage to the current which flows inside of the system. The impedance seen from the input for Figure 3.1 is given in Equation 3.1.

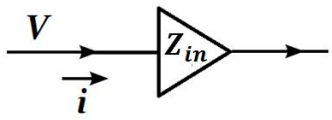

Figure 3.1 : A system without feedback.

$$\frac{V}{i} = Z_{in} \tag{3.1}$$

Figure 3.2 shows the positive feedback system. The impedance seen from the input for Figure 3.2 is shown in Equation 3.2.

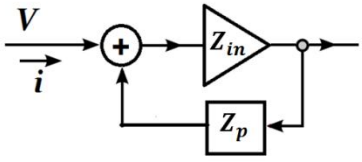

Figure 3.2 : The positive feedback system.

$$\frac{V}{i} = \left\{1 - \frac{Z_p}{Z_{in}}\right\} z_{in} \quad \textbf{(3.2)}$$

The impedance value is reduced by the ratio of Z_p/Z_{in}. The ratio of Z_p/Z_{in} must select lower than one for positive impedance values. Negative impedance can also be obtained by using positive feedback.

The negative feedback system is shown in Figure 3.3. The impedance seen from the Figure 3.3 negative feedback system input is shown in Equation 3.3.

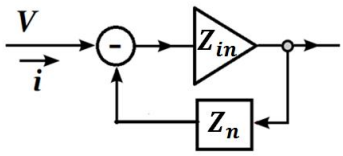

Figure 3.3 : The negative feedback system.

$$\frac{V}{i} = \left\{1 + \frac{Z_n}{Z_{in}}\right\} z_{in} \quad \textbf{(3.3)}$$

It is obviously seen from Equation 3.2 and 3.3 the positive feedback system decreases the input impedance more than the negative feedback system.

The CMOS structure of the low impedance current differencing unit developed by positive feedback system is given in Figure 3.4. In Table 3.1 the performance parameters of the circuit is seen. The size of transistors is shown in Table 3.2.

The change of output terminal current according to the P terminal input current and N terminal input current are given in Figure 3.5 and Figure 3.6. The Z terminal current dynamic range was found between -30µA, 30µA. The frequency responses of the input impedances at P and N terminals and the output impedances at Z terminal are given in Figure 3.7, 3.8, 3.9, respectively. The input resistances for proposed current differencing unit at N and P input terminal were found 410.798Ω, 194.013Ω, respectively. The output resistance at Z terminal was found 372.327kΩ. The bandwidth of the ratio Z terminal current respect to P and N terminal current are given in Figure 3.10, 3.11, respectively.

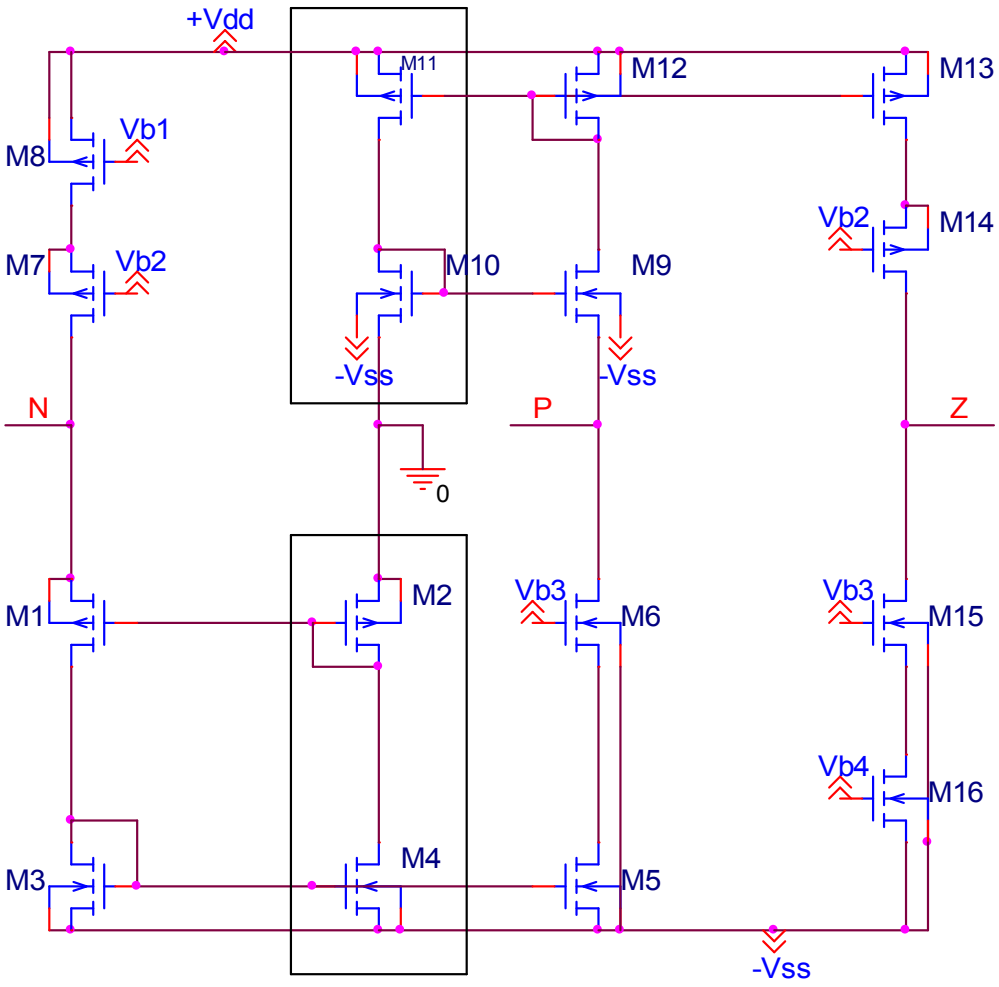

Figure 3.4 : The current differencing unit with positive feedback system [17].

The input resistances of the current differencing unit with positive feedback system is given in Equation 3.4, 3.5 [17]. The biasing voltages are selectected V_{b1}=300mV, V_{b2}=-400mV, V_{b3}=100mV, V_{b4}=-500mV.

$$r_{in-} \simeq \frac{1}{g_{m1}g_{m3}}\left\{\left(g_{ds1}+g_{m3}+g_{ds3}\right)-\frac{g_{m1}g_{m4}}{g_{ds4}+g_{m2}+g_{ds2}}\right\} \quad \textbf{(3.4)}$$

$$r_{in+} \simeq \frac{1}{g_{m9}g_{m12}}\left\{\left(g_{ds9}+g_{m12}+g_{ds12}\right)-\frac{g_{m9}g_{m11}}{g_{ds11}+g_{m10}+g_{ds10}}\right\} \quad \textbf{(3.5)}$$

The defining equation of the CMOS structure is given in Equation 3.6.

$$I_z = I_p - I_n \quad \textbf{(3.6)}$$

Table 3.1 : Simulation results of the current differencing unit structure.

Power Supply	±0.9V
Z terminal current dynamic range	-30µA ≤ Iz ≤ 30µA
Iz/In (-3dB) bandwidth	177.207MHz
Iz/Ip (-3dB) bandwidth	234.14MHz
P terminal input impedance	194.013Ω
P terminal phase margin	47.764°
N terminal input impedance	410.798Ω
P terminal phase margin	57.50°
Z terminal output impedance	372.327kΩ
Current tracking error(%)	1,04
Power Consumption	276.12µW

Table 3.2 : Transistors size of the current differencing unit structure.

Transistors	(W/L)
M1,M2	120µ/0.36µ
M3,M4,M5,M6,M7,M8	12µ/0.36µ
M9,M10	120µ/0.36µ
M11,M12,M13,M14,M15,M16	12µ/0.36µ

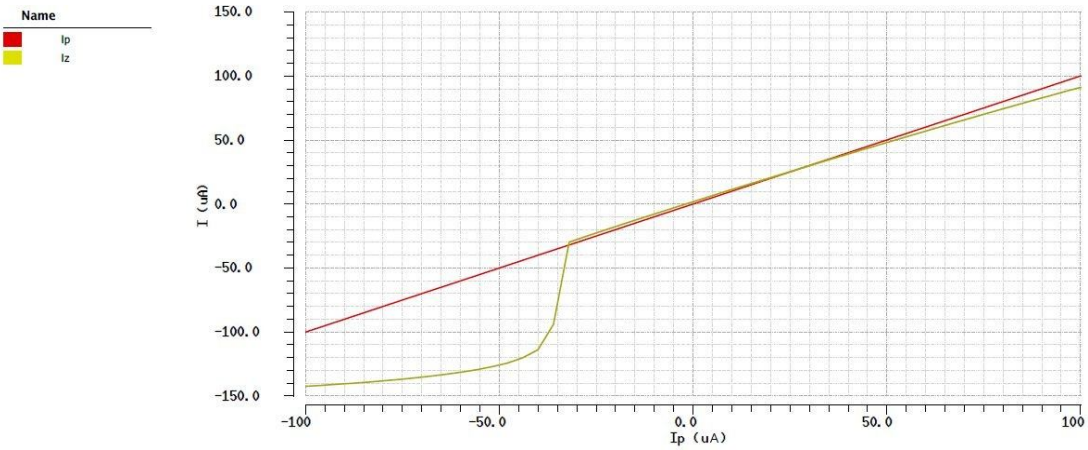

Figure 3.5 : The output terminal current according to the P terminal input current.

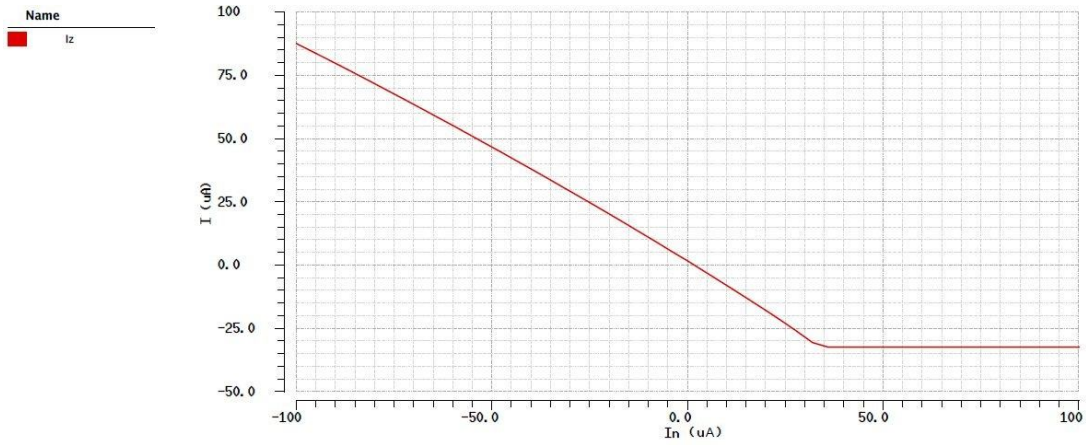

Figure 3.6 : The output terminal current according to the P terminal input current.

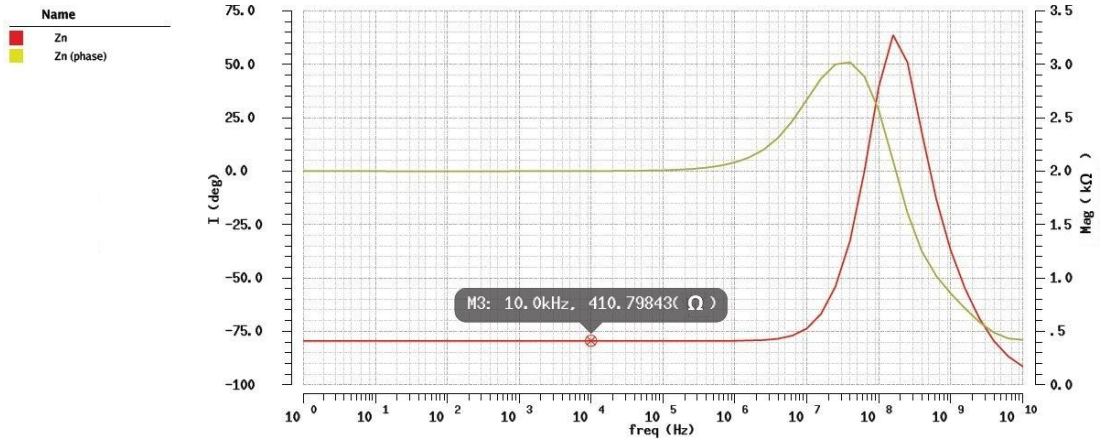

Figure 3.7 : The frequency responses of the input impedance at N.

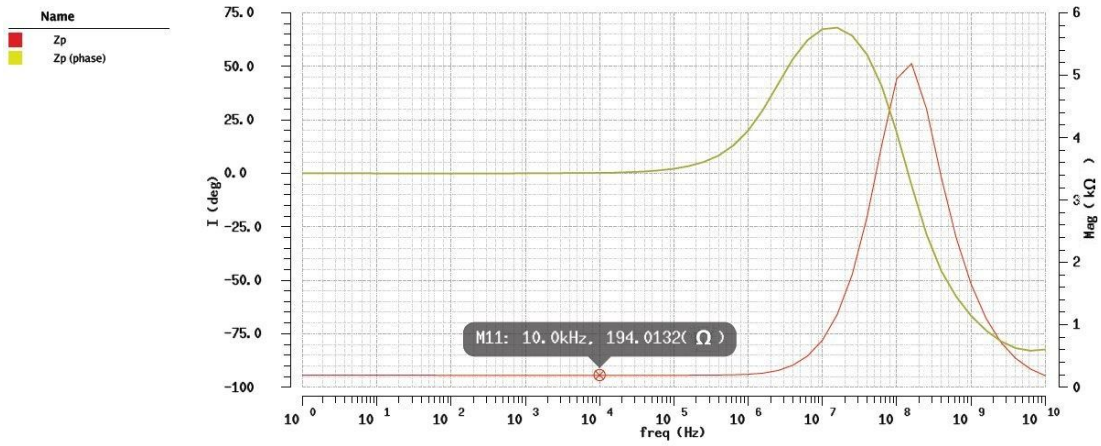

Figure 3.8 : The frequency responses of the input impedance at P.

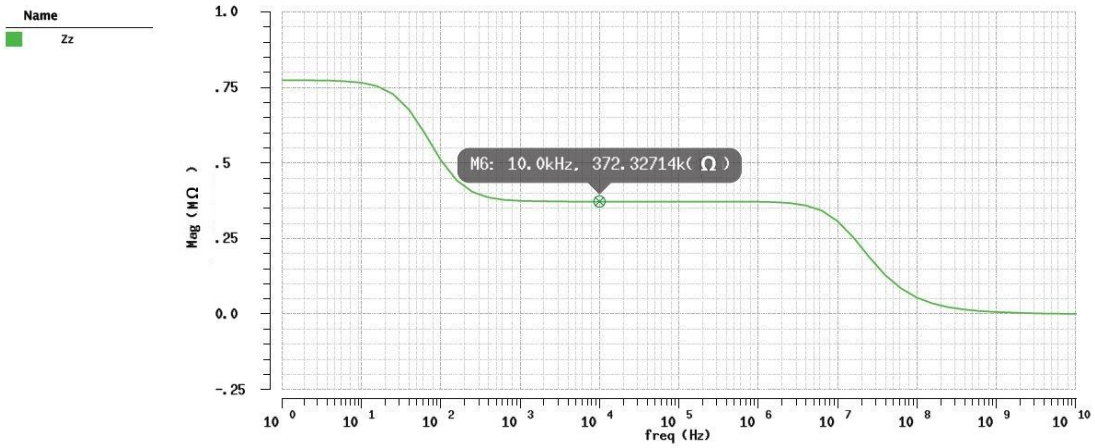

Figure 3.9 : The frequency responses of the input impedance at Z.

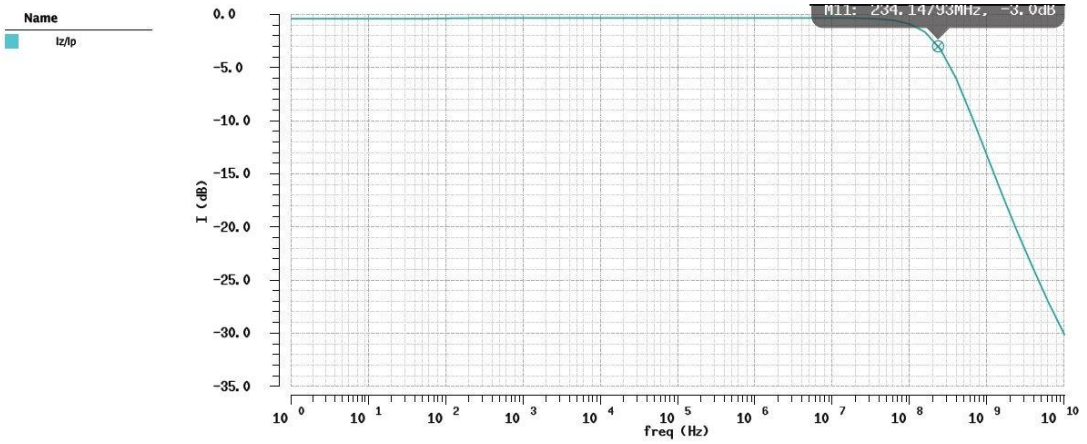

Figure 3.10 : The bandwidth of the ratio Z terminal current respect to P.

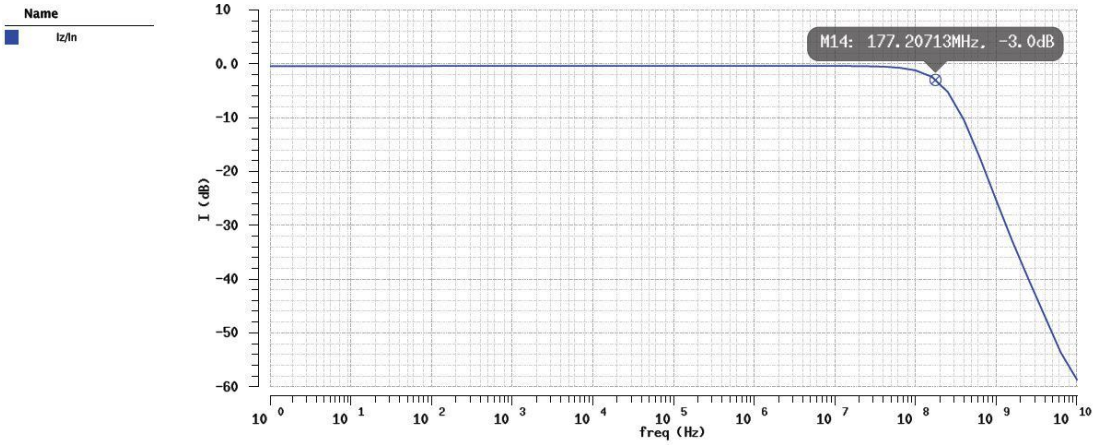

Figure 3.11 : The bandwidth of the ratio Z terminal current respect to N.

The comparison of three current differencing unit structures is given in Table 3.3. The input resistance of the The input resistances of the positive feedback system is lower than the others.

Table 3.3 : Simulation results of the three current differencing unit structure.

	The First Current Differencing Unit	The Second Current Differencing Unit	The current differencing unit with positive feedback system.
Power Supply	±0.9V	±0.9V	±0.9V
Z terminal current dynamic range	-100µA ≤ Iz ≤ 100µA	-28µA ≤ Iz ≤ 28µA	-30µA ≤ Iz ≤ 30µA
Iz/In (-3dB) bandwidth	540.335MHz	354,774MHz	177.207MHz
Iz/Ip (-3dB) bandwidth	692.879MHz	417.224MHz	234.14MHz
P terminal input impedance	600.248Ω	6.206kΩ	194.013Ω
N terminal input impedance	233.798Ω	4.273kΩ	410.798Ω
Z terminal output impedance	129.529kΩ	295.682kΩ	372.327kΩ
Current tracking error (%)	1,04	1,86	1,04
Power Consumption	256.45µW	189.35µW	276.12µW

4. NEW ACTIVE BLOCKS

4.1 ZC-CDTA

ZC-CDTA(Z Copy Current Differencing Transconductance Amplifier) is a new current mode active element, introduced recently. Z-Copy Current Differencing Transconductance Amplifier is developed from CDTA. CDTA (Current Differencing Transconductance Amplifier) is a five-terminal current-mode active element proposed by D. Biolek in 2003. CDTA consists of two input terminal, one intermediate terminal and two output terminals. Inputs are differential and they take the difference between the currents applied to the input. This current difference is transferred to the intermediate terminal and it converted to the voltage with the aid of external resistance. This voltage multiplied by transconductance parameter of the operational transconductance amplifier converted to the balanced current at output of the Current Differencing Transconductance Amplifier. The symbol and the schematic view of the CDTA is given in the Figure 4.1 and Figure 4.2, respectively.

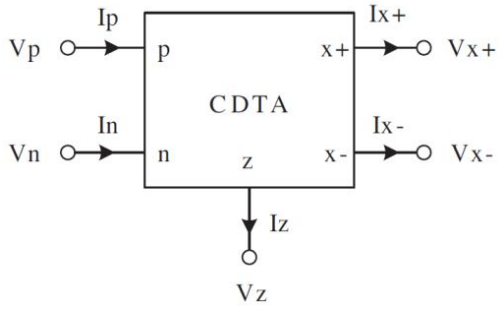

Figure 4.1 : The schematic view of the CDTA [9].

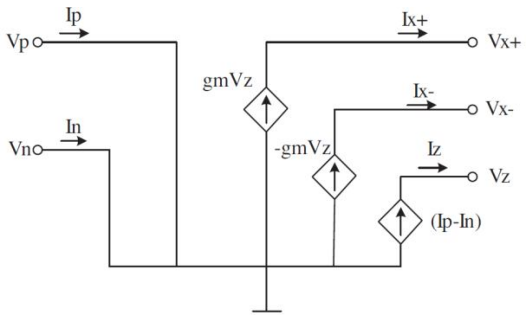

Figure 4.2 : The block diagram of the CDTA [9].

Furthermore, the Z Copy Current Differencing Transconductance Amplifier has additional Z terminal output Z copy called. The ZC-CDTA increases the universality of CDTA. Third generation current conveyor (CCIII) is used to copy the z terminal current instead of a classical current mirror. The current sensing is perfectly done by the aid of CCIII. The symbol and the schematic view of the ZC-CDTA are given in the Figure 4.3 and Figure 4.4, respectively. The proposed circuit structure for the ZC-CDTA is given in Figure 4.5. ZC-CDTA defining equation matrix and its basic operations formulas are given in Equation 4.1, 4.2, 4.3, 4.4.

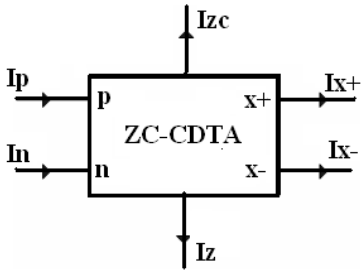

Figure 4.3 : The schematic view of the ZC-CDTA.

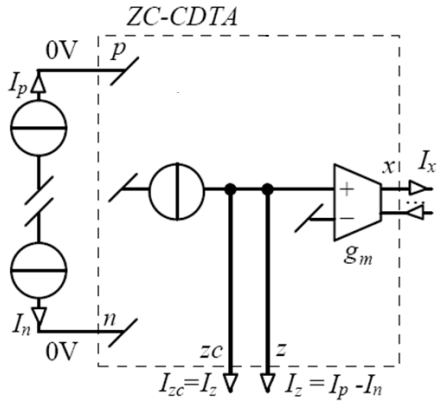

Figure 4.4 : The block diagram of the ZC-CDTA [10].

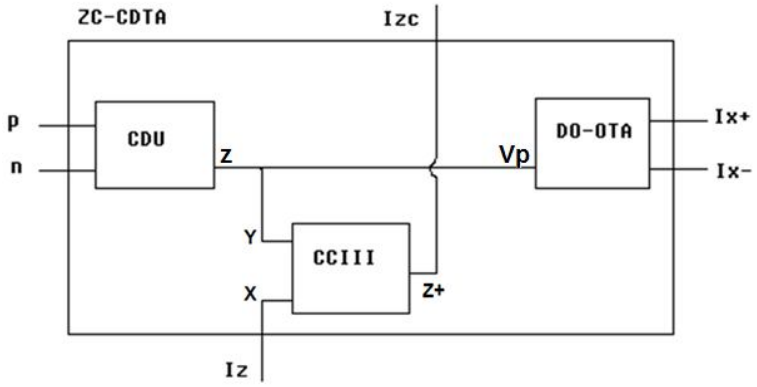

Figure 4.5 : The proposed circuit structure for the ZC-CDTA.

$$\begin{pmatrix} V_p \\ V_n \\ i_z \\ i_x \\ i_{zc} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & \pm g_m & 0 \\ 0 & 0 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} i_p \\ i_n \\ V_x \\ V_z \\ i_z \end{pmatrix} \quad \textbf{(4.1)}$$

$$V_p = V_n = 0 \quad \textbf{(4.2)}$$

$$I_z = I_{zc} = I_p - I_n \quad \textbf{(4.3)}$$

$$I_{x+} = g_m V_z \, , \; I_{x-} = -g_m V_z \quad \textbf{(4.4)}$$

The defining equation of the ZC-CDTA in Figure 4.4 becomes in Equation 4.5 by considering the deviation of the voltage and current gains from their ideal values.

$$\begin{pmatrix} V_p \\ V_n \\ i_z \\ i_x \\ i_{zc} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \alpha_p & -\alpha_n & 0 & 0 & 0 \\ 0 & 0 & 0 & \pm g_m & 0 \\ 0 & 0 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} i_p \\ i_n \\ V_x \\ V_z \\ i_z \end{pmatrix} \quad \textbf{(4.5)}$$

α_p and α_n are the current gain. $\alpha_p = 1 - \varepsilon_p$ and $\alpha_n = 1 - \varepsilon_n$. Here ε_p and ε_n are the error of current tracking, their absolute value are very close to zero.

4.2 ZC-CDBA

ZC-CDBA (Z Copy Current Differencing Buffered Amplifier) introduced recently as a new current mode signal processing active element. CDBA forms the foundation of Z-Copy Current Differencing Buffered Amplifier. CDBA (Current Differencing Buffered Amplifier) is a four-terminal current-mode active element proposed by C. Acar in 1999. CDBA has two low impedance input terminal, one high impedance output terminal and one low impedance intermediate terminal. Here, a current through the z-terminal follows the difference of the currents through the p-terminal and n-terminal. Input terminals p and n are internally grounded.

The active element Current Differencing Buffered Amplifier circuit symbol is shown in Figure 4.6, where p and n are input terminals and w and z are output terminals. This element is equivalent to the circuit in Figure 4.7, which involves dependent current and voltage sources.

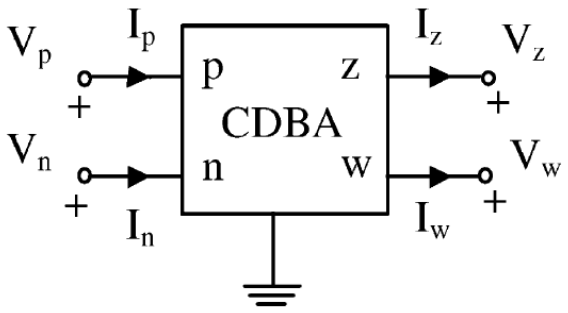

Figure 4.6 : The schematic view of the CDBA [8].

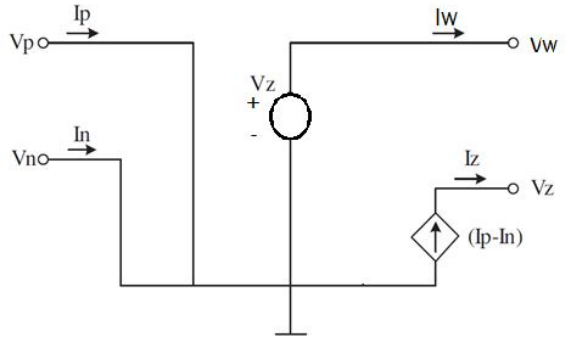

Figure 4.7 : The block diagram of the CDBA [8].

Z Copy Current Differencing Buffered Amplifier has additional Z terminal output. The ZC-CDTA increases the universality of CDBA. Third generation current conveyor (CCIII) is used to copy the z terminal. Current detection is precisely done with the help of CCIII. The symbol and the schematic view of the ZC-CDBA is given in the Figure 4.8 and Figure 4.9, respectively. The designed circuit structure for the ZC-CDBA circuit is given in Figure 4.10. ZC-CDBA defining equation matrix and its basic operations formulas are given in Equation 4.6, 4.7, 4.8, 4.9.

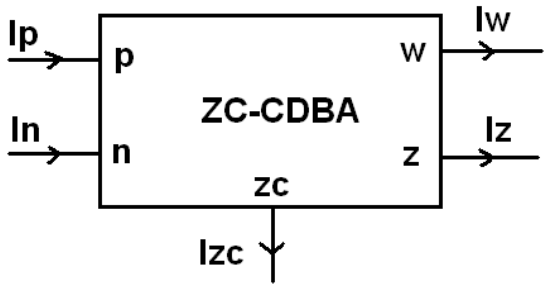

Figure 4.8 : The schematic view of the ZC-CDBA.

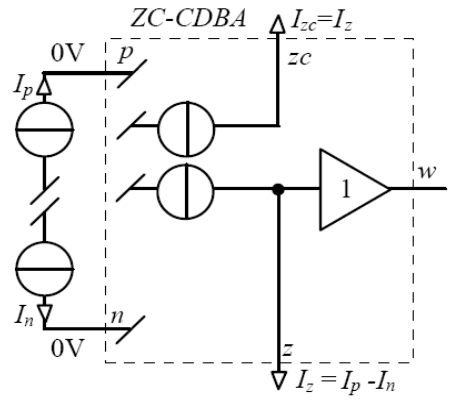

Figure 4.9 : The block diagram of the ZC-CDBA.

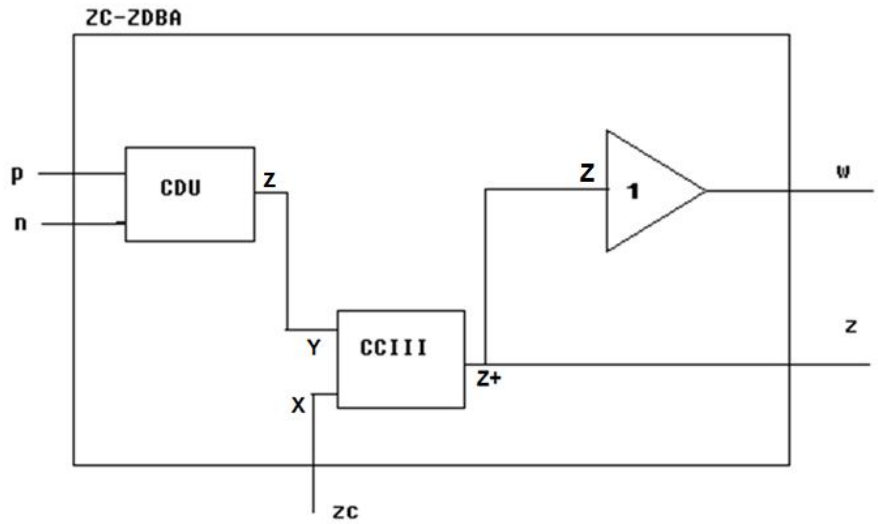

Figure 4.10 : The designed circuit structure for the ZC-CDBA.

$$\begin{pmatrix} i_z \\ i_{zc} \\ v_w \\ v_p \\ v_n \end{pmatrix} = \begin{pmatrix} 0 & 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} v_z \\ i_w \\ i_p \\ i_n \\ i_z \end{pmatrix} \tag{4.6}$$

$$i_z = i_{zc} = i_p - i_n \tag{4.7}$$

$$V_w = V_z \tag{4.8}$$

$$V_p = V_n = 0 \tag{4.9}$$

4.3 ZC-CG-CDBA

ZC-CG-CDBA (Z Copy Controlled Gain Current Differencing Buffered Amplifier) is a new current mode active element, introduced recently. Z-Copy Controlled Gain Current Differencing Buffered Amplifier is developed from Current Differencing Buffered Amplifier.

The active element Z Copy Controlled Gain Current Differencing Buffered Amplifier circuit symbol is shown in Figure 4.9, where p and n are input terminals and w and z are output terminals. This element is equivalent to the circuit in terms of dependent current and voltage sources in Figure 4.10. In Figure 4.13, the designed circuit for ZC-CG-CDBA is given. The z terminal output current gain changeable by the help of electronically controllable second generation current conveyor.

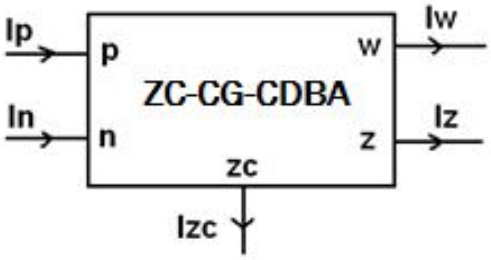

Figure 4.11 : The schematic view of the ZC-CG-CDBA.

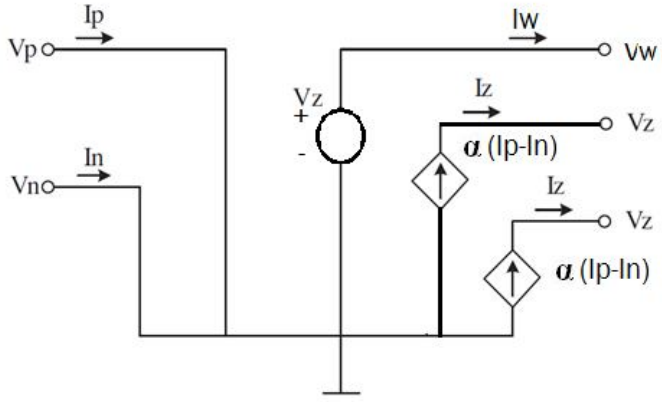

Figure 4.12 : The block diagram of the ZC-CG-CDBA.

The circuit description matrix of the Z Copy Controlled Gain Current Differencing Buffered Amplifier and the operation are given in Equation 4.10, 4.11, 4.12, 4.13,

respectively. The different point from the Z Copy Current Differencing Buffered Amplifier is the current gain seen in Equation 4.10 and 4.11.

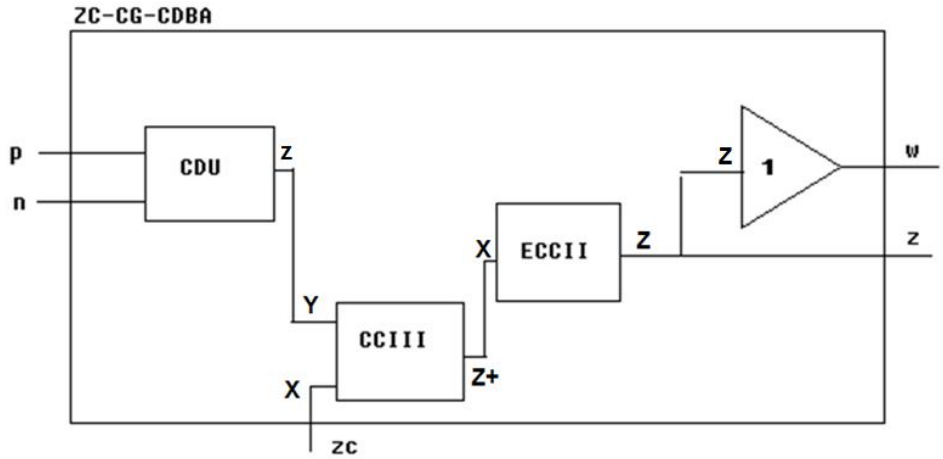

Figure 4.13 : The designed circuit for the ZC-CG-CDBA.

$$\begin{pmatrix} i_z \\ i_{zc} \\ v_w \\ v_p \\ v_n \end{pmatrix} = \begin{pmatrix} 0 & 0 & \alpha & -\alpha & 0 \\ 0 & 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} v_z \\ i_w \\ i_p \\ i_n \\ i_z \end{pmatrix} \quad \textbf{(4.10)}$$

$$i_z = i_{zc} = \alpha(i_p - i_n) \quad \textbf{(4.11)}$$

$$V_w = V_z \quad \textbf{(4.12)}$$

$$V_p = V_n = 0 \quad \textbf{(4.13)}$$

5. LAYOUT AND POST-LAYOUT SIMULATIONS

The layout for the Z copied current differencing buffered amplifier and Z copied current differencing transconductance amplifier are performed with the Cadence package.

5.1 Layout of the ZC-CDBA

In this chapter, the CMOS structure of the Z copied current differencing buffered amplifier, layout of the ZC-CDBA and the post-layout simulations of the ZC-CDBA will be given.

The Z copy for the ZC-CDTA, ZC-CDBA and ZC-CG-CDBA are realized with CCIII proposed by Fabre A. The CMOS inner structure of the ZC-CDBA in this chapter is realized without the third generation current conveyor.

The classical current mirror is used for realization of the Z copy. The main reason of the using classical current mirror is the design of the low power consumption CMOS inner structure for the ZC-CDTA, ZC-CDBA and ZC-CG-CDBA. The main disadvantage of using classical current mirror for Z copy terminal is the current tracking problem for the high impedance load. The current tracking is negligible for low impedance load. The additional disadvantage of the third generation current conveyor is the increasing of the complexity of the device. The complexity of the device decreases the operating frequency level of the circuit.

The CMOS structure for the Z copied current differencing buffered amplifier is given in Figure 5.1. The layout of the ZC-CDBA is given in Figure 5.2. The simulation results of the ZC-CDBA and the transistor sizes of the ZC-CDBA are given in Table 5.1 and 5.2, respectively. The biasing voltages are selectected as V_{b1}=300mV, V_{b2}=-400mV, V_{b3}=100mV, V_{b4}=-500mV. The bias current I_b is 50μA.

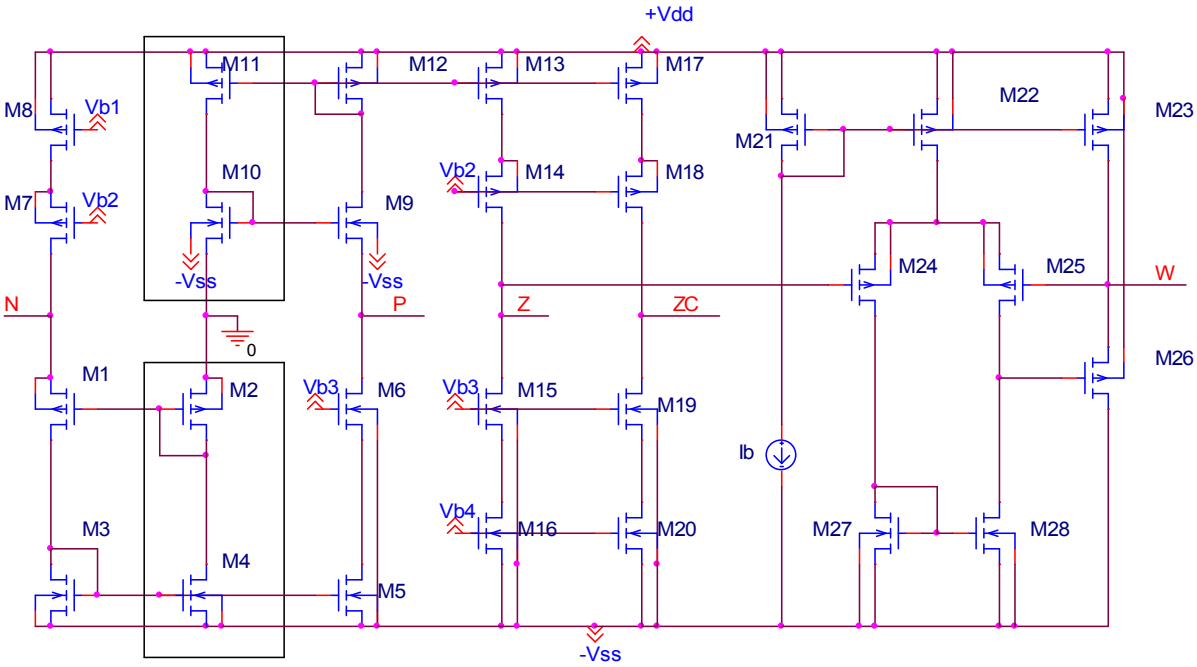

Figure 5.1 : ZC-CDBA CMOS Realization.

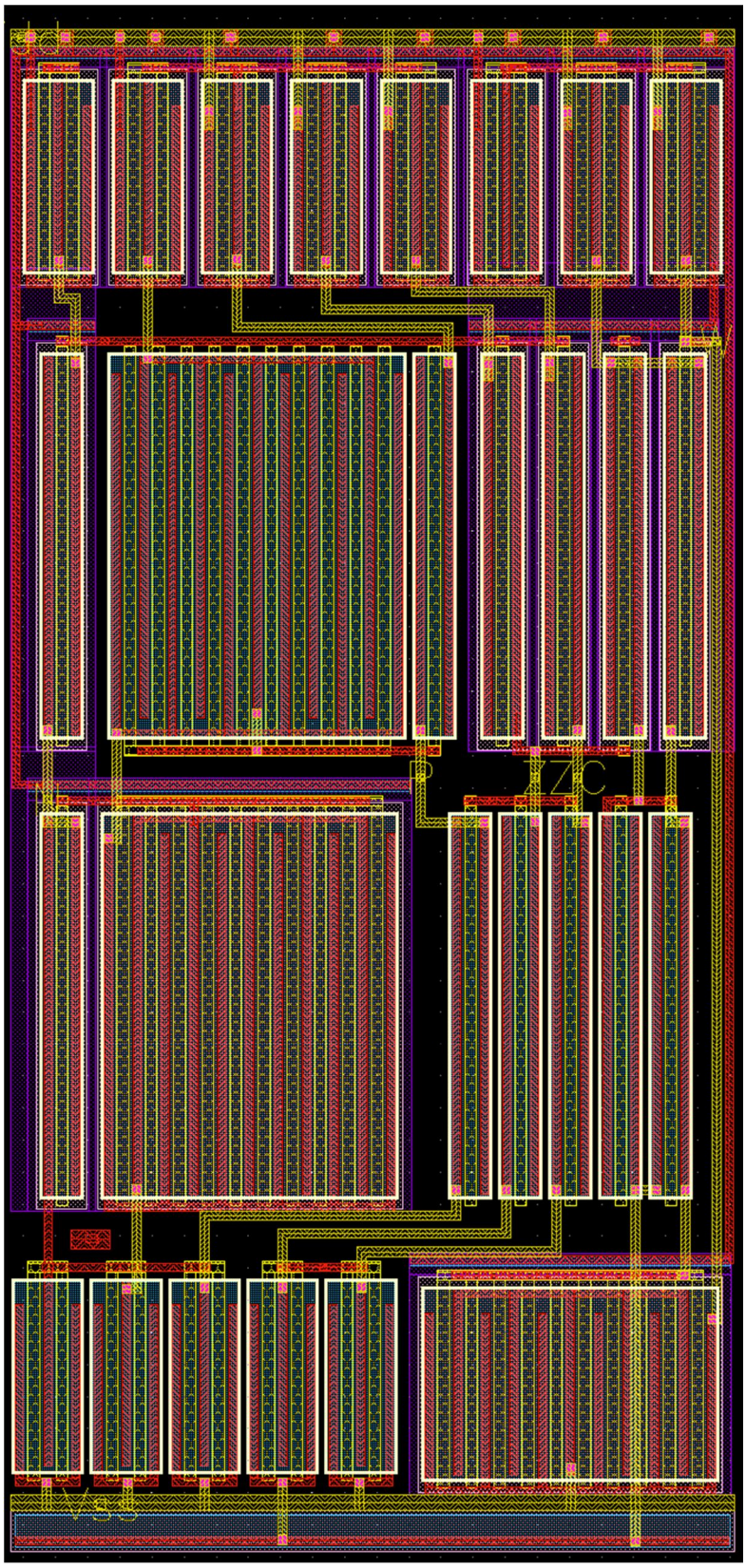

Figure 5.2 : Layout of the ZC-CDBA.

Table 5.1 : The simulation results of the ZC-CDBA.

Power Supply	±0.9V
Z terminal current dynamic range	-50μA ≤ Iz ≤ 50μA
W terminal voltage dynamic range	-215mV ≤ Vw ≤ 215mV
Iz/In (-3dB) bandwidth	299.681MHz
Iz/Ip (-3dB) bandwidth	347.789MHz
P terminal input impedance	530.762Ω
N terminal input impedance	1.224kΩ
W terminal output impedance	303.240Ω
Z terminal output impedance	1.673MΩ
Vw/Vz (-3dB) bandwidth	393.220MHz
Power Consumption	343.46μW

Table 5.2 : The transistor sizes of the ZC-CDBA.

Transistors	(W/L)
M1	12μ/0.36μ x 1
M2	12μ/0.36μ x 10
M3,M4,M5	6μ/0.36μ x 2
M6,M7	12μ/0.36μ x 1
M8	6μ/0.36μ x 2
M9	12μ/0.36μ x 1
M10	12μ/0.36μ x 10
M11,M12,M13	6μ/0.36μ x 2
M14,M15	12μ/0.36μ x 1
M16,M17	6μ/0.36μ x 2
M18,M19	12μ/0.36μ x 1
M20, M21,M22,M23	6μ/0.36μ x 2
M24,M25	12μ/0.36μ x 1
M26	12μ/0.36μ x 5
M27,M28	12μ/0.36μ x 1

The Z output terminal current according to the N input terminal current, the Z output terminal current according to the P input terminal current, the ZC output terminal current according to the Z terminal output current, the W output terminal voltage according to the Z output terminal voltage, Iz/In bandwidth, Iz/Ip bandwidth, Vw/Vz bandwidth, the N input terminal impedance, the P input terminal impedance, the W output terminal impedance, the Z output terminal impedance are given in Figure 5.3, 5.4, 5.5, 5.6, 5.7, 5.8, 5.9, 5.10, 5.11, 5.12, 5.13, respectively.

The Z copy output terminal current is perfectly follow the Z output terminal current with the aid of classical current mirror. But for high impedance load this tracking is destroyed.

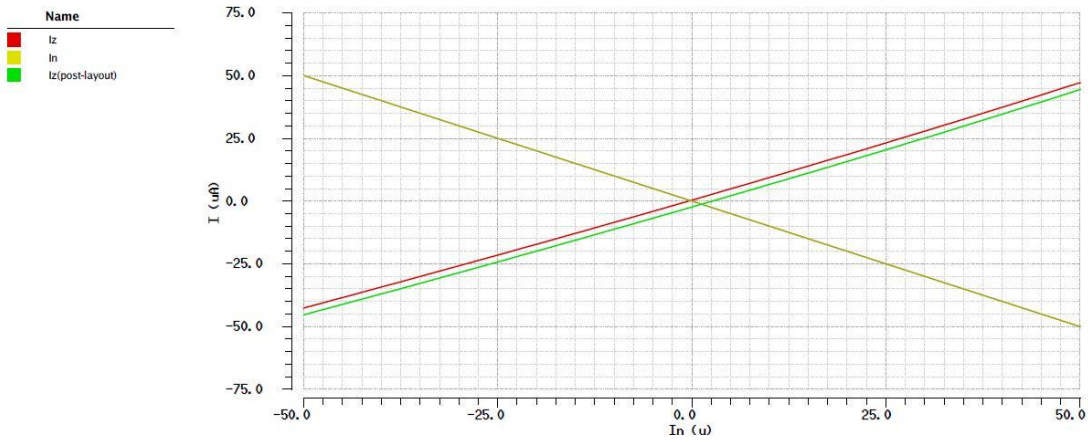

Figure 5.3 : The Z output terminal current according to N input terminal current.

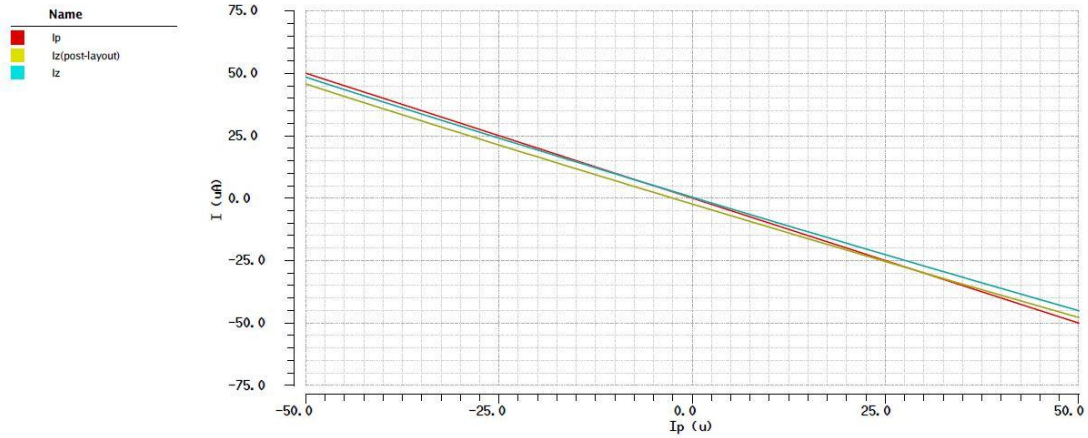

Figure 5.4 : The Z output terminal current according to P input terminal current.

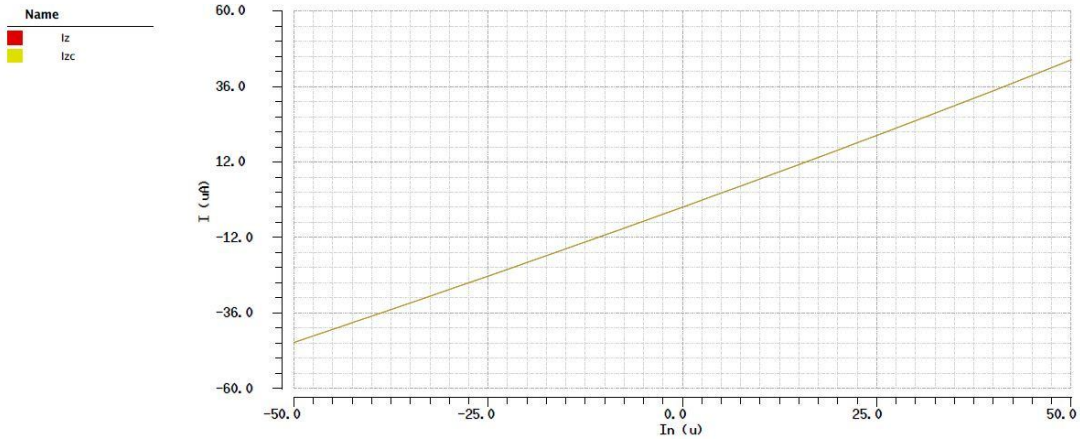

Figure 5.5 : The ZC output terminal current according to Z terminal output current.

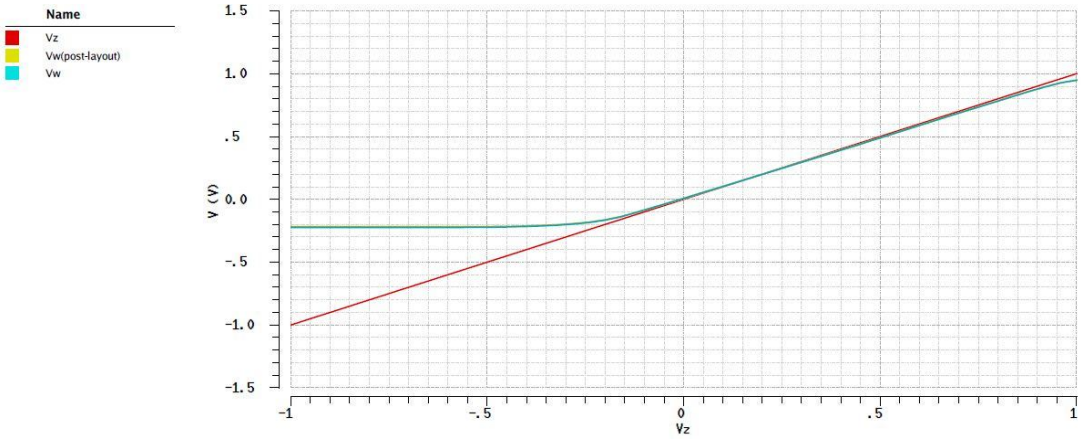

Figure 5.6 : The W output terminal voltage according to Z output terminal voltage.

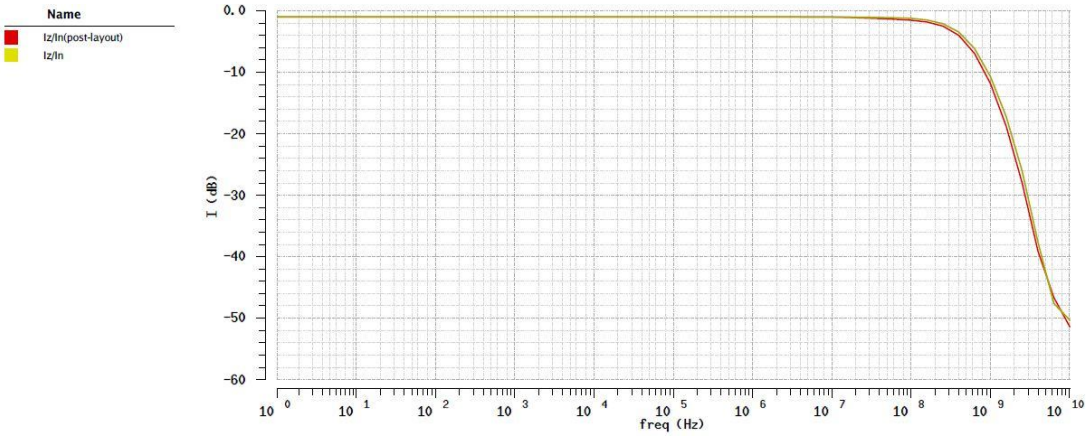

Figure 5.7 : Iz/In bandwidth.

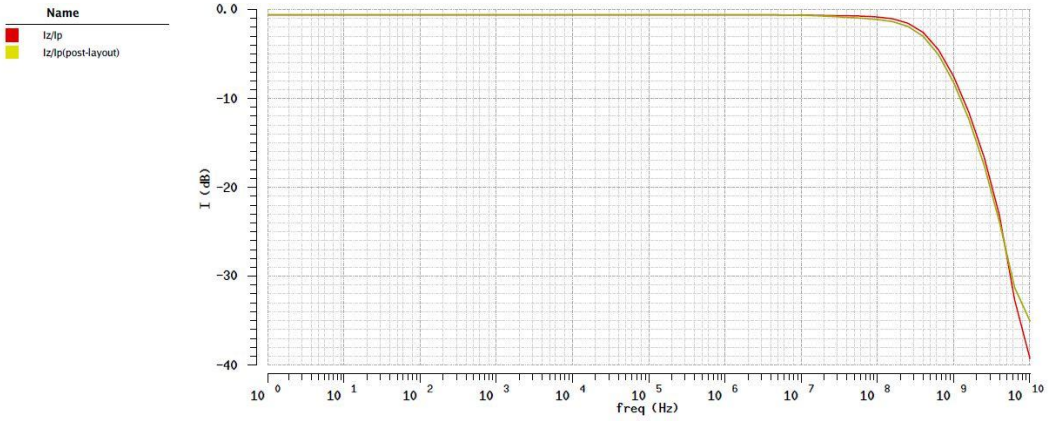

Figure 5.8 : Iz/Ip bandwidth.

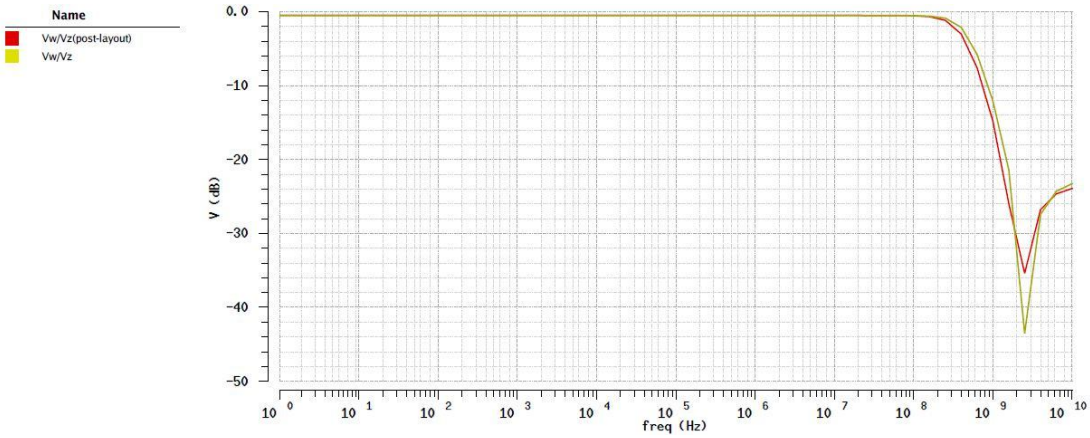

Figure 5.9 : Vw/Vz bandwidth.

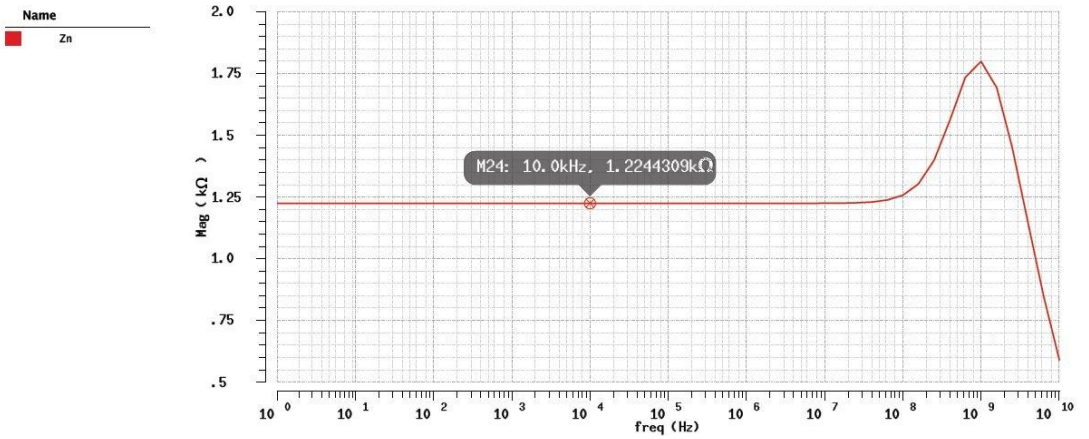

Figure 5.10 : The N input terminal impedance.

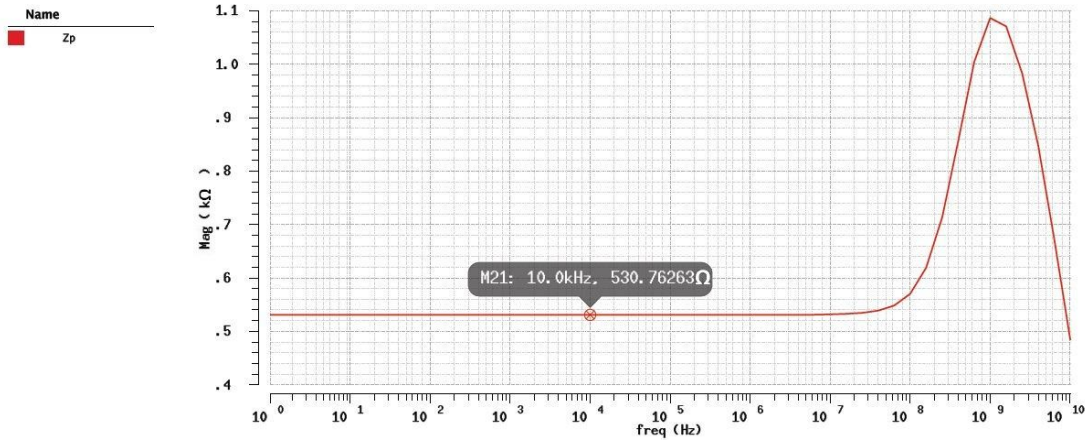

Figure 5.11 : The P input terminal impedance.

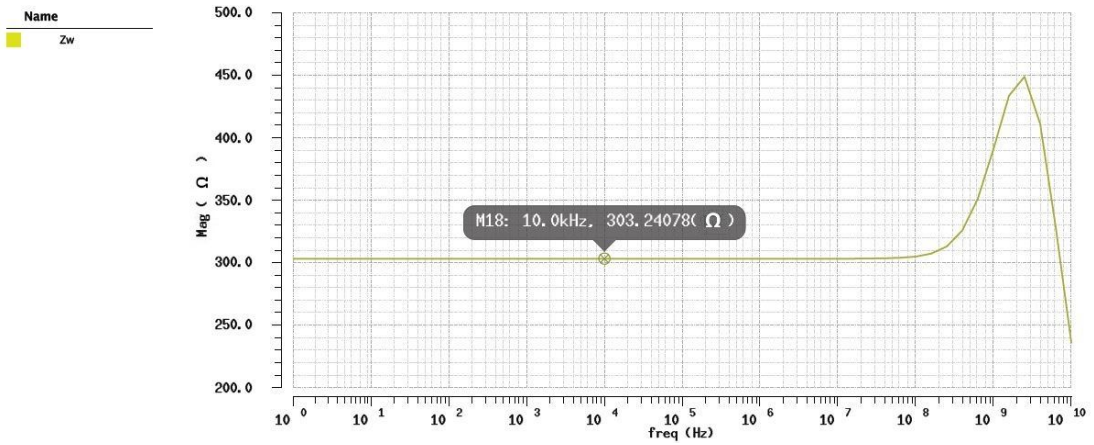

Figure 5.12 : The W output terminal impedance.

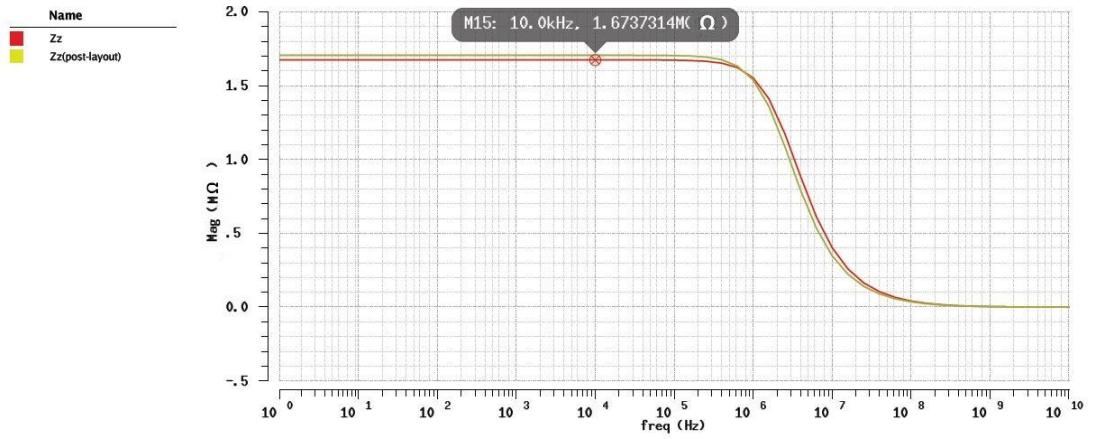

Figure 5.13 : The Z output terminal impedance.

Iz/In bandwidth is found 299,681MHz from the Figure 5.7. Iz/Ip bandwidth is observed 347.789MHz from the Figure 5.8. Vw/Vz bandwidth also is found as 393,220MHz from Figure 5.9. In conclusion, all the simulations are compatible with the post-layout simulations.

5.2 Layout of the ZC-CDTA

In this chapter of the thesis the layout of the Z copied current differencing transconductance amplifier is given. The CMOS realization of the ZC-CDTA is performed with the CCIII.

The firs current differencing unit structure given in Figure 2.2, the third generation current conveyor and the Arbel-Goldmiz floating current source structure are used in

the CMOS realization. The layout also performed according to the CMOS structure. The layout of the ZC-CDTA is given in the Figure 5.14.

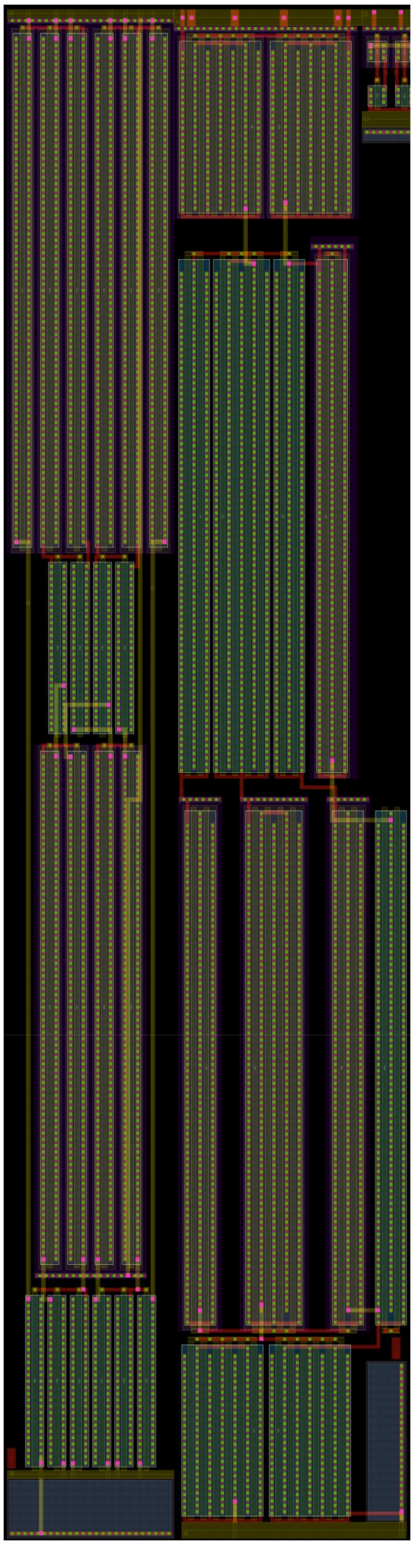

Figure 5.14 : Layout of the ZC-CDTA.

6. APPLICATION CIRCUITS

6.1 ZC-CDTA and Its Biquad Filter Application

The biquad filter is a very important filter structure for analog signal processing. There are many applications such as processing, TV receivers and wireless communication stages require narrow band pass tuned amplifiers such as video signal. By using the filter topology shown in Figure 6.1, a fourth order band pass filter was implemented. The proposed universal filter, employing Z copy current differencing transconductance amplifiers, is shown in Figure 6.2. Each of the proposed circuits is composed of 2 ZC-CDTAs. The configuration uses only two capacitors, without any resistors. Thanks to Z Copy Current Differencing Transconductance Amplifier an high pass section is obtained for the CDTA biquad application in Figure 6.1. The capacitors C_1 and C_2 are 1.8pF. The capacitors C_3 and C_4 are 1.8pF.

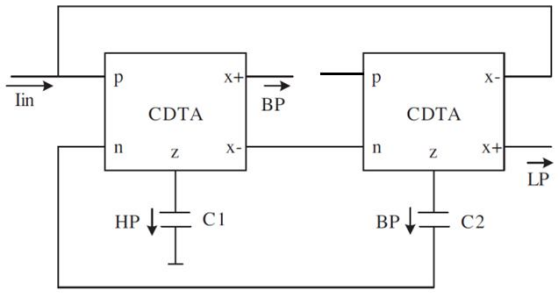

Figure 6.1 : Proposed biquad filters employing CDTAs [22].

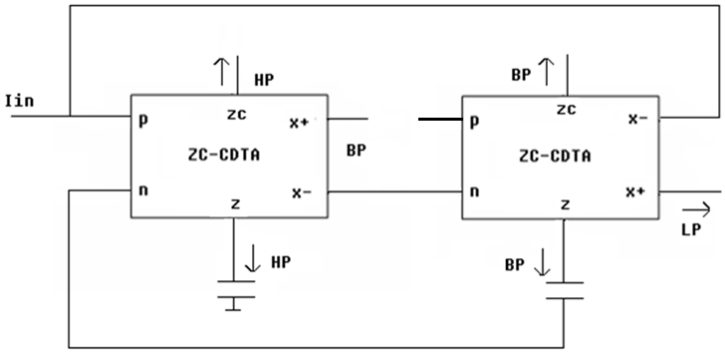

Figure 6.2 : Filter structure based on ZC-CDTA [18].

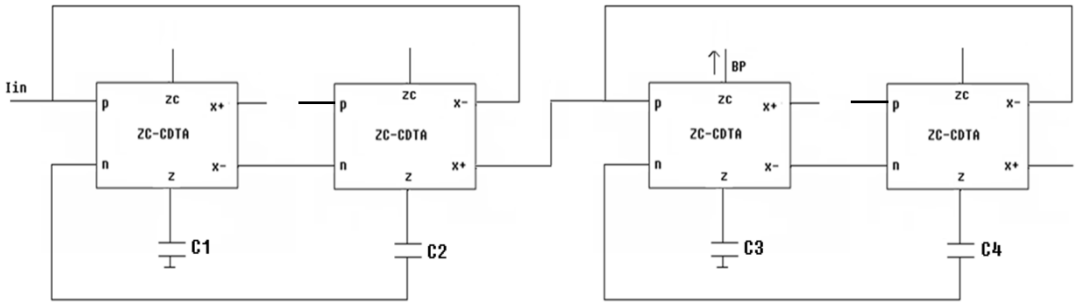

Figure 6.3 : The biquad filter structure [18].

The high-pass filter transfer function, band-pass filter transfer function, low-pass filter transfer function, the pole angular frequency ω_0 and the quality factor Q are given in Equation6.1, 6.2, 6.3, 6.4, 6.5, respectively [22].

The second order filter characteristics with post-layout simulations, the fourth order filter characteristics with ideal simulations, the fourth order filter characteristics with post-layout simulations and the total harmonic distortion of the ZC-CDTA fourth order filter structure according to the input signal level at 10MHz are given in Figure 6.4, 6.5, 6.6, 6.7, respectively.

$$\frac{I_{HP}}{I_{IN}} = \frac{C_1 C_2 s^2}{g_{m1} g_{m2} + C_2 g_{m1} s + C_1 C_2 s^2} \tag{6.1}$$

$$\frac{I_{BP}}{I_{IN}} = \frac{C_2 g_{m1} s}{g_{m1} g_{m2} + C_2 g_{m1} s + C_1 C_2 s^2} \tag{6.2}$$

$$\frac{I_{LP}}{I_{IN}} = \frac{g_{m1} g_{m2}}{g_{m1} g_{m2} + C_2 g_{m1} s + C_1 C_2 s^2} \tag{6.3}$$

$$\omega_0 = \sqrt{\frac{g_{m1} g_{m2}}{C_1 C_2}} \tag{6.4}$$

$$Q = \sqrt{\frac{g_{m2} C_1}{g_{m1} C_2}} \tag{6.5}$$

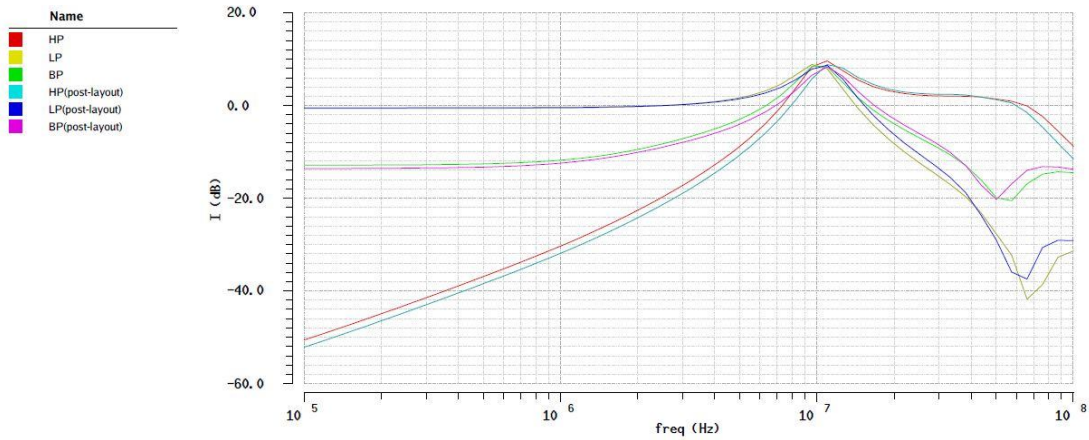

Figure 6.4 : The second order filter characteristics with post-layout simulations.

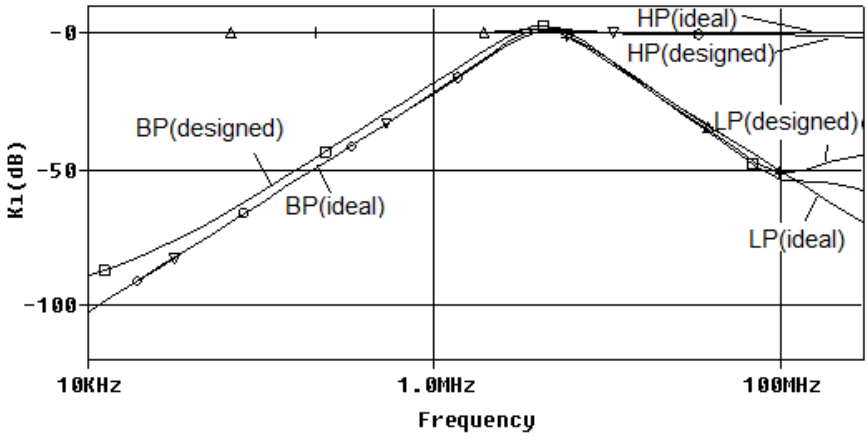

Figure 6.5 : The fourth order filter characteristics with ideal simulations.

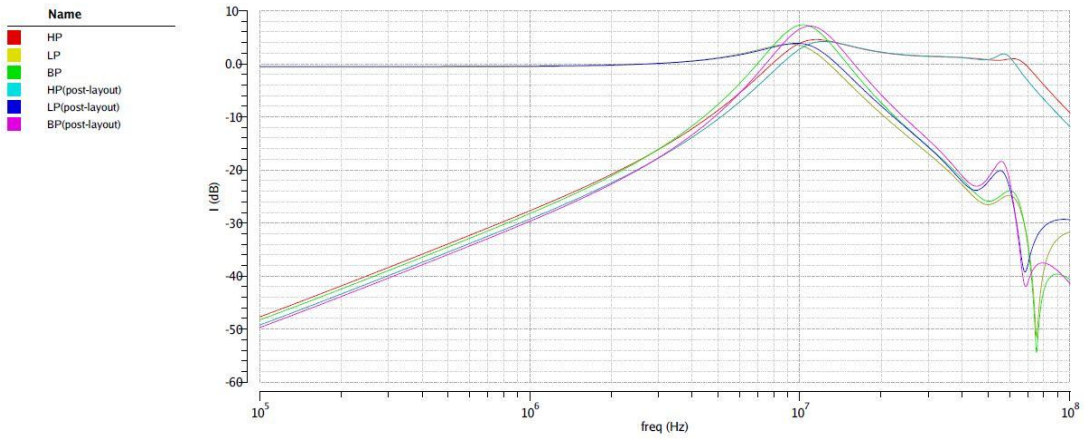

Figure 6.6 : The fourth order filter characteristics with post-layout simulations.

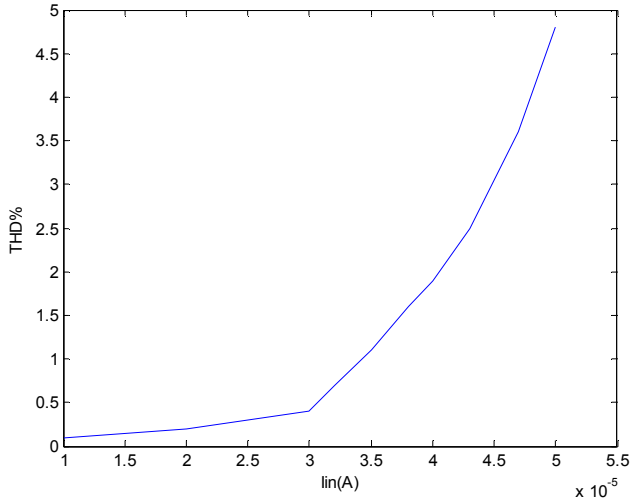

Figure 6.7 : The (THD) total harmonic distortion of ZC-CDTA fourth order filter structure .

6.2 ZC-CDBA and Its KHN Filter Application

KHN filter structure is one of the widely used filter structure in analog signal processing. KHN filter is proposed by Kerwin, Huelsman, Newcomb using state-variable synthesis in 1967. It is also produced commercially. The most important characteristic of the KHN filter transfer function is the adequacy for different type of filter implementation (band pass, high pass, low pass) at the same time. KHN filter another important property is the conformity for low sensitivity realization.

The filter structure is shown in Figure 6.8. The structure of the KHN filter has two band pass filter sections, two high pass filter sections and one low pass filter section. One of the high pass filter section is high impedance. The capacitors C_1 and C_2 are 5pF. The resistors R_1 and R_2 are 20kΩ.

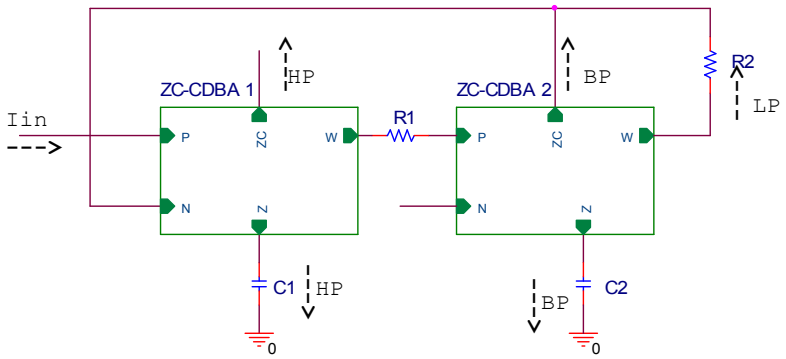

Figure 6.8 : The KHN filter structure [20].

The filter current transfer functions are yielded by hand calculations. The high-pass filter transfer function, band-pass filter transfer function, low-pass filter transfer function, the pole angular frequency ω_0 and the quality factor Q are given in Equation 6.6, 6.7, 6.8, 6.9, 6.10, respectively.

$$\frac{I_{HP}}{I_{IN}} = \frac{s^2}{s^2 + s\frac{G_1}{C_1} + \frac{G_1 G_2}{C_1 C_2}} \tag{6.6}$$

$$\frac{I_{BP}}{I_{IN}} = \frac{s\frac{G_1}{C_1}}{s^2 + s\frac{G_1}{C_1} + \frac{G_1 G_2}{C_1 C_2}} \tag{6.7}$$

$$\frac{I_{LP}}{I_{IN}} = \frac{\frac{G_1 G_2}{C_1 C_2}}{s^2 + s\frac{G_1}{C_1} + \frac{G_1 G_2}{C_1 C_2}} \tag{6.8}$$

$$\omega_0 = \sqrt{\frac{G_1 G_2}{C_1 C_2}} \tag{6.9}$$

$$Q = \sqrt{\frac{G_2 C_1}{G_1 C_2}} \tag{6.10}$$

Sensitivity analyses of the proposed filter with respect to active and passive components yield the following Equation 6.11, 6.12, respectively.

$$S_{G_1}^{W_0} = S_{G_2}^{W_0} = -S_{C_1}^{W_0} = -S_{C_2}^{W_0} = 0.5 \tag{6.11}$$

$$S_{G_2}^{Q} = S_{C_1}^{Q} = -S_{G1}^{Q} = -S_{C_2}^{Q} = 0.5 \tag{6.12}$$

The filter characteristics of the ZC-CDBA filter structure are given in Figure 6.9. The total harmonic distortion of ZC-CDBA filter structure according to the input signal level at 1.9MHz is given in Figure 6.10.

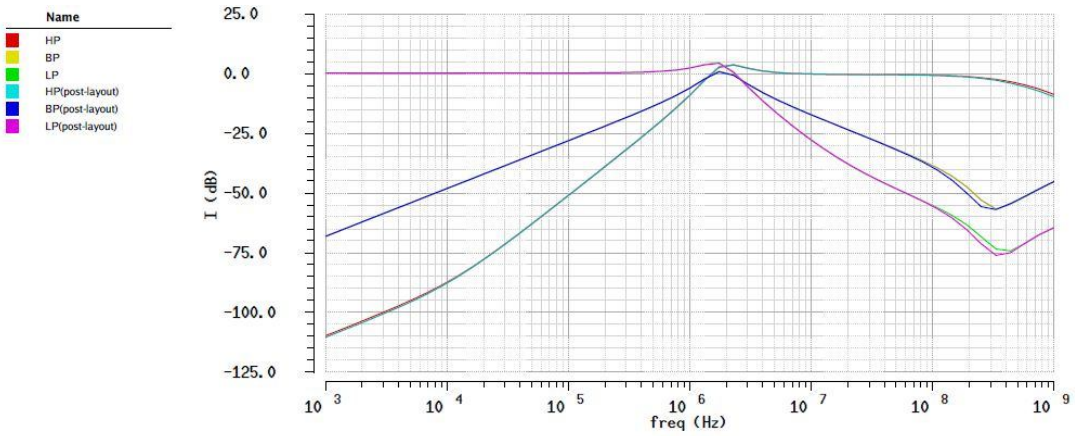

Figure 6.9 : The filter characteristics of the ZC-CDBA filter structure.

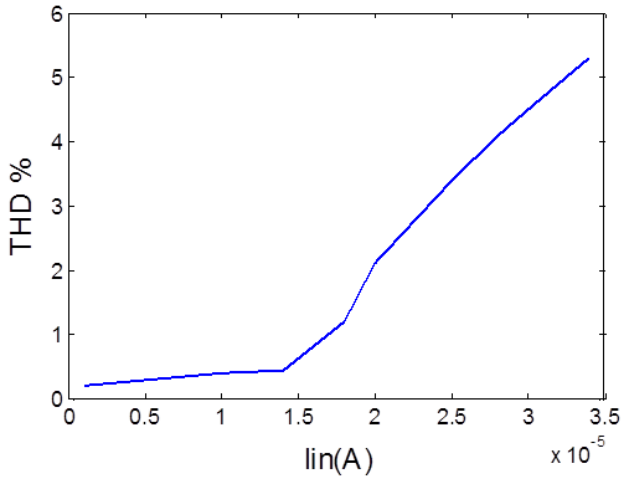

Figure 6.10 : The total harmonic distortion of ZC-CDBA filter structure at center frequency.

6.3 ZC-CG-CDBA and Its Frequency Agile Filter Application

The frequency agile filter structure is proposed by Fabre and his team to be used in encrypted communication structure. The designed frequency agile filter structure is also applicable to the global positioning systems using different protocols in different continents at the same. The proposed structure provides the signals that use different global positioning system protocols to be processed on a single discrete filter. The designed agile filter structure is given in Figure 6.11. The KHN filter structure proposed for Z-Copy Current Differencing Buffered Amplifier in Figure 6.8 is adapted for frequency agile filter structure. The capacitors C_1 and C_2 are 10pF. The resistors R_1 and R_2 are 20kΩ.

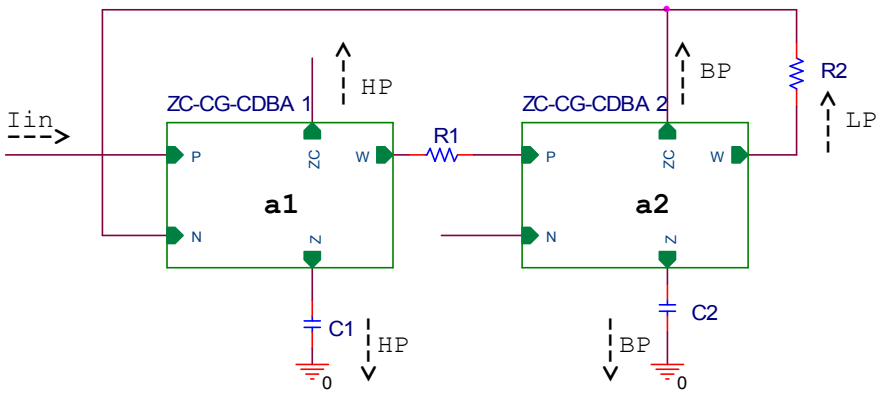

Figure 6.11 : The frequency agile filter structure [21].

The frequency agile filter transfer functions, the quality factor and the natural frequency are given in Equation 6.13, 6.14, 6.15, 6.16, 6.17, 6.18, 6.19, respectively.

$$\frac{I_{HP}}{I_{IN}} = \frac{\alpha_1 s^2}{D(s)} \tag{6.13}$$

$$\frac{I_{BP}}{I_{IN}} = \frac{\alpha_1 \frac{G_1}{C_1} s}{D(s)} \tag{6.14}$$

$$\frac{I_{LP}}{I_{IN}} = \frac{\frac{\alpha_1 \alpha_2 G_1 G_2}{C_1 C_2}}{D(s)} \tag{6.15}$$

$$D(s) = s^2 + s\frac{\alpha_1 G_1}{C_1} + \frac{\alpha_1 \alpha_2 G_1 G_2}{C_1 C_2} \tag{6.16}$$

$$\omega_0 = \sqrt{\frac{\alpha_1 \alpha_2 G_1 G_2}{C_1 C_2}} \tag{6.17}$$

$$Q = \sqrt{\frac{\alpha_2 C_1 G_2}{\alpha_1 C_2 G_1}} \tag{6.18}$$

The quality factor and the cut-off frequency of the filter change with the current gain. The disadvantage of this frequency agile filter circuit structure given in the Figure 6.11 is the stability of the quality factor.

Sensitivity analyses of the proposed filter with respect to active and passive components yield the following Equation 6.19, 6.20, respectively.

$$S_{G_1}^{\omega_0} = S_{G_2}^{\omega_0} = -S_{C_1}^{\omega_0} = -S_{C_2}^{\omega_0} = 0.5\alpha_1\alpha_2 \qquad \textbf{(6.19)}$$

$$S_{C_1}^{Q} = S_{G_2}^{Q} = -S_{C_2}^{Q} = -S_{G_1}^{Q} = 0.5\frac{\alpha_2}{\alpha_1} \qquad \textbf{(6.20)}$$

The filter characteristics of ZC-CG-CDBA for unity gain of ECCII, the total harmonic distortion, the effect of the current gain α_1 to the band-pass filter, the effect of the current gain α_1 to the high-pass filter and the effect of the current gain α_1 to the low-pass filter are given in Figure 6.12, 6.13, 6.14, 6.15 and 6.16, respectively.

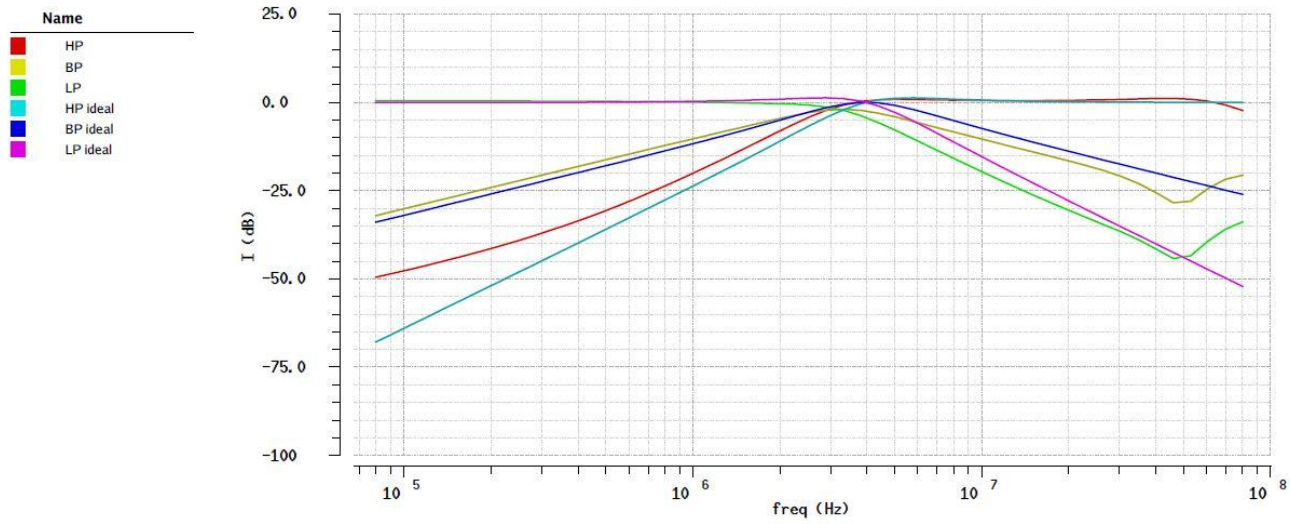

Figure 6.12 : The filter characteristics of ZC-CG-CDBA for unity gain of ECCII.

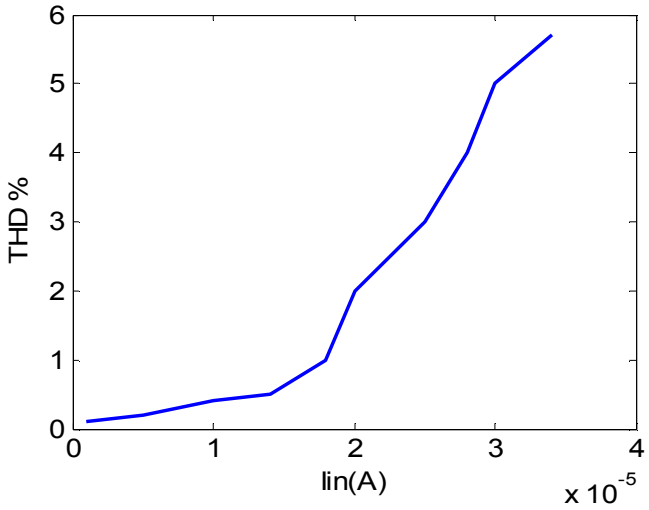

Figure 6.13 : The total harmonic distortion of ZC-CG-CDBA filter at 4MHz input signal.

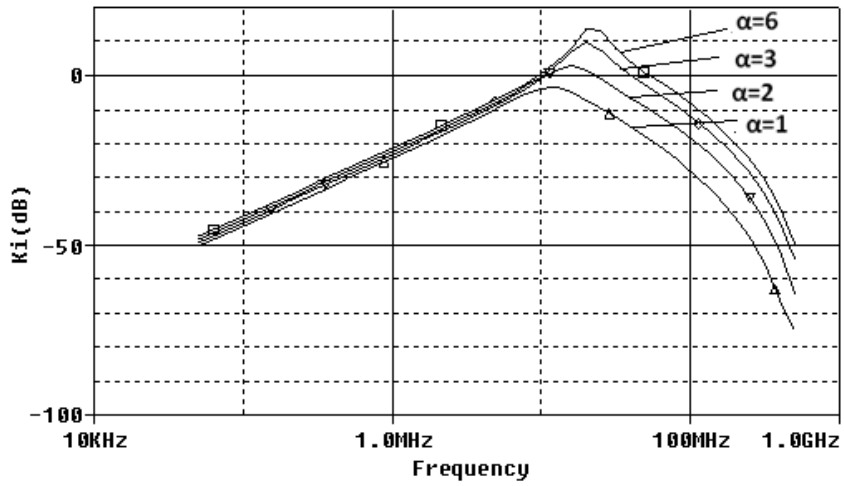

Figure 6.14 : The effect of the current gain α_1 to the band-pass section.

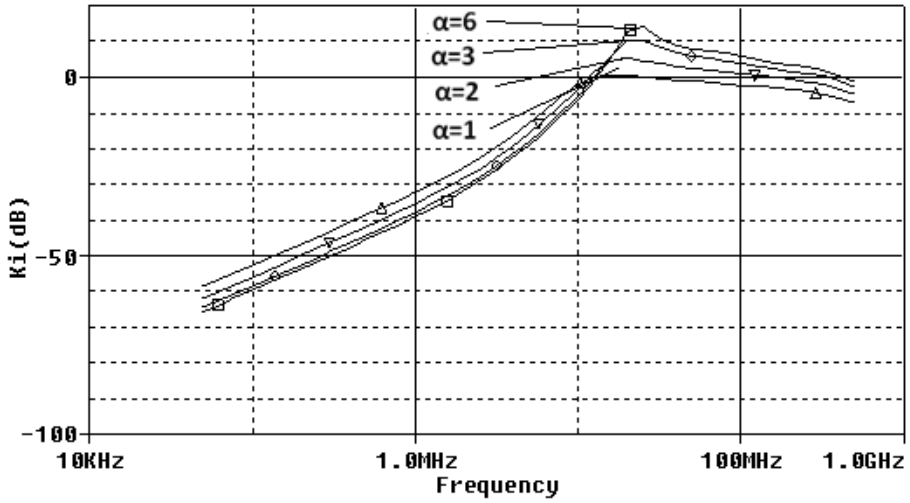

Figure 6.15 : The effect of the current gain α_1 to the high-pass section.

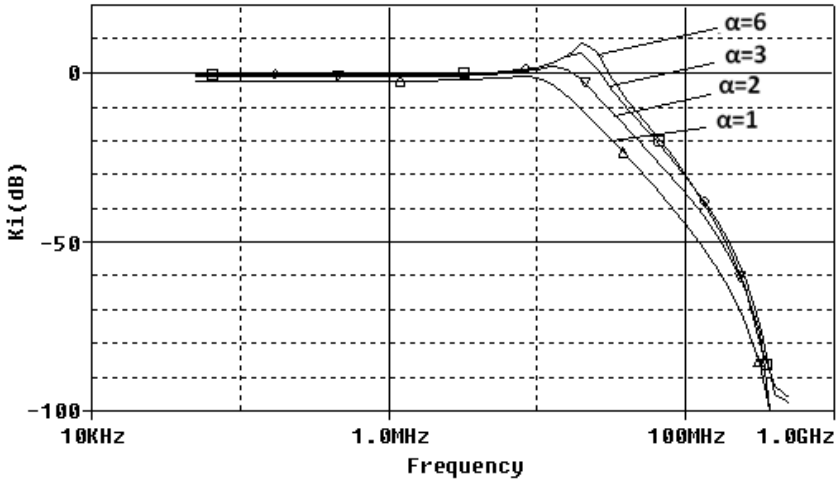

Figure 6.16 : The effect of the current gain α_1 to the low-pass section.

6.4 ZC-CDTA and its Frequency Agile Filter Structure

Frequency, bandwidths, modulation can be controllable using computer tools in Software defined radio, or SDR [23, 24, 25]. Reconfigurable receiver is possible to adapt to any frequency, band-width, modulation, etc., corresponding to the standards which were pre-selected.

Cognitive radio which searches and uses a suitable band refers to wireless architectures in which a communication system does not operate in a fixed band [26].

The software defined radio system is also applicable to provide a new solution for global positioning system to reply to the needs of five bands containing GPS, GLONASS, Galileo, Beidou, GNSS [27, 28]. It is inevitable for the biggest possible versatility of future global navigation systems, including GPS, GLONASS, Beidou, GNSS and Galileo.

Such architectures require reconfigurable analog elements: LNA, local oscillators, mixers and filters [26].

The Z copied current differencing transconductance amplifier second order filter structure is modified with a feedback system to obtain reconfigurable filter structure. This structure also called as frequency agile filter.

The second order filter structure which includes band-pass and low-pass output is given in Figure 6.17. The low-pass and band-pass filter output must be high impedance for current mode reconfigurable applications. The gain at f_0 of the band pass output is $G_{BP} = 1$ and -3 dB bandwidth is $g_{m1}/2\pi C_1$. The gain for the low pass output is $g_{m1}g_{m2}$. Figure 6.18 shows the second order current mode frequency agile filter general structure developed with second order filter structure. The output of the low pass section is applied to the input as feedback with a gain A obtained from electronically controllable second generation current conveyor.

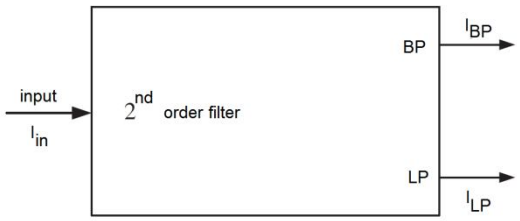

Figure 6.17 : The second order filter structure [26].

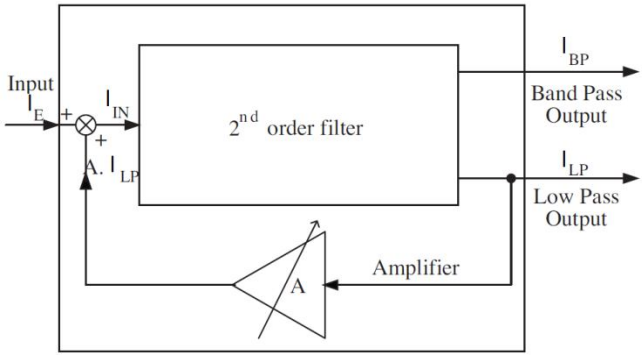

Figure 6.18 : The second order current mode frequency agile filter general structure with feedback [26].

The formulation $I_E = I_{in} - A.I_{LP}$ gives the input signal of the new circuit. The band pass function is then,

$$\frac{I_{BP}}{I_E} = \frac{\dfrac{C_2 g_{m1} s}{(1 - A g_{m1} g_{m2})}}{1 + \dfrac{C_2 g_{m1} s}{(1 - A g_{m1} g_{m2})} + \dfrac{C_1 C_2 s^2}{(1 - A g_{m1} g_{m2})}} \tag{6.21}$$

The gain at f_0 of the band pass output is $G_{BP} = 1$, remains the same as before.

The center frequency and the quality factor of the new filter structure is then,

$$\frac{(1 - A g_{m1} g_{m2})}{2\pi\sqrt{C_1 C_2}} \tag{6.22}$$

$$\sqrt{(1 - A g_{m1} g_{m2})}\,\frac{\sqrt{C_1 C_2}}{C_2 g_{m1}} \tag{6.23}$$

Electronically controllable second generation current conveyor is used to change the center frequency of the second order filter with the I_A current. The new current mode filter structure is given in Figure 6.19. The band pass output of frequency agile filter is given in Figure 6.20. The capacitors C_1 and C_2 are 10pF.

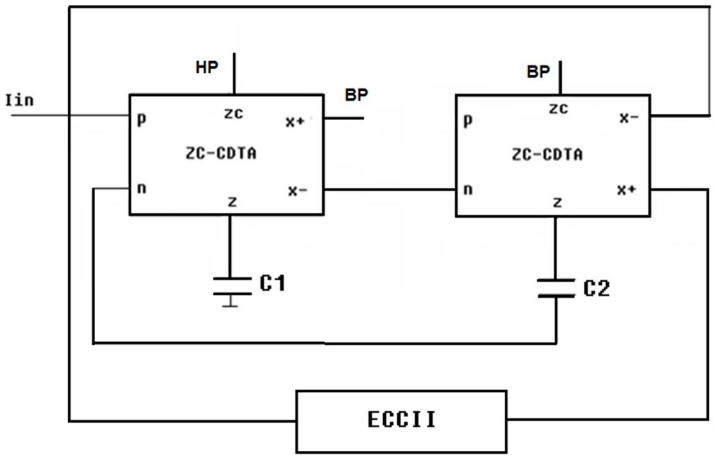

Figure 6.19 : The new current mode frequency agile filter structure.

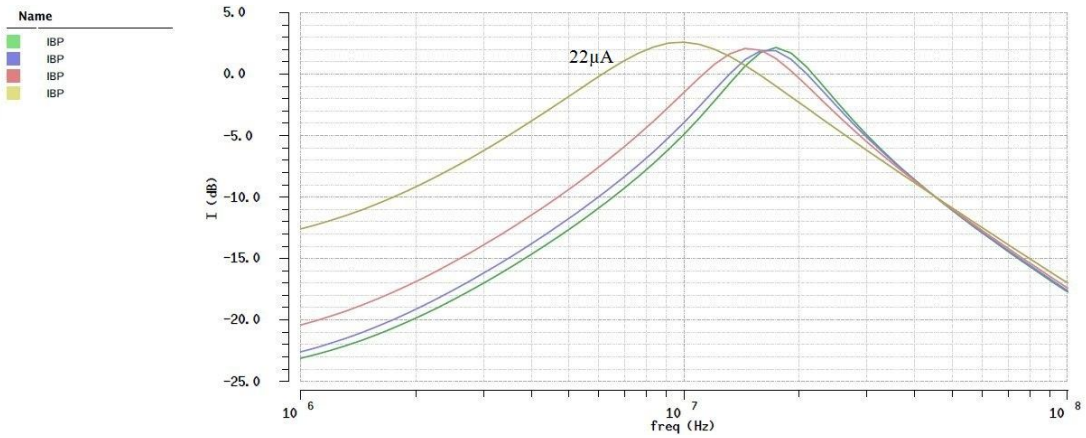

Figure 6.20 : Frequency agile filter band pass output for bias current I_A=5 µA, 10 µA, 16 µA, 22 µA.

The center frequency of band pass filter 10 MHz, 13 MHz, 16 MHz and 17 MHz are obtained for bias current I_A=22 µA, 16 µA, 10 µA, 5 µA respectively. The I_C, I_B bias currents of ECCII are selected as 60 µA.

7. CONCLUSIONS AND RECOMMENDATIONS

In this thesis ZC-CDTA (Z-Copy Current Differencing Transconductance Amplifier), ZC-CDBA (Z-Copy Current Differencing Buffered Amplifier) and ZC-CG-CDBA (Z-Copy Controlled Gain Current Differencing Buffered Amplifier) CMOS internal structures were presented. A modified biquad filter application with ZC-CDTA, a new KHN filter application with ZC-CDBA, a frequency filter application with ZC-CG-CDBA and a frequency filter application with ZC-CDTA were also proposed in this work.

In Chapter 3, low input impedance current differencing unit with positive feedback was presented. The advantages of the positive feedback system to reduce input impedances were also investigated in the same chapter.

In Chapter 4, the realization method for ZC-CDTA, ZC-CDBA and ZC-CG-CDBA were presented. The third generation current conveyor was used for obtaining the Z copy terminal current.

In Chapter 5, the Z copied current differencing buffered amplifier CMOS realization without CCIII was presented. The classical current mirror structure was used for realizing the Z copy terminal current. The advantages and disadvantages of the CCIII and the classical current mirror were investigated in this chapter. The layout of the ZC-CDBA and post-layout simulations of the ZC-CDBA were also shown. The Z copied current differencing transconductance amplifier layout was also given in this chapter. The post-layout and the pre-layout simulations are compatible with each other.

In Chapter 6 the KHN, biquad and frequency agile filters characteristics were presented. The filter chracteristics were tested with the ideal characteristics of the filters. The sensitivity analysis of the proposed KHN filter structure and frequency agile filter structure were given in this chapter of the thesis. The total harmonic distortions according to input signal magnitude were also given for all applications.

The Cadence environment was used for the design simulations. 0.18µm AMS parameters were used for all simulations of the ZC-CDTA, ZC-CDBA, ZC-CG-CDBA and sub-circuits of these new active elements. The designed circuit behaviors were tested with respect to theory.

The presented circuit and filters can be considered as another alternative for the circuit designer realized with CMOS and BJT technologies.

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CURRICULUM VITAE

Name Surname:	**ERSİN ALAYBEYOĞLU**
Place and Date of Birth:	**KASTAMONU/TURKEY 16.09.1986**
Address:	**Dept. of Electronics and Communication Engineering, Istanbul Technical University, Maslak, Istanbul, Turkey**
E-Mail:	**ersinalaybeyoglu@gmail.com**
B. Sc:	**Electrical-Electronic Engineering,Hacettepe University, Ankara, Turkey**

List of Publications:

E. Alaybeyoğlu, H. Kuntman, ” A New CMOS ZC-CDTA Realization And Its Filter Application”, ELECO '2012: Elektrik – Elektronik ve Bilgisayar Mühendisliği Sempozyumu, Bildiri Kitabı, s.262-266, 29 Kasım - 01 Aralık 2012, Bursa, Turkey.

A. Güney, **E. Alaybeyoğlu** and H. Kuntman, “New CMOS Realization of Z Copy Voltage Differencing Buffered Amplifier and Its Current-Mode Filter Application”, Proc. of DTIS'13: 8th International conference on Design & Technology of Integrated Systems, Abu Dhabi, United Arab Emirates., from March 26 to 28, 2013.

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E. Alaybeyoğlu, H. Kuntman, "Low Input Impedance Current Differencing Unit for Current Mode Active Devices Improved by Positive Feedback and ZC-CDBA Application Circuit", submitted to ELECO 2013, Bursa, Turkey.

E. Alaybeyoğlu, H. Kuntman, " A New CMOS ZC-CDTA Realization And Its Filter Application", submitted to TJEECS "Turkish Journal of Electrical Engineering & Computer Sciences".