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Electrical characterization of CeO_2/Si interface properties of metal-oxide-semiconductor field-effect transistors with CeO_2 gate dielectric

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Metal-oxide-semiconductor field-effect transistors with CeO_2 gate dielectrics were fabricated. The lowest interface trap density (D_{it}) of CeO_2/Si interface in comparison with other high-κ gated diodes is 1.47×10^{12} cm^{-2} eV^{-1} due to the very low lattice mismatch of CeO_2/Si. The interfacial properties were characterized by gated-diode measurements. The surface recombination velocity (s_0) and the minority carrier lifetime in the field-induced depletion region ($\tau_{0,\mathrm{FIJ}}$) measured from the gated diodes are about 1.03×10^4 cm/s and 2.73×10^{-8} s, respectively. The effective capture cross section of surface state (σ_s) extracted using the gated diode technique and the subthreshold swing measurement is about 8.68×10^{-15} cm^2. © *2008 American Institute of Physics*.
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With aggressive scaling of the dimensions of complementary metal-oxide-semiconductor (MOS) transistors, the issues of gate leakage current, static power consumption, and gate dielectric reliability become more important. Recently, high-dielectric-constant (high-κ) materials have been widely researched for replacing SiO_2 beyond the sub-45-nm technology node.[1–3] Among various high-κ dielectrics, cerium oxide (CeO_2) is considered as a potential candidate for high-κ dielectric application. CeO_2 has many superior properties such as good thermal stability on silicon,[4] a high value of dielectric constant (20–26), a large bandgap ($\sim$6 eV), and a very small lattice mismatch with silicon (Δa=0.35%).[5–7] However, some of the CeO_2/Si interface properties such as the effective capture cross section and the surface recombination velocity have not been fully addressed.

In this work, the CeO_2 thin films were deposited by radio frequency (rf) magnetron sputtering. The capacitance-voltage (*C-V*) measurements were made on Al/CeO_2/*p*-Si MOS capacitors. The current-voltage (*I-V*) characteristics were investigated by using Al/CeO_2/*p*-Si MOS field-effect transistors (MOSFETs). Moreover, the subthreshold measurement[8] and gated diode technique[9,10] were utilized to analyze high-κ/Si interfacial characteristics.

(100) *p*-type silicon wafers (1–5 Ω cm) were used as the starting substrate. After standard RCA clean and HF dip, the source and drain areas were defined by wet etching and doped by phosphorous (P) diffusion. The CeO_2 films were deposited by rf magnetron sputtering in argon (Ar) ambient at room temperature. The postdeposition annealing was performed at 500 °C in N_2 ambient for 60 s. The aluminum (Al) electrodes were deposited using reactive dc magnetron sputtering and patterned by a wet etching process using H_3PO_4. Postmetallization annealing was performed at 400 °C in N_2 ambient for 3 min. The thickness, refractive index, and energy bandgap of CeO_2 films were measured by N&K analyzer. The current-voltage (*I-V*) and the capacitance-voltage (*C-V*) characteristics were measured by Keithley 236 electrometer and MI494 HF *CV*/*IV* meter, respectively.

Figure 1 shows the *C-V* curve of MOS capacitor with CeO_2 dielectric annealed at 500 °C in nitrogen for 60 s. The dielectric constant and equivalent oxide thickness of the CeO_2 thin film extracted from the accumulation region are about 23.2 and 1.88 nm, respectively. Figure 2 shows the I_{DS}-V_{DS} characteristics of *n*-channel MOSFETs with CeO_2 gate dielectric. The inset in Fig. 2 shows the I_{DS}-V_{GS} curve. The subthreshold swing and the density of interface traps per area and energy (D_{it}) determined from the subthreshold region of the I_{DS}-V_{GS} curve are 67.1 mV/decade and 1.47×10^{12} cm^{-2} eV^{-1}, respectively. A I_{on}/I_{off} ratio is about 10^5–10^6 at V_{DS}=0.1 V, revealing that the MOSFETs with CeO_2 gate dielectrics have a good current switch ability.

The inset in Fig. 3 shows the setup of the gated diode measurement using a floating source and a grounded substrate of the MOSFETs. The drain corresponding to the substrate is reversely biased (V_R=V_{DB}). When the gate voltage (V_G) is less than the flatband voltage V_{FB}, the CeO_2/Si inter-

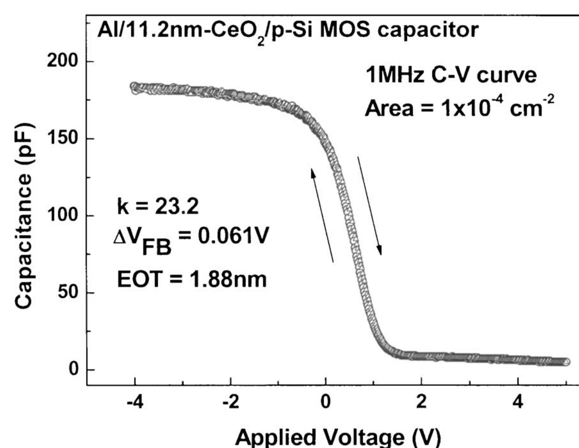

FIG. 1. The *C-V* curve of MOS capacitor with Ce_2O_3 dielectric annealed at 500 °C in nitrogen for 60 s.

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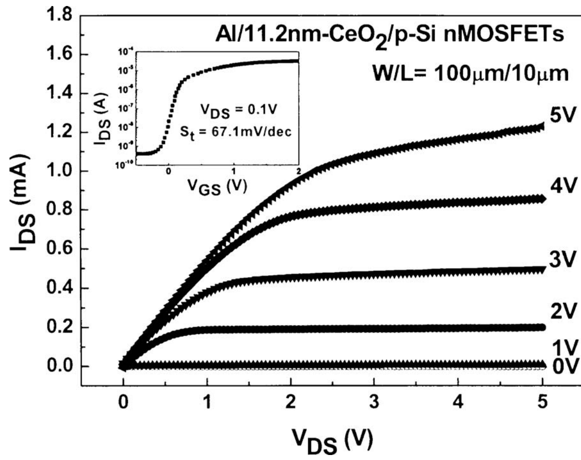

FIG. 2. The I_{DS}-V_{DS} characteristics of *n*MOSFETs with CeO_2 gate dielectric at various gate voltages V_{GS}. The inset shows the I_{DS}-V_{GS} characteristics of *n*MOSFETs with CeO_2 gate dielectric at V_{DS}=0.1 V.

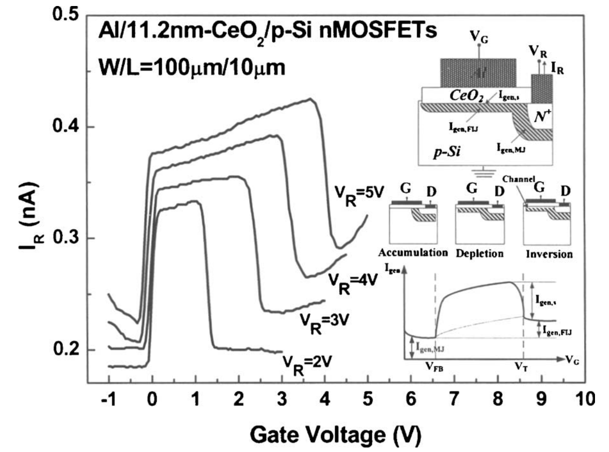

FIG. 3. The reverse diode current I_R of the gated diode with CeO_2 gate dielectric is plotted as a function of gate voltage V_G at various reverse bias V_R. The inset shows the effect of the depletion region on the reverse current I_R at various gate voltages V_G with a fixed reverse bias V_R.

face is in the accumulation mode and the reverse current (I_R) is introduced by the generation-recombination (*GR*) centers in the depletion region of the metallurgical junction ($I_{gen,MJ}$). When $V_{FB} < V_G < V_T$ (where V_T is the threshold voltage), the field-induced junction is depleted and an increase of the reverse current originates from the generation of the electron-hole pairs at the generation-recombination centers of the field-induced junction depletion region ($I_{gen,FIJ}$) and at those of the surface region ($I_{gen,s}$). The field-induced region is in the inversion mode and the reverse current is reduced by filling the interface states with the minority carriers when $V_T < V_G$. Figure 3 shows the I_R-V_G gated diode characteristics of the MOSFETs with CeO_2 gate dielectrics. The magnitude of the reverse current depends on the density of the *GR* centers and the volume of the depletion region and, therefore, is the sum of the generation currents in the metallurgical junction depletion volume and the field-induced junction depletion volume. Based on the Shockley–Read–Hall theory for single-level centers,[8] the equations of the gated diode measurement are summarized as[9,11–13]

$$I_{gen,MJ} = qU_{MJ}A_{MJ}W, \tag{1}$$

$$I_{gen,FIJ} = qU_{FIJ}A_g W_{d,max} = \frac{qn_i A_g W_{d,max}}{2\tau_{0,FIJ}}, \tag{2}$$

$$I_{gen,s} = \frac{qn_i A_g s_0}{2}, \tag{3}$$

$$s_0 = \sigma_s v_{th} N_{it} = \sigma_s v_{th}(\pi kTD_{it}), \tag{4}$$

$$W = \sqrt{\frac{2\varepsilon_{Si}}{q}(V_{bi}+V_R)\left(\frac{1}{N_A}+\frac{1}{N_D}\right)}, \tag{5}$$

$$W_{d,max} = \sqrt{\frac{2\varepsilon_{Si}}{qN_A}(2\phi_F + V_R)}, \tag{6}$$

where the U_{MJ} and U_{FIJ} are *GR* rates of the carriers per unit volume in the depletion region of the metallurgical junction and in that of the field-induced junction; A_{MJ} and A_g are the areas of the metallurgical junction and of the gate, respectively; W is the width of the depletion region of the metallurgical junction; $W_{d,max}$ is the maximum width of the surface depletion region; $n_i = 1.45 \times 10^{10}$ cm^{-3} is the intrinsic carrier concentration of Si; $\tau_{0,FIJ}$ is the minority carrier lifetime in the depletion region of the field-induced junction; s_0 is the surface recombination velocity; σ_s is the effective capture cross section; $v_{th} = 10^7$ cm/s is the thermal velocity; N_{it} is the density of the single-level surface *GR* centers per unit area; D_{it} is the density of uniformly distributed surface *GR* centers per unit area and energy; V_{bi} is the built-in potential of the *p-n* junction; and ϕ_F is the quasi-Fermi potential of the majority carriers in the substrate.

In this experiment, the interface trap density per area and energy (D_{it}) measured from the subthreshold swing is about 1.47×10^{12} cm^{-2} eV^{-1}. The minority carrier lifetime in the field-induced junction depletion region ($\tau_{0,FIJ}$) determined by the gated diode measurement is about 2.73×10^{-8} s. The surface recombination velocity (s_0) extracted from the reverse diode current ($I_{gen,s}$) at V_R=3 V in the surface region is 1.03×10^4 cm/s. The effective capture cross section (σ_s) is

TABLE I. A comparison of the experimental results of gated diodes with SiO_2, ZrO_2, and CeO_2 (this work) gate dielectrics. The V_R for CeO_2 gated diodes is 3 V.

Gate dielectrics	$I_{gen,MJ}$ (A/cm^2)	$I_{gen,s}$ (A/cm^2)	$I_{gen,FIJ}$ (A/cm^2)	s_0 (cm/s)	σ_s (cm^2)	N_{it} (cm^{-2})	D_{it} (cm^{-2} eV^{-1})	$\tau_{0,FIJ}$ (s)
SiO_2[a]	10^{-4}	10^{-8}	$\sim 1.1 \times 10^{-4}$	5	1×10^{-16}	5×10^9	5×10^{10}	10^{-5}
ZrO_2[b]	1.3×10^{-6}	4.1×10^{-6}	5.7×10^{-6}	3.5×10^3	5.8×10^{-16}	6.0×10^{11}	7.4×10^{12}	2.6×10^{-6}
CeO_2[c]	2.01×10^{-5}	1.2×10^{-5}	3.4×10^{-6}	1.03×10^4	8.68×10^{-15}	1.19×10^{11}	1.47×10^{12}	2.73×10^{-8}

[a]References 8, 9, and 14.
[b]Reference 15.
[c]This work.

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determined to be about 8.68×10^{-15} cm^2. Table I summarizes the parameters of this experiment and are compared with those of SiO_2 and ZrO_2 extracted by the same method.[8,9,14,15] The results show that the D_{it} and N_{it} values of MOSFETs with CeO_2 gate dielectric are smaller than those with ZrO_2 gate dielectric. The effective capture cross section σ_s at the CeO_2/Si interface is larger than that at the ZrO_2/Si interface.

In summary, MOSFETs with CeO_2 gate dielectric were fabricated. Using the gated diode technique and the subthreshold measurement, the surface recombination velocity (s_0), effective capture cross section (σ_s), and interface trap density per area (N_{it}) were characterized. The experimental results show that D_{it} and N_{it} of MOSFETs with CeO_2 gate dielectric are the lowest in comparison with other high-κ gated diodes. The reason of the low D_{it} and N_{it} values with CeO_2 gate dielectric is attributed to the very low lattice mismatch of CeO_2/Si interface. The effective capture cross section σ_s at the CeO_2/Si interface is about 2 orders of magnitude larger than that at the SiO_2/Si interface and about 1.5 orders of magnitude larger than that at the ZrO_2/Si interface.

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