Metal-ferroelectric (BiFeO3)-insulator (Y2O3)-semiconductor capacitors and field effect transistors for nonvolatile memory applications

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Citation: Appl. Phys. Lett. **94**, 142905 (2009); doi: 10.1063/1.3114403

View online: http://dx.doi.org/10.1063/1.3114403

View Table of Contents: http://apl.aip.org/resource/1/APPLAB/v94/i14

Published by the American Institute of Physics.

Metal-ferroelectric ($BiFeO_3$)-insulator (Y_2O_3)-semiconductor capacitors and field effect transistors for nonvolatile memory applications

Chih-Ming Lin,[1] Wen-chieh Shih,[1] Ingram Yin-ku Chang,[1] Pi-Chun Juan,[2] and Joseph Ya-min Lee[1,a)]

[1]*Department of Electrical Engineering and Institute of Electronics Engineering, National Tsing Hua University, Hsinchu 30013, Taiwan*

[2]*Department of Materials Engineering, Mingchi University of Technology, 84 Gungjuan Road, Taishan 243, Taiwan*

(Received 11 September 2008; accepted 9 March 2009; published online 8 April 2009)

Metal-ferroelectric-insulator-semiconductor capacitors and field effect transistors with $Al/BiFeO_3/Y_2O_3/Si$ structure were fabricated and characterized for nonvolatile memory applications. The capacitance-voltage curves exhibit a maximum clockwise memory window of 0.92 V. The minimum leakage current density is 2×10^{-7} A/cm^2 at an applied voltage of 5 V. The capacitance-voltage memory window as a function of the sweep voltage range was investigated. The I_{DS}-V_{GS} curves of metal-ferroelectric-insulator-semiconductor transistors show a maximum memory window of 0.84 V. The drain current on/off ratio maintained more than three orders of magnitude after an elapsed time of 10^4 s. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3114403]

Ferroelectric random access memory (FRAM) is a promising candidate for nonvolatile memories. FRAM with one transistor and one ferroelectric capacitor (1T1C) per cell has been used for commercial applications. However, limited storage density and destructive readout operation are drawbacks for 1T1C FRAM.[1] The ferroelectric field effect transistor with metal-ferroelectric-insulator-silicon (MFIS) structure has a great potential for nonvolatile memories because of its high speed, single-device structure, low power consumption, and nondestructive readout operation.[1,2] Many ferroelectric materials such as $YMnO_3$,[3] $Pb(Zr_xTi_{1-x})O_3$ (PZT) (Ref. 4), and $SrBi_2Ta_2O_9$ (SBT) (Ref. 5) were used for MFIS application. Recently, multiferroic $BiFeO_3$ (BFO) has attracted much attention due to its high Curie temperature (T_C) of about 850 °C and high Neel temperature (T_N) of about 370 °C.[6–8] In comparison with other ferroelectric materials such as PZT and SBT, low crystallization temperature[9] and large remnant polarization (P_r) (Ref. 10) are the desirable properties of BFO to fabricate MFIS devices. The purpose of the insulator layer is to prevent the reaction and interdiffusion between the ferroelectric layer and the silicon substrate as well as to improve the retention properties.[11,12] In order to minimize the voltage across the insulator layer, high dielectric constant insulators are desirable. Furthermore, low leakage current, good interface characteristics, and compatibility with silicon device processing are required in choosing the insulating layer. The dielectric constant of Y_2O_3 ranges form 12 to 18 (Ref. 13) and Y_2O_3 is thermodynamically stable in contact with silicon.[14] Y_2O_3 film is also known to improve the electrical properties of MFIS structure such as memory window, leakage current, and retention.[15] In this work, the electrical properties of $Al/BFO/Y_2O_3/Si$ MFIS capacitors and transistors with the ferroelectric layer annealed at different temperatures were reported.

P-type, (100) orientation, 4 in. diameter silicon wafers (1–5 Ω cm) were used as the starting substrates. A 500 nm sacrificial SiO_2 used for implant mask layer was grown on the silicon wafers by wet oxidation. The oxide on the backside was then removed. The source and drain areas were implanted with phosphorous and annealed at 900 °C in N_2 for 60 s. A standard dip etch ($HF:H_2O=1:10$) was performed before insulating film deposition. The insulating layer Y_2O_3 was deposited by rf magnetron sputtering at room temperature in pure argon gas. The Y_2O_3 film thickness is about 10 nm. After deposition, the Y_2O_3 films were rapid thermal annealed (RTA) in nitrogen at 500 °C for 60 s. The contact regions of Y_2O_3 layer were etched by buffered oxide etch. The ferroelectric layer BFO was deposited by rf magnetron sputtering. The Bi/Fe atom percentage ratio was examined by x-ray photoelectron spectroscopy. The Bi/Fe ratio of the $BiFeO_3$ film composition was about 0.95. The BFO thin film is about 120 nm thick. The BFO films were RTA in nitrogen at 500 or 600 °C for 60 s in order to crystallize the BFO film. The contact regions of BFO layer were etched by $HF/HNO_3/H_2O$ etching solution. The ratio of $HF/HNO_3/H_2O$ was 1/1/100. Finally, a 150 nm thick aluminum was used as the top electrode. Aluminum was deposited by dc sputtering. The aluminum pattern was etched by

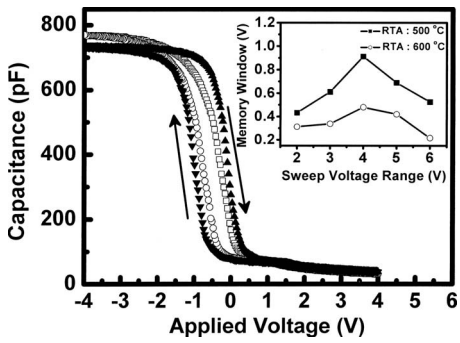

FIG. 1. High-frequency (1 MHz) capacitance-voltage (*C-V*) curves of $Al/BFO/Y_2O_3/p$-Si capacitors with a sweep voltage range of 4 V. The samples were annealed at 500 or 600 °C. The inset shows the memory windows of $Al/BFO/Y_2O_3/p$-Si capacitors as a function of the sweep voltage range.

a)Electronic mail: ymlee@ee.nthu.edu.tw.

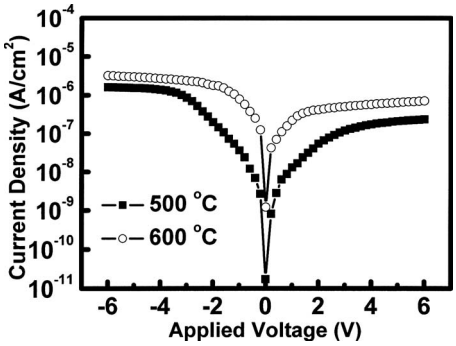

FIG. 2. The current density-voltage (J-V) characteristics of Al/BFO/Y_2O_3/p-Si capacitors with BFO layer annealed at 500 or 600 °C.

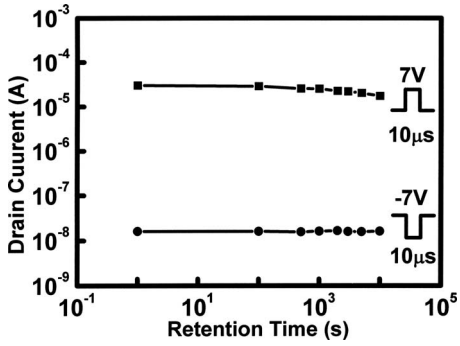

FIG. 4. The drain current versus time (I_{DS}-t) measurement of Al/BFO/Y_2O_3/p-Si MFIS transistor.

H_3PO_4. The postmetallization annealing was performed at 400 °C in N_2 for 30 s.

The capacitance-voltage (C-V) and current-voltage (I-V) characteristics were measured using C-V meter (MegaBytek Mi–494) and Keithley 236 electrometer, respectively.

Figure 1 shows the typical C-V curves of Al/BFO/Y_2O_3/Si capacitors with the BFO layer annealed at 500 or 600 °C for 60 s in nitrogen. The sweep voltage range is 4 V. The C-V characteristics exhibit clockwise hysteresis loops due to the ferroelectric polarization of $BiFeO_3$. The memory window is defined as the voltage shift when the bias voltage is swept from accumulation to inversion and back. The inset shows the memory window measured from the C-V curves of MFIS capacitors with a sweep voltage from ±2 to ±6 V. The memory window depends on the magnitude of the applied voltage range. The memory window increases with the sweep voltage range from 2 to 4 V but decreases from 4 to 6 V due to charge injection. This indicates that the charge injection effect becomes more serious when the applied voltage range is larger than 4 V. The maximum memory window of C-V curves is 0.92 V at a sweep voltage range of 4 V for BFO layer annealed at 500 °C and 0.48 V at 600 °C. The theoretical memory window $\Delta W \approx 2d_f E_c$ (Ref. 13) was 1.14 V, where the coercive field (E_c) is 47.5 kV/cm and d_f is the BFO thickness of 120 nm. If the charge injection effect was considered, the theoretical memory window should be modified as $\Delta W \approx 2d_f E_c - V_{ci}$,[14] where V_{ci} is the voltage shift due to charge injection. V_{ci} was calculated to be 0.22 V. The memory windows of MFIS capacitors annealed at 500 °C were larger than those annealed at 600 °C. Consequently, the C-V characteristics of MFIS capacitors with BFO layer annealed at 500 °C show better properties than those annealed at 600 °C.

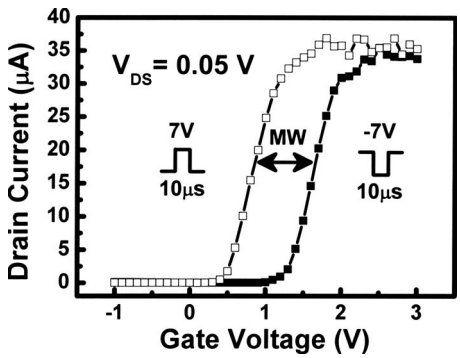

FIG. 3. The I_{DS}-V_{GS} characteristics of Al/BFO/Y_2O_3/p-Si MFIS transistor after negative and positive poling voltage pulses. MW stands for memory window. The channel width and length were 100 and 10 μm, respectively.

The leakage current plays an important role in controlling the charge retention properties of memory devices. Figure 2 shows the current density-voltage (J-V) characteristics of Al/BFO/Y_2O_3/Si capacitors annealed at 500 or 600 °C for 60 s in N_2. The leakage current density of MFIS capacitors annealed at 500 °C was about 2×10^{-7} A/cm^2 at an applied gate voltage of 5 V. However, when the annealing temperature increases to 600 °C, the leakage current density increases from 2×10^{-7} to 6.5×10^{-7} A/cm^2. From x-ray diffraction result, other phases appeared at the annealing temperature of 600 °C and the leakage current increased.

The I_{DS}-V_{GS} memory window of Al/BFO/Y_2O_3/Si MFIS transistors was measured using samples annealed at 500 °C. Figure 3 shows the I_{DS}-V_{GS} characteristics with writing pulse voltages of −7 and 7 V and a pulse width of 10 μs. The orientation of I_{DS}-V_{GS} hysteresis loop was determined by ferroelectric polarization. The I_{DS}-V_{GS} memory window was 0.84 V.

Figure 4 shows the retention time measurement of Al/BFO/Y_2O_3/Si metal-ferroelectric-insulator-silicon field-effect transistor (MFISFET). The retention time was measured after applying writing pulses of −7 and 7 V with a pulse width of 10 μs. The drain current on/off ratio was larger than three orders of magnitude after applying these pulses. As shown in Fig. 4, the Al/BFO/Y_2O_3/Si MFISFETs still maintained a drain current on/off ratio of more than three orders of magnitude after an elapsed time of 10^4 s.

In summary, the different annealing temperatures of 500 and 600 °C were used to crystallize the BFO thin films. MFIS capacitors annealed at 500 °C show better electrical properties than those annealed at 600 °C. A leakage current density of 2×10^{-7} A/cm^2 and a memory window of 0.92 V were observed at the BFO annealing temperature of 500 °C. The I_{DS}-V_{GS} memory window was 0.84 V with a poling pulse voltage of ±7 V and a duration of 10 μs. The Al/BFO/Y_2O_3/Si transistors exhibit excellent retention time. The Al/BFO/Y_2O_3/Si field effect transistors show good potential for nonvolatile memory applications.

The authors wish to thank the National Science Council of Taiwan, Republic of China for supporting this work under Grant No. NSC96-2221-E-007-160.

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