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Electrical Characteristics of High Quality La_2O_3 Gate Dielectric with Equivalent Oxide Thickness of 5 Å

Y. H. Wu, M. Y. Yang, Albert Chin, *Senior Member, IEEE*, W. J. Chen, and C. M. Kwei

***Abstract*—Electrical and reliability properties of ultrathin La_2O_3 gate dielectric have been investigated. The measured capacitance of 33 Å La_2O_3 gate dielectric is 7.2 μF/cm^2 that gives an effective K value of 27 and an equivalent oxide thickness of 4.8 Å. Good dielectric integrity is evidenced from the low leakage current density of 0.06 A/cm^2 at -1 V, high effective breakdown field of 13.5 MV/cm, low interface-trap density of 3×10^{10} eV^{-1}/cm^2, and excellent reliability with more than 10 years lifetime even at 2 V bias. In addition to high K, these dielectric properties are very close to conventional thermal SiO_2.**

***Index Terms*—High K dielectric, leakage current, reliability.**

I. Introduction

According to scaling rule, high K gate dielectric [1]–[9] with equivalent oxide thickness (EOT) below 10–15 Å will soon be required for sub-0.1 μm devices. Unfortunately, the effective EOT value of some high K dielectrics may be limited by the interface reaction region between dielectric and Si. Therefore, the search for thermodynamically stable high K dielectric on Si is the essential factor to achieve a small EOT. In addition to low EOT and leakage current, the high K gate dielectric must have good interface property, high thermal stability, good reliability, and process compatibility to current VLSI technology. Recently, we have developed the Al_2O_3 material [9] that can satisfy almost all the above requirement and has a $K(\sim 9)$ higher than Si_3N_4. However, further reduction of EOT below 10 Å is difficult because of relatively low K. In this letter, we have studied the dielectric integrity of La_2O_3 that has a very high effective $K(\sim 27)$ and better thermodynamic stability on Si than Al_2O_3. In additional to the small EOT of 4.8 Å, good dielectric integrity and lifetime longer than ten years at 2 V is achieved.

II. Experimental

Standard p-type Si wafers were used in this study. After device isolation, native oxide is suppressed by HF-vapor passivation [9]–[11] and *in-situ* thermal desorption followed by amorphous La layer deposition. Low temperature oxidation at temperatures of 400–500 °C for 1 h is performed and annealed at 900 °C in nitrogen ambient. The dielectric thickness is carefully measured by ellipsometer that is calibrated by cross-sectional TEM. The direct oxidation of deposited La to form high K La_2O_3 is a very simple process and similar to conventional thermal SiO_2 in comparison with CVD [12] or sputtering deposited [13] gate dielectric. Al gate is used for MOS devices to reduce gate depletion or accumulation width. Dielectric leakage current, D_{it}, and reliability are characterized by current–voltage (*I–V*), capacitance–voltage (*C–V*), and time-dependent-dielectric-breakdown (TDDB), respectively. Typical device size is 100 μm $\times$100 μm.

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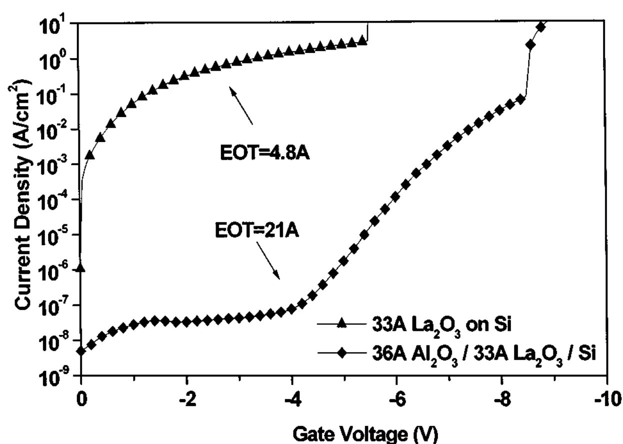

Fig. 1. *J–V* characteristics of 33 Å La_2O_3 and 36 Å Al_2O_3/33 Å La_2O_3 gate dielectrics on Si. The stacked structure is used to reduce the leakage current for further *C–V* measurement.

III. Results and Discussion

Fig. 1 shows the *J–V* characteristics of 33 Å La_2O_3 and 36 Å Al_2O_3/33 Å La_2O_3 MOS devices measured under accumulation. For 33 Å La_2O_3, a low leakage current of 0.06 A/cm^2 at -1 V and a high breakdown field of 13.5 MV/cm (by deducting flatband voltage) are obtained that are suitable for sub-μm devices application. However, according to the electric displacement continuity at high K dielectric and Si interface

$$\varepsilon_0 K E_d = \varepsilon_{\rm Si} E_{\rm Si}. \tag{1}$$

Significant potential drop in Si is expected that may overestimate the actual breakdown electric field in La_2O_3 due to the high K. Because the leakage current in La_2O_3 is still too high for quasistatic *C–V*, we have used the stacked 36 Å Al_2O_3/33 Å La_2O_3/Si structure to lower the leakage current for D_{it} measurement.

Fig. 2 shows the *C–V* characteristics of 33 Å La_2O_3 and stacked 36 Å Al_2O_3/33 Å La_2O_3 on Si, where effective K and EOT can be calculated by $t_d C/\varepsilon_o A$ and $\varepsilon_{ox} t_d/\varepsilon_0 K$, re-

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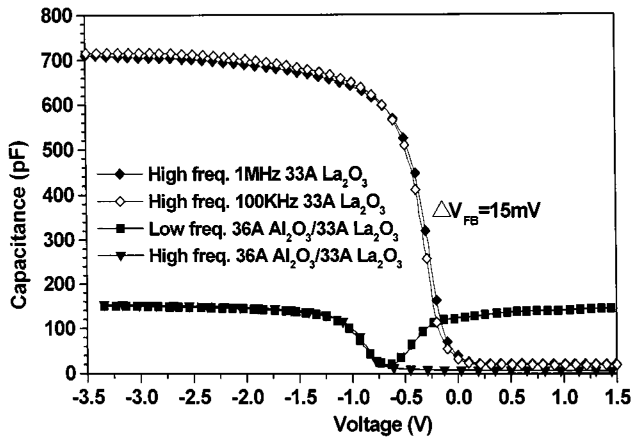


Fig. 2. *C–V* characteristics of 33 Å La_2O_3 and 36 Å Al_2O_3/33 Å La_2O_3 gate dielectrics on Si.

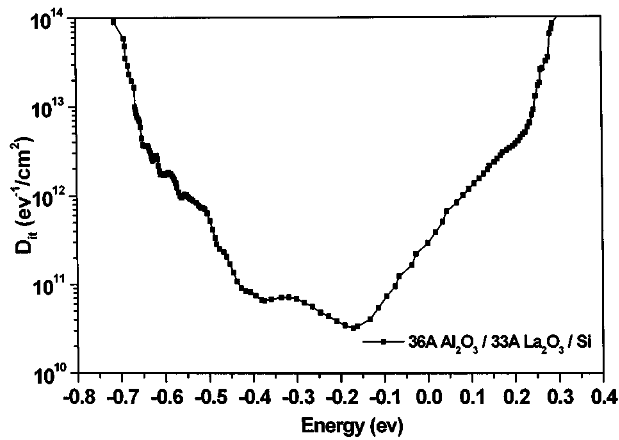
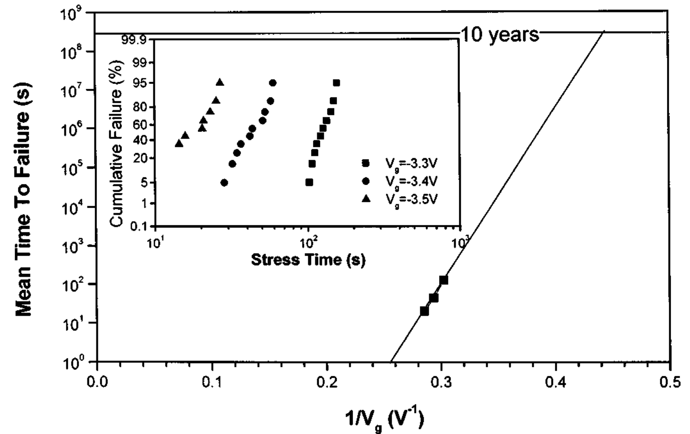
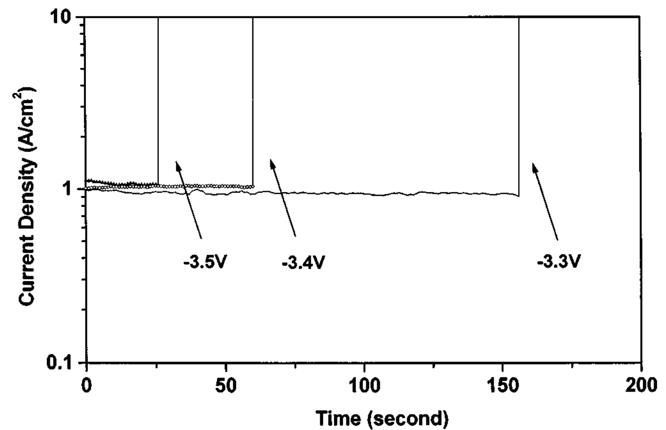


Fig. 3. Interface-trap density of 36 Å Al_2O_3/33 Å La_2O_3 gate dielectric on Si.



(a)



(b)

Fig. 4. (a) Extrapolated maximum voltage for ten years lifetime and cumulative breakdown distribution, and (b) the time evolution of gate current for 33 Å La_2O_3 gate dielectrics with different bias voltages.

spectively. As shown in Fig. 2, a capacitance of 7.2 μF/cm^2 is measured that gives 33 Å La_2O_3 effective K and EOT of 27 and 4.8 Å, respectively. To our best knowledge, the 4.8 Å EOT is the smallest value reported so far. The small frequency dispersion of 15 mV is measured that suggests the good dielectric quality. This very low EOT is believed to be due to the high thermodynamic stability as contact with Si. In conventional thermal SiO2, a ~3 Å thickness deduction by quantum correction (QC) is required from EOT to obtain the actual physical thickness [14].However, a smaller QC is expected in high K dielectric because of the smaller valence band barrier and hole wave function penetration:

$$\Psi \sim \exp(-kx) = \exp\left(-\frac{\sqrt{2m_d^*E}}{\hbar}x\right). \tag{2}$$

An additional 1 Å QC reduction is obtained in high K dielectric if the valence band barrier is lowered to 2 eV. Furthermore, due to the strong electric field and voltage drop [14], [15] in Si shown in (1), the hole wave function can be further pushed closer to interface. Because of lacking important dielectric property and full quantum-mechanical solution, an effective K is used here although a physical K of 39 is obtained by assuming a 1.5 Å QC.

We have further plotted the D_{it} as a function of energy from quasistatic and high frequency *C–V* curves. As shown in Fig. 3, a minimum D_{it} of 3×10^{10} eV^{-1}/cm^2 is obtained that is the same as current advanced oxynitride [16] and close to conventional thermal SiO_2. This is the lowest reported D_{it} for high K dielectrics other than oxynitride. Although a flatband voltage shift is expected due to the increased dielectric charge resulted from additional 36 Å Al_2O_3, an accurate D_{it} can still be obtained because D_{it} is calculated from the difference between quasistatic and high frequencies *C–V* curves. The low D_{it} is extremely important for practical CMOS based integrated circuit application, because it is directly related to 1/f noise at low frequencies [16].

We have investigated gate dielectric reliability of 33 Å La_2O_3 with small 4.8 Å EOT and low leakage current. Fig. 4(a) shows the extrapolated operation voltage for ten years lifetime obtained from inserted cumulative TDDB distribution that is calculated from the time evolution of gate current shown in Fig. 4(b). Although charges trapping and de-trapping are observed, no observable soft breakdown is found instead of hard breakdown that may be due to the low electric field inside gate dielectric. The breakdown time increases as decreasing stress voltage from 3.5 to 3.3 V and an operation voltage of 2.3 V is obtained for ten years operation with 50%

mean-time-to-failure. This result suggests La_2O_3 gate dielectric is suitable for continuous operation even at VLSI generations of current 0.18 μm and beyond.

IV. CONCLUSIONS

We have developed a new high K La $_2O_3$ with good dielectric integrity formed by a very simple process using direct oxidizing the deposit La on Si.

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