Low-Loss Single and Differential Semi-Coaxial Interconnects in Standard CMOS Process

Jun-De Jin[1], Shawn S. H. Hsu[1], Ming-Ta Yang[2], and Sally Liu[2]

[1]Dept. of Electrical Engineering and Institute of Electronics Engineering,
National Tsing Hua University, Hsinchu, Taiwan 300, R.O.C.
[2]Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan 300-77, R.O.C.
Tel: 886-3-5731278; Fax: 886-3-5752120; Email: shhsu@ee.nthu.edu.tw

Abstract — The low-loss single semi-coaxial (S-SC) and differential semi-coaxial (D-SC) interconnects based on a standard 0.18-μm CMOS process are presented for the first time. Compared to the attenuation constant (α) reported for microstrip and CPW interconnects in CMOS process, the S-SC line shows the lowest loss of 0.90 dB/mm at 50 GHz. The D-SC line also presents a very low differential-mode α of ~ 1.00 dB/mm at high frequencies. The characteristics of D-SC lines for differential-mode and common-mode are also investigated in details based on the measured mixed-mode S-parameters.

Index Terms — CMOS, CPW, differential line, microstrip, semi-coaxial interconnects.

I. INTRODUCTION

As the operation frequency of the silicon-based integrated-circuits dramatically increases, the impacts of interconnects on the circuit performance become non-negligible [1]-[2]. For high frequency circuits, the commonly used interconnect structures are the microstrip (MS) line [3]-[4] and coplanar-waveguide (CPW) [4]-[6]. For Si-based ICs, however, they may not be the best candidates due to the crosstalk between the signal lines (MS line) and the signal loss from the lossy Si substrate (CPW) [7].

Intuitively, a coaxial line is probably one of the best choices for low loss and low crosstalk interconnects at high frequencies. In this study, low-loss interconnects with a semi-coaxial (SC) structure are realized by utilizing the multiple metal layers in modern CMOS process. Both single SC (S-SC) and differential SC (D-SC) lines are designed and characterized. With a semi-rounded ground plane, the SC line structure can be expected to present characteristics close to ideal transmission lines. Similar concepts have been reported in [8], but only with simulated results of S-SC lines in SOI process. Investigation on both S-SC and D-SC lines in standard CMOS technologies has not been reported to date.

In this paper, the low-loss S-SC and D-SC lines are designed and characterized from 0.2 to 50 GHz. Section II compares different interconnect structures, and describes the design procedure. Section III presents measured results and discussions of S-SC and D-SC lines. The characteristics of D-SC lines for differential-mode and common-mode are also investigated in details based on the measured mixed-mode S-parameters [9]. Section IV concludes this work.

II. DESIGN OF S-SC AND D-SC INTERCONNECTS

Three different RF interconnect structures in CMOS process are shown in Fig. 1. As shown in Fig. 1(a), the MS line suffers from signal crosstalk, while possesses a good shielding from the lossy Si substrate. On the other hand, the CPW can be expected to show better crosstalk elimination by the two adjacent ground lines, as shown in Fig. 1(b). However, this structure cannot prevent the loss introduced by the unshielded Si substrate, which is referred as substrate skin effect [7]. By using a semi-rounded ground plane, as shown in Fig. 1(c) and (d), the SC lines provide a perfect shielding of the signal lines from the crosstalk and the lossy substrate to achieve a low-loss characteristic over a wide frequency range.

The designed SC lines were fabricated in a standard 1P6M 0.18-μm CMOS process. The signal line utilizes the top-metal layer (M6) with a thickness of 2.34 μm, while the semi-
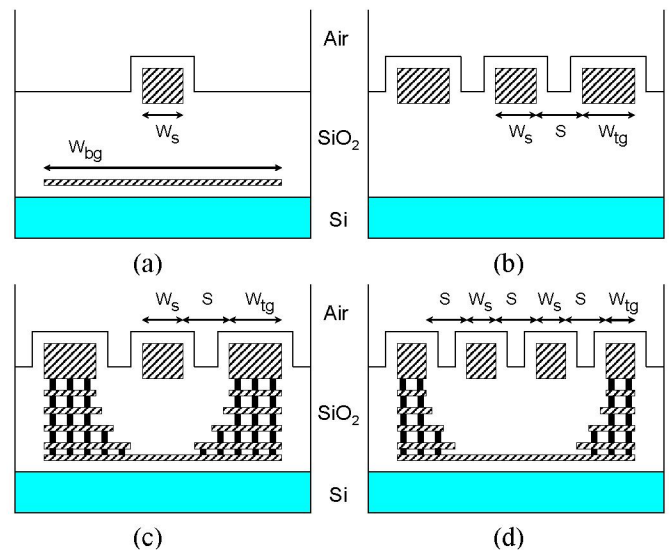

Fig. 1. RF interconnect structures for (a) MS line, (b) CPW, (c) SC line, (d) differential SC line in a standard 1P6M CMOS process.

TABLE I
GEOMETRIES OF DESIGNED SC LINES (L = 400 μm)

	W_s (μm)	S (μm)	W_{tg} (μm)	Z_0 (Ω)
S-SC1, D-SC1	15	2.4	15	33
S-SC2, D-SC2	15	79.5	15	50
S-SC3, D-SC3	5	2.4	5	50
S-SC4, D-SC4	5	10.8	5	75

rounded ground planes employs the multiple metal layers from M1 to M6. For S-SC lines, the geometries were designed by the empirical equations for Z_0 [10] with three different characteristic impedances (Z_0) of 33, 50, and 75 Ω, as summarized in Table I. The W_{tg} was designed the same as W_s, and the W_s, S, and W_{tg} of the D-SC lines are identical to those of the S-SC lines. The length of all SC lines is 400 μm due to the limited chip area.

III. MEASUREMENT RESULTS AND DISCUSSIONS

The S-SC lines were measured on-wafer with Cascade coplanar ground-signal-ground (GSG) infinity probes and Agilent 8510XF two-port vector network analyzer (VNA) from 0.2 to 50 GHz, and D-SC lines with GSGSG infinity probes and Agilent E8364A four-port PNA. For the Si-based interconnects measurements, de-embedding becomes a critical issue due to the low signal level and the lossy Si substrate. In this study, special cares were taken for the probing pads to achieve an accurate de-embedded procedure. First, a grounded M1 is applied underneath the probing pads to eliminate the generation of frequency-dependent series resistance and inductance from the lossy Si substrate [7]. Second, the pads area is minimized to 50 × 50 μm² to alleviate the parallel parasitic capacitance.

A. Characteristics of S-SC Lines

After de-embedding, Z_0 and attenuation constant (α) of the S-SC lines were both extracted from the measured S-parameters [11], as shown in Fig. 2. The line S-SC2 presents an α of 0.90 dB/mm at 50 GHz. Compared to the α values of 5.04 dB/mm (MS line) and 1.22 dB/mm (CPW) previously reported in a 0.13-μm CMOS process with a top metal thickness of 3.3 μm [4], the CMOS SC line here shows a substantially lower value even with a smaller top-metal thickness of 2.34 μm. This can be attributed to the lossy Si substrate is perfectly shielded and the semi-coaxial structure can support a wave propagation close to an ideal TEM mode.

Also observed from Fig. 2, the dependence of α on the interconnect geometry can be understood by the equation of a low-loss interconnect:
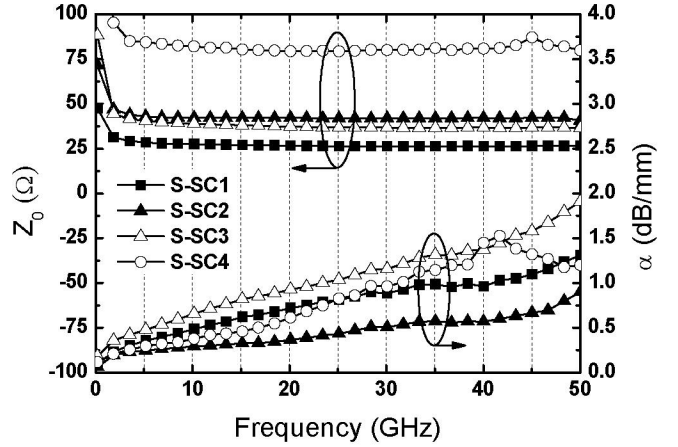

Fig. 2. Z_0 and α for S-SC lines (L = 400 μm).

$$\alpha = \frac{R}{2Z_0} \qquad (1)$$

where R is the distributed resistance. As can be seen, α is not only proportional to R but also inversely proportional to Z_0. From a comparison between the lines with the same W_s, a larger Z_0 results in a smaller α. For lines with the same Z_0, the wider line (S-SC2) presents a lower loss. The trends of α in Fig. 2 are all consistent with (1).

B. Characteristics of D-SC Lines

Since a four-port D-SC line is driven by both the differential- and common-mode signals, the RF characteristics are usually described using the mixed-mode S-parameters. Four 2×2 matrixes are included, and referred as the S-parameters of differential-mode (S_{dd}), common-mode (S_{cc}), differential-to-common-mode (S_{dc}), and common-to-differential-mode (S_{cd}). The measured four-port S-parameters of D-SC lines are converted to the mixed-mode S-parameters [12]. For a symmetric differential line as studied here, S_{dc} and S_{cd} are not existed, and only S_{dd} and S_{cc} are discussed. The measured differential-mode Z_0 (Z_{0dd}) and α (α_{dd}) can be calculated from S_{dd}, while the common-mode Z_0 (Z_{0cc}) was obtained from S_{cc}. As shown in Fig. 3, the line D-SC2 shows the lowest α_{dd} of ~ 1.00 dB/mm at around 50 GHz, which can be explained by the similar reasons of the S-SC lines. In addition, for a weakly coupled differential line, Z_{0dd} should be ~ $2Z_0$ and Z_{0cc} ~ $Z_0/2$. This can be observed from line D-SC2 due to a large signal line spacing (S) of 79.5 μm is employed.

Fig. 4(a) is the distributed $RLGC$ circuit model of a symmetric differential line including the coupling effect between the two signal lines. The distributed mutual inductance (L_m) and capacitance (C_m) describe the intensity of current coupling and voltage coupling, respectively. The four-port differential line model can be converted to one differential- and one common-mode two-port circuit models,
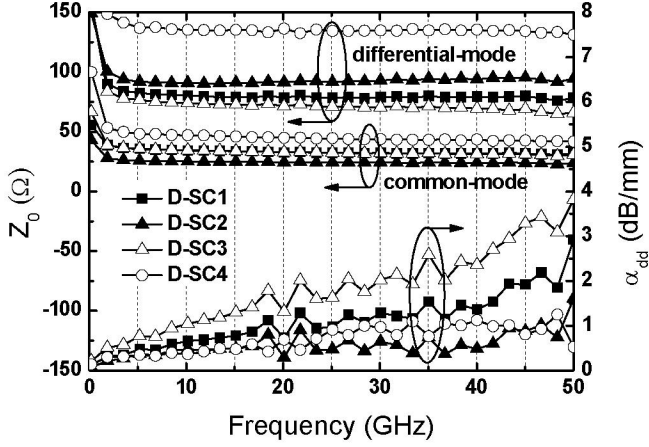
Fig. 3. Differential-mode Z_0 (Z_{0dd}), common-mode Z_0 (Z_{0cc}), and differential-mode α (α_{dd}) for D-SC lines (L = 400 μm).
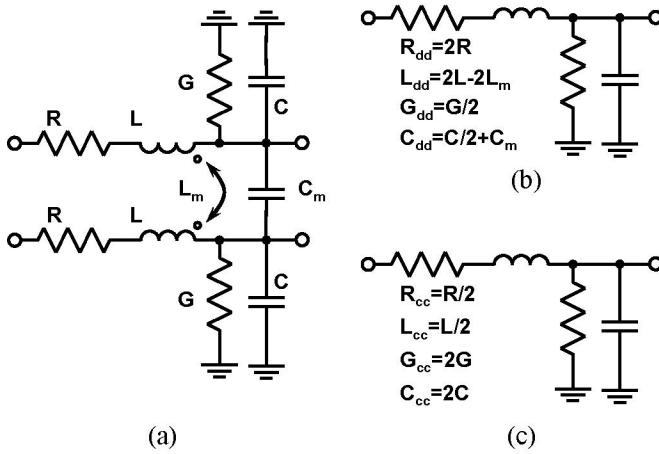

Fig. 4. Distributed $RLGC$ circuit model for a symmetric differential line: (a) four-port model, (b) differential-mode, (c) common-mode.

as shown in Fig. 4(b) and (c), respectively. The relation between the four-port and the two-port circuits are also indicated in the figure.

Fig. 5 and Fig. 6 present the extracted distributed $RLGC$ components for differential- and common-mode circuit models, respectively. As shown in Fig. 5(a) and Fig. 6(a), R_{dd} and R_{cc} increase with frequency due to skin effect and proximity effect. In addition, the observed $2R_{cc}$ is higher than $R_{dd}/2$, instead of equal in an ideal case. This can be attributed to the common-mode signal currents repel each other at the edges of the signal lines, while the differential-mode attract each other both due to proximity effect. Both effects reduce the current cross section but the repelled condition results in a relatively smaller area. The L_{dd} and L_{cc} decrease rapidly at low frequencies due to the current loop area is reduced both by skin and proximity effects. At high frequencies, the frequency
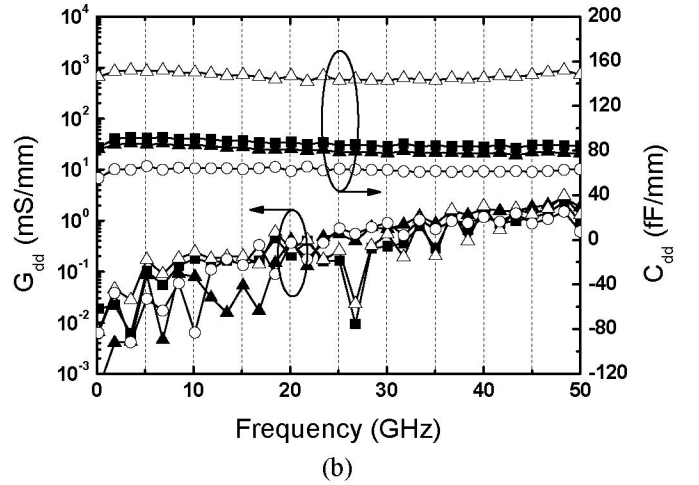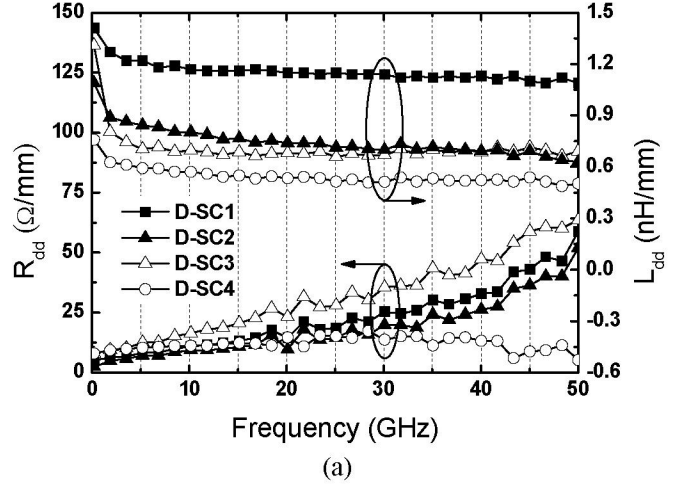

(a)

(b)

Fig. 5. Differential-mode (a) RL and (b) GC for D-SC lines.

dependence of inductance becomes smaller due to the total current loop area approaches a minimum value.

The increased G_{dd} and G_{cc} with frequency can be attributed to the dielectric conductivity, which is proportional to frequency, as shown in Fig. 5(b) and Fig. 6(b). In addition, the almost frequency-independent C_{dd} and C_{cc} suggest that the dispersion effect of the equivalent dielectric constant is very small.

IV. CONCLUSIONS

In this paper, the low-loss S-SC and D-SC lines in a standard CMOS process were investigated for the first time. The S-SC and D-SC lines present the lowest α of 0.90 dB/mm and α_{dd} of ~ 1.00 dB/mm at 50 GHz, respectively. The mixed-mode S-parameters were adopted to characterize the four-port D-SC lines. The observed trends of distributed $RLGC$ components of D-SC lines were explained in details. The results can be very useful for high-frequency interconnect
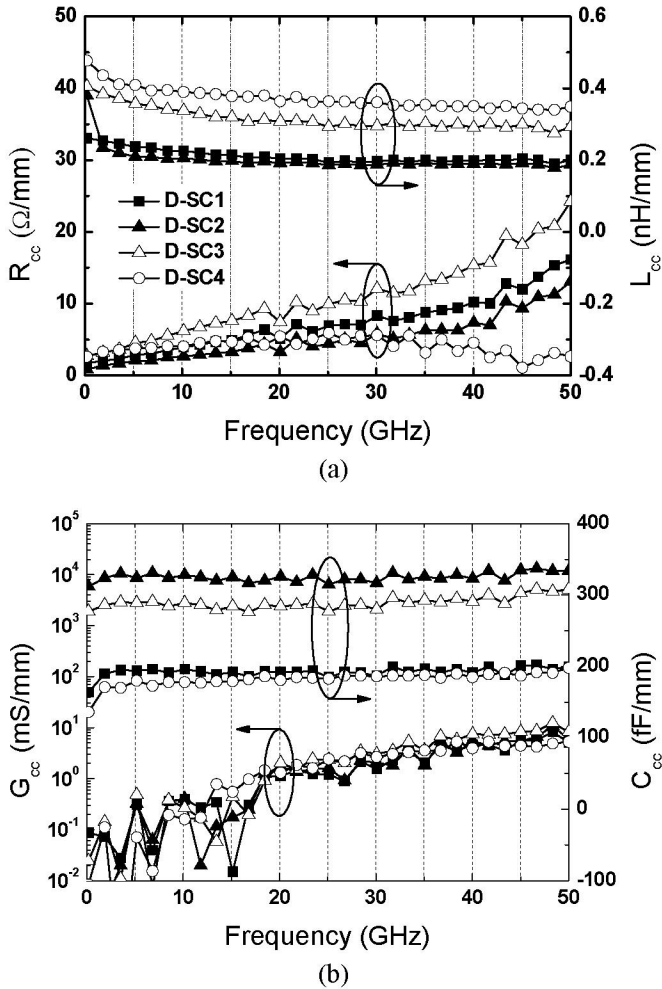
Fig. 6. Common-mode (a) *RL* and (b) *GC* for D-SC lines.

design optimization of both single-ended and differential circuits in standard CMOS processes.

REFERENCES

[1] R.-C. Liu, T.-P. Wang, L.-H. Lu, H. Wang, S.-H. Wang, and C.-P. Chao, "An 80GHz traveling-wave amplifier in a 90nm CMOS technology," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 154-155, Feb. 2005.

[2] P.-C. Huang, M.-D. Tsai, H. Wang, C.-H. Chen, and C.-S. Chang, "A 114GHz VCO in 0.13μm CMOS technology," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 404-405, Feb. 2005.

[3] B. A. Floyd, S. K. Reynolds, U. R. Pfeiffer, T. Zwick, T. Beukema, and B. Gaucher, "SiGe bipolar transceiver circuits operating at 60 GHz," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 156-167, Jan. 2005.

[4] M.T. Yang, P. P.C. Ho, T.J. Yeh, Y.J. Wang, D. C.W. Kuo, and et al., "On the millimeter-wave characteristics and model of on-chip interconnect transmission lines up to 110 GHz," in *IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 1819-1822, June 2005.

[5] C. H. Doan, S. Emami, A. M. Niknejad, and R. W. Brodersen, "Millimeter-wave CMOS design," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 144-155, Jan. 2005.

[6] B. Kleveland, T. H. Lee, and S. S. Wong, "50-GHz interconnect design in standard silicon technology," in *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 3, pp. 1913-1916, June 1998.

[7] H. Ymeri, B. Nauwelaers, K. Maex, D. D. Roest, and S. Vandenberghe, "Accurate analytic expressions for frequency-dependent inductance and resistance of single on-chip interconnects on conductive silicon substrate," *Physics Letters A*, vol. 28, pp. 195-198, Jan. 2002.

[8] J. Kim, B. Jung, P. Cheung, and R. Harjani, "Novel CMOS low-loss transmission line structure," in *IEEE Radio and Wireless Conf.*, pp. 235-238, Sept. 2004.

[9] D. E. Bockelman and W. R. Eisenstadt, "Combined differential and common-mode scattering parameters: theory and simulation," *IEEE Trans. Microw. Theory Tech.*, vol. 43, no. 7, pp. 1530-1539, July 1995.

[10] G. Ghione and C. Naldi, "Parameters of coplanar waveguides with lower ground plane," *Electronics Letters*, vol. 19, no. 18, pp. 734-735, Sept. 1983.

[11] Y. Eo and W. R. Eisenstadt, "High-speed VLSI interconnect modeling based on S-parameter measurements," *IEEE Trans. Comp., Hybrides, Manufact. Technol.*, vol. 16, no. 5, pp. 555-562, Aug. 1993.

[12] S. Baek, S. Ahn, J. Park, J. Kim, J. Kim, and J.-H. Cho, "Accurate high frequency lossy model of differential signal line including mode-conversion and common-mode propagation effect," in *Int. Symp. Electromagn. Compat.*, vol. 2, pp. 562-566, Aug. 2004.