UNIVERSITY OF FUKUI
Fukui, Japan

Mechanism and Suppression of Current Collapse in AlGaN/GaN High Electron Mobility Transistors

(AlGaN/GaN HEMT における電流コラプスの機構と抑制)

A Dissertation Submitted to the University of Fukui
for the Degree of Doctor of Engineering

in

Electrical and Electronics Engineering

by

Md. Tanvir Hasan

Committee in charge:
Professor Akihiro Hashimoto, Chair
Professor Kazutoshi Fukui
Professor Toshio Katsuyama
Professor Masaaki Kuzuhara, Advisor

September 2013

This dissertation is dedicated to my parents and supervisor, who gave me life and inspiration to keep living it.

Abstract

Mechanism and Suppression of Current Collapse in AlGaN/GaN High Electron Mobility Transistors

An AlGaN/GaN-based high-electron-mobility transistor (HEMT) is considered as an excellent candidate for future power devices due to its high breakdown voltage, high saturation drain current and low on-resistance (R_{on}). However, current collapse, i.e., dispersion of drain current or increased dynamic R_{on}, is regarded as one of the most critical issues to be solved for actual power-switching applications. Even though there have been remarkable improvements in growth and device technologies, it is still essential to understand mechanism of current collapse and ways to get rid of it. In this work, I have investigated the effect of passivation on current collapse in AlGaN/GaN HEMTs. A detailed analysis on trapping effects and localization of traps has been made. In order to suppress current collapse in AlGaN/GaN HEMTs, field plate (FP) structured devices have been studied.

Drain current dispersion measurements have been performed for AlGaN/GaN HEMTs having different passivation films such as SiN and Al_2O_3. Passivated devices exhibited dispersion between static and pulsed current-voltage characteristics. The maximum drain current for SiN passivated devices was improved by around 25% at pulsed measurements as compared to its static value, whereas Al_2O_3 passivated devices exhibited that of around 56% deterioration. The drain current was decreased with increasing on-state duration time for SiN passivated devices, while it was increased for Al_2O_3 passivated devices. The mechanism responsible for the increase of drain current with on-state duration time by AlGaN surface traps is proposed, while GaN buffer traps reasonably govern the decrease of drain current.

Effects of SiN passivation on current collapse have been studied by monitoring the dynamic change in R_{on}. The normalized dynamic R_{on} was decreased with increasing SiN-deposition temperature and became high with increasing off-state drain bias voltages. The normalized dynamic R_{on} was also decreased with increasing annealing

temperature. These results indicate that the SiN/AlGaN interface trap density is reduced with increasing both SiN-deposition and annealing temperatures.

Current collapse measurements have been performed for AlGaN/GaN HEMTs having identical breakdown voltages but with different FP lengths. The results indicated that applying more positive on-state gate biases resulted in pronounced recovery in the dynamic R_{on} for the FP device, whereas no gate-bias effects were observed for the device without FP. The mechanism responsible for the reduced current collapse by FP is proposed, in which the key role is played during on-state by the quick field-effect recovery of partial channel depletion caused by electron trapping at AlGaN surface states between gate and drain.

The above studies indicate that the current collapse is suppressed by good passivation film and longer FP with more positive on-state gate biases in AlGaN/GaN HEMTs for future high-power applications.

Contents

Chapter 1
Introduction

1.1 Background

Power electronics is a technological domain that deals with electric power conversion by switching, which plays an important role in the management and control of the electric energy network. Figure 1.1 shows application areas of power electronics, where high-efficiency switching devices are used [1]. The low power loss feature of a switching device is an essential factor in energy conversion. The power loss of a switching device is divided into conduction loss and switching loss. An ideal electrical switch is one that shows zero resistance in the on state, and a resistance of infinity in the off state. However, these two requests always have a trade-off relationship. In the electric power conversion, handling of high voltage is often required, while the power loss should be minimized as much as possible. From these requirements, switching devices are usually qualified by the indices of specific on-resistance (R_{on}) and blocking voltage.

Conventionally, power electronics has been developed on the basis of Si devices such as the metal–oxide–semiconductor field effect transistor (MOSFET), gate turn-off thyristor (GTO) and insulated gate bipolar transistor (IGBT); however, the essential limit of these Si devices has been revealed. The expectation for small and low-loss switching devices based on wideband-gap semiconductors such as SiC and GaN has recently increased, owing to their superior material properties. In fact, the innovation has come to exhibit a reality owing to the recent progress of device process and crystal growth technologies for these wide band-gap

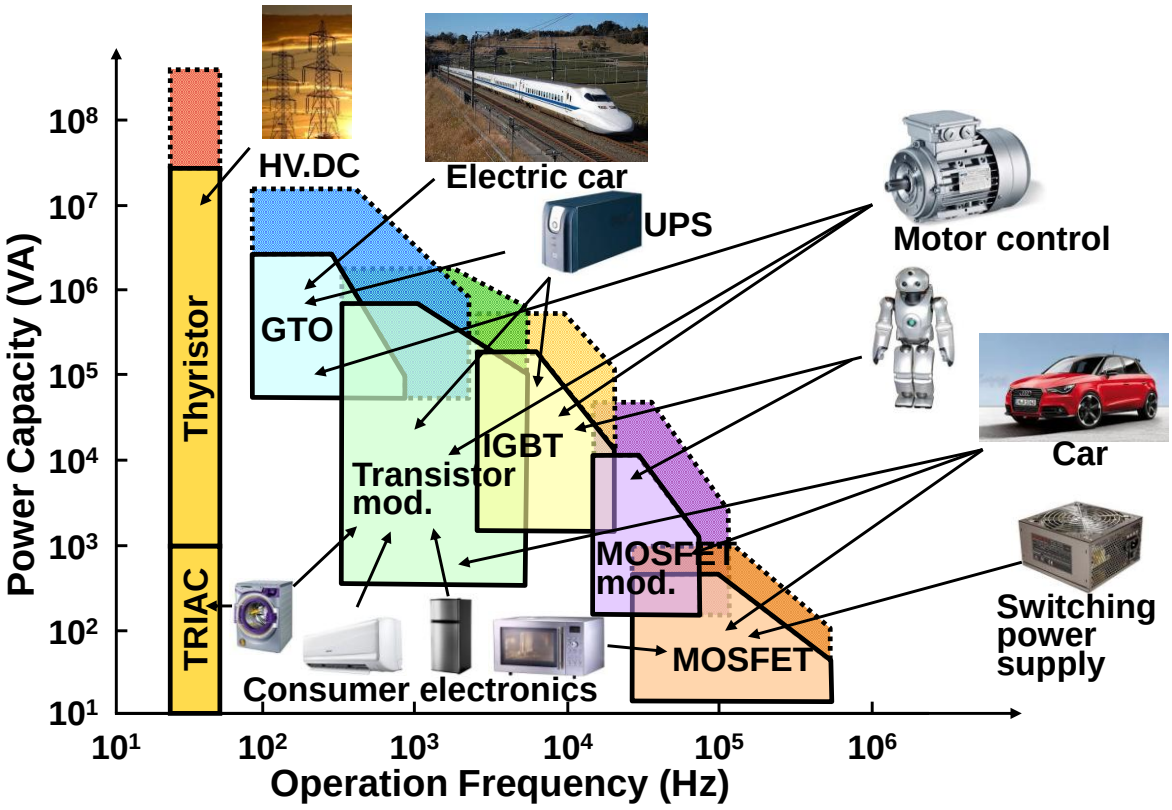


Fig.1.1. Various application areas of power electronics, where high-efficiency switching devices are used [1].

semiconductors [1-5]. Table 1.1 shows material parameters for various materials [2]. Especially, wide band-gap GaN-based materials have superior properties as follows. AlGaN/GaN heterostructures have a high density of two-dimensional electron gas (2DEG) due to strong polarization effects. The theoretical peak-electron velocity of GaN reaches 2.8×10^7cm/s at a very high field of 140 kV/cm [6]. Baliga's figure-of-merits [3] clearly show that wide band-gap GaN-based materials have superiority in high-power applications since they have high breakdown field and high mobility compared with Si. Therefore, an AlGaN/GaN-based high-electron-mobility transistor (HEMT) is considered as an excellent candidate for future power devices due to its high breakdown voltage, high saturation drain current, and low R_{on} [3]. Recently, impressive device performances in AlGaN/GaN HEMTs have been reported such as high output power of 40 W/mm at 4 GHz [7], current gain cut-off frequency of 370 GHz breakdown voltage of 10400 V [9].

Table 1.1 Material parameters related for various materials [2]. Baliga's figure of merit is an indicator for power device's performance. Note that all the symbols stand for a meaning in a general nomenclature of device physics.

Parameter	Si	GaAs	4H-SiC	GaN
Band-gap (eV)	1.12	1.43	3.26	3.4
Electron Mobility (cm^2/Vs)	600 (MOS)	6000	720 (bulk)	2000 (2DEG)
Peak Elec. Velocity (cm/s)	1×10^7	2×10^7	2×10^7	2.8×10^7
Breakdown Field (MV/cm)	0.4	0.5	2.0	3.3
Dielectric Constant	11.4	12.9	10	9.5
Baliga FOM*	1	22	132	1560

*Baliga FOM: $\varepsilon\mu E_{CR}^3$ (Limit for on-resistance power FET)

Figure 1.2 shows the power switching operation of a HEMT [2]. For ideal-switching operation of HEMT, the zero off-state current and the zero on-state voltage are required to obtain no power loss with 100% efficiency. However, there is a leakage current in the off state and the R_{on} is not zero during on state, as shown in Fig. 1.2. The R_{on} becomes a major problem for power-switching applications. In actual operation, additionally increased dynamic R_{on}, i.e., current collapse is regarded as one of the most critical issues to be solved [10-15]. One of the main reasons is trapping effect in AlGaN/GaN HEMTs. Figure 1.3 shows a sketch of an AlGaN/ GaN HEMT's current–voltage characteristics with different drain voltage [2]. The dynamic R_{on} is increased with increasing drain voltage. This effect is recoverable with time. In general, trapping effects mean electron capturing by traps somewhere in AlGaN/GaN heterostructures. The captured electrons reduce the sheet electron density in the channel to keep the overall charge neutrality, leading to increase dynamic R_{on}. These traps are mostly related to crystalline imperfection induced during material growth and device processing: (i) defects in the AlGaN/GaN heterostructures are due to lattice mismatch with foreign substrates such as SiC and sapphire, unintentional impurities, and compensation doping; (ii) device fabrication processing can impose thermal, physical, and chemical damage. In addition, the activity of traps changes under high-power operation, degrading static/RF performance of AlGaN/GaN HEMTs. Thus, to minimize

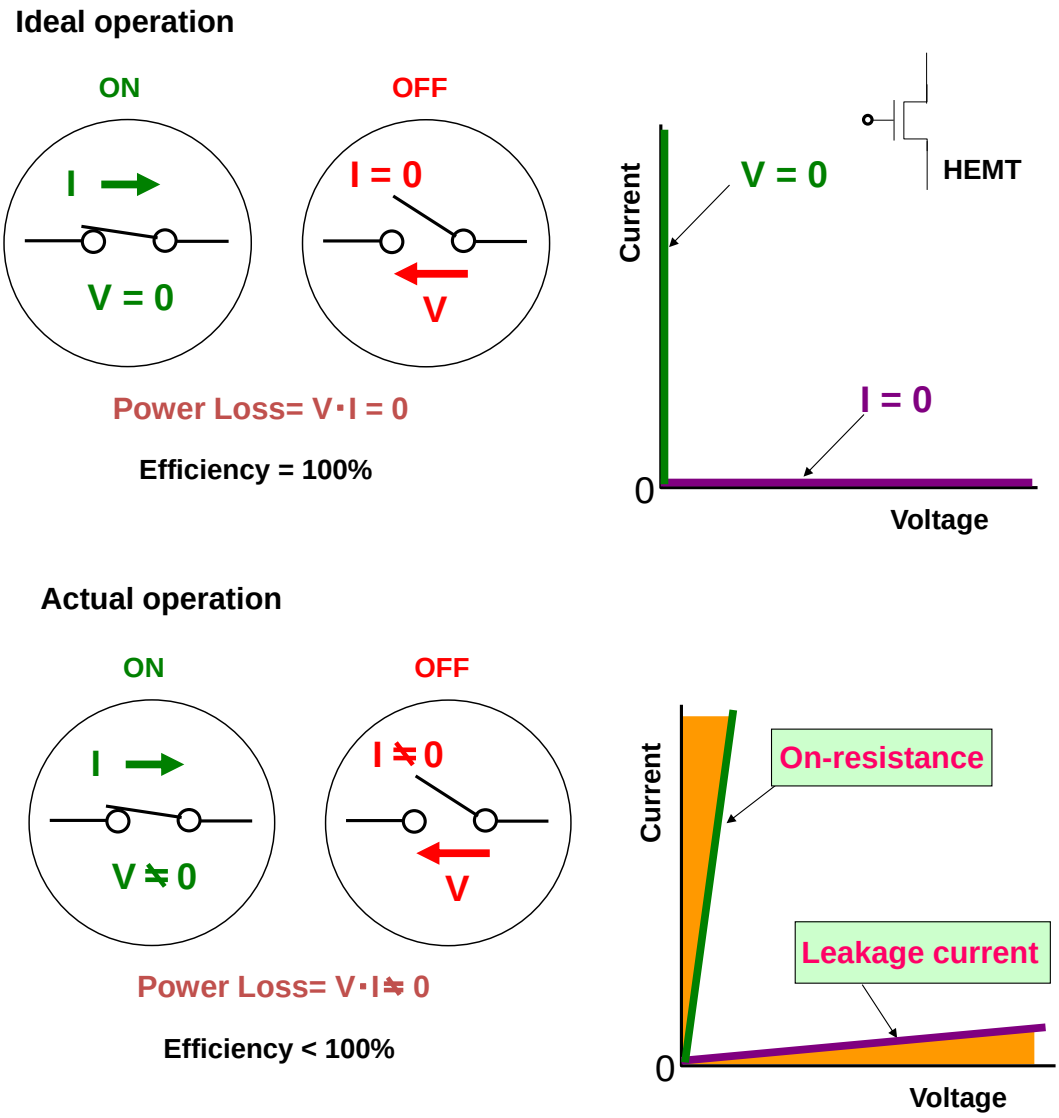


Fig. 1.2 Power-switching operation of a HEMT [2].

trapping effects through control of surface/interface states, development of advanced material growth, advanced device fabrication process techniques and novel device structures are key research themes in AlGaN/GaN HEMTs for power-switching applications.

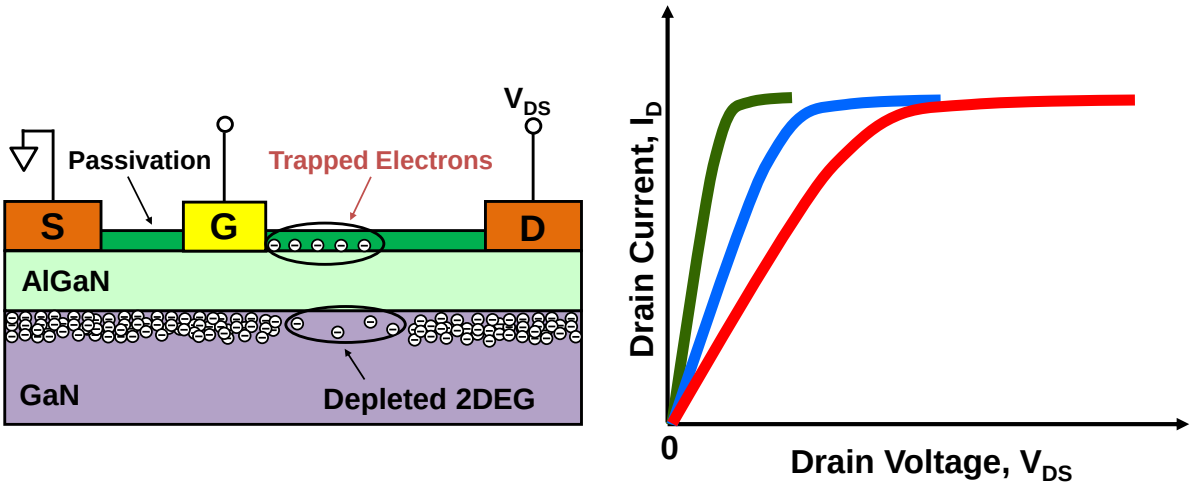


Fig. 1.3.Sketch of an AlGaN/GaN HEMT and its *I*–*V* characteristics with different V_{DS} [2].

Many efforts for high performance AlGaN/GaN HEMTs have been made to suppress current dispersion and increased dynamic on-resistance, which are directly related to modification of surface/interface states in AlGaN/GaN heterostructures. These modifications are surface passivation [16-18], a thin AlN barrier layer in AlGaN/GaN interface [19], application of a field plate [20], surface treatments with chemicals or plasma [21], and post-gate-annealing [22-23]. It has been reported that possible sources of surface states in GaN-based materials are electrically active states at threading dislocations, and nitrogen vacancies and oxygen impurities as shallow surface donors [24-27]. In addition, many researchers have investigated the origin, location, and density of traps and reported various physical models of trapping mechanisms [14, 28-32]. Among various techniques to engineer electrically active surface states on device performance mentioned above, a popular way is surface passivation with dielectrics such as Si_3N_4 and oxide [17, 18, 28, 33, 34]. Some groups have reported that surface passivation reduces electron trapping near the AlGaN surface [17, 35-36]. The passivation of surface traps has been generally meant for removal of trap states to prevent charge trapping causing current dispersion [17]. However, this explanation can be contradictory to surface donor theory by raising a question of trap sources as well as 2DEG source [31]. The drain current level increase after passivation indicates that 2DEG density increases, and net surface charge and net AlGaN/GaN interface charge become less negative and less positive, respectively. So, several groups suggested that the improved current after

passivation can be attributed to increase in positive charge at dielectric/AlGaN interface [17, 18, 33, 34, 36]. Some more explanations for passivation effects have also been proposed. First, the passivation process increases density of surface states (i.e., donor-likely states). Second, the passivation layer buries traps to become inaccessible to electrons from the gate [28]. Third, the passivation layer reduces edge electric field near the gate at drain side, leading to minimize electron injection from the gate to AlGaN surface [30]. This suppression of the (peak) electric field near the gate edge at drain side is more dominant in field-plate (FP) HEMTs, resulting in increased breakdown voltage and hence reduced electron trapping on the AlGaN surface [20, 37-42]. Evidently, no experimental evidences have been identified to date with respect to the effect of FP on the dynamic switching performance of AlGaN/GaN HEMTs. Thus, it is still very essential to understand the mechanism and suppression of current collapse in AlGaN/GaN HEMTs.

1.2 Objectives of this research

The objectives of this research are the following:

(i) Develop a pulsed *I-V* system for precise evaluation of AlGaN/GaN HEMTs performance.

(ii) Investigate the distinct electrical behavior of AlGaN/GaN HEMTs through study on passivation film effects using static and pulsed *I-V* characterization under different pulse widths and quiescent biases. Clarify the electron capture/emission phenomena, interpret effects of measurement conditions on trap activity, and qualitatively analyze trapping effects on AlGaN/GaN HEMTs performance.

(iii) Investigate the passivation film-deposition temperature effect on dynamic performance in AlGaN/GaN HEMTs. Also, study the post-annealing temperature effect on current collapse.

(iv) Introduce FP structures for suppression of current collapse in AlGaN/GaN HEMTs. Also study the mechanism of current collapse suppression.

1.3 Dissertation organization

Chapter 2 introduces basic properties of III-nitride semiconductors including polarization effects, the formation of 2DEG and velocity-field characteristics. Finally, the operation of AlGaN/GaN HEMTs, current collapse, and trade-off between on-resistance and breakdown voltage are explained.

Chapter 3 illustrates the fabrication of AlGaN/GaN HEMT including optimization of etching using ICP-RIE for mesa isolation, photolithography process, ohmic formation, gate metallization, and passivation film-deposition process. The dynamic characterization procedures are also described.

Chapter 4 shows quantitative characterization of trapping effects on AlGaN/GaN HEMTs based on very short pulsed $I-V$ measurements using different quiescent biases (QBs). Various approaches have been made to understand the mechanism of electrons trapping, such as different passivation films, SiN-deposition temperature effect, and post-annealing temperature effect.

Chapter 5 covers suppression of current collapse in AlGaN/GaN HEMTs using FP structure. The device process and characteristics are described. Effects of FP on current collapse in AlGaN/GaN HEMTs are also discussed. A model is proposed to explain the suppression mechanism of current collapse in AlGaN/GaN HEMTs.

Chapter 6 provides the conclusions that can be drawn from the work described in this thesis and provides recommendations for future research.

References

[1] H. Okumura, “Present status and future prospect of wide gap semiconductor high-power devices”, Jpn. J. Appl. Phys., vol. 45, pp.9001-9010, 2006.

[2] M. Kuzuhara, “Nitride power devices: Future perspectives”, Int. RCIQE/CREST joint workshop, Hokkaido University, March 1-2, 2010.

[3] E. Johnson, "Physical limitations on frequency and power parameters of transistors," in IRE International Convention Record, 1965, pp. 27-34.

[4] I. Akasaki and H. Amano, “Crystal growth and conductivity control of group III nitride semiconductors and their application to short wavelength light emitters”, Jpn. J. Appl. Phys., vol. 36, pp.5393-5408, 1997.

[5] H. Matsunami, “Technological Breakthroughs in Growth Control of Silicon Carbide for High Power Electronic Devices”, Jpn. J. Appl. Phys., vol. 43, pp.6835-6847, 2004.

[6] S. O'Leary, B. Foutz, M. Shur, and L. Eastman, "Steady-state and transient electron transport within the III–V nitride semiconductors, GaN, AlN, and InN: Areview," Journal of Materials Science: Materials in Electronics, vol. 17, pp. 87-126, 2006.

[7] Y-F Wu, M. Moore, A. Saxler, T. Wisleder, and P. Parikh, “40-W/mm double field-plated GaN HEMTs”, IEEE 64th Device Research Conference proc., 2006, pp.151-2.

[8] Y.Yue, Z. Hu, J.Guo, B. S.-Rodriguez, G. Li, R. Wang, F.Faria, T. Fang, B. Song, X.Gao, S.Guo, T.Kosel, G. Snider, P. Fay, D. Jena, and H. Xing, “InAlN/AlN/GaN HEMTs with regrown ohmic contacts and $f_T$of 370 GHz”, lEEE Electron Device Lett., vol. 33, no. 7, pp. 988–990, July 2012.

[9] M. Yanagihara, Y. Uemoto, T. Ueda, T. Tanaka, and D. Ueda, “Recent advances in GaN transistors for future emerging applications”, Phys. Status Solidi A,vol. 206, no. 6, pp. 1221– 1227, 2009.

[10] U. K. Mishra, L. Shen, T. E. Kazior, and W. Yi-Feng, "GaN-Based RF Power Devices and Amplifiers," Proceedings of the IEEE, vol. 96, pp. 287-305, 2008.

[11] M. A. Khan, Q. Chen, C. J. Sun, J. W. Yang, M. Blasingame, M. S. Shur, and H. Park, “Enhancement and depletion mode GaN/AlGaN heterostructure field effect transistors”, Appl. Phys. Lett., vol. 68, p. 514, 1996.

[12] X. Hu, G. Simin, J. Yang, M. A. Khan, R. Gaska, and M. S. Shur, “Enhancement mode

AlGaN/GaN HFET with selectively grown pn junction gate", Electron. Lett., vol. 36, no. 8, pp. 753-754, 2000.

[13] M. A. Khan, M. S. Shur, Q. C. Chen, and J. N. Kuznia, "Current/voltage characteristic collapse in AlGaN/GaN heterostructure insulated gate field effect transistors at high drain bias," Electronics Letters, vol. 30, pp. 2175-2176, 1994.

[14] P. B. Klein and S. C. Binari, "Photoionization spectroscopy of deep defects responsible for current collapse in nitride-based field effect transistors," J. Phys.: Cond. Matt., p. R1641, 2003.

[15] N. Q. Zhang, B. Moran, S. P. DenBaars, U. K. Mishra, X. W. Wang, and T. P. Ma, "Effects of surface traps on breakdown voltage and switching speed of GaN power switching HEMTs," in IEDM Technical Digest. International, 2001, pp. 25.5.1-25.5.4.

[16] Y. Ohno, T. Nakao, S. Kishimoto, K. Maezawa, and T. Mizutani, "Effects of surface passivation on breakdown ofAlGaN/GaN high-electron-mobility transistors," Appl. Phys.Lett., vol. 84, pp. 2184-2186, 2004.

[17] B. Luo, J. W. Johnson, J.Kim, R. M. Mehandru, F. Ren,B. P. Gila, A. H. Onstine, C. R. Abernathy, S. J. Pearton, A. G. Baca, R. D. Briggs, R. J. Shul, C. Monier, and J. Han, "Influence of MgO and Sc_2O_3passivation on AlGaN/GaN high-electron mobility transistors," Appl. Phys.Lett., vol. 80, pp. 1661-1663, 2002.

[18] S.Arulkumaran, T. Egawa, H. Ishikawa, T. Jimbo, and Y. Sano, "Surface passivation effects on AlGaN/GaN high-electron-mobility transistors with SiO_2, Si_3N_4, and silicon oxynitride," Appl. Phys.Lett.,vol. 84, pp. 613-615, 2004.

[19] J. S. Lee, J. W. Kim, J. H. Lee, C. S. Kim, J. E. Oh, and M. W. Shin, "Reduction of current collapse in AlGaN/GaN HFETs using AlN interfacial layer," Electronics Lett., vol. 39, pp. 750-752, 2003.

[20] Y. F. Wu, A. Saxler, M. Moore, R. P. Smith, S. Sheppard, P. M. Chavarkar, T. Wisleder, U. K. Mishra, and P. Parikh, "30-W/mm GaNHEMTs by field plate optimization," IEEE Electron Device Lett,, vol. 25, pp. 117-119, Mar 2004.

[21] A. P. Edwards, J. A. Mittereder, S. C. Binari, D. S. Katzer, D. F. Storm, and J. A. Roussos, "Improved reliability of AlGaN-GaN HEMTs using an NH_3/plasma treatment prior to SiN passivation," IEEE Electron DeviceLett., vol. 26, pp. 225-227, 2005.

[22] N. Miura, T. Nanjo, M. Suita, T. Oishi,Y. Abe, T. Ozeki, H.Ishikawa, T. Egawa,and T.

Jimbo, "Thermal annealing effects on Ni/Au based Schottky contacts on n-GaN and AlGaN/GaN with insertion of high work function metal," Solid-State Electronics, vol. 48, pp. 689-695, May 2004.

[23] H. Kim, J. Lee, D. Liu, and W.Lu, "Gate current leakage and breakdown mechanism in unpassivated AlGaN/GaN high electron mobility transistors by post-gate annealing," Appl. Phys. Lett., vol. 86, pp. 143505-3, 2005.

[24] P. J. Hansen, Y. E. Strausser, A. N. Erickson, E. J. Tarsa, P. Kozodoy, E. G.Brazel, J. P. Ibbetson, U. Mishra, V. Narayanamurti, S. P. DenBaars, and J. S. Speck, "Scanning capacitance microscopy imaging of threading dislocations in GaN films grown on (0001) sapphire by metal organic chemical vapor deposition," Appl. Phys. Lett., vol. 72, pp. 2247-2249, 1998.

[25] H. J. Im, Y. Ding, J. P. Pelz, B. Heying, and J. S. Speck, "Characterization of individual threading dislocations in GaN using ballistic electron emission microscopy," Phys. Rev. Lett., vol. 87, p. 106802, Sep 2001.

[26] J. W. P. Hsu, M. J. Manfra, D. V. Lang, S. Richter, S. N. G. Chu, A. M. Sergent, R. N. Kleiman, L. N. Pfeiffer, and R. J. Molnar, "Inhomogeneous spatial distribution of reverse bias leakage in GaN Schottky diodes," Appl. Phys. Lett., vol. 78, pp. 1685-1687, 2001.

[27] D. M. Schaadt, E. J. Miller, E. T. Yu, and J. M. Redwing, "Lateral variations in threshold voltage of an $Al_xGa_{1-x}N$/GaN heterostructure field-effect transistor measured by scanning capacitance spectroscopy," Appl. Phys. Lett., vol. 78, pp. 88-90, 2001.

[28] R. Vetury, N. Q. Zhang, S. Keller, and U. K. Mishra, "The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs," IEEE Trans. Electron Devices, vol. 48, pp. 560-566, 2001.

[29] O. Mitrofanov and M. Manfra, "Mechanisms of gate lag in GaN/AlGaN/GaN high electron mobility transistors," Superlattices and Microstructures, vol. 34, pp. 33-53, 2003.

[30] M. Faqir, G. Verzellesi, A. Chini, F. Fantini, F. Danesin, G. Meneghesso, E.Zanoni, and C. Dua, "Mechanismsof RF current collapse inAlGaN/GaN High Electron Mobility Transistors," IEEE Trans. Device and Materials Reliability, vol. 8, pp. 240-247, 2008.

[31] J. P. Ibbetson, P. T. Fini, K. D. Ness, S. P. DenBaars, J. S. Speck, and U. K. Mishra, "Polarization effects, surface states, and the source of electrons in AlGaN/GaN

heterostructure field effect transistors," Appl. Phys.Lett., vol. 77, pp. 250-252, 2000.

[32] G. Koley, V. Tilak, L. F. Eastman, and M. G. Spencer, "Slow transients observed in AlGaN/GaN HFETs: effects of SiN_x passivation and UV illumination," IEEE Trans. Electron Devices, vol. 50, pp. 886-893, 2003.

[33] G. Koley and M. G. Spencer, "On the origin of the two-dimensional electron gas at the AlGaN/GaN heterostructure interface," Appl. Phys.Lett., vol. 86, p. 3, Jan 2005.

[34] T. R. Prunty, J. A. Smart, E. N. Chumbes, B. K. Ridley, L. F. Eastman, and J. R. Shealy, "Passivation of AlGaN/GaN heterostructures with silicon nitride for insulated gate transistors," in Proc. High Performance Devices, 2000 (IEEE/Cornell Conference) 2000, pp. 208-214.

[35] Y. Ando, Y. Okamoto, H. Miyamoto, N. Hayama, T. Nakayama, K. Kasahara, and M. Kuzuhara, "A 110-W AlGaN/GaN heterojunction FET on thinned sapphire substrate," in IEDM Technical Digest. 2001, pp. 17.3.1-17.3.4.

[36] B. M. Green, K. K. Chu, E. M. Chumbes, J. A. Smart, J. R. Shealy, and L. F. Eastman, "The effect of surface passivation on the microwave characteristics of undoped AlGaN/GaN HEMTs," IEEE Electron Device Lett., , vol. 21, pp. 268-270, 2000.

[37] Y. Ando, Y. Okamoto, H. Miyamoto, T. Nakayama, T. Inoue, and M. Kuzuhara,"10-W/mm AlGaN-GaN HFET with a field modulating plate," IEEE Electron Device Lett., vol. 24, pp. 289-291, 2003.

[38] W. Saito, Y. Kakiuchi, T. Nitta, Y. Saito, T. Noda, H. Fujimoto, A. Yoshioka, T. Ohno, and M. Yamaguchi, "Field-plate structure dependence of current collapse phenomena in high-voltage GaN-HEMTs," IEEE Electron Device Lett., vol. 31, no. 7, pp. 659–661, Jul. 2010.

[39] A. Brannick, N. A. Zakhleniuk, B. K. Ridley, J. R. Shealy, W. J. Schaff, and L. F. Eastman, "Influence of field plate on the transient operation of the AlGaN/GaN HEMT," IEEE Electron Device Lett., vol. 30, no. 5, pp. 436–438, May 2009.

[40] W. Saito, T. Nitta, Y. Kakiuchi, Y. Saito, K. Tsuda, I. Omura, and M. Yamaguchi, "Suppression of dynamic On-resistance increase and gate charge measurements in high-voltage GaN-HEMTs with optimized field-plate structure," IEEE Trans. Electron Devices, vol. 54, no. 8, pp. 1825–1830, Aug. 2007.

[41] H. Ishida, D. Shibata, M. Yanagihara, Y. Uemoto, H. Matsuo, T. Ueda, T. Tanaka, and D. Ueda, "Unlimited high breakdown voltage by natural super junction of polarized semiconductor," IEEE Electron Device Lett., vol. 29, no. 10, pp. 1087–1089, Oct. 2008.

[42] Z. Tang, S. Huang, Q. Jiang, S. Liu, C. Liu, and K.J. Chen, "High-voltage (600-V) low-leakage low-current-collapse AlGaN/GaN HEMTs with AlN/SiN_x passivation," IEEE Electron Device Lett., vol. 34, no. 3, pp. 366–368, Mar. 2013.

Chapter 2
Fundamentals of AlGaN/GaN HEMTs

2.1 Introduction

In recent years AlGaN/GaN high-electron-mobility transistor (HEMT) has attracted much interest for high-power devices. Many active research groups are intensively working and reporting worldwide on AlGaN/GaN HEMTs. Although the performance achieved in AlGaN/GaN HEMTs is remarkable, fundamentals of material and device properties of AlGaN/GaN HEMTs is still a pending issue The value of some of basic material parameters is unknown. Important device properties, such as polarization, gate leakage, electron velocity, are still highly controversial issues. In this chapter, fundamentals of AlGaN/GaN material and its application in HEMTs will be discussed.

2.2 High-electron-mobility transistor

The development of heterostructures in the 1980s offered the opportunity of tremendous progress in the performance of microwave transistors. HEMT is a field effect device based on a heterostructure with different band-gap materials. To describe the structure and operation of a HEMT device, a GaAs-based HEMT is considered. A conventional AlGaAs/ GaAs HEMT and its band diagram are illustrated in Fig. 2.1. The wide band-gap AlGaAs material is n-type, but it is depleted of free carriers by the reverse or zero-biased Schottky contact, while the narrow band-gap GaAs material is undoped. At the boundary between two

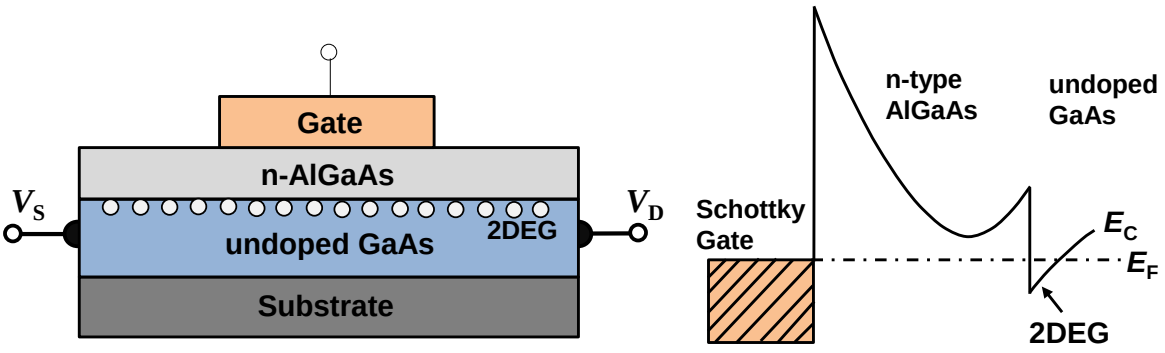


Fig. 2.1. Conventional AlGaAs/GaAs HEMT structure and its band diagram under zero gate bias.

materials, the band-gap discontinuities cause the conduction band of GaAs to dip below the Fermi level, creating a potential well with a high carrier concentration. This region of high carrier density is very thin, so that it is named two-dimensional electron gas (2DEG). The electrons of 2DEG travel along the GaAs channel without encountering ionized donor atoms. This makes them to have high mobility, favoring fast response times and high-frequency operation.

2.3 Properties of III-nitride semiconductors

The III-nitrides AlN, GaN, and InN can crystallize in the following three crystal structures: wurtzite, zinc-blende, and rock-salt. The chemical bonds of III-nitride compounds such as GaN are predominantly covalent, which means that each atom is tetrahedrally bonded to four atoms of the other type. Because of the large difference in electronegativity of Ga and N atoms, there is a significant ionic contribution to the bond which determines the stability of respective structural phase. Atomic arrangement in both Ga-face and N-face wurtzite GaN crystal is shown in Fig. 2.2 [1]. There is no inversion symmetry in this lattice along the direction from a Ga atom to the nearest neighbor N atom. Wurtzite GaN crystals have two distinct faces, commonly known as Ga-face and N-face, which correspond to (0001) and $(000\bar{1})$ crystalline faces. For N-face material this can be obtained by flipping the Ga-face material upside-down. It has to be noted that for Ga-face material the N atom is stacked

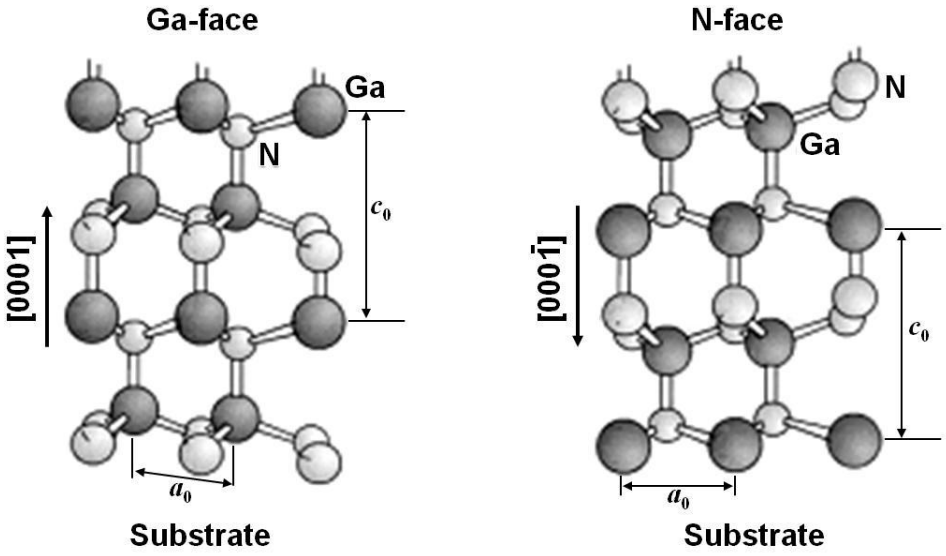


Fig. 2.2. Atomic arrangement in both Ga-face and N-face wurtzite GaN crystal [1].

directly over the Ga atom and vice versa for N-face. The two parameters define the wurtzite lattice. These are the edge length of the basal hexagon (a_o) and the height of the hexagonal lattice cell (c_o) along the [0001] direction. The subscript "0" indicates that these values are those of the equilibrium lattice. The lattice constants $a(x)$ and $c(x)$ of $Al_xGa_{1-x}N$ are predicted to follow the composition-weighted average between the binary compounds AlN and GaN (Vegard's law) [2]:

$$\begin{aligned} a_{\mathrm{AlGaN}}(x) &= (3.1986 - 0.0891x)\,\mathring{\mathrm{A}} \\ c_{\mathrm{AlGaN}}(x) &= (5.2262 - 0.2323x)\,\mathring{\mathrm{A}} \end{aligned} \qquad (2.1)$$

The graphical representation of the lattice constants $a(x)$ and $c(x)$ of wurtzite III nitride alloys are shown in Fig. 2.3. The calculated values are in good agreement with the reported experimental values [3-6] for wurtzite AlGaN.

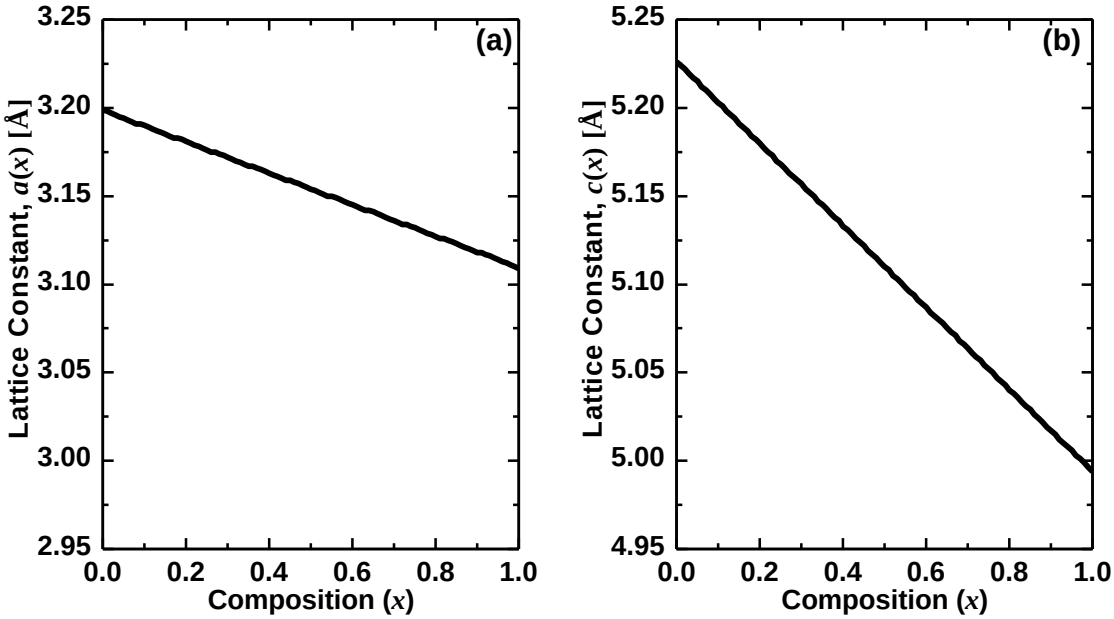


Fig. 2.3. (a) The edge length of the basal hexagon, lattice constant $a(x)$ and (b) the height of the hexagonal lattice cell, lattice constant $c(x)$ for wurtzite $Al_xGa_{1-x}N$ are calculated using the Vegard's law.

Usually, GaN materials are typically grown on a different substrate material using a heteroepitaxial growth technique, since bulk crystal growth of GaN is presently very difficult. Sapphire is a common substrate material for the epitaxial growth of GaN. However, there is a 14% lattice mismatch between hexagonal GaN and sapphire. Careful control of the initial growth conditions is important and low-temperature-grown GaN and AlN are typically used as a buffer layer [3]. SiC is also a widely employed substrate for epitaxial growth of GaN. SiC has a rather small lattice mismatch of 3% with GaN and exhibits a large thermal conductivity of 4.5 W/cm-K, which is very beneficial for high-power device applications. Since GaN is composed of Ga with a large ionic radius and N with a small ionic radius and thus forms a slightly distorted tetrahedral arrangement, it exhibits spontaneous polarization. When AlGaN is grown on GaN, piezoelectric polarization is further added due to the tensile stress generated in the AlGaN layer. With these two polarization effects, a fixed positive charge is generated near the AlGaN/GaN heterointerface in the AlGaN layer and correspondingly two-dimensional electron gas is induced in the GaN layer. The density of free electrons in GaN increases with increasing Al content of AlGaN and reaches about 1.7×10^{13} cm^{-2} when the Al content is increased to 25 to 30%. It is a unique characteristic of the

AlGaN/GaN heterostructure that a high density of two-dimensional electrons is achieved without the addition of any donor impurities to the AlGaN layer.

2.4 Polarization effects

Polarization in III-nitride materials is a crucial material property that enables and determines the actual operation of nitride based devices. The basis for macroscopic polarization in materials with bound charges is a microscopic polarization of atoms due to bonds between atoms, when the center of negative charge (electrons) shifts away from the center of the positive charge (nuclei) [7]. Such a polarized atom constitutes a dipole with a dipole moment ***p***. Polarization state of a material can be then described by the vector of electric polarization *P*, which is defined as a total dipole moment of a unit volume. If the dipoles are identical and their concentration is n, the formula can be expressed as

$$\vec{P} = n\,\vec{p} = \frac{\vec{p}}{\Omega_0}. \qquad (2.2)$$

Where, Ω_0 is a volume that is occupied by a single dipole. If there is no electric field present, most materials have no dipoles or the orientation of the dipoles is random and hence the total polarization is zero. However, in low symmetry compound crystals, this may not be true and the asymmetry of the bonding may form dipoles, which are consequently a source of polarization. A condition for a structure to exhibit piezoelectric polarization P_{PE}, which is a polarization originating in a mechanical deformation, is to lack a center of symmetry. Moreover, if the crystal class has either no rotation axis or a single rotation axis, which is not an inversion axis, the bonding in this crystal will be intrinsically asymmetric. Under this condition, the material acts as a pyroelectric and shows a built-in spontaneous polarization P_{SP}, even without any mechanical or electrical perturbation. This low symmetry axis in the crystal, parallel with the built-in polarization, is called the pyroelectric axis. Another class of materials that show polarization in absence of the electric field are ferroelectrics. In these materials, P_{SP} can be inverted by applying a strong electrostatic field. This effect allows an accurate measurement of the spontaneous polarization, P_{SP}, which is not possible in pyroelectrics. Figure 2.4 shows the P_{SP} of III-nitride materials.

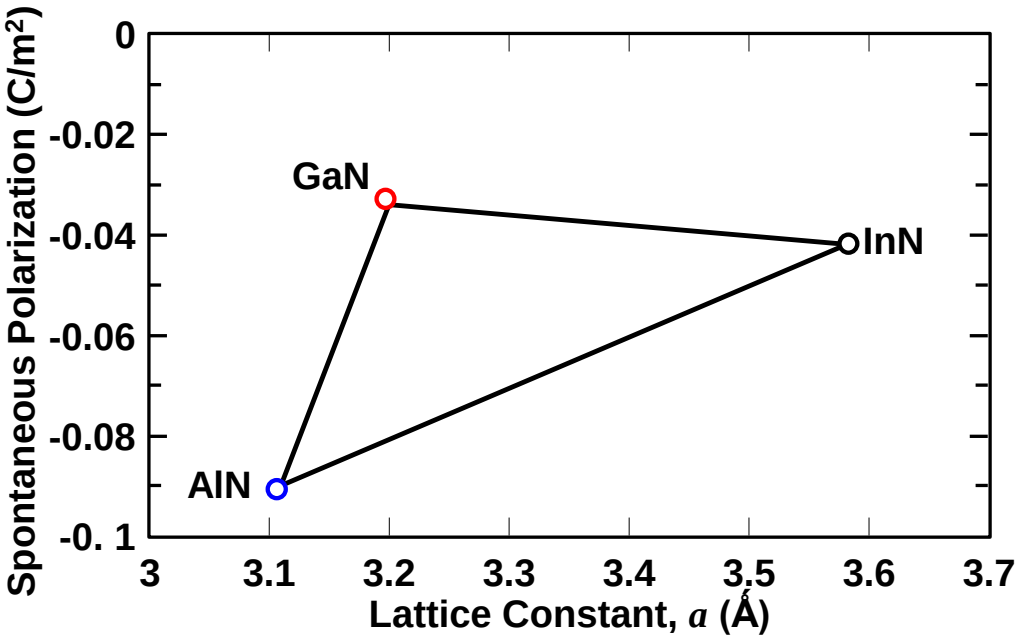


Fig. 2.4. Spontaneous polarization of III-nitride materials.

In wurtzite crystals, the sp^3 hybridization is not perfect and the bond along the [0001] direction has a different ionicity than the other bonds and hence the wurtzites show the spontaneous polarization. The macroscopic polarization arises in low symmetry crystals due to a perturbation (built-in, mechanical, electrical, etc.) in the crystal symmetry or more accurately, in the bond symmetry. For small strains, the polarization depends on strain linearly. If there is a non-zero polarization at zero strain, we call this polarization spontaneous. There is no other difference between piezoelectric and spontaneous polarization. The total polarization is a sum of both types of polarization, $P = P_{SP} + P_{PE}$. The piezoelectric polarization can be expressed, in various ways, e.g., as [8]

$$P_i^{PE} = \sum_{jk} d_{ijk} t_{jk} = \sum_{jk} d_{ijk} \left(\sum_{lm} C_{jklm} \varepsilon_{lm} \right) = \sum_{lm} e_{ilm} \varepsilon_{lm} = \sum_{lm} e_{ilm} \left(\sum_{lm} S_{lmjk} t_{jk} \right). \quad (2.3)$$

Here, piezoelectric constants are denoted as e (= dC), piezoelectric moduli are d (= eS), elastic constants (stiffness) are C and elastic compliances are S (= C^{-1}). The variables depend on external conditions (electric field E, stress t, and the resulting strain ε) and therefore

can take different forms.

In GaN based HEMT devices, the GaN layer is usually several orders of magnitude thicker than the AlGaN layer, which is only several nanometers thick. Therefore, it is a possible assumption that the GaN layer will be fully relaxed, and hence show no piezoelectric polarization, while the AlGaN layer will be strained. Therefore, strain can be expressed as

$$\varepsilon = \frac{a(0) - a(x)}{a(x)} \qquad (2.4)$$

where, x is the Al fraction of AlGaN layer. The $a(0)$ and $a(x)$ are lattice constants of an unstrained GaN and strained $Al_xGa_{1-x}N$ layer, respectively. Figure 2.5 shows the lattice constants (in this simplified drawing, the atoms that have to form bonds are represented by red dots) of an unstrained AlGaN are different from that of an unstrained GaN (left). When AlGaN grows on the top of GaN, the constant of AlGaN has to match the lattice constant of GaN. This exerts a strong stress on the grown AlGaN layer. This stress causes strain (right) in both of the basal plane (ε_1) and the growth (ε_3) directions, respectively. The dashed line represents an unstrained piece of AlGaN. In piezoelectric materials, the strain results in polarization field P_{PE}. The Ga-face growth is assumed here. The structure in the middle represents the orientation of the wurtzite structure in the heterostructure. In equation 2.3, the relation

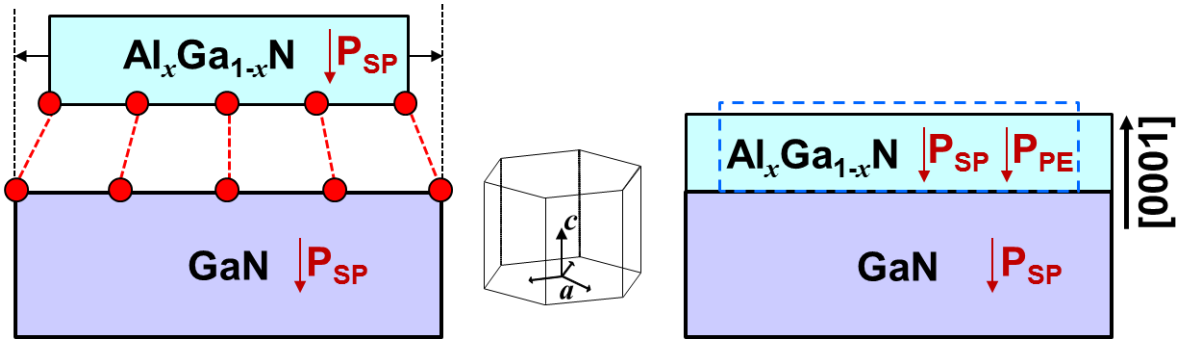


Fig. 2.5. Stain effect of an AlGaN/GaN heterostructure.

between piezoelectric polarization, P_{PE} and strain, ε depends on the form of piezoelectric constant matrix [9] and the equality of strain in basal and growth direction ($\varepsilon_1 = \varepsilon_3$). It means that shear strains are absent in the polarization vector. Therefore, P_{PE} can be expressed as

$$P_3^{PE} = 2e_{31}\varepsilon_1 + e_{33}\varepsilon_3 \tag{2.5}$$

and the relation between the strain along the polar axis (in the growth direction) ε_3 and in the basal plane ε_1 as

$$\varepsilon_3 = -2\frac{C_{13}}{C_{33}}\varepsilon_1. \tag{2.6}$$

Combining the previous formulas give the expression of piezoelectric polarization as

$$P_3^{PE} = 2\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right)\varepsilon_1 = 2d_{31}\left(C_{11} + C_{12} - 2\frac{C_{13}^2}{C_{33}}\right)\varepsilon_1. \tag{2.7}$$

In the case of $Al_{0.25}Ga_{0.75}N$/GaN heterostructure, the barrier layer grows with a lateral strain $\varepsilon_1 \approx 8\times10^{-3}$ and stress ≈ 3.6 GPa.

2.5 Polarization induced charge

A polarization induced charge density given by $\sigma = \nabla P$ is associated with a gradient of polarization in space is [10]. In analogy, at an abrupt interface of a top/bottom layer (AlGaN/GaN heterostructures) the polarization can decrease or increase within a bilayer, causing a polarization sheet charge density defined by [10]

$$\begin{aligned}\sigma &= P_{GaN} - P_{AlGaN} = P_{GaN}^{SP} + P_{GaN}^{PE} - P_{AlGaN}^{SP} - P_{AlGaN}^{PE} \\ &= P^{SP}(0) + P^{PE}(0) - P^{SP}(x) - P^{PE}(x)\end{aligned} \tag{2.8}$$

where, the argument x is the Al fraction of $Al_xGa_{1-x}N$. Since the GaN layer is usually several

orders of magnitude thicker than AlGaN, it is considered to be relaxed and hence without piezoelectric polarization, $P_{PE}(0) = 0$. Since, according to Fig. 2.4, the magnitude of the spontaneous polarization is higher in AlGaN than in GaN, there will be a positive charge at the AlGaN/GaN interface. However, there is usually a material that lacks any polarization (either air or a passivation layer) at the AlGaN surface of the device. Figure 2.6 shows calculated polarization charge (i.e., sheet charge, σ/e) at the AlGaN/GaN interface caused by the spontaneous and piezoelectric polarization versus alloy composition, proving that the contribution of both kinds of polarization to the sheet charge is nearly the same [1]. For x = 0.25, a remarkably high sheet charge σ/e of 1.4×10^{13} cm^{-2}. These calculated sheet charges located at the AlGaN/GaN interface are about ten times higher than in comparable heterostructures of other III–V heterostructures [11] thus high polarization induced sheet carrier concentrations may be expected.

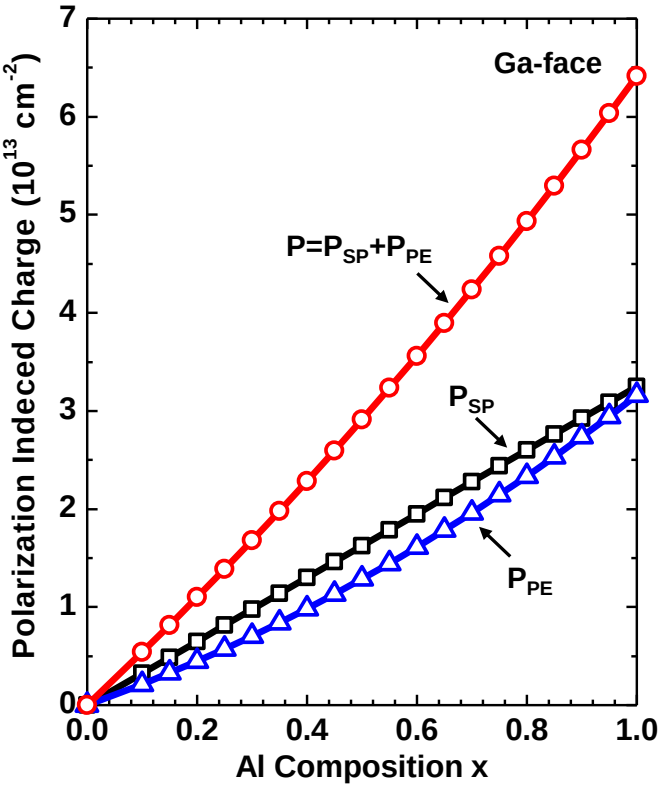


Fig. 2.6. Calculated polarization charge density caused by spontaneous and piezoelectric polarization at the lower interface of a Ga-face GaN/AlGaN/GaN heterostructure vs alloy composition of the barrier.

2.6 Formation of 2DEG

In order to calculate the electronic states and charge density at the interface, the 1D Schrödinger equation coupled with the Poisson's equation needs to be solved self consistently [12-17]. As a result, two major features are observed: there is a charge setback from the interface, and there is an upward shift of the conduction band edge corresponding to formation of a bound state in the presence of the approximately triangular potential well at the interface. Within single band effective mass theory, the 1D Schrödinger wave equation can be written as [18,19]

$$-\frac{\hbar^2}{2}\frac{d^2}{dz^2}\frac{1}{m^*(z)}\phi_i(z)+V(z)\phi_i(z)=E_i\phi_i(z) \qquad (2.9)$$

where, m^* is the electron effective mass, ϕ_i is the wave function of ith subband, E_i is the energy of ith subband, V is the potential energy. The $V(z)$ can be expressed as

$$V(z)=-q\psi(z)+\Delta E_C+V_{xc} \qquad (2.10)$$

where, ψ is the electrostatic potential, ΔE_C is the conduction band discontinuity, and V_{xc} is the energy of the local exchange-correlation potential. Once the Schrödinger equation is solved for the envelope functions and the subband energy levels, the electron sheet charge density for each subband can be calculated by applying Fermi statistics

$$n_i=\frac{m^*k_BT}{\pi\hbar^2}\ln\left[1+\exp\left(\frac{E_f-E_i}{k_BT}\right)\right], \qquad (2.11)$$

where, E_f is the Fermi energy. The electron density at position z is then easily calculated by

$$n_{2D}(z)=\sum_i n_i|\psi_i(z)|^2. \qquad (2.12)$$

The Poisson equation needs to be solved in terms of the displacement field, $D(z)$[18]

$$\nabla \cdot D(z) = \rho(z), \qquad (2.13)$$

where, total charge density, $\rho(z) = -[n(z) - p(z) - N_D^+(z) + N_A^-(z)]$. Here, N^+_D and N^-_A are ionized donor and acceptor densities, respectively. $n(z)$ and $p(z)$ are free electron and hole carrier concentrations, respectively. However, a hole, the donor, acceptor is assumed to be not present in the analysis of AlGaN/GaN. Therefore, the presence of polarization charge density, $\sigma(z)$, it can be represented as

$$\rho(z) = -[n(z) - \sigma(z)] \qquad (2.14)$$

In order to distinguish the two-dimensional electrons in the quantum well region, a cut-off value is used, which is set to the highest subband level used in the Schrödinger equation. The free electron density below this threshold value is set to 0. Equations (2.9) and (2.12) are solved self-consistently until the potential converges. The simulated heterostructure consists of a 25-nm AlGaN and a 1-μm GaN layer from the gate to the substrate, as shown in Fig. 2.7. Both GaN and AlGaN layers are assumed undope. A Schottky barrier height, Φ_B, of 0.8 eV for the metal-AlGaN interface is considered. Figure 2.8 shows results of the Schrödinger-Poisson self-consistent calculation for Al content of 0.25 in the heterostructure, with gate bias V_{GS}=0 V. The conduction band, the subband energy and the 2D electron density are shown in the figure. Two subbands are taken into account for both cases.

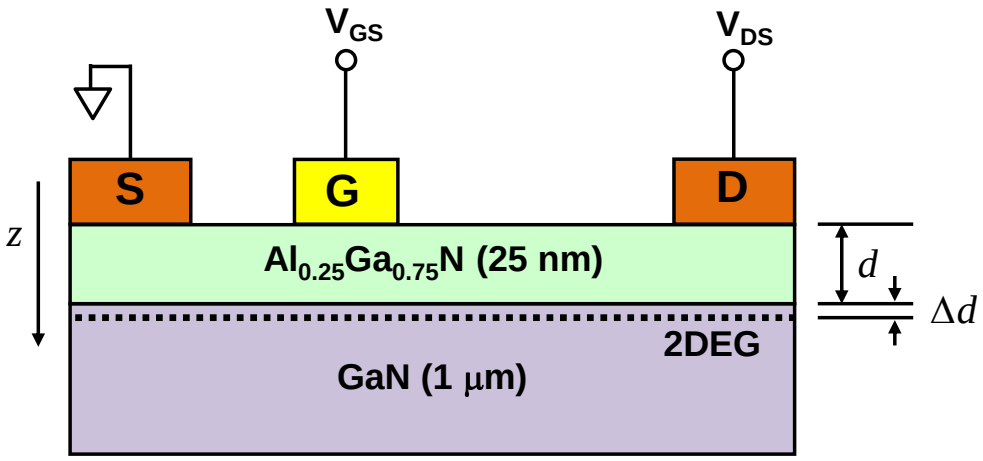


Fig. 2.7 An AlGaN/GaN HEMT.

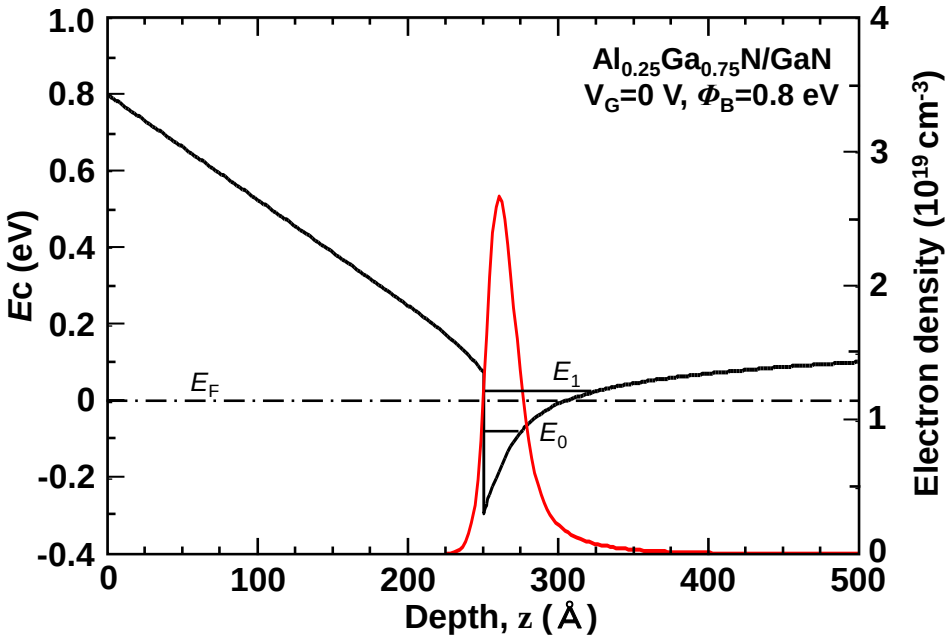


Fig. 2.8. Results of Schrödinger-Poisson self-consistent calculation at $Al_{0.25}Ga_{0.75}N$/GaN heterostructure.

Figure 2.9 shows the conduction band of the AlGaN/GaN heterostructure, where Φ_B is a Schottky barrier. Under the gate of an AlGaN/GaN HEMT, Schottky barrier is modified by the applied gate voltage.

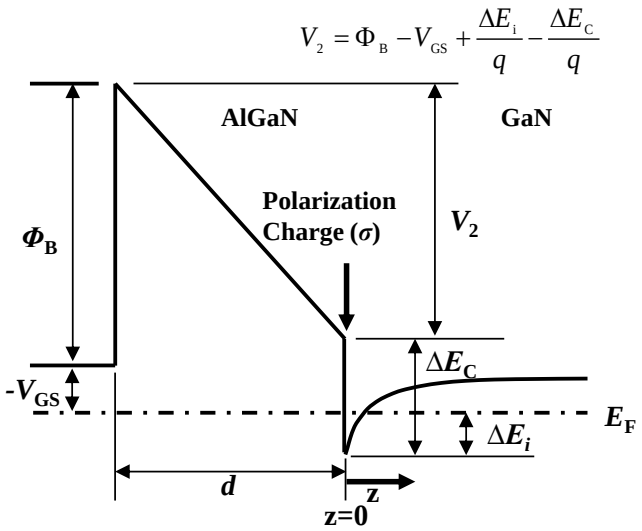


Fig. 2.9. Vertical cross-section of the conduction band of the AlGaN/GaN heterostructure.

The Fermi level is denoted by E_F and ΔE_C is the conduction band offset. The ΔE_i is the subband energy. The boundary conditions are:

If, z=0, then $V(z)$=0
and z=-d, then $V(z)$=-V_2

The potential energy $V(z)$ is found from the solution of Poisson's equation

$$\frac{d^2V(z)}{dz^2} = -\frac{q\sigma(z)}{\varepsilon}, \tag{2.15}$$

where, ε (=$\varepsilon_0\varepsilon_r$) is the dielectric constant of AlGaN layer and $\sigma(z)$ is the polarization charge density. The conduction band potential of AlGaN is defined by V_2.

$$V_2 = -F_S \cdot d + \frac{q\sigma d}{\varepsilon} \tag{2.16}$$

where, F_s is the hetero-surface electric field and d is a thickness of the AlGaN layer. By Gauss's theorem, the relationship between F_s and 2DEG carrier (n_{2D}) can be represented

$$qn_{2D} = \varepsilon F_S \tag{2.17}$$

From the equations 2.16 and 2.17, F_s can be replaced and the relationship between n_{2D} and V_{GS} is

$$\begin{aligned} n_{2D} &= \frac{\varepsilon}{qd}\left\{V_{GS} - \left(\Phi_B - \frac{\Delta E_C}{q} - \frac{q\sigma d}{\varepsilon} + \frac{\Delta E_i}{q}\right)\right\} \\ &= \frac{\varepsilon}{q(d+\Delta d)}\{V_{GS} - V_T\}, \end{aligned} \tag{2.18}$$

where, V_T is the threshold voltage. It can be expressed as

$$V_T = \Phi_B - \frac{\Delta E_C}{q} - \frac{q\sigma d}{\varepsilon} + \frac{\Delta E_i}{q}, \qquad (2.19)$$

here, Δd and E_{F0} are the following:

$$\Delta d = \frac{\varepsilon a}{q} \quad , \quad \Delta E_i = E_{F0} + a n_{2D}.$$

Figure 2.10 shows the conduction band diagram of an AlGaN/GaN HEMT with applied gate bias voltage, V_{GS}. The on-state (a) and off-state (b) conduction band profiles of a device are also shown.

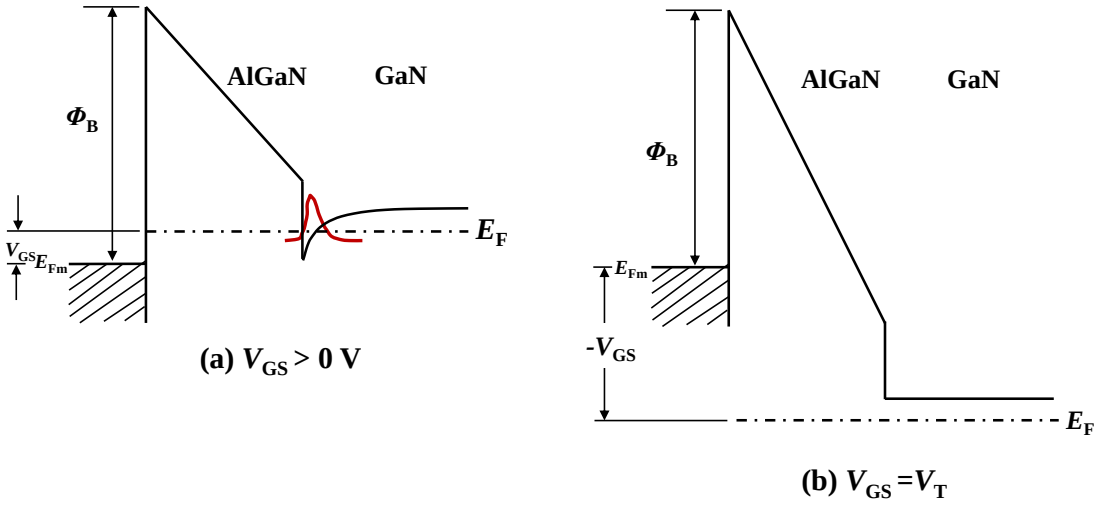


Fig. 2.10. The conduction band diagram of an AlGaN/GaN HEMT. (a) A fully open channel where the applied V_{GS} is positive. b) Flat band condition where $V_{GS}=V_T$.

2.7 Velocity-field characteristics

When an electron distribution is subjected to an electric field, the electrons tend to move in the field direction (opposite to the field *F*) and gain velocity from the field. However, because of imperfections, they scatter in random directions. A steady state is established in which the electrons have some net drift velocity in the field direction. In most electronic devices a significant portion of the electronic transport occurs under strong electric fields.

This is especially true of field effect transistors. At such high fields (F ~ 1-100 kV/cm) the electrons get "hot" and acquire a high average energy. The extra energy comes due to the strong electric fields. The drift velocities are also quite high. The description of electrons at such high electric fields is quite complex and requires either numerical techniques or computer simulations.

For long-channel devices, the field is low enough that the carrier velocity is treated as being proportional to the field, i.e., constant mobility. At low fields the drift velocity increases linearly with the field, and the slope corresponds to a constant mobility ($\mu=v/F$). At higher fields, the carrier velocity deviates from a linear dependence. It becomes lower than simple extrapolation from the low-field slope, and eventually saturates to a value called saturation velocity, v_s. In drift-diffusion simulations of AlGaN/GaN HEMTs, the use of the proper electron transport model is critical. Traditionally, the high-field transport model of electrons was assumed to follow [20] as

$$v(E) = \frac{\mu F}{(1+(\mu F / v_s)^{\beta_c})^{1/\beta_c}}. \qquad (2.20)$$

This formula is used for Si and other semiconductors with a similar band structure. Here, parameter β_C = 1.7 for GaN [20]. The low-field mobility depends on temperature and doping concentration. Figure 2.11 shows the calculated velocity–field characteristics of an AlGaN/GaN HEMT for steady state condition. At room temperature, high-field mobility, μ=1700 $cm^2V^{-1}sec^{-1}$ is considered [20]. The peak electron velocity of $v_s=2.5\times10^7$ cm/s is calculated. However, for transient state condition of devices, mobility is not constant. It depends on different kind of scattering mechanisms such as acoustic phonon scattering, polar and non -polar optical phonon scattering, and piezoelectric scattering [19-20].

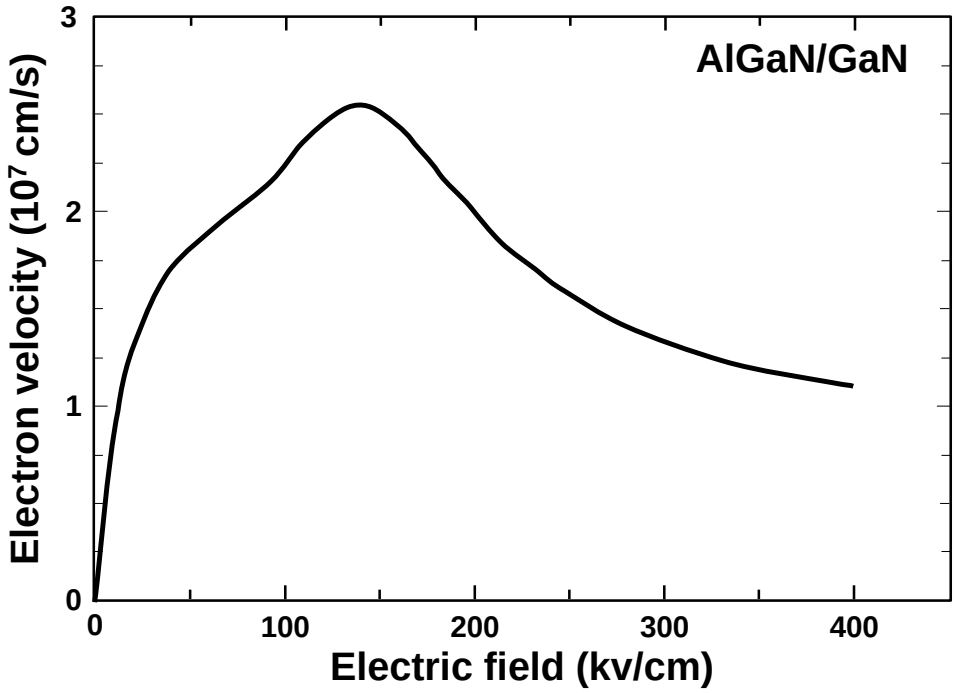


Fig. 2.11. Electron velocity versus electric field of an AlGaN/GaN HEMT.

2.8 Principle of operation

Figure 2.12 shows a schematic view of an AlGaN/GaN HEMT device. In a real transistor, the length of the device is much larger than the thickness of the AlGaN barrier. The current flows between the ohmic contacts, from drain to source, and it is modulated by the voltage applied at the gate (i.e., Schottky contact). The drain current, I_D can be represented as a function of $n_{2D}(x)$ and $V(x)$ in the lateral direction.

$$I_D = W_G q n_{2D}(x) \mu \left(\frac{\partial V(x)}{\partial x} \right), \tag{2.21}$$

where, μ is the channel electron mobility and W_G is the gate width. By integrating from source side of the gate edge (x =0) to drain side of gate edge ($x = L_G$), the I_D is obtained as

$$I_D = \frac{\varepsilon \mu W_G}{(d + \Delta d) L_G} \left\{ (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right\} \tag{2.22}$$

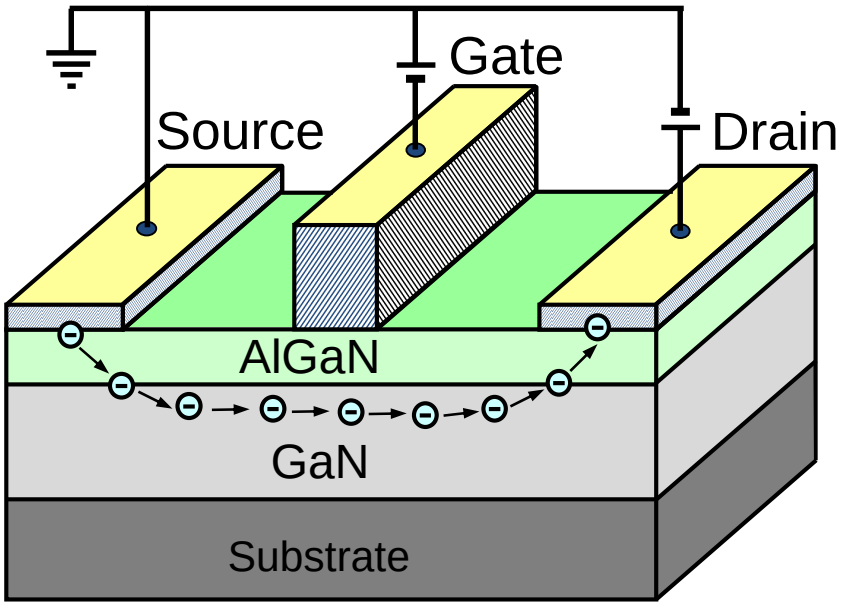


Fig. 2.12. Schematic structure of an AlGaN/GaN HEMT device. The figure is not to scale.

where, the drain-to-source voltage is defined as V_{DS}. When V_{DS} is small, the electron velocity is simply proportional to the electric field ($v=\mu F$). Further, assuming that the saturation current occurs when the electric field at the drain side of the gate exceeds the saturation velocity ($v_s=\mu F_s$) and the longitudinal field distribution in the channel where the potential is below the saturation voltage. The saturation drain current can be expressed as

$$I_D^S = \frac{\varepsilon\mu W_G E_S}{d+\Delta d}\left\{\sqrt{(V_G - V_T)^2 + E_S^2 L_G^2} - E_S L_G\right\} \tag{2.23}$$

In this equation, E_s is an electric field that drift velocity reaches a peak speed in electric field characteristic. Moreover, in the short gate HEMT, L_g is small enough compared to (V_{GS}-V_T) / F_s, thus, the I_D^s can be expressed as

$$I_D^S = \frac{\varepsilon W_G v_S}{d+\Delta d}(V_{GS} - V_T). \tag{2.24}$$

If the I_D^s varies linearly with the V_{GS}, the g_m is a constant value, which is proportional to the saturation velocity. It is also inversely proportional to the distance from gate to channel (i.e.,

d+Δd). This distance can be designed to be smaller for obtaining high g_m. The transconductance (g_m) is expressed as

$$g_m = \frac{\varepsilon W_G v_S}{d + \Delta d}. \qquad (2.25)$$

It is a major feature of an AlGaN/GaN HEMT. Combine of equations 2.24 and 2.25 are expressed as

$$I_D^S = g_m (V_{GS} - V_T). \qquad (2.26)$$

Figs. 2.13 and 2.14 show the current voltage and the transconductance characteristics of an AlGaN/GaN HEMT.

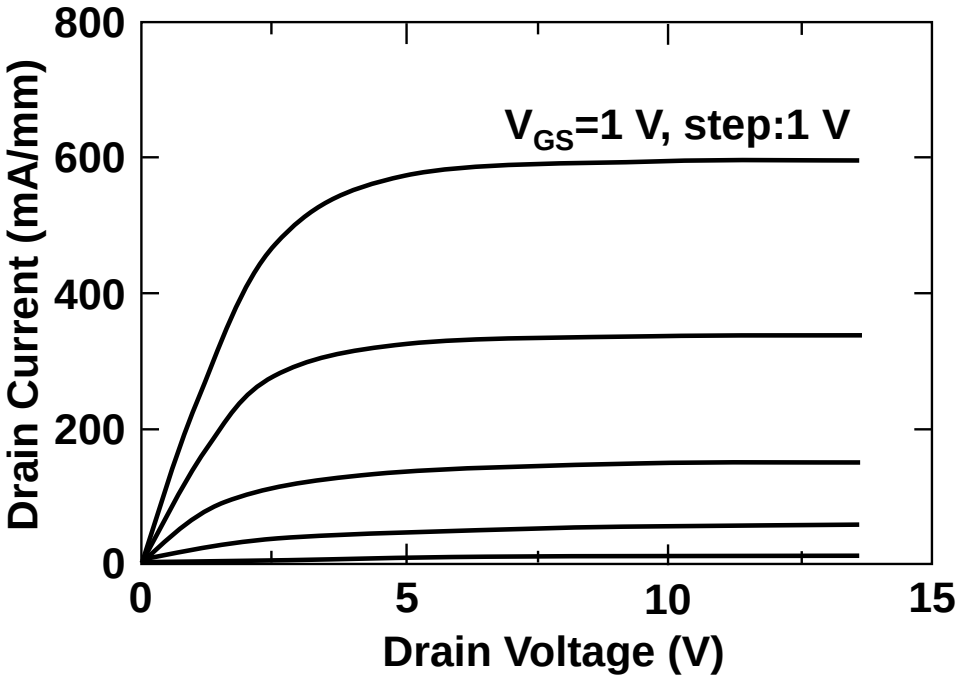


Fig. 2.13 Typical current-voltage characteristics of an AlGaN/GaN HEMT.

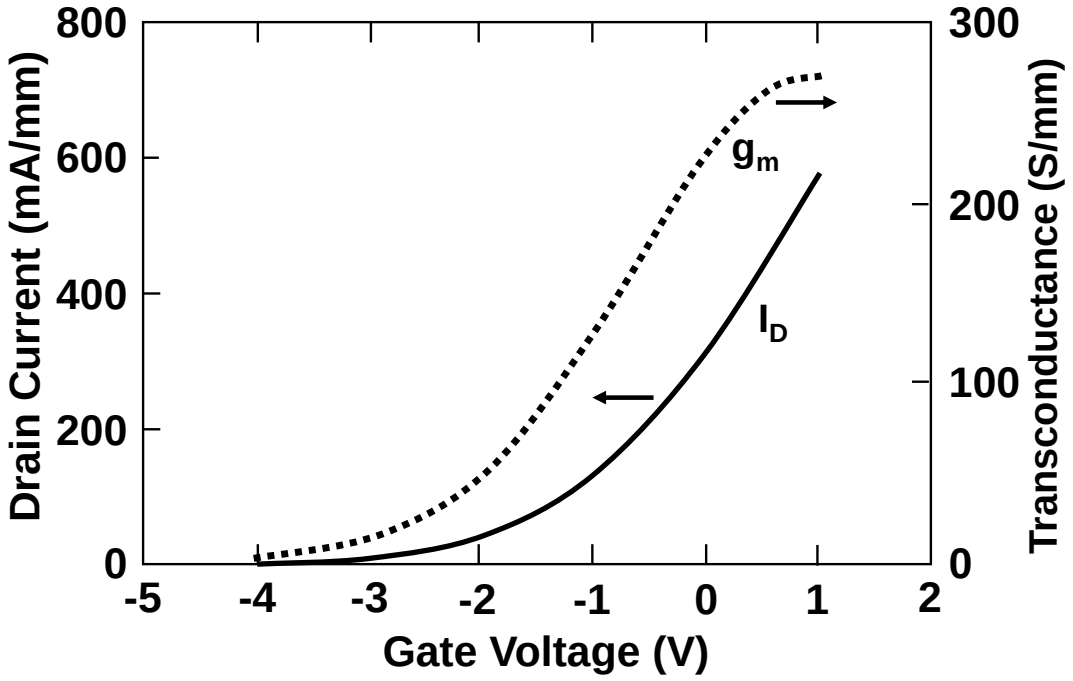


Fig. 2.14 Typical drain current and transconductance as a function gate voltage of an AlGaN/GaN HEMT.

2.9 Current collapse

In the literature, the term current collapse is used with two meanings. In a wider sense, it means a class of phenomena that lead to drain current degradation and increased dynamic R_{on}. Historically, however, it was defined, during the development of GaAs-based HEMTs, as a persistent yet recoverable reduction of the static current at a high drain bias voltage [21]. Some of the other phenomena that fall under the wider meaning of the current collapse are gate and drain lag, and static-pulse dispersion. Gate (drain) lag refers to I_D transient in response to gate (drain) voltage pulses keeping the drain (gate) voltage constant. The corresponding measurement techniques are combined in the pulsed *I-V* measurements, in which both the gate and drain voltages are pulsed at the same time from a quiescent bias. Figure 2.15 shows a sketch of AlGaN/ GaN HEMT's *I-V* characteristics before (solid lines) and after (dotted lines) current collapse. The leakage current from the gate and carrier trapping in general, into the surface and buffer traps is the physical cause behind the current collapse class of the phenomena.

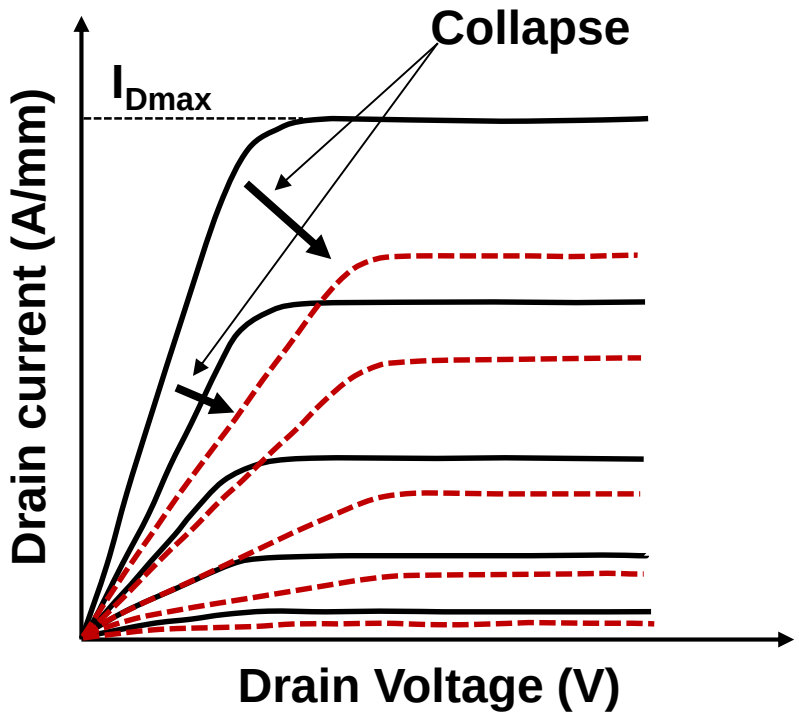


Fig.2.15 A sketch of AlGaN/ GaN HEMT's current–voltage characteristics before (solid lines) and after (dotted lines) current collapse.

The term traps refers to energy states in the band-gap of a semiconductor. The origin of traps can be a consequence of several factors, e.g., crystal defects, dislocations, or the presence of impurities. These trap states may be empty or occupied by electrons, which has an impact on the charge they carry. Trap states in the upper part (above the neutral level) of the band gap (closer to the conduction band) are acceptor-like, neutral when empty and negatively charged when occupied. Trap states in the lower part (below the neutral level) of the band gap (closer to the valence band) are donor-like, positively charged when empty and neutral when occupied. Traps at the interface or the surface of a device play an important role in the device operation and performance. One of the conclusions of Section 2.4 was that there is large negative charge at the surface of the device. The negative charge would repel the electrons away from the interface and deplete the channel. Moreover, there is a question, what is the origin of the electrons in 2DEG. It was suggested that, after the growth, during the cooling process, free electrons would compensate the polarization-induced charge [22]. As a different solution to both problems, nowadays widely accepted, it

was suggested that surface donor-like traps could be the source of both the channel electrons and the positive charge, screening the large negative polarization-induced charge [23-25]. For thin AlGaN barrier thickness, the surface trap level is below the Fermi level, the traps are occupied and hence neutral as shown in Fig. 2.16 (a). At a critical barrier thickness, the surface traps reach the Fermi level and the electrons from these traps are driven into the Fermi level and the electrons from these traps are driven into the channel by the strong polarization-induced electric field in AlGaN [24]. The band diagram, with the energy level of the surface traps, with varying barrier thickness is shown in Fig. 2.16 (a). As the donor-like traps are emptied, they become positively charged and in effect they reduce (by passivation) the negative charge. In the absence of holes, the energy of these traps has been theoretically predicted to be ~1.65 eV in $Al_{0.35}Ga_{0.65}N$ [25].

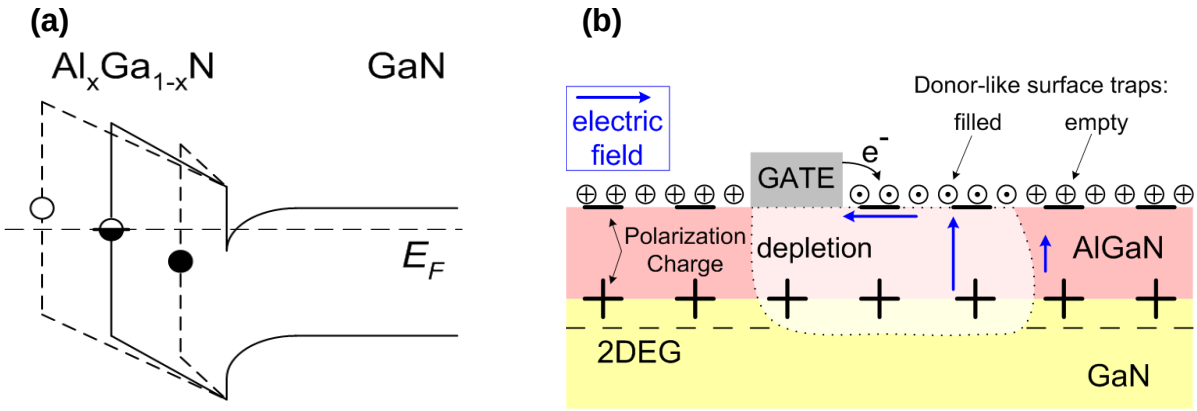


Fig. 2.16. The effect of surface traps on 2DEG creation, reduction of the negative surface charge and current collapse. (a)The trap energy level is below the Fermi level and the states are filled for thin AlGaN barrier [24]. (b) Surface trapping effects [25].

At large negative gate voltage, electrons from gate may leak to the trap states in the ungated surfaces and create a "virtual gate" and modulate the depletion region, as shown in Fig. 2.16 (b). In pulsed operation, the gate voltage changes abruptly and since the response of the trapped electrons is not immediate, it leads to RF drain current collapse phenomenon. The transient time constants depend on the energy level of the traps [26]. The surface donor-like traps used to explain the origin of 2DEG can explain RF current collapse with time constants on the order of seconds [27], as observed experimentally [28].

However, transients with shorter time constants (10-100 μs) can be explained by the existence of surface donors with energy level 0.3 eV [27] and 0.25 eV [29].

Mantra et. al. has investigated the field-dependence of active traps to interpret trapping/ detrapping in the barrier near the AlGaN surface [30-32]. Figure 2.17 shows energy band diagram of a trapping center in the presence of electric field together with three possible mechanisms of electron emission [32]. First, trapped electrons are thermally ionized over the lowered barrier (Poole-Frenkel effect) on the conduction band and drift down to the channel. Second, combination of thermal energy and electric field can lead to the phonon-assisted tunneling (PAT). Finally, direct tunneling can happen when the bands are sufficiently tilted. If the emission process of trapped charge in AlGaN barrier follows the Poole-Frenkel electron emission among three different-type emissions, the emission rate (e) should be proportional to $\exp(\sqrt{F})$ or $\exp(\alpha\sqrt{V_D})$, where F is an electric field, V_D is an applied voltage between gate and drain, and α is a correlation constant between the applied voltage

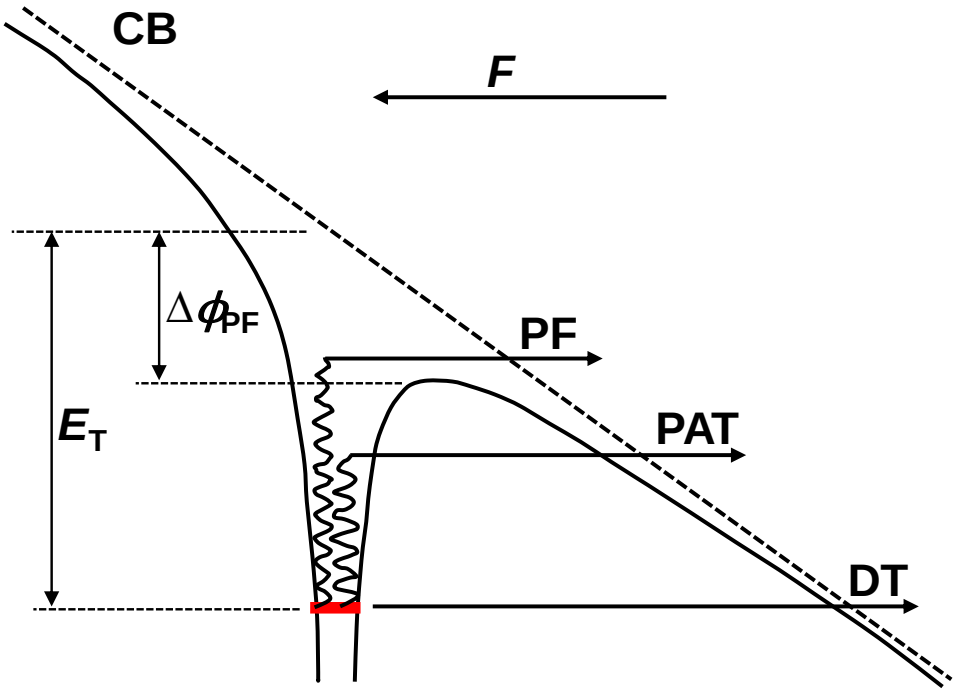


Fig. 2.17. Energy diagram of the trapping center in the presence of the electric field. Arrows indicate the possible mechanisms of electron emission: thermal ionization over the lowered barrier (Poole-Frenkel effect), direct tunneling (DT) into the conduction band (CB), and phonon assisted tunneling (PAT).

and the lowering of the trap potential. The relationship between emission rate and V_D at V_{GS}= 0 V is derived from the combination of following three equations [32]. First, assuming that the emission is a thermally activated process, the emission rate from trap level can be expressed by the following Arrhenius equation:

$$e = AT^2 \exp\left(-\frac{E_i}{kT}\right). \tag{2.27}$$

Second, the barrier decrease ($\Delta\phi_{\mathrm{PF}}$) due to the high electric field (Poole-Frenkel effect) is proportional to the square root of the applied electric field (F) as follows:

$$\Delta\phi_{\mathrm{PF}} = \left(\frac{q^3}{\pi\varepsilon}\right)^{1/2}\sqrt{F} = \beta\sqrt{F}, \tag{2.28}$$

where, q is a unit of electron charge and ε is the dielectric constant. Third, the ionization energy as a function of a field can be written as:

$$E_i(F) = E_i(0) - \beta\sqrt{F}, \tag{2.29}$$

where, $E_i(0)$=E_{T} is the binding energy of the electron on the trap in zero field. Finally, the field-dependent emission rate equation is deduced as:

$$e(F) = e(0)\exp\left(\frac{\Delta\phi_{PF}}{kT}\right) = e(0)\exp(\beta\sqrt{V_D}). \tag{2.30}$$

More strictly, the field-dependent emission rate equation should include built-in potential due to polarization field in AlGaN/GaN barrier (~10^6 V/cm). The emission rate can be rewritten as:

$$e(F) = e(0)\exp(\beta\sqrt{V_D + V_{bi}}), \tag{2.31}$$

where, $V_{bi}[=(\Phi_B - \Delta E_C + E_{Fi})/d_{AlGaN}]$ is the built-in voltage across AlGaN barrier, Φ_B is the barrier height at the AlGaN surface, ΔE_C is the conduction band offset between AlGaN and GaN, and E_{Fi} is the difference between Fermi level and GaN conduction band edge at the AlGaN/GaN interface. It is considered that Poole-Frenkel type emission is dominant for the trapped charge near the AlGaN surface. It is inferred that the trapped electrons stay near the AlGaN surface below a certain V_{DS} (or V_D), resulting in channel depletion and drain current collapse, until V_{DS} is large enough for phonon-assisted field emission or direct field emission from the surface to the channel.

2.11 Trade-off between on-resistance and breakdown voltage

One of the most unique features of power semiconductor devices is their ability to withstand high voltages. The desire to control larger power levels has encouraged the development of power devices with larger breakdown voltages**.** In a semiconductor, the ability to sustain high voltages without the onset of significant current flow is limited by the avalanche breakdown phenomenon, which is dependent on the electric field distribution within the structure. High electric fields can be created within the interior of power devices as well as at their edges. The design optimization of power devices must be performed to meet the breakdown voltage requirements for the application while minimizing the on-state voltage drop, so that the power dissipation is reduced. The resistance of the ideal drift region can then be related to the basic properties of the semiconductor material. Such semiconductor structure own a triangular electric field distribution, as shown in Fig. 2.18, within a uniformly doped drift region with the slope of the field profile being determined by the doping concentration. The maximum voltage that can be supported by the drift region is determined by the maximum electric field (E_m) reaching the critical electric field (E_c) for breakdown for the semiconductor material. The critical electric field for breakdown and the doping concentration then determine the maximum depletion width (W_D). The resistance of ideal drift region of area, A, is given by:

$$R \cdot A = \int_0^{W_D} \rho(x)dx = \int_0^{W_D} \frac{dx}{q\mu_n N_D(x)}. \qquad (2.32)$$

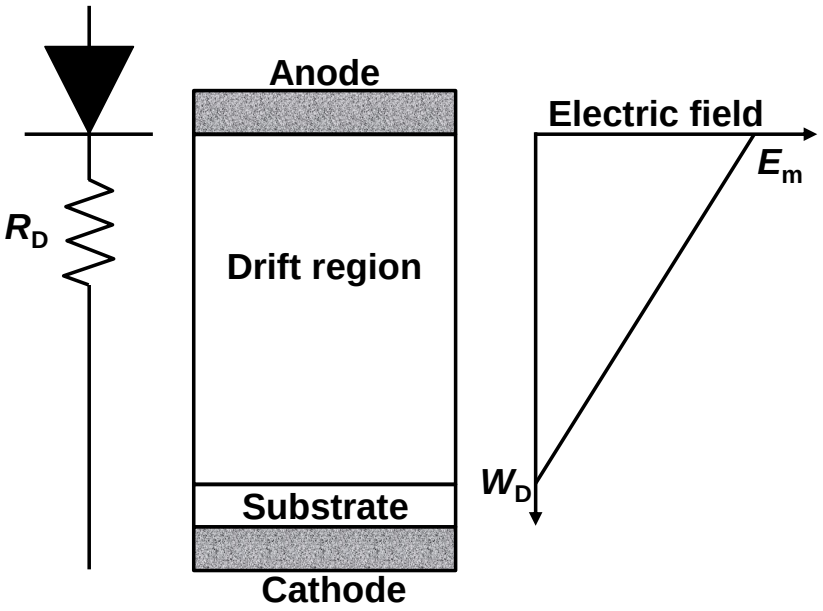


Fig. 2.18 An ideal drift region and its electric field distribution.

The specific resistance (resistance per unit area) of the ideal uniformly doped drift region is therefore:

$$R_{on,sp} = \left(\frac{W_D}{q\mu_n N_D} \right). \tag{2.33}$$

The depletion width under breakdown conditions is given by:

$$W_D = \frac{2V_{BR}}{E_C} \tag{2.34}$$

where V_{BR} is the desired breakdown voltage. The doping concentration in the drift region required to obtain this V_{BR} is given by:

$$N_D = \frac{\varepsilon_S E_C^2}{2qV_{BR}}. \tag{2.35}$$

Combining these relationships, the specific resistance of the ideal drift region is obtained:

$$R_{on,-ideal} = \frac{4V_{\mathrm{BR}}{}^2}{\varepsilon_S \mu_n E_C^3}. \tag{2.36}$$

The denominator of this equation ($\varepsilon_S \mu_n E_C^3$) is commonly referred to as Baliga's figure of merit for power devices. It is an indicator of the impact of the semiconductor material properties on the resistance of the drift region. Material parameters are mentioned in chapter 1, Table I. Figure 2.19 shows sum of specific on resistance of the drift region and the ohmic contact resistance versus breakdown voltage for Si, SiC and GaN. The theoretical total specific on-resistance is used as theoretical limits along this work for benchmarking the results in this work with the state-of-the-art devices.

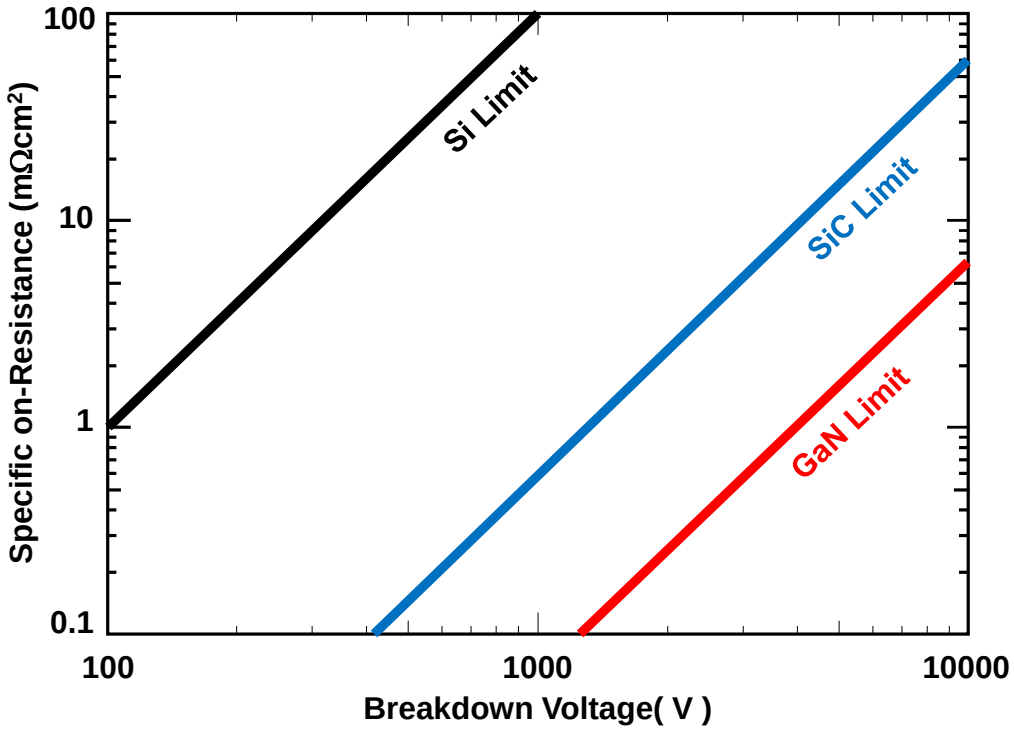


Fig. 2.19. Sum of specific on resistance of the drift region and the ohmic contact resistance versus breakdown voltage for Si, SiC, and GaN.

In switching operation the transistors alternate between on-state were the gate opens the channel and allow the carriers flow through the device and off-state were the gate closes the channel and blocks the current of carriers. At off-state the gate potential, V_{GS}, is lower than the device's threshold potential, V_T, and considered as sub-threshold conditions. For efficient switching the off-state operation point conditions should be at high positive drain voltage and negligible drain current therefore a strong gate blocking capability is required. At very high

positive drain voltage condition the blocking capability of the device degrades and gives rise to sub-threshold leakage, (STL), current. The sub-threshold leakage current will increase and become significant then will reduce the efficiency of the switching. A significant leakage current is considered as three orders of magnitude lower than the device's maximal output current therefore a common used value is 0.1 mA/mm. At high voltages, currents that are higher than this value may initiate destructive processes in the device therefore it is considered to be the starting point of the device breakdown. Thus, the breakdown voltage is usually defined as the voltage at which the drain current exceeds the traditional value of 0.1 mA/mm in three terminal measurements. By increasing the potential difference at the drain terminal the charge carriers would drift by electrical forces to the lower potential through intermediate potential levels and states and will reach eventually to the drain terminal. The path of the charge carriers through these intermediate potential states is the device blocking weakness and it determines the mechanisms of the device breakdown.

References

[1] O. Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, et al., "Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures", J. Appl. Phys., vol. 85, pp. 3222–33, 1999.

[2] A. Zoroddu, F. Bernardini, P. Ruggerone and V. Fiorentini, Phys. Rev. B, Vol. 64, pp. 45208, 2001.

[3] S-H. Wei, L. G. Ferreira, J. E. Bernard and A. Zunger, Phys. Rev. B, vol. 42, p. 9622, 1990.

[4] H Angerer et al., Appl. Phys. Lett., vol. 71, p. 1504, 1997.

[5] T. Peng, J. Piprek, G. Qiu, J. O. Olowolafe, K. M. Unruh, C. P. Swann and E. F. Schubert, Appl. Phys. Lett., vol. 71, p. 2439, 1997.

[6] L. Bellaiche, S-H Wei and A. Zunger, Phys. Rev. B, vol. 56, p. 13872, 1997.

[7] F. Bernardini, "Spontaneous and Piezoelectric Polarization: Basic Theory vs. Practical Recipes," in Nitride Semiconductor Devices: Principles and Simulation, J. Piprek, Ed.: Wiley-VCH Verlag GmbH & Co. 2007, ch. 3, pp. 49-68.

[8] J. F. Nye, Physical Properties of Crystals: Their Representation by Tensors and Matrices: Oxford University Press, USA, 1985.

[9] F. Bernardini and V. Fiorentini, "Nonlinear Behavior of Spontaneous and Piezoelectric Polarization in III-V Nitride Alloys," Physica Status Solidi (a), vol. 190, no. 1, pp. 65-73, 2002.

[10] O. Ambacher, B. Foutz, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, et al., "Two dimensional electron gases induced by spontaneous and piezoelectric polarization in undoped and doped AlGaN/GaN heterostructures", J. Appl. Phys., vol. 87, pp. 334–44, 2000.

[11] F. Bernardini and V. Fiorentini, "Nonlinear macroscopic polarization in III-V nitride alloys," Physical Review B, vol. 64, no. 8, p. 085207, 2001.

[12] P. Feynman and H. Kleinert, "Effective classical partition functions", Phys. Rev. A, vol. 34, pp. 5080-5084, 1986.

[13] D.K. Ferry, "The onset of quantization in ultra-submicron semiconductor devices", Superlatt. Microstruct., vol. 27, pp. 61-66, 2000.

[14] I. Knezevic, D.Z. Vasileska, D.K. Ferry, "Impact of strong quantum confinement on the performance of a highly asymmetric device structure: Monte Carlo particle-based simulation of a focused-ion-beam MOSFET", IEEE Trans. Electron Devices, vol. 49, pp. 1019-1026, June 2002.

[15] L. Shifen, R. Akis, and D.K. Ferry, "Correspondence between quantum and classical motion: comparing Bohmian mechanics with a smoothed effective potential approach", Phys. Lett. A, vol. 274, pp. 75-83, Sep. 2000.

[16] Y. Li, T. Tang, and X. Wang, "Modeling of Quantum Effects for Ultrathin Oxide MOS Structures with an Effective Potential", IEEE Trans. Nanotechnology, vol. 1, pp. 238-242, Dec. 2002.

[17] D. Vasileska and S.S. Ahmed, "Narrow-width SOI devices: The role of quantum-mechanical size quantization effect and unintentional doping on the device operation", IEEE Trans. Electron Devices, vol. 52, pp. 227-236, Feb. 2005.

[18] F. Sacconi, A.D. Carlo, P. Lugli, and H. Morkoç, "Spontaneous and piezoelectric polarization effects on the output characteristics of AlGaN/GaN heterojunction modulation doped FETs", IEEE Trans. Electron Devices, vol. 48, pp. 450-457, Mar. 2001.

[19] S. Yamakawa, PhD Thesis, Arizona state University, 2005.

[20] T. Palacios and U. K. Mishra,"AlGaN/GaN High Electron Mobility Transistors," in Nitride Semiconductor Devices: Principles and Simulation, J. Piprek, Ed.: Wiley-VCH Verlag & Co., 2007, ch. 10, pp. 211-233.

[21] S. C. Binari, P. B. Klein, and T. E. Kazior, "Trapping effects in GaN and SiC microwave FETs,"Proceedings of the IEEE, vol. 90, no. 6, pp. 1048-1058, 2002.

[22] P. B. Klein and S. C. Binari, "Photoionization spectroscopy of deep defects responsible for current collapse in nitride-based field effect transistors," J. Phys.: Cond. Matt., p. R1641, 2003.

[23] I. P. Smorchkova, C. R. Elsass, J. P. Ibbetson, R. Vetury, B. Heying, P. Fini, E. Haus, S. P. DenBaars, J. S. Speck, and U. K. Mishra, "Polarization-induced charge and electron mobility in AlGaN/GaN heterostructures grown by plasma-assisted molecular-beam epitaxy," J. Appl. Phys., vol. 86, no. 8, pp. 4520-4526, 1999.

[24] J. P. Ibbetson, P. T. Fini, K. D. Ness, S. P. DenBaars, J. S. Speck, and U. K. Mishra, "Polarization effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field effect transistors," Appl. Phys. Lett., vol. 77, no. 2, pp. 250-252, 2000.

[25] R. Vetury, N.Q. Zhang, S. Keller, and U.K. Mishra, "The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs," IEEE Trans. Electron Devices, vol. 48, no. 3, pp.560-566, 2001.

[26] J. M. Tirado, J. L. Sanchez-Rojas, and J. I. Izpura, "Simulation of surface state effects in the transient response of AlGaN/GaN HEMT and GaN MESFET devices," Semiconductor Science and Technology, vol. 21, no. 8, pp. 1150-1159, 2006.

[27] G. Meneghesso, G. Verzellesi, R. Pierobon, F. Rampazzo, A. Chini, U.K. Mishra, C. Canali, and E. Zanoni, "Surface-related drain current dispersion effects in AlGaN-GaN HEMTs," Electron Devices, IEEE Transactions on, vol. 51, no. 10, pp. 1554-1561, 2004.

[28] G. Koley, V. Tilak, L. F. Eastman, and M. G. Spencer, "Slow transients observed in

AlGaN/GaN HFETs: effects of SiN_x passivation and UV illumination," Electron Devices, IEEE Trans. on, vol. 50, no. 4, pp. 886-893, 2003.

[29] J. M. Tirado, J. L. Sanchez-Rojas, and J. I. Izpura, "Trapping Effects in the Transient Response of AlGaN/GaN HEMT Devices," Electron Devices, IEEE Trans. on, vol. 54, pp. 410-417, 2007.

[30] O. Mitrofanov and M. Manfra, "Mechanisms of gate lag in GaN/AlGaN/GaN high electron mobility transistors," Superlattices and Microstructures, vol. 34, pp. 33-53, 2003.

[31] O. Mitrofanov and M. Manfra, "Dynamics of trapped charge in GaN/AlGaN/GaN high electron mobility transistors grown by plasma-assisted molecular beam epitaxy," Applied Physics Letters, vol. 84, pp. 422-424, 2004.

[32] O. Mitrofanov and M. Manfra, "Poole-Frenkel electron emission from the traps in AlGaN/GaN transistors," Journal of Applied Physics, vol. 95, pp. 6414-6419, 2004.

Chapter 3
Device processing and characterization procedure

3.1 Introduction

This chapter illustrates fabrication processes of AlGaN/GaN HEMT including optimization of dry-etching using ICP-RIE for mesa isolation and photolithography process. Pulsed *I-V* measurements conditions are also described for dynamic performances evaluation.

3.2 Device fabrication

The epitaxial wafers used were grown on c-plane three inch sapphire substrates by metal organic vapor phase epitaxy (MOVPE). It consists of a 1-μm GaN channel, and a 25-nm $Al_{0.25}Ga_{0.75}N$ barrier. The Hall mobility and sheet electron density were 1483 cm^2/Vs and 1.01×10^{13} cm^{-2}, respectively at room temperature. Before starting the HEMT process, AlGaN/GaN-heterostructure samples have to be cleaned by degreasing process. The following fabrication processes were done, such as mesa-isolation, ohmic metallization, Schottky metal contact formation, passivation film deposition. Note that additional metal layer (i.e., pad) was deposited for a better conduction and surface roughness for all annealed ohmic contacts and Schottky contact. Pad metals deposition process was not included since it is the same as Schottky contact formation using photolithography.

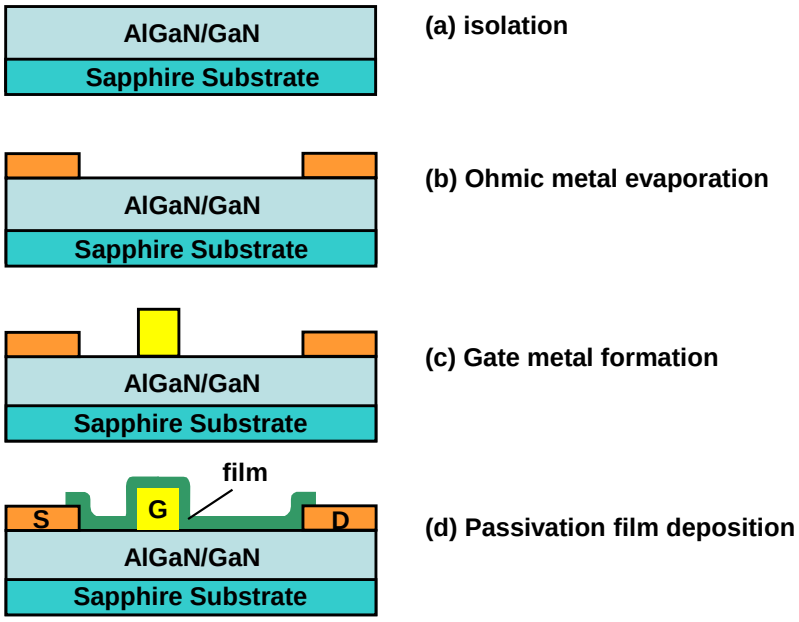


Fig. 3.1. Process sequence of AlGaN/GaN HEMTs.

3.2.1 Mesa isolation

Figure 3.1 shows fabrication process sequence of AlGaN/GaN HEMTs. Device fabrication began with mesa isolation using Cl_2/BCl_3-based inductively coupled plasma reactive ion etching (RIE). In order to reduce leakage current, mesa isolation was performed. The epitaxial wafer was etched from top of the AlGaN layer to 100-nm depth of GaN-buffer layers. Figure 3.2 shows the SAMCO Model RIE-200iP system, which was employed in this

Fig. 3.2 A reactive ion etching system.

work. The etching was done photolithography processes using PFI photoresist. The ICP power and bias were set up as 50 W and 100 V, respectively. The BCl_3 gas was introduced to the chamber at a flow rate of 4 sccm.

3.2.2 Ohmic metallization

Ohmic patterns were formed with evaporating Ti/Al/Mo/Au (15/160/35/50-nm) metals, then alloyed at 850 °C for 30 s in N_2 flow. Vacuum evaporation was used for the deposition of metals on devices. The EIKO e-beam evaporator was used in this work, as shown in Fig. 3.3. This evaporation source consists of a crucible with center cavity to hold the metal source. A high-temperature filament locates in the side of the crucible. A high current was passed through the filament to boil off the metal. The metal was evaporated to deposit on the wafer, which was held at the top of chamber.

Fig. 3.3. An e-beam evaporator system.

After the evaporation of ohmic contacts, the wafer was subjected to the lift-off technique. The wafer was immersed in a solution (acetone) capable of dissolving the photoresist for around 10 min. Then, the sample was taken out and immediately acetone spraying was done manually. The deposited metal on the resists lifted off quickly and only metals remained on contact holes. The sample was then subjected to ultrasonic agitation in ethanol to completely

lift off all metals. Since two layer photoresists were applied in this work, only top photoresist, PFI, was removed by acetone. Thus, the wafer was baked on the hot plate at 100^{o}C for 20 min to remove the remained PMGI photoresist. Then, the wafer was re-immersed and ultrasonic-agitated again in acetone and ethanol, respectively to completely remove all unnecessary particles. Finally, the wafer was accomplished using O_2 plasma reactor (YAMATO PR-500) in order to re-confirm for removing any remaining photoresist and rinsed in de-ionized water.

After lift-off, annealing was performed using rapid thermal annealing (RTA) system, as shown in Fig. 3.4. Devices were annealed in N_2 atmosphere with 850 °C for 30 s. The contact resistance of 0.34 Ωmm was measured.

Fig. 3.4. A rapid thermal annealing system.

3.2.3 Schottky formation

Ni/Au (50/180-nm) was used as Schottky gate metallization. Same e-beam system was used for gate formation.

3.2.4 Passivation film deposition

Devices were made having passivation film of SiN and that of Al_2O_3 for controlling the surface condition. SiN and Al_2O_3 films were deposited on devices using sputter system and atomic layer deposition (ALD) system, respectively. The thickness of passivation film was 150-nm.

Sputtering is a physical vapor deposition (PVD) technique used for precision coating of thin films. The wafer is placed in a vacuum chamber for deposition of SiN. The DC sputtering system (TOKUDA Model CFS-4ES) was empoloyed in this work, as shown in Fig. 3.5. Four types of devices were fabricated having SiN with different deposition temperatures, i.e., 100, 150, 200, and 250°C. Argon (15 sccm) and nitrogen (30 sccm) gases were introduced to the vacuum chamber under the pressure of approximately 5×10^{-4} Pa. The SiN-deposition rate was around 4 nm/min.

Fig. 3.5. A DC sputtering system.

The deposition of Al_2O_3 was carried out by atomic layer deposition (ALD) system (Savannah S100-4PVP, Cambridge NanoTech), as shown in Fig. 3.6. The deposition rate of Al_2O_3 was shown in Fig. 3.6 (b).

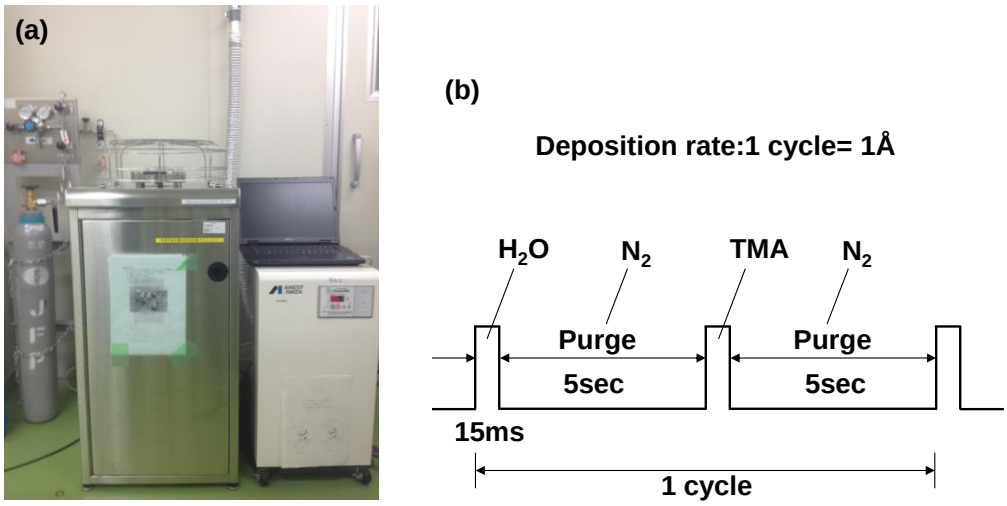


Fig. 3.6. (a) An atomic layer deposition system and (b) deposition cycle.

3.3 Device Characterization

Figure 3.7 shows (a) schematic cross-sectional view and (b) top view of the fabricated AlGaN/GaN HEMT. The gate-to-source distance (L_{GS}), gate length (L_G) and gate-to-drain distance (L_{GD}) were 2, 3, and 10 μm, respectively. The gate width was 200 μm with one finger.

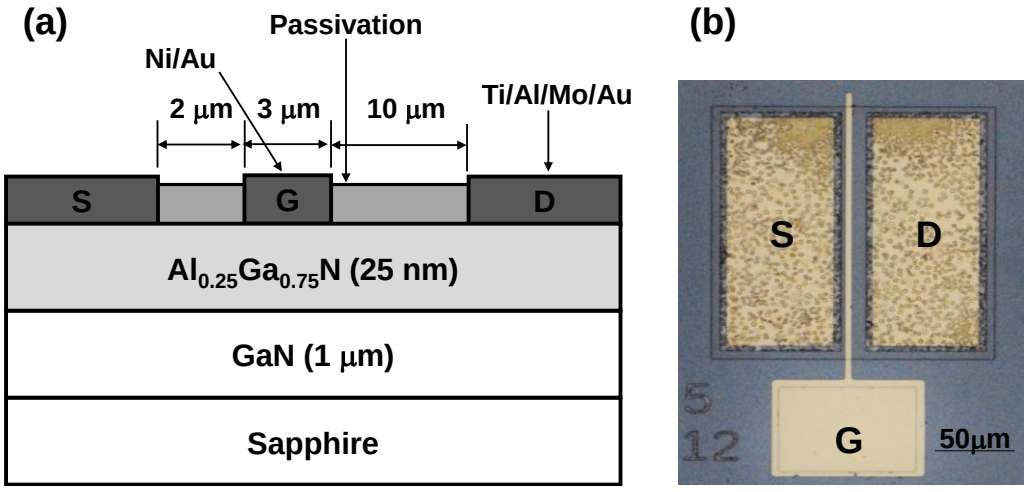
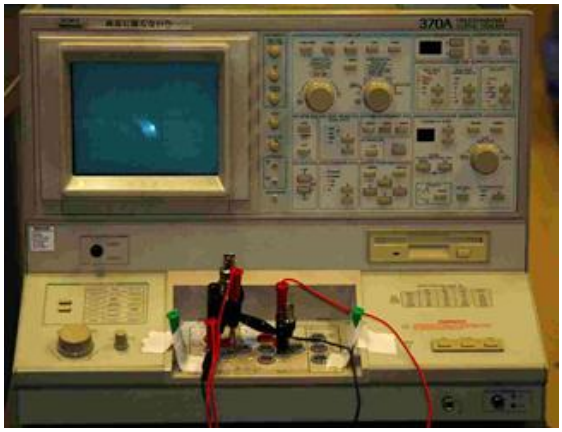


Fig. 3.7. (a) Schematic cross-sectional view and (b) top view of the fabricated AlGaN/GaN HEMT.

Figure 3.8 shows static characterization systems, which were employed in this work. In order to evaluate dynamic performance of AlGaN/GaN HEMTs, I have developed a pulsed *I-V* measurement system. Gate lag and current collapse of AlGaN/ GaN HEMTs have been investigated using this system.

(a) Agilent4155C and 41501B

(b) Cascade Microtech probe station



(c) SONY Tektronix 370A PROGRAMMABLE CURVE TRACER

Fig. 3.8. Semiconductor parameter analyzer with cascade microtech probe station and curve tracer.

Figure 3.9 shows the schematic of measurement system, which was employed for dynamic performance evaluation. A probe station (Apollowave α-100), a pulse generator (IWATSU DG 8000), an oscilloscope (LeCroy WaveRunner 204Xi-A) and a power supply (TEXIO PA600-0.1B) were empolyed, as shown in Fig. 3.10. Alongside the oscilloscope, a current probe (LeCroy CP030) and a passive probe (LeCroy PP011) were used for storing drain current and drain voltage, respectively. The load resistance (R_L) was varied from 10 Ω

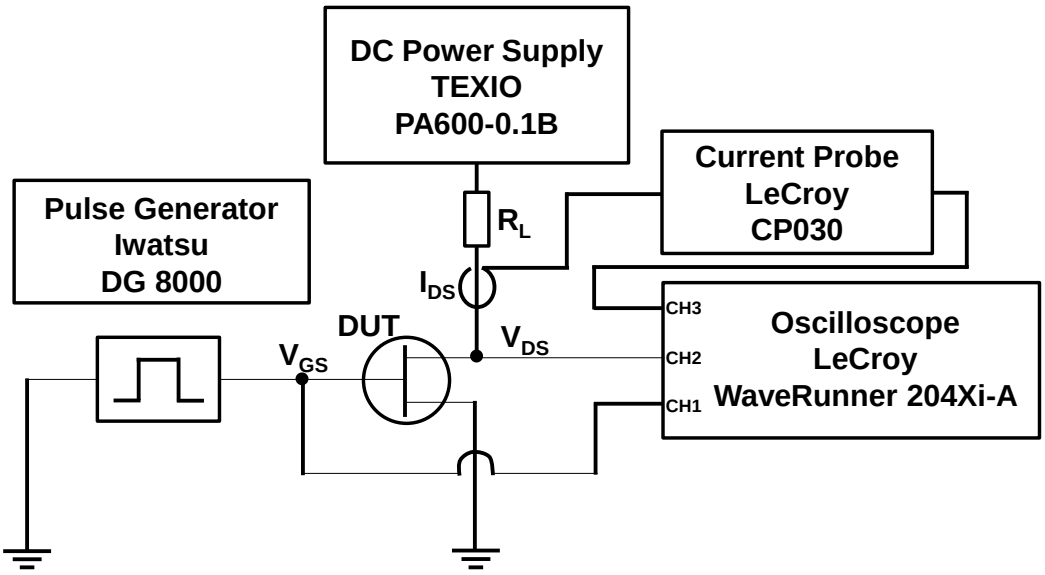


Fig. 3.9. Schematic of developed dynamic *I-V* testing system.

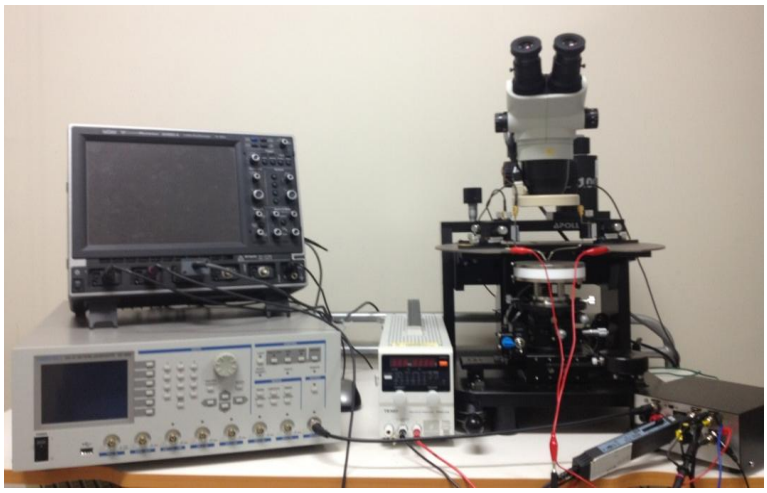


Fig. 3.10. Illustration of the developed dynamic testing system.

to 30 kΩ for measurement aspect. The pulse generator has 6 channels and can apply voltage up to ±10 V with pulse frequency of 10 MHz, while the power supply can apply voltage up to 250 V. Oscilloscope has 4 channels with maximum 2 GHz frequency pulse. The current probe is able to measure current up to 30 A, and passive probe is able to measure voltage up to 400 V. Figure 3.11 shows the equivalent circuit and impedance matching circuit. Impedance matching is employed for reducing the early stage oscillation of output signals. Table I shows the present status of pulsed *I-V* measurement system. My developed system is

able to measure a high bias voltage of 250 V with minimum measurement time of 300 ns.

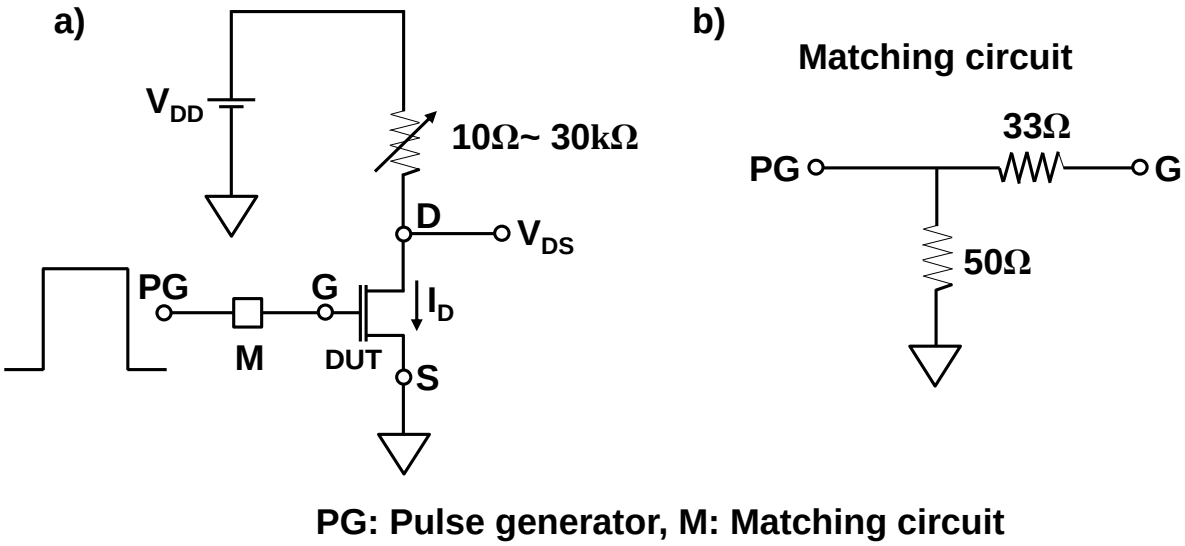


Fig. 3.11. (a) Equivalent circuit and (b) matching circuit.

Table I. Present status of pulsed *I-V* measurement system.

Year	Authors	Company /Institution	Min. meas. time	Off-state bias voltage (V)	References
2013	Tang et. al	HKUST	100 ms	200	[1]
2010	Saito et. al.	Toshiba Co.	25 ms	300	[2]
2013	Yu et. al.	UCAC	12 ms	200	[3]
2004	Meneghesso et. al.	Università di Padova	1 ms	10	[4]
2010		Agilent (B1505A)	500 μs	100	[5]
2010	Medjdoub et. al.	IMEC	400 ns	50	[6]
2009	Saadat et. al.	MIT	200 ns	10	[7]
This work			300 ns	250	

3.3.1 Gate-lag measurements

The gate voltage (V_{GS}) was switched from an off state (V_{GS}=-5 V, below the threshold voltage of -3.7 V) to an on state for each constant drain voltage (V_{DS}) in pulsed *I-V* characterizations as shown in Fig. 3.12. The on-state V_{GS} was varied 1 to -3 V and V_{DS} was also measured up to 20 V with a fixed R_L=100 Ω. The on-state duration time (t_{on}) and the off-state duration time (t_{off}) were fixed at 1 μs and 10 ms, respectively, to eliminate the influence of device self-heating effect.

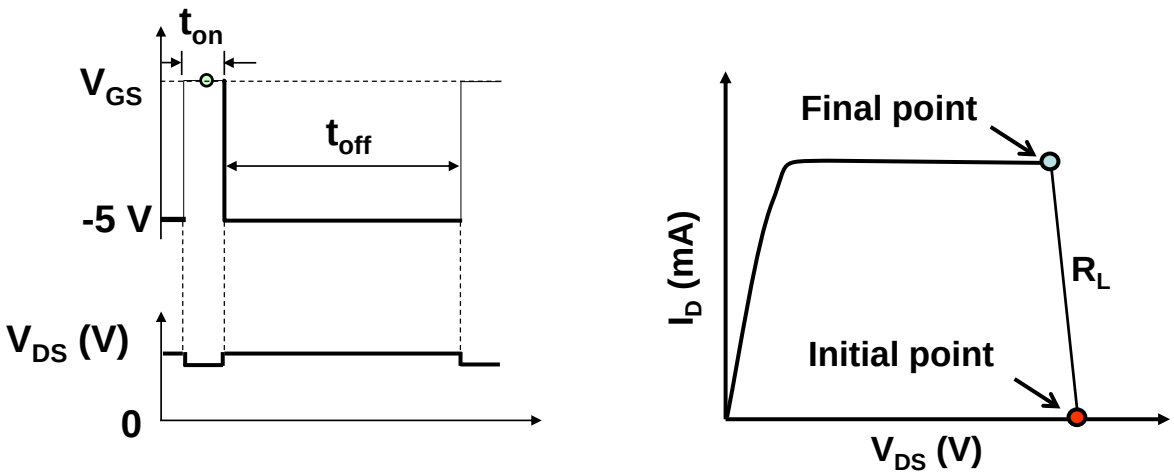


Fig. 3.12. Pulsed condition for gate-lag measurements.

3.3.2 Current collapse measurements

Characterization of the dynamic R_{on} was carried out by on-wafer pulsed measurements, where the V_{GS} was switched from off-state (V_{GS}=-5 V, below the threshold voltage of -3.7 V) to on-state (V_{GS}=1 V), while applying a V_{DS} up to 200 V. The R_L was connected in series with the tested device and was adjusted so that R_{on} was reasonably measured in the linear region, i.e., below 1/4 of the maximum drain current. The t_{on} and t_{off} were fixed at 1 μs and 10 ms, respectively. The transient output current was measured by a current probe (LeCroy CP030). Figure 3.13 shows pulsed biasing condition for current collapse measurements. Current collapse is a phenomenon; however it was numerically expressed in this work. Figure 3.14 shows the definition of current collapse. The current collapse was defined by normalized dynamic R_{on}, where the R_{on} value measured at t_{on}=1 μs and was normalized by

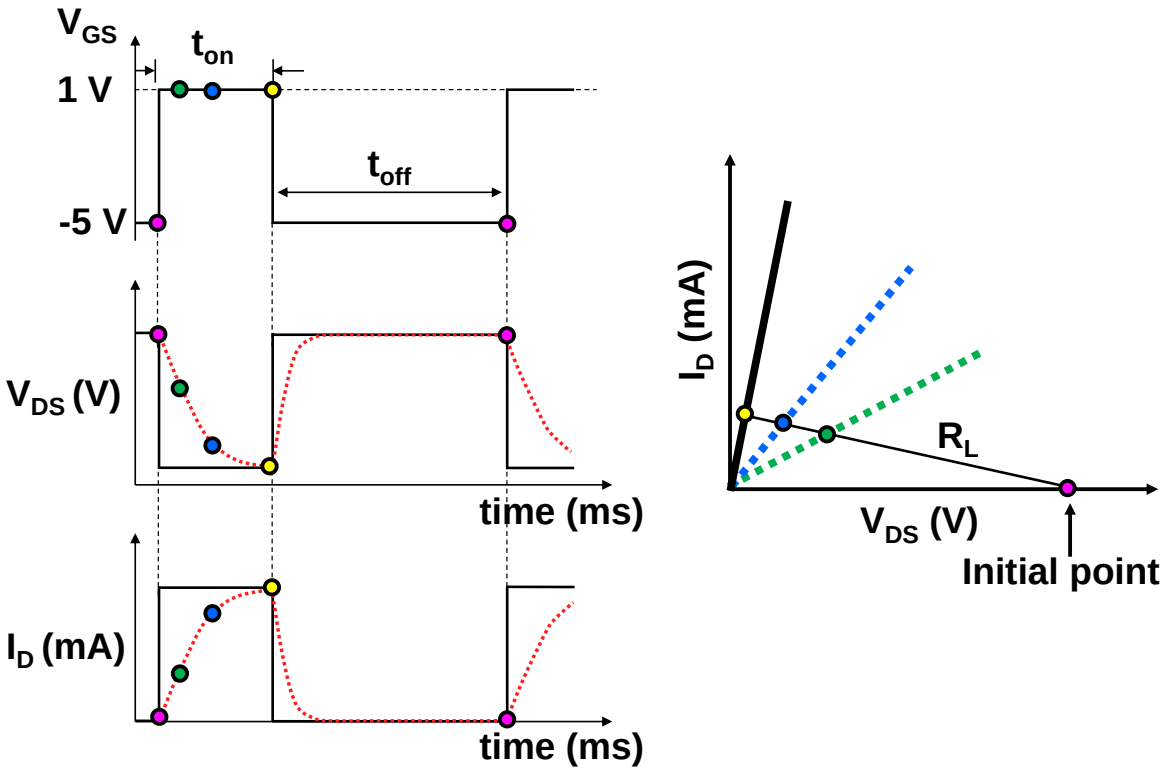


Fig. 3.13. Pulsed condition for current collapse measurements.

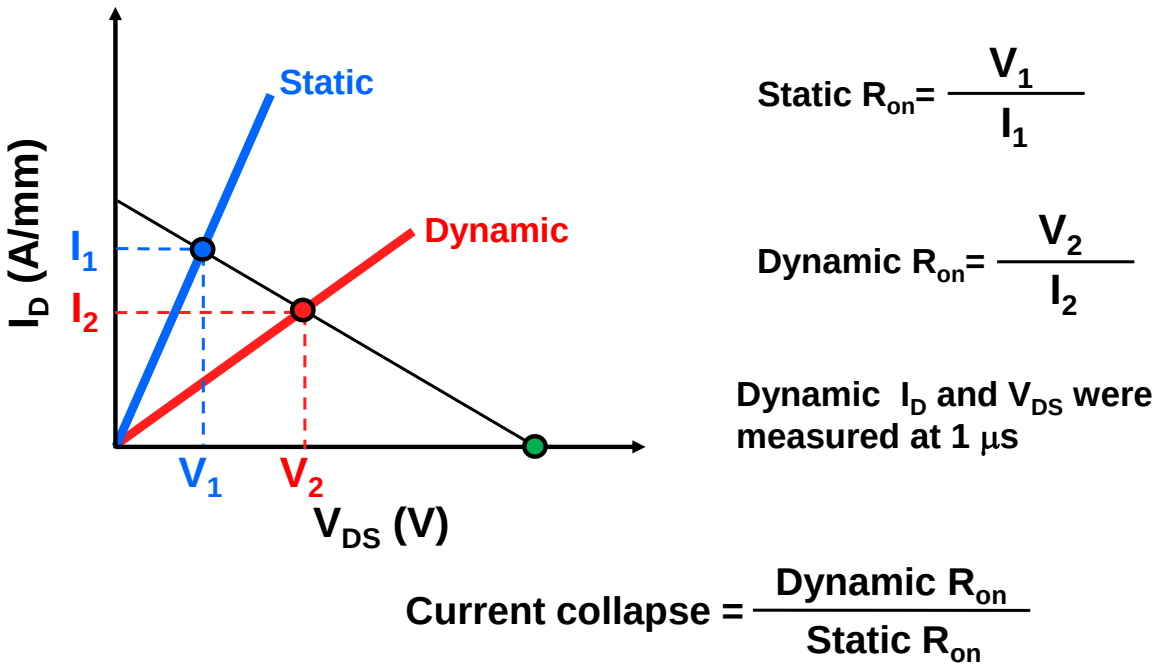


Fig. 3.14. Definition of current collapse.

its static value. Figure 3.15 shows time-dependent drain output waveforms, which was measured with a constant R_L of 15 kΩ at V_{DS}=200 V. Although the drain current waveform exhibited an oscillatory response in the early stage (up to 200 ns), our setup was able to stably measure the drain current response with a minimum measurement time of 300 ns. The measurement accuracy of on-state current was about ±0.03 mA and that of voltage was less than ±0.1 V.

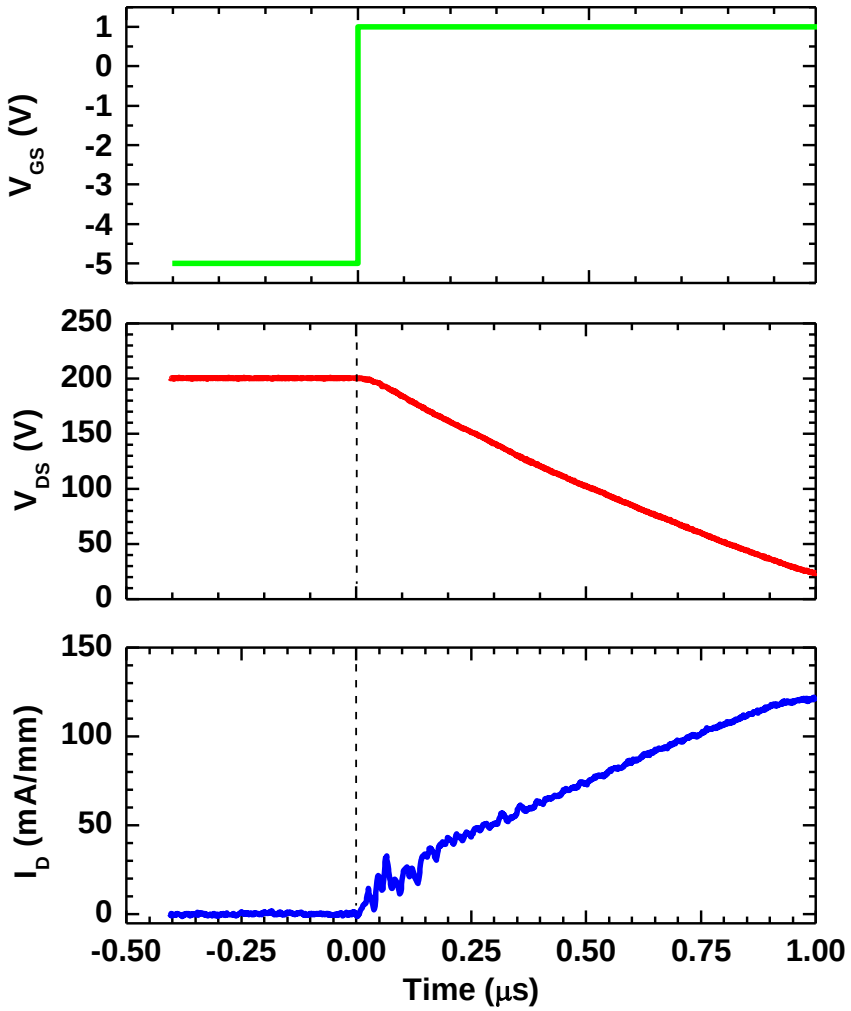


Fig. 3.15. Input gate voltage and output drain transients of AlGaN/GaN HEMT. Pulsed mode is operated with 15 kΩ load line with off-state V_{DS} of 200 V.

References

[1] Z. Tang, S. Huang, Q. Jiang, S. Liu, C. Liu, and K. J. Chen, “High-voltage (600-V) low-leakage, low-current-collapse AlGaN/GaN HEMTs With AlN/SiN_x passivation, IEEE Electron Devices Lett., vol. 34, no. 3, pp. 366-69, March 2013.

[2] W. Saito, Y. Kakiuchi, T. Nitta, Y. Saito, T. Noda, H. Fujimoto, A. Yoshioka, T. Ohno, and M. Yamaguchi, “Field-plate structure dependence of current collapse phenomena in high-voltage GaN-HEMTs, IEEE Electron Devices Lett., vol. 31, no. 7, pp. 659-61, July 2010.

[3] G. Yu, Yue W., Y. Cai, Z. Dong, C. Zeng, and B. Zhang, “Dynamic characterizations of AlGaN/GaN HEMTs with field plates using a double-gate structure, IEEE Electron Devices Lett., vol. 34, no. 2, pp.217-19, Feb. 2013.

[4] G. Meneghesso, G. Verzellesi, R. Pierobon, F. Rampazzo, A. Chini, U.K. Mishra, C. Canali, and E. Zanoni, "Surface-related drain current dispersion effects in AlGaN-GaN HEMTs," IEEE Trans. on Electron Devices, , vol. 51, no. 10, pp. 1554-1561, 2004.

[5] http://www.home.agilent.com/en/pd-1480796-pn-B1505A/power-device-analyzer-curve-tracer?cc=US&lc=eng

[6] F. Medjdoub, J. Derluyn, K. Cheng, M. Leys, S. Degroote, D. Marcon, D. Visalli, M. Van Hove, M. Germain, and G. Borghs, “Low on-resistance high-breakdown normally off AlN/GaN/AlGaN DHFET on Si substrate, IEEE Electron Devices Lett., vol. 31, no. 2, pp.111-13, Feb. 2010.

[7] O. I. Saadat, J. W. Chung, E. L. Piner, and T. Palacios, “Gate-first AlGaN/GaN HEMT technology for high-frequency applications, IEEE Electron Devices Lett., vol. 30, no. 12, pp. 1254-56, Feb. 2009.

Chapter 4
Effects of surface-passivation film on current collapse

4.1 Introduction

AlGaN/GaN high-electron-mobility transistors (HEMTs) are, nowadays, major interest for their high-power performance capabilities [1-3]. However, current collapse is the prime issue which limits power-switching performances in AlGaN/GaN HEMTs [4-11]. Various techniques have been reported as an effective approach to suppress current collapse, such as surface passivation and surface charge control with GaN cap layer [12-17]. Saadat et al. reported that AlGaN/GaN HEMTs passivated with Al_2O_3 exhibited the reduction in drain current when the on-state gate pulse times was changed from 200 ns to 1 ms [18]. Evidently, no detail explanation has been made to date regarding reduction in drain current of AlGaN/GaN HEMTs with increasing on-state gate pulse time. In order to improve the output power and switching performance of AlGaN/GaN HEMTs, understanding and proper inclusion of drain current dispersion effects are very essential.

In this chapter, drain current dispersion has been studied for AlGaN/GaN HEMTs passivated with SiN and those of Al_2O_3. A fixed drain voltage (V_{DS}) was applied to the drain, while the gate is pulsed from off state to different on state values, where 100 Ω load resistance (R_L) was connected in series with tested devices. The static and pulsed current-voltage (*I-V*) characteristics were measured. Drain current transients were measured to

analyze the influence of surface passivation in AlGaN/GaN HEMTs. The mechanism has been proposed to explain drain current dispersion in AlGaN/GaN HEMTs. Effects of SiN-deposition temperature and post-annealing temperature on dynamic on-resistance (R_{on}) have also been studied.

4.2 Device *I-V* characteristics

4.2.1 Static *I-V* characteristics

The static current-voltage (*I-V*) characteristics were measured for all the devices. All the devices were measured at room temperature and in the dark. Essentially the same static characteristics have been measured for devices passivated with SiN and those of Al_2O_3, as shown in Figs. 4.1 (a) and (b). Devices exhibited a maximum drain current (I_{Dmax}) of 376 mA/mm, measured at a gate voltage (V_{GS}) of 1 V, with a static R_{on} of 10.5 Ωmm. The threshold voltage was -3.8 V, which was defined as the gate bias at a drain current of 1 μA/mm.

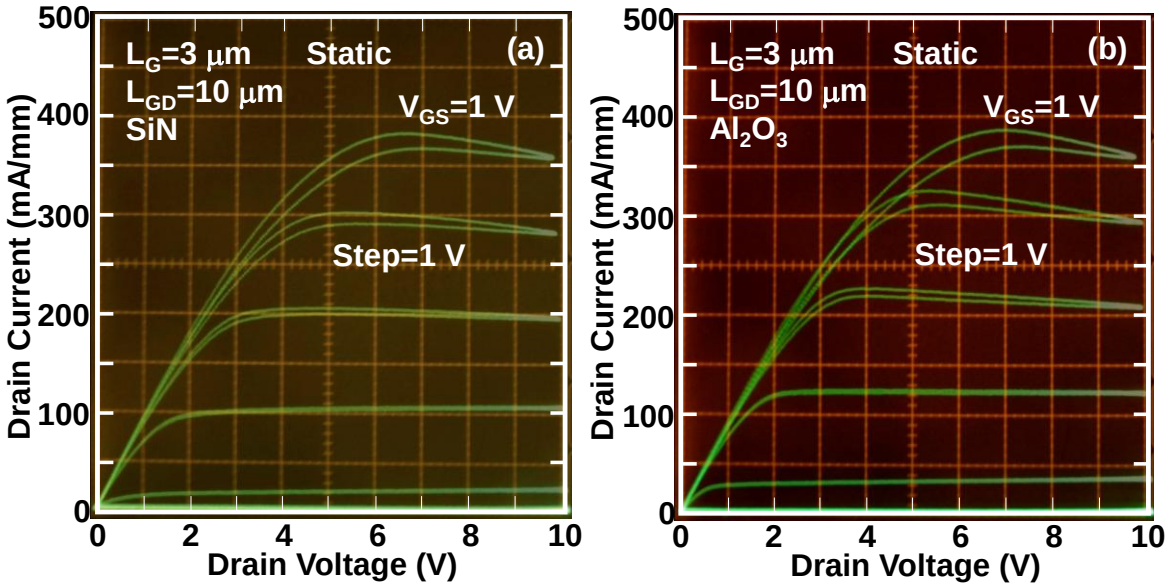


Fig. 4.1. Static current-voltage of devices passivated with (a) SiN and (b) Al_2O_3.

4.2.2 Pulsed *I-V* characteristics

Figure 4.2 shows the pulsed *I-V* characteristics of fabricated devices, which were also measured at room temperature and in the dark. A fixed V_{DS} was applied to the drain, whereas the V_{GS} was pulsed from off state (V_{GS}=-5 V) to different on state values. The on-state duration time (t_{on}) was fixed at 1 μs, while the gate was kept in the off state for 10 ms in order to allow a constant trapping time, as shown in Fig. 4.2 (a). Devices exhibited I_{Dmax} of 473 mA/mm and 165 mA/mm for devices passivated with SiN and those of Al_2O_3, respectively, as shown in Fig. 4.2 (b) and (c). The measured static and pulsed *I–V* curves were quite different by changing passivation film on the AlGaN surface of devices. The I_{Dmax} at V_{GS}=1 V provided by devices passivated with SiN in pulsed measurements was higher about 25% with respect to that of static measurements, whereas it was observed lower by about 56% for devices passivated with Al_2O_3. These results indicate that those discrepancies

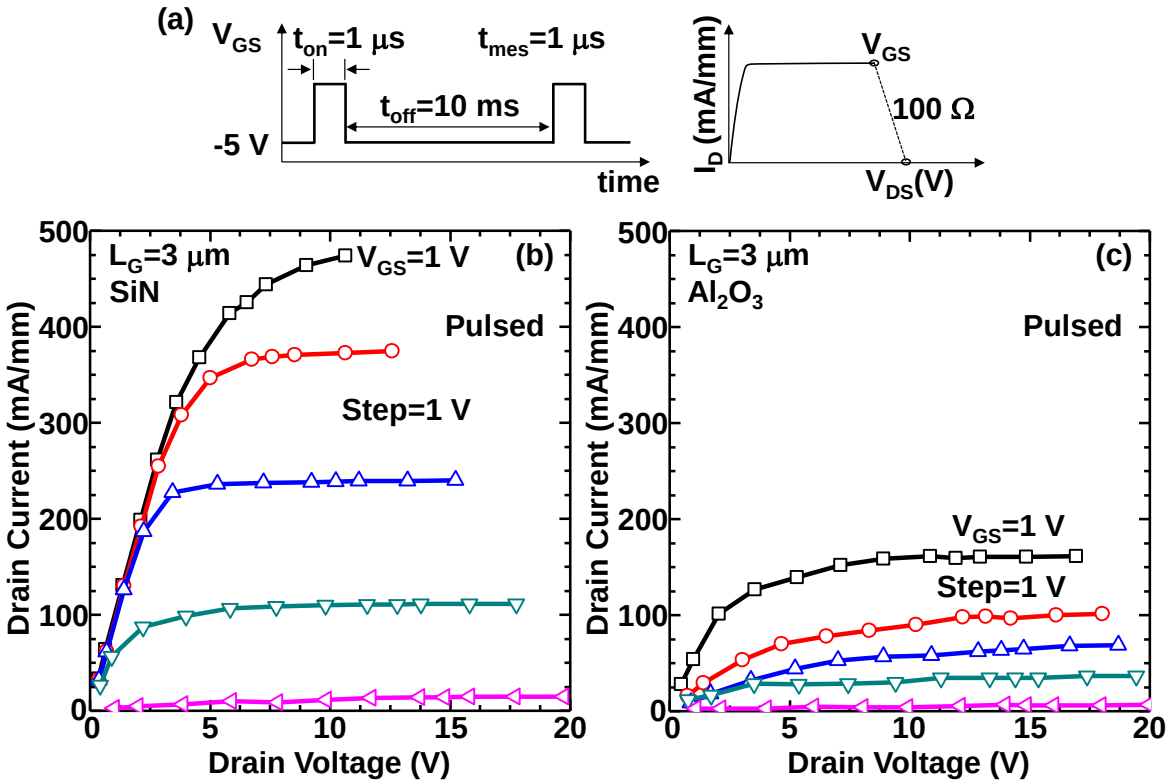


Fig. 4.2. (a) Timing diagram of gate pulsed voltage, which is operated with 100 Ω load line. Pulsed current-voltage characteristics of AlGaN/GaN HEMTs with (b) SiN and (c) Al_2O_3 passivation films.

are due in part to trapping effects. The responsible trapping centers could be located in several regions, including the AlGaN surface, the AlGaN barrier layer, and the GaN buffer layer. Drain transients were analyzed to clarify trapping mechanisms.

4.3 Drain current transients

Time-dependent drain current (I_D) was measured with a quiescent bias (V_{GSq}, V_{DSq}) = (-5, 20) V for both passivated devices, as shown in Fig. 4.3. Figure 4.3 (a) shows I_D dependence on t_{on} with a fixed t_{off}=10 ms. The I_D was decreased up to t_{on}=10 μs and here after it was increased with increasing t_{on} for Al_2O_3 passivated devices. On other hand, SiN passivated devices exhibited only decrease of I_D with increasing t_{on}. The decrease of I_D with t_{on} could not be explained by the device self-heating due to small on-state duration with long enough t_{off} for both passivated devices. Next the t_{on} was kept constant and t_{off} was varied up to 1 sec. Figure 4.3 (b) shows the I_D dependence on t_{off} with a fixed t_{on}=1 μs, where the I_D was measured at 1 μs. For SiN passivated devices, the I_D was increased up to t_{off}=100 μs and here after it was almost constant with increasing t_{off}. However, the I_D was decreased up to t_{off}=10 ms and was almost constant over t_{off}=10 ms for Al_2O_3 passivated devices. These results indicate that the increase of I_D is associated with emission of captured electrons, whereas the decrease of I_D is concomitant with capturing of electrons into traps. Devices passivated with Al_2O_3 exhibited very seriously degraded I_D response with a long recovery time (more than 1 sec) before steady state condition was reached (see Fig. 4.3 (a)), while the I_D recovery was faster (around 100 μs) for devices passivated with SiN (see Fig. 4.3 (b)). These results suggest that there are at least two distinct mechanisms, which dominate I_D transients at short times and at long times. The long time transients are associated with conventional traps. The short time transients are associated with a different mechanism and both devices suffer from it. This suggests that they might be associated with an intrinsic aspect of the heterostructure.

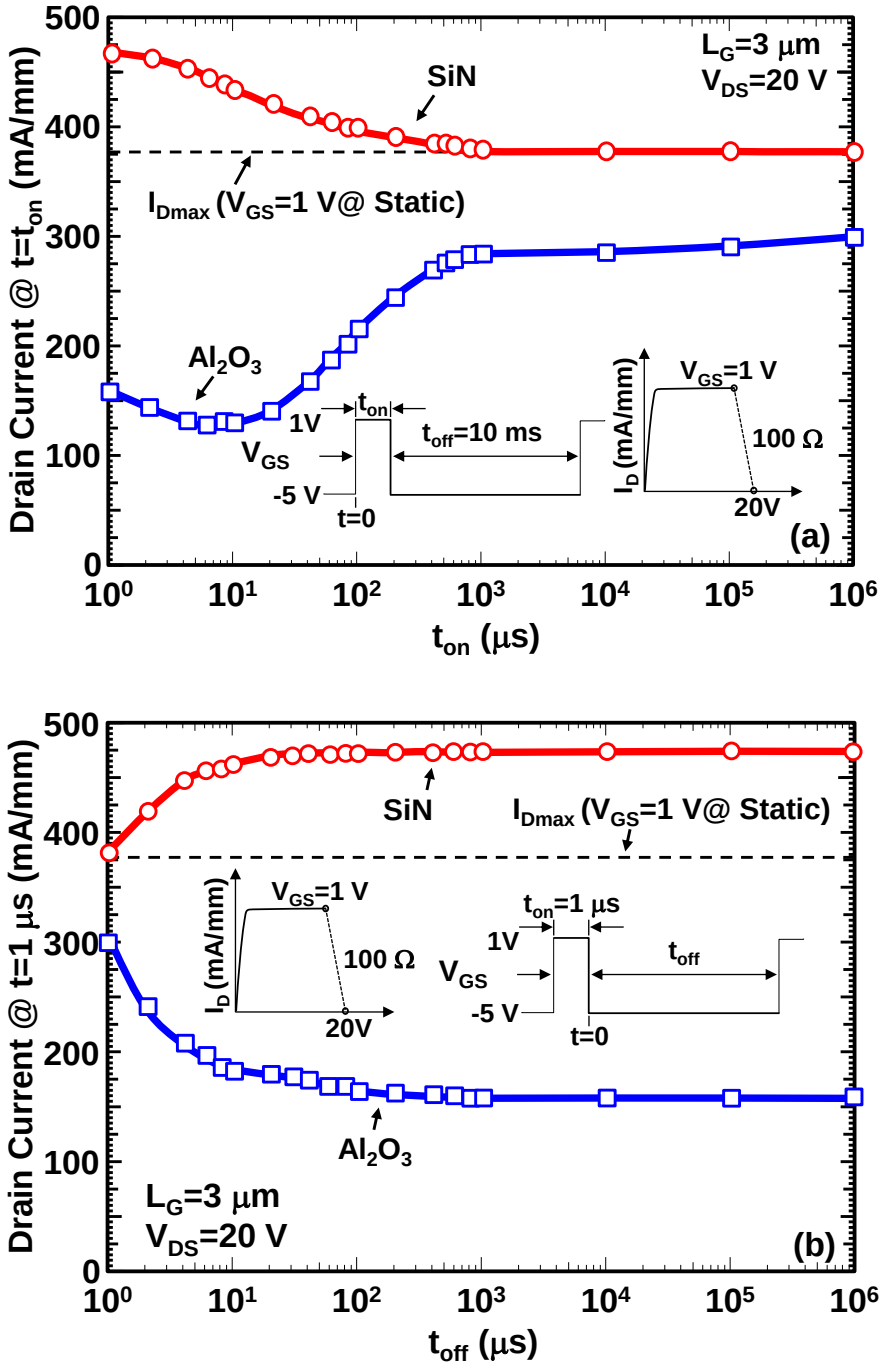


Fig. 4.3. Dependence of drain current responses on (a) t_{on} and (b) t_{off} for devices passivated with SiN and those of Al_2O_3. Pulsed mode is operated with 100 Ω load line with off-state drain bias voltage of 20 V. Insert of Figs. (a) and (b) show pulsed sequence. Dotted line shows the maximum drain current level at static condition for both passivated devices.

The leakage current is reasonably responsible for capturing of electrons during off state. Figure 4.4 shows the two-terminal gate-to-drain leakage current as a function of gate-to-drain voltage (V_{GD}). SiN passivated devices showed one order of magnitude small leakage current as compared to that of Al_2O_3 passivated devices at V_{GD}=-70 V. These results indicate that during off state, the rate of electron capture at the passivation/AlGaN interface is higher for Al_2O_3 passivated devices as compared to SiN passivated devices.

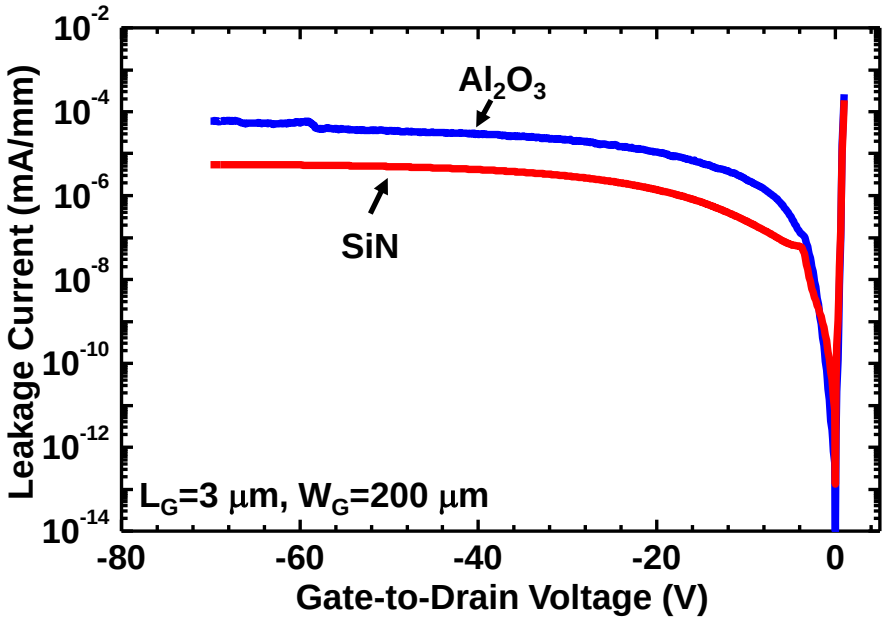


Fig. 4.4. Two-terminal gate-to-drain leakage current as a function of gate-to-drain voltage for devices passivated with SiN and those of Al_2O_3.

4.4 Mechanism of drain current dispersion

Figure 4.5 shows the schematic diagram of device operations under on and off states for AlGaN/GaN HEMTs passivated with SiN and those of Al_2O_3. During off state, channel 2DEG electrons are fully depleted under the gate (see Figs. 4.5 (a) and (b)). Due to strong reverse electric fields applied between gate and drain during off state, electrons are injected from the gate edge as leakage currents and are assumed to be trapped at the passivation/AlGaN interface. The electron trap density is assumed low for SiN passivated devices as compared to that of Al_2O_3 passivated devices. Those trapped electrons contribute to partly deplete channel 2DEG electrons near the gate edge in the drain side. Next the gate

voltage is switched to on state (V_{GS}=1 V), resulting in quick generation of electron accumulation under the gate (see Figs. 4.5 (c) and (d)). However, emission of captured electrons does not occur within a short period of time (i.e., less than 10 μs). Hence it takes rather a long time before steady state condition is reached for Al_2O_3 passivated devices (see Figs. 4.5 (c) and (a)). On the other hand, the I_D was observed to decrease at initial short period of on-state duration time, which could not be explained by emission of captured electrons. Similar decrease of I_D was observed for SiN passivated devices (see Fig. 4.3 (a)). Therefore, these short time transients might be associated with an inherent characteristic of

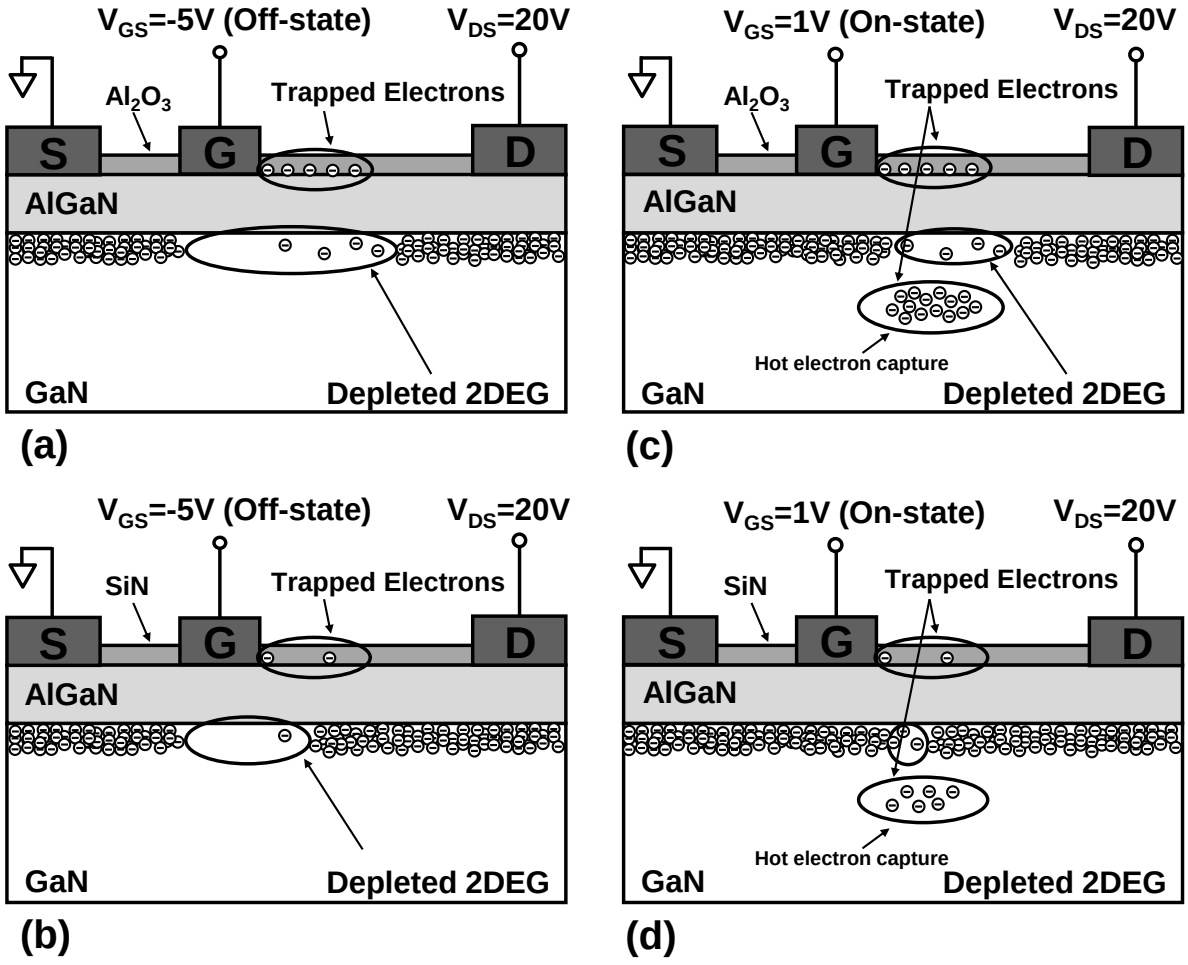


Fig. 4.5. Schematic diagrams of device operation for AlGaN/GaN HEMTs. (a) Device under off state with Al_2O_3 passivated device, (b) device under off state with SiN passivated device, (c) device under on state Al_2O_3 passivated device, and (d) device under on state with SiN passivated device.

the heterostructure. During on state, there is a high possibility for capturing of hot electrons due to strong horizontal electric field. This leads to decrease of 2DEG electrons, resulting in decrease of I_D. The measured drain transients indicate that the decrease of I_D is observed due to capturing of hot electrons in buffer layer, as shown in Figs. 4.5 (c) and (d). However, these measured results cannot conclusively rule out the possibility that capturing of hot electrons in AlGaN layer. Typically, high density of trap charges is located in GaN buffer. It is believed that trap charge density in GaN buffer is much higher than that of AlGaN layer due to improvement of epitaxial growth technology. Therefore, it is reasonably concluded that GaN buffer layer is one of the source of traps to capture electron during on state, leading to decrease of I_D in AlGaN/GaN HEMTs. In addition, the reduction amount of I_D was higher at t_{on}=10 μs for devices passivated with SiN as compared to that of devices passivated with Al_2O_3, as shown in Fig. 4.3 (a).

4.5 Load line: from gate-lag to current collapse

Figure 4.6 shows the load line effect on current collapse with different off-state V_{DS}. The R_L was varied from 100 to 5000 Ω for change the on-state applied V_{DS}. During on state, the

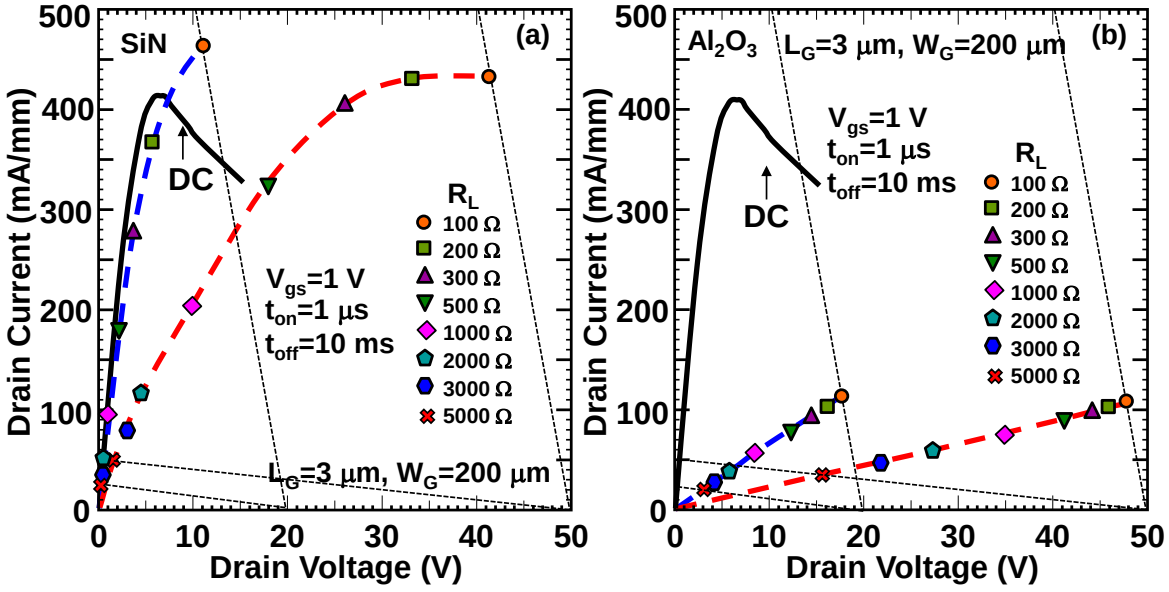


Fig. 4.6. Effect of load line on current collapse with different off-state drain voltage for (a) devices passivated with (a) SiN and (b) Al_2O_3.

horizontal electric field is high for gate lag measurements, while it is comparatively low for current collapse measurements. Therefore, during on state, electrons are captured in buffer traps for high horizontal electric field, leading to decrease of I_D. During off state, leakage current was increased with increasing V_{DS}. Thus, more electrons were captured into passivation/AlGaN interface traps. These lead to increase dynamic R_{on}, as shown by red dotted line in both Figs. 4.6 (a) and (b). These results suggest that high off-state V_{DS} is essential to evaluate the switching performance of AlGaN/GaN HEMTs.

4.6 SiN-deposition temperature

Four types of devices were fabricated having SiN passivation film with different deposition temperatures, i.e., 100, 150, 200, and 250°C for controlling the AlGaN surface condition. SiN was deposited by sputtering with a thickness of 150-nm. Essentially the same static characteristics have been measured for devices regardless of SiN-deposition temperatures. All the devices were measured at room temperature and in the dark. The I_{Dmax} defined at V_{GS}=1 V was around 440 mA/mm. Table I shows summary of device characteristics with different SiN-deposition temperatures (T_{depo}). The leakage current was reduced with increasing T_{depo}. Next dynamic characteristics have been studied for power switching applications.

Table I Summary of device characteristics with different SiN-deposition temperatures.

SiN-deposition temperature	I_{Dmax} @V_{GS}=1V	R_{on} @V_{GS}=1V	V_T	gm_{max}	I_{leak} @V_{GD}=-200V	V_{BR} @I_D=0.1 mA/mm
(ºC)	(mA/mm)	(Ωmm)	(V)	(mS/mm)	(mA/mm)	(V)
100	420	10.4	-3.8	110	2.2×10^{-4}	500
150	420	9.6	-3.8	112	0.8×10^{-4}	500
200	422	9.7	-3.8	114	0.3×10^{-4}	510
250	420	9.5	-3.8	117	0.2×10^{-4}	500

4.6.1 Dynamic on-resistance

A critical requirement in power electronics is obtaining a very low R_{on} immediately after switching from an off state with high voltage to an on state with low voltage. In AlGaN/GaN HEMTs, power switching problems are major issues [19-24]. Therefore, it is very essential to understand the dynamic performance of AlGaN/GaN HEMTs. In this work, the dynamic R_{on} has measured for different SiN-deposition temperatures. Characterization of the dynamic R_{on} was carried out by on-wafer pulsed measurements, where the V_{GS} was switched from an off state (V_{GS}=-5 V, below the threshold voltage of -3.8 V) to an on state (V_{GS}=1 V), while applying a V_{DS} up to 100 V. The R_L was connected in series with the tested device and was adjusted so that R_{on} was reasonably measured in the linear region, i.e., below 1/4 of the I_{Dmax}. In order to fill all traps (i.e., SiN/AlGaN interface traps) by electrons, the t_{off} was varied with a fixed t_{on} of 1 μs. To represent the magnitude of current collapse quantitatively, we have defined the current collapse, where the R_{on} value measured at t_{on}=1 μs was normalized by its static value. Figure 4.7 shows current collapse as a function of off-state duration time. Current collapse was almost constant over t_{off} = 100 μs. Thus, the t_{off} was fixed at 10 ms for further dynamic R_{on} measurements. Figure 4.8 shows dependence of R_{on} on T_{depo}. The R_{on} was decreased with increasing T_{depo}. The reduction amount of R_{on} was larger for pulsed measurements as compare that of static measurements. The R_{on} is expressed as

$$R_{on} = 2R_C + R_S + R_{CH} + R_D, \qquad (4.1)$$

where, R_C is the source and drain contact resistance, R_S is the parasitic source resistance, R_{CH} is the channel resistance, and R_D is the parasitic drain resistance. Since, devices were fabricated on same wafer and cut into four pieces for deposition of SiN with different temperatures, R_C and R_S were same for all devices. The increase of R_{on} may be brought from R_{CH} and R_D. If traps exist between gate and drain, there is a possibility to increase of both R_{CH} and R_D. In addition, GaN buffer layer was same for all devices and only AlGaN surface condition was changed. Therefore, the effects of GaN buffer traps on increase of dynamic R_{on} are negligible as compared to those of AlGaN surface traps.

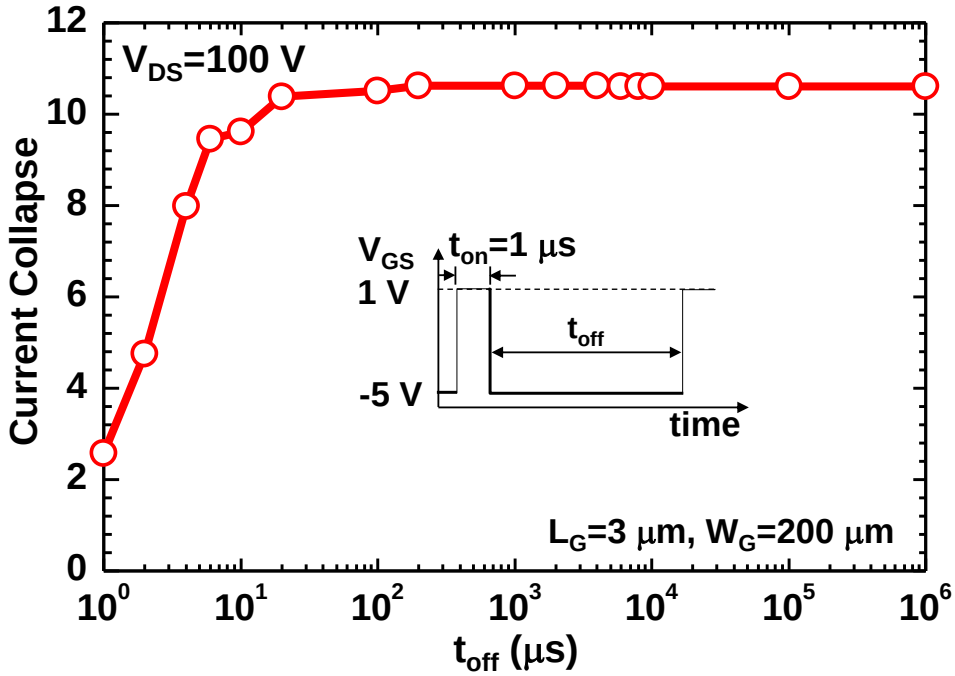


Fig. 4.7. Current collapse as a function of off-state duration time (t_{off}) with a fixed t_{on}=1 μs.

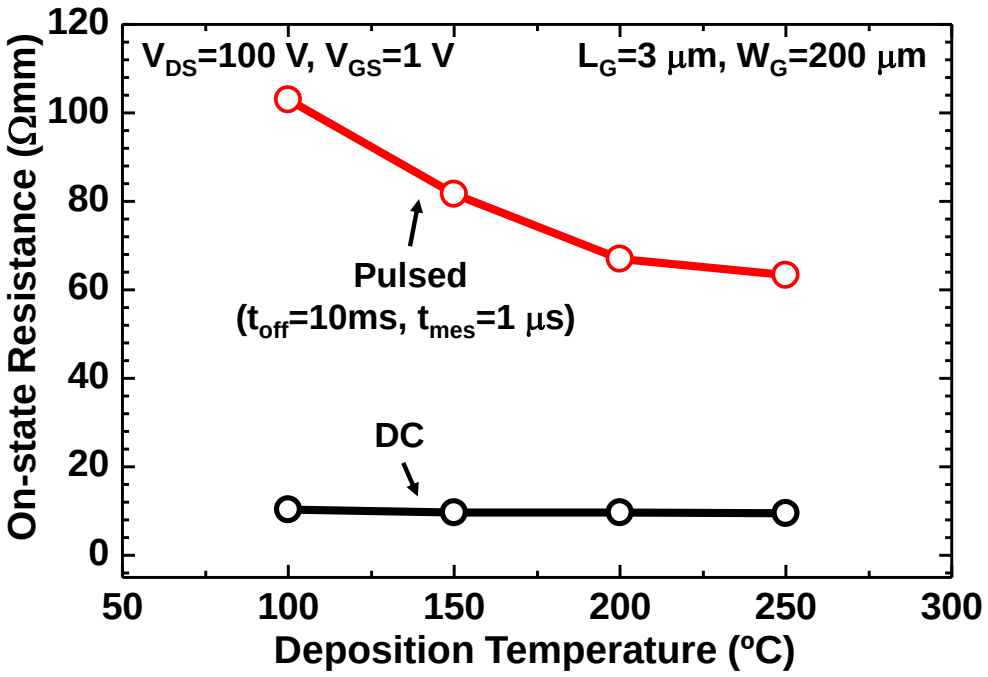


Fig. 4.8. On-state resistance vs. SiN-deposition temperature.

Figure 4.9 shows current collapse as a function of T_{depo} with different off-state V_{DS}. Devices with high V_{DS} showed large current collapse due to increase of horizontal fields between gate and drain. Current collapse was reduced with increasing T_{depo} from 100 to 250ºC at V_{DS}=100 V. These results indicate that the trap density is reduced with increasing T_{depo}.

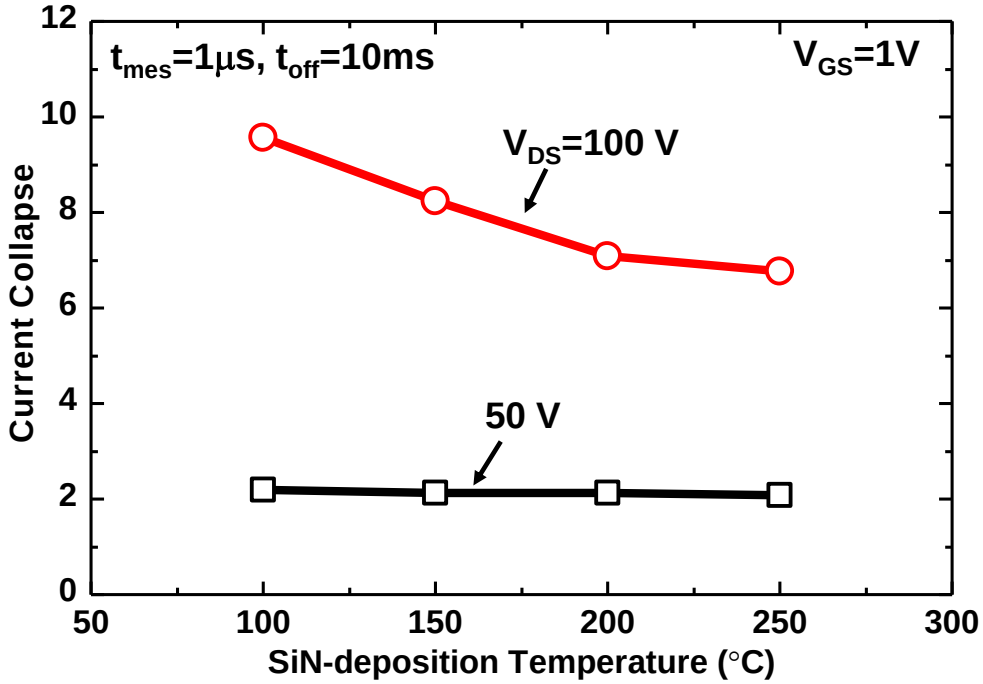


Fig. 4.9. Current collapse as a function of SiN-deposition temperature.

4.6.2 Time dependent current collapse

Figure 4.10 shows dependence of current collapse on on-state measuring time (t_{mes}) with different T_{depo}. The current collapse was decreased with increasing t_{mes} for a fixed t_{off} of 10 ms. Devices with T_{depo}=100ºC showed longer recovery time as compared to that of devices with T_{depo}=250ºC. During off state, electrons were assumed to be injected from gate to AlGaN surface defects near the gate edge of a drain side under a large surface electric field. When device switched from off state to on state, it took long time to emit trapped electrons. Thus, devices exhibited increased dynamic R_{on}. These results indicate that the emission time constant is longer for SiN passivation with low T_{depo}, suggesting that deeper traps are responsible for devices with low T_{depo} SiN.

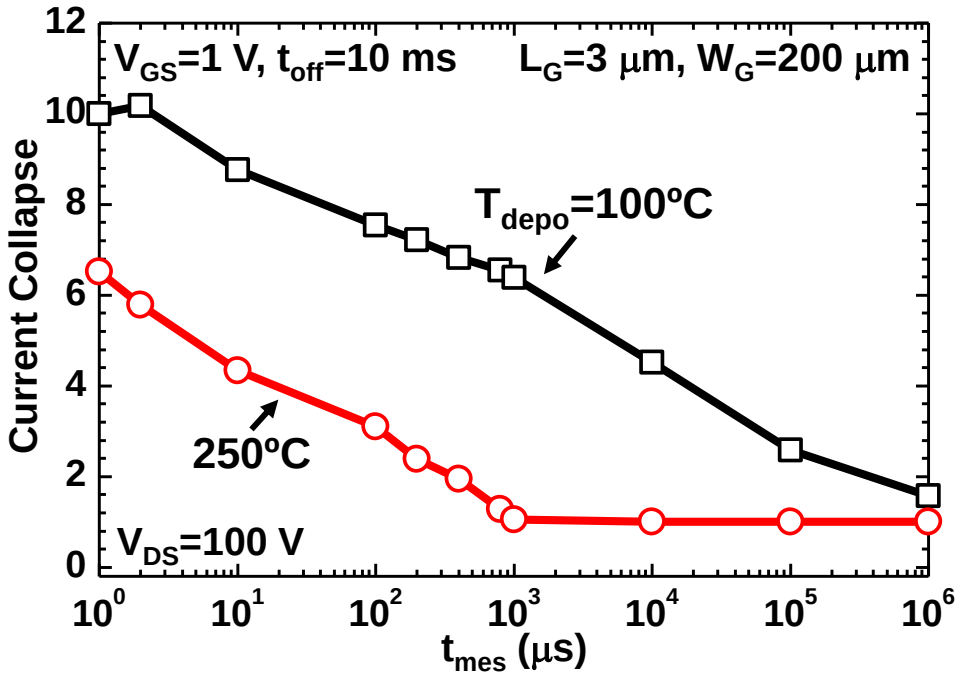


Fig. 4.10. Dependence of current collapse on on-state measurement time (t_{mes}).

4.7 Post-annealing temperature

Annealing effects on Schottky contacts in AlGaN/GaN heterostructures have been frequently reported by showing improvement in electrical properties such as reduction of reverse leakage current, improvement of Schottky barrier height, and breakdown voltage [25-32]. Miura et al. proposed that annealing process could reduce interface traps between metal and AlGaN or form the island-like Ni oxide, leading to reduction in leakage current [26-27]. Many works of annealing effects on AlGaN/GaN Schottky diodes have been reported so far in terms of surface/interface states using electrical characterization. Physical changes by post-annealing are expected: the modification of Schottky metal/AlGaN interface and the AlGaN surface states. Both cases affect trapping activities of surface/interface states, e.g., trap assisted tunneling [25, 33] as a leakage current mechanism, and surface trapping as virtual gate formation causing current dispersion [7]. In order to reduce current collapse, post-annealing has been performed.

Post-annealing temperature was varied from 300 to 500°C. It was performed for 10 min in N_2 chamber. Figure 4.11 shows the effect of post-annealing temperature on current collapse with different off-state V_{DS}. Current collapse was reduced with increasing post-annealing temperature. These results indicate that the SiN/AlGaN interface is re-constructed (i.e., reduce oxygen vacancies) by post-annealing temperature, leading to decrease of interface trap density. Figure 4.12 shows dependence of current collapse on SiN-deposition temperature with different post-annealing temperatures. The effect of post-annealing temperature on current collapse was comparatively low for devices with T_{depo}=250°C. The gate leakage current of annealed devices was reduced by one order of magnitude as compared to virgin devices, as shown in Fig. 4.13. The suppression of gate leakage current could be described on the basis of AlGaN surface phenomena. During the growth of AlGaN/GaN heterostructure, oxygen impurities are incorporated unintentionally. These

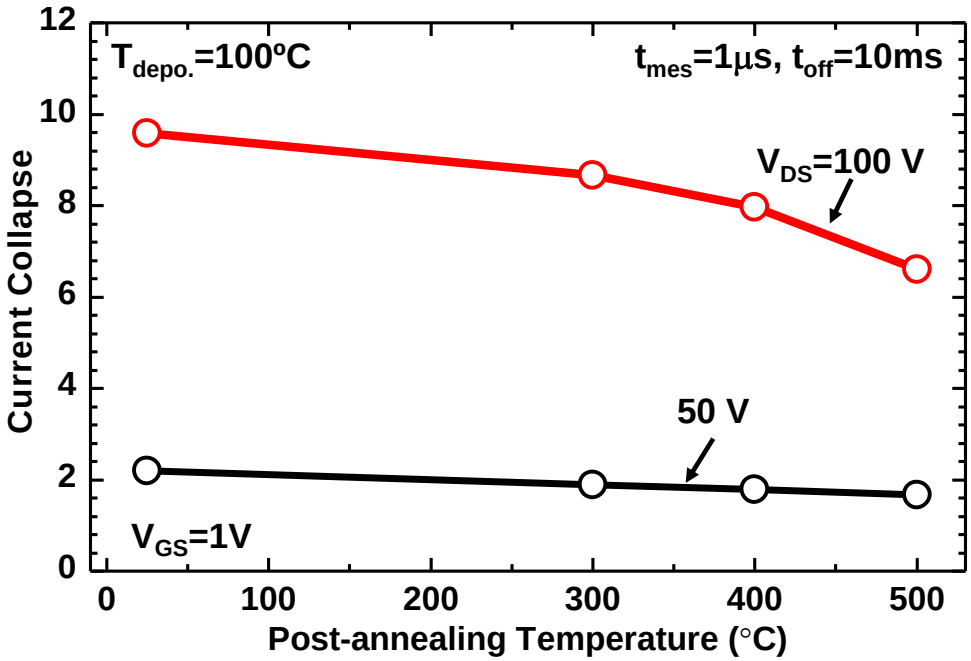


Fig. 4.11. Current collapse vs. post-annealing temperature.

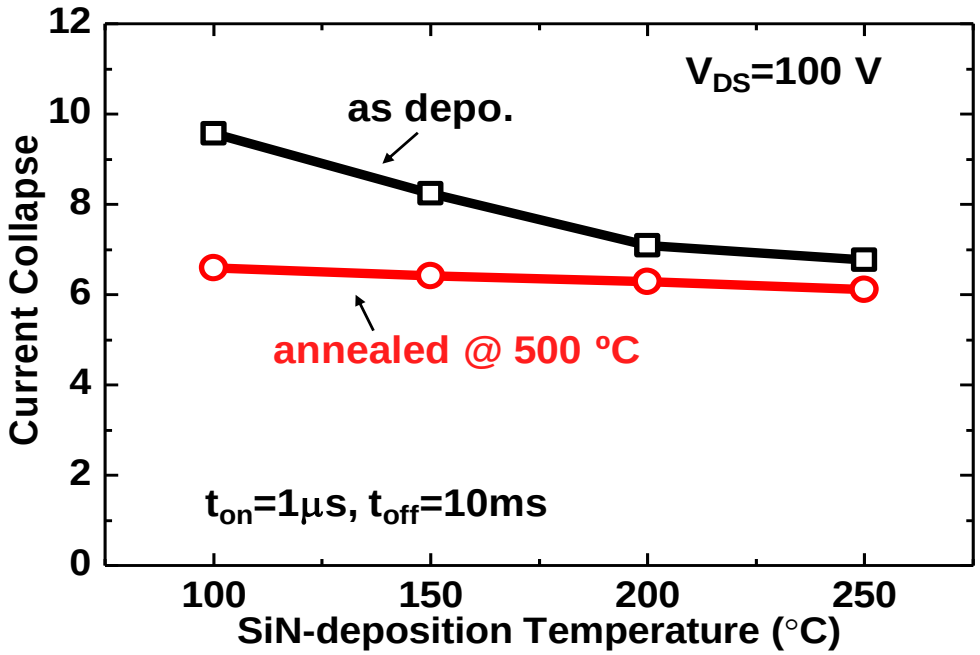


Fig. 4.12. Current collapse vs. SiN-deposition temperature with different post-annealing temperatures.

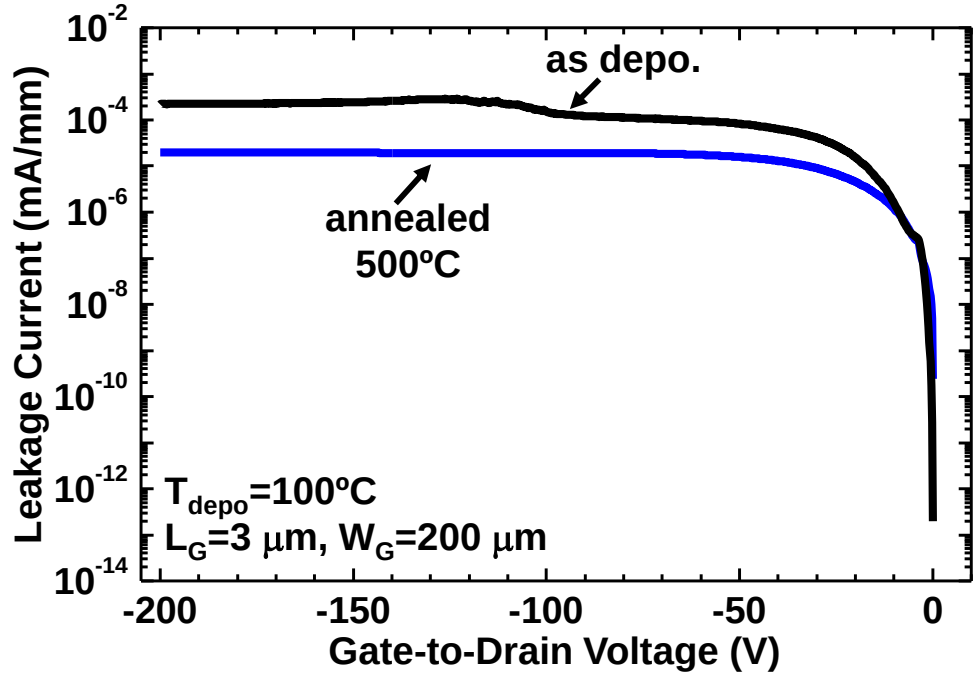


Fig. 4.13. Two-terminal gate-to-drain leakage current as a function of gate-to-drain voltage for devices with post-annealing effect.

oxygen impurities existing on the AlGaN surface lead tunneling transport at the Schottky/AlGaN interface. This tunneling transport is responsible for high gate leakage current. The presence of unintentional oxide impurities on the AlGaN surface is irresistible and the consequent high gate leakage is unavoidable. Therefore, the leakage current density could be reduced considerably by a high-temperature annealing.

4.8 Summary

This work has been investigated drain current dispersion effects in AlGaN/GaN HEMTs with different passivation films. The maximum drain current for SiN passivated devices was enlarged by around 25% at t_{on}=1 μs as compared to that of its static value, while it was reduced by around 56% for Al_2O_3 passivated devices. The drain current was decreased with increasing t_{on} and was increased with increasing t_{off} for SiN passivated devices, while Al_2O_3 passivated devices exhibited vice versa. These results indicate that the trap density at Al_2O_3/AlGaN is comparatively higher than that of SiN/AlGaN. Both passivated devices are suffered with buffer associated traps during on-state duration time.

The effect of SiN-deposition temperature on dynamic R_{on} has been investigated. Current collapse was decreased with increasing SiN-deposition temperature. It was also decreased with increasing post-annealing temperature. These results indicate that the SiN/AlGaN interface trap density is reduced with increasing the sputtered SiN-deposition and annealing temperatures.

From above discussion, it is reasonably concluded that since a low trap density exists at the SiN/AlGaN interface, current collapse is reduced due to deposition of SiN passivation on the AlGaN surface of devices. However, the suppression of current collapse is not enough for device applications. A new approach is very much essential for further reduction of current collapse. Therefore, field-plate structure has been proposed for more reduction of current collapse. The effect of gate-field plate on current collapse will be discussed in the next chapter.

References

[1] F. Benkhelifa, D. Krausse, S. Mueller, R. Quay, and M. Mikulla, "Al-GaN/GaN HEMTs for high voltage applications," in Proc. 5th Space Agency—MOD (ESAMOD) Round Table Workshop GaN Component Technol., Noordwijk, Netherlands, 2010.

[2] D. Maier, M. Alomari, N. Grandjean, J.-F. Carlin, M.-A. Diforte-Poisson, C. Dua, A. Chuvilin, D. Troadec, C. Gaquière, U. Kaiser, S. L. Delage, and E. Kohn, "Testing the temperature limits of GaN-based HEMT devices, "IEEE Trans. Device Mater. Rel., vol. 10, no. 4, pp. 427–436, Dec. 2010.

[3] Y. Ohno and M. Kuzuhara, "Application of GaN-based heterojunction FETs for advanced wireless communication", IEEE Trans Electron Devices, vol. 48, pp. 517-523, 2001.

[4] J. Everts, J. Das, J. van den Keybus, M. Germain, and J. Driesen, "GaN based power transistors for future power electronic converters," in Proc. IEEE Benelux Young Res. Symp., Leuven, Belgium, 2010.

[5] R. Chu, A. Corrion, M. Chen, R. Li, D. Wong, D. Zehnder, B. Hughes, and K. Boutros, "1200-V normally off GaN-on-Si field-effect transistors with low dynamic ON-resistance," IEEE Electron Device Lett., vol. 32, no. 5, pp. 632–634, May 2011.

[6] I. Daumiller, D. Theron, C. Gaquiere, A. Vescan, R. Dietrich, A. Wieszt, H. Leier, R. Vetury, U. K. Mishra, I. P. Smorchkova, N. X. Nguyen, and E. Kohn, "Current instabilities in GaN-based devices," IEEE Electron Device Lett., vol. 22, pp. 62–64, Feb. 2001.

[7] R. Vetury, N. Q. Zhang, S. Keller, and U. K. Mishra, "The impact of surface states on the dc and RF characteristics of AlGaN–GaN HFETs," IEEE Trans. Electron Devices, vol. 48, pp. 560–566, Mar. 2001.

[8] T. Kikkawa, M. Nagahara, N. Okamoto, Y. Tateno, Y. Yamaguchi, N. Hara, K. Joshin, and P. M. Asbeck,"Surface-charge controlled AlGaN–GaN power HFET without current collapse and g_m dispersion," in IEDM Tech. Dig., 2001, pp. 585–588.

[9] S. C. Binari, K. Ikossi, J. A. Roussos, W. Kruppa, D. Park, H. B. Dietrich, D. D. Koleske, A. E. Wickenden, and R. L. Henry, "Trapping effects and microwave power performance in AlGaN–GaN HEMTs," IEEE Trans. Electron Devices, vol. 48, pp.

465–471, Mar. 2001.

[10] E. Kohn, I. Daumiller, M. Kunze, M. Neuburger, M. Seyboth, T. J. Jenkins, J. S. Sewell, J. Van Norstand, Y. Smorchkova, and U. K. Mishra, "Transient characteristics of GaN-based heterostructure field-effect transistors," IEEE Trans. Microwave Theory Tech., vol. 51, pp. 634–642, Feb. 2003.

[11] B. M. Green, V. Tilak, V. S. Kaper, J. A. Smart, J. R. Shealy, and L. F. Eastman, "Microwave power limits of AlGaN–GaN HEMTs under pulsed-bias operation," IEEE Trans. Microwave Theory Tech., vol. 51, pp. 618–623, Feb. 2003.

[12] B. M. Green, K. K. Chu, E. M. Chumbes, J. A. Smart, J. R. Shealy, and L. F. Eastman, "The effect of surface passivation on the microwave characteristics of undoped AlGaN–GaN HEMTs,"IEEE Electron Device Lett., vol. 21, pp. 268–270, June 2000.

[13] A. V. Vertiatchikh, L. F. Eastman, W. J. Schaff, and T. Prunty,"Effect of surface passivation of AlGaN–GaN heterostructurefield-effect transistor," Electron. Lett., vol. 38, no. 8, pp. 388–389, 2002.

[14] G. Koley, V. Tilak, L. F. Eastman, and M. G. Spencer, "Slow transients observed in AlGaN HFETs: Effects of SiN passivation and UV illumination," IEEE Trans. Electron Devices, vol. 50, pp. 886–893, May 2003.

[15] V. Tilak, B. Green, H. Kim, R. Dimitrov, J. Smart, W. J. Schaff, J. R. Shealy, and L. F. Eastman,"Effect of passivation on AlGaN–GaN HEMT device performance," in Proc. IEEE Int. Symp. Compound Semiconductors, 2000, pp. 357–363.

[16] R. Coffie, D. Buttari, S. Heikman, S. Keller, A. Chini, L. Shen, and U. K. Mishra, "p-capped GaN-AlGaN–GaN high-electron mobility transistors (HEMTs),"IEEE Electron Device Lett., vol. 23, pp. 588–590, July 2002.

[17] A. Jimenez, D. Buttari, D. Jena, R. Coffie, S. Heikman, N. Q. Zhang, L. Shen, E. Calleja, E. Munoz, J. Speck, and U. K. Mishra, "Effect of p-doped overlayer thickness on RF-dispersion in GaN junction FETs," IEEE Electron Device Lett., vol. 23, pp. 306–308, Apr. 2002.

[18] Omair I. Saadat, Jinwook W. Chung, Edwin L. Piner, and Tomás Palacios, "Gate-first AlGaN/GaN HEMT technology for high-frequency applications." IEEE Electron Device Lett., vol. 30, pp.1254-56, Dec. 2009.

[19] H. Kambayashi, Y. Satoh, S. Ootomo, T. Kokawa, T. Nomura, S. Kato, and T.-S. P.

Chow, “Over 100 A operation normally-off AlGaN/GaN hybrid MOS-HEFT on Si substrate with high-breakdown voltage”, Solid-State Electron. Vol. 54, no. 6, June 2010.

[20] A. Nakajima, S. Yagi, M. Shimizu, K. Adachi, and H. Okumura, “Hot Electron Induced Current Collapse in AlGaN/GaN HEMTs”, Mater. Sci. Forum.556, 1035 (2007).

[21] Dimitris Pavlidis, Pouya Valizadeh, and S. H. Hsu, presented at the 13th GaAS Symposium-Paris, 2005.

[22] M. Tajima and T. Hashizume, “Impact of gate and passivation structures on current collapse of AlGaN/GaN high-electron-mobility transistors under Off-state-bias stress”, Jpn. J. Appl. Phys. Part 1, vol.50, p.061001, 2011.

[23] W. Saito, T. Nitta, Y. Kakiuchi, Y. Saito, K. Tsuda, I. Omura, and M. Yamaguchi, “Suppression of dynamic on-resistance increase and gate charge measurements in high-voltage GaN-HEMTs with optimized field-plate structure”, IEEE Trans. Electron Devices, vol. 54, no.8, pp. 1825-30, Aug. 2007.

[24] F. Medjdoub, J. Derluyn, K. Cheng, M. Leys, S. Degroote, D. Marcon, D. Visalli, M. Van Hove, M. Germain, and G. Borghs, “Low On-Resistance High-Breakdown Normally Off AlN/GaN/AlGaN DHFET on Si Substrate”, IEEE Electron Device Lett. vol. 31, no. 2, pp. 111-13, 2010.

[25] H. Kim, J. Lee, D. Liu, and W.Lu, "Gate current leakage and breakdown mechanism in unpassivated AlGaN/GaN high electron mobility transistors by post-gate annealing," Appl. Phys. Lett., vol. 86, p. 143505, 2005.

[26] N. Miura, T. Oishi, T.Nanjo, M. Suita, Y. Abe, T.Ozeki, H. Ishikawa, and T. Egawa, "Effects of interfacial thin metal layer for high-performance Pt-Au-based Schottky contacts to AlGaN-GaN," IEEE Trans. Electron Devices, vol. 51, pp. 297-303, Mar 2004.

[27] N. Miura, T. Nanjo, M. Suita, T. Oishi,Y. Abe, T. Ozeki, H.Ishikawa, T. Egawa, and T. Jimbo, "Thermal annealing effects on Ni/Au based Schottky contacts on n-GaN and AlGaN/GaN with insertion of high work function metal," Solid-State Electronics, vol. 48, pp. 689-695, May 2004.

[28] C. M. Jeon, H. W. Jang, and J. L. Lee, "Thermally stable Ir Schottky contact on

AlGaN/GaN heterostructure," Appl. Phys. Lett., vol. 82, pp. 391-393, Jan 2003.

[29] Y. K. Su, P. C. Chang, C. H. Chen, S. J. Chang, C. L. Yu, C. T. Lee, H. Y. Lee, J. Gong, P. C. Chen, and C. H. Wang, "Nitride-based MSM UV photo detectors with photo-chemical annealing Schottky contacts," Solid-State Electron., vol. 49, pp. 459-463, Mar 2005.

[30] J. Lee, D. Liu, H. Kim, and W. Lu, "Post processing annealing effects on direct current and microwave performance of AlGaN/GaN high electron mobility transistors," Appl. Phys. Lett., vol. 85, pp. 2631-33, 2004.

[31] S. Arulkumaran, T. Egawa, H. Ishikawa, M. Umeno, and T. Jimbo, "Effects of annealing on Ti, Pd, and Ni/n-$Al_{0.11}Ga_{0.89}N$ Schottky diodes," IEEE Trans. Electron Devices, vol. 48, pp. 573-580, 2001.

[32] H. Kim, J. Lee, and W. Lu, "Post-annealing effects on trapping behaviors in AlGaN/GaN HEMTs," physica status solidi (a), vol. 202, pp. 841-845, 2005.

[33] S. Karmalkar, D. M. Sathaiya, and M.S. Shur, "Mechanism of the reverse gate leakage in AlGaN/GaN high electron mobility transistors," Appl. Phys. Lett., vol. 82, pp. 3976-3978, 2003.

Chapter 5
Current collapse suppression by gate field-plate

5.1 Introduction

An AlGaN/GaN-based high-electron-mobility transistor (HEMT) is considered as an excellent candidate for future power devices due to its high breakdown voltage, high saturation drain current, and low on-resistance (R_{on}) [1-2]. However, increased dynamic R_{on} by current collapse is regarded as one of the most critical issues to be solved for actual power-switching applications [3-4]. Various techniques have been reported as an effective approach to suppress current collapse, such as surface passivation [5], surface charge control with GaN cap layer [6], and field plate (FP) structure [7-10]. Saito et al. reported that the FP approach enhanced the breakdown voltage and hence suppressed the increase of dynamic R_{on} due to relaxation of electric field crowding at the gate edge in the drain side [9]. Brannick et al. reported by their computer simulation that FP was effective to reduce electron trapping by limiting tunneling injection of electrons into surface traps located in the gate-to-drain region [10]. Evidently, no experimental evidences have been identified to date with respect to the effect of FP on the dynamic switching performance of AlGaN/GaN HEMTs.

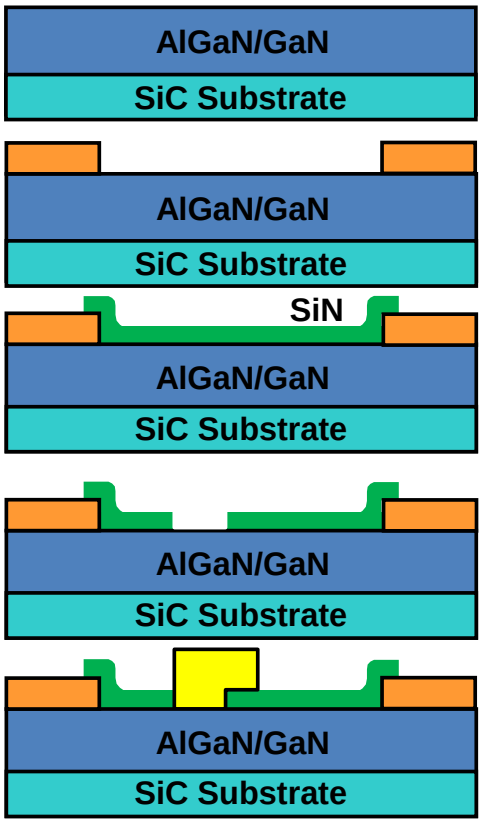
In this chapter, measurement results of dynamic R_{on} for a series of AlGaN/GaN HEMTs with essentially the same breakdown voltage but with different FP lengths have been discussed. Dramatic reduction in current collapse is presented for the FP device, in which

trap-induced increase in the gate-to-drain access resistance is quickly recovered by the field effect of positively biased FP electrode.

5.2 Fabrication of devices with field-plate

The epitaxial structure used in this work was grown by MOCVD on a 4H-SiC substrate. It consists of a 500-nm GaN channel, and a 25-nm $Al_{0.25}Ga_{0.75}N$ barrier. Hall-effect measurements showed a two-dimensional electron gas (2DEG) density of 1.01×10^{13} cm^{-2} and an electron mobility of 1500 cm^2/Vs.

Figure 5.1 shows the fabrication process of devices with FP electrode. HEMT device fabrication began with mesa isolation using BCl_3/Cl_2-based inductively coupled plasma reactive ion etching. Source and drain ohmic contacts were formed by e-beam evaporation of Ti/Al/Mo/Au metal stacks, followed by rapid thermal annealing at 850 °C for 30 s in a N_2



(a) Epi growth and device isolation by ICP with BCl_3 /Cl_2.

(b) Ohmic metal evaporation by Ti/Al/Mo/Au (15/160/35/50nm) and annealed at 850 ºC, 30sec.

(c) Surface passivation by sputtered SiN.

(d) Then gate window opening by dry-etching with CF_4.

(e) Gate metal and FP electrode evaporation by Ni/Au (50/180nm).

Fig. 5.1. Field-plate structured device process sequence.

atmosphere. The contact resistance of 0.34 Ωmm was measured. Devices were then passivated with a 200-nm sputter-deposited SiN film. The gate window was opened by dry etching of the SiN film, followed by Schottky gate and FP formation with Ni/Au. Figure 5.2 shows (a) a schematic cross-sectional view and (b) a top view of the fabricated AlGaN/GaN HEMTs with FP electrode. The gate length, gate-to-source distance, and gate width were fixed at 3, 3, and 100 μm, respectively.

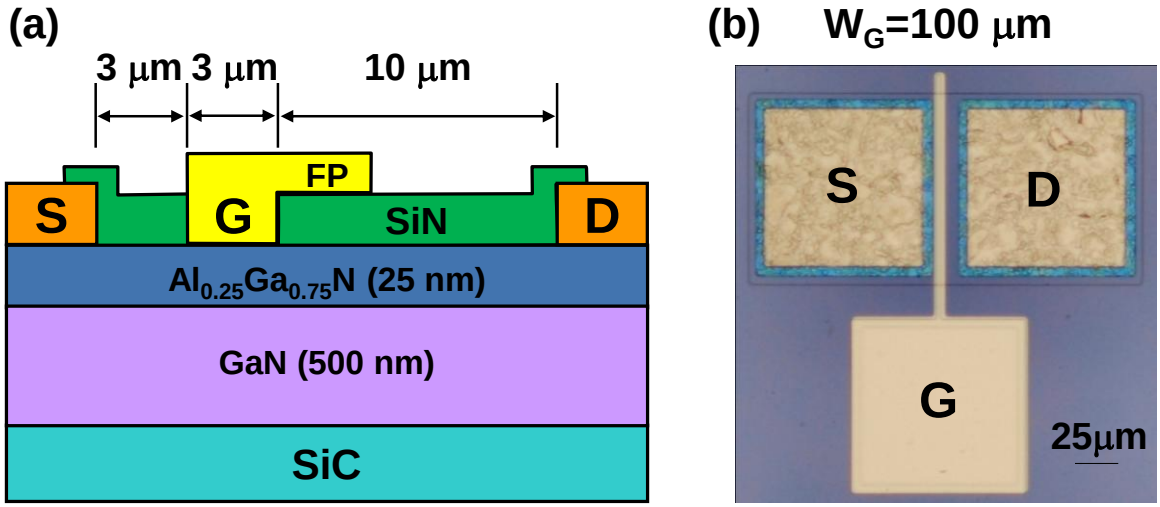


Fig. 5.2. (a) Schematic cross-sectional view and (b) top view of the fabricated AlGaN/GaN HEMTs with FP electrode.

5.3 Device characteristics

Essentially the same static characteristics have been measured for devices with and without FP electrode, as shown in Fig. 5.3. With a gate-to-drain distance (L_{GD}) of 10 μm, the maximum drain current defined at gate voltage (V_{GS}) of 1 V was 500 mA/mm and the gate-to-drain leakage current was 10^{-7} A/mm measured at a bias voltage of 200V. Figure 5.4 shows static R_{on} and breakdown voltage as a function of L_{GD} for devices without FP. The off-state source-to-drain breakdown voltage was defined at a drain current of 0.1 mA/mm, as shown in insert. During the measurements, the back side of SiC substrate was kept floating. Almost the same dependence of static R_{on} and breakdown voltage on L_{GD} has been measured

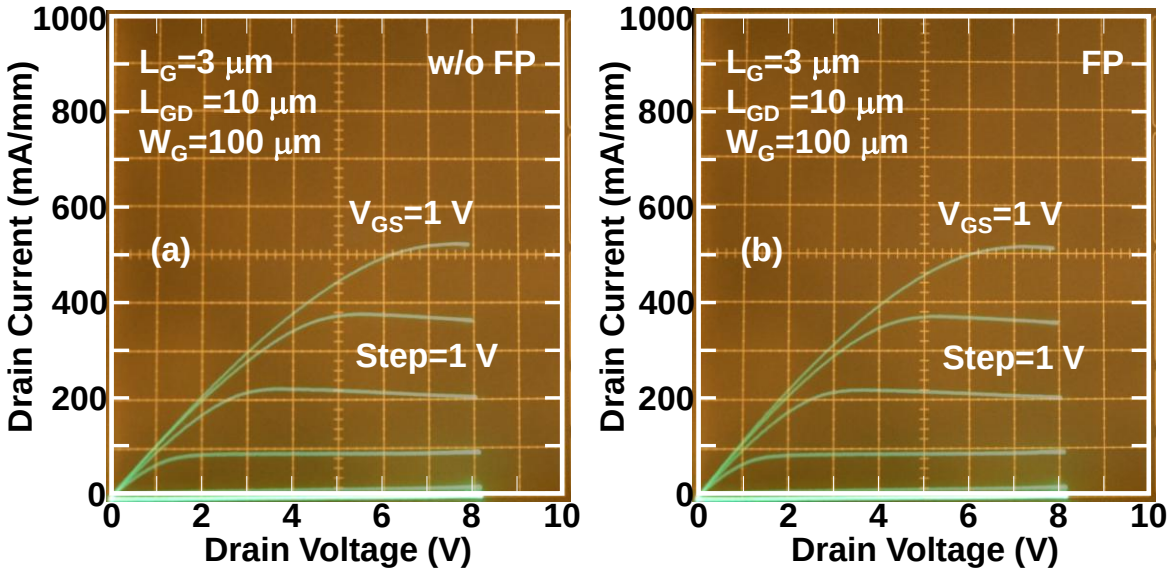


Fig. 5.3. Static *I-V* characteristics of devices (a) without and (b) with FP electrode.

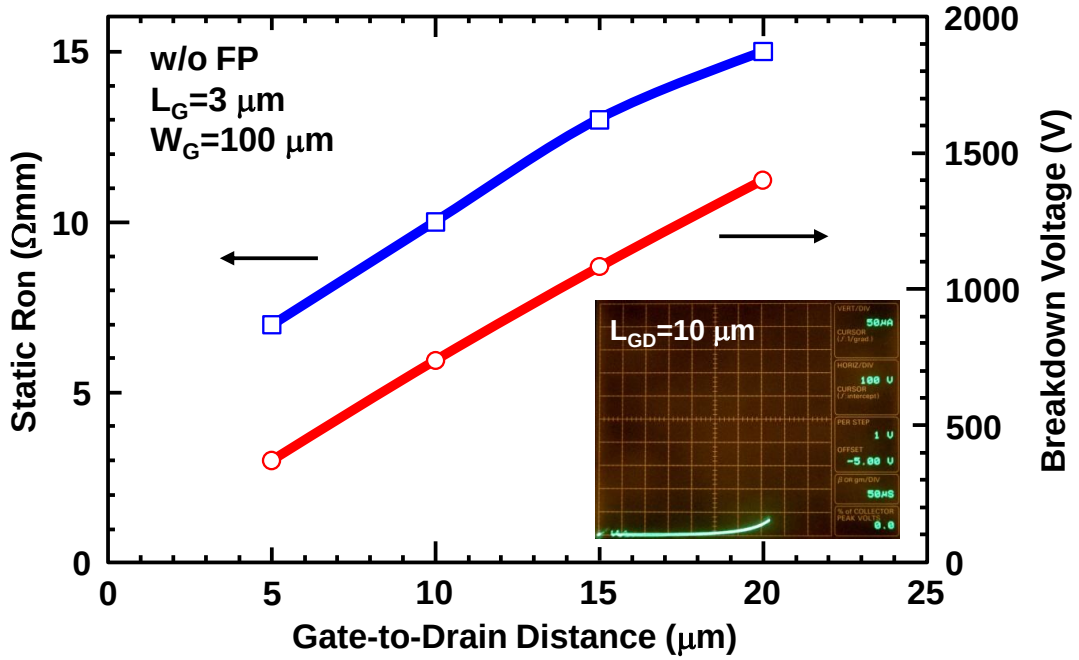


Fig. 5.4. Static on-resistance and breakdown voltage as a function of gate-to-drain distance (L_{GD}) for AlGaN/GaN HEMTs without field plate. Inset shows breakdown characteristics for the device with L_{GD}=10 μm.

for devices with different FP length (L_{FP}) of 1, 3, and 5 μm. Here, to avoid possible breakdown between FP and drain, L_{FP} of 1 μm was only formed for the device with L_{GD}=5 μm. The static R_{on} and the breakdown voltage were in the range of 9.5-10.7 Ωmm and 700-740 V, respectively, for devices with L_{GD}=10 μm. The linear increase in the breakdown voltage, as shown in Fig. 5.4, suggests that the horizontal electric field would not be crowded near the gate edge. High density of negative polarization charges (1.1×10^{13} cm^{-2}) is located at AlGaN surface, which is believed to be much higher than the typical trap charge density (orders of 10^{12} cm^{-2}). As a result, electric field distribution of the device is mostly governed by polarization charge during off state under high drain-to-source bias voltages. Thanks to this uniform electric field distribution due to polarization charge at the AlGaN surface, linear dependence of breakdown voltage on L_{GD} have been observed, which was suggested by the natural super-junction model [11]. The conventional model, based on surface trapping and extension of virtual gate, may also explain the increasing tendency of breakdown voltage with L_{GD}, but it would not guarantee the excellent linear increase with L_{GD} that have been observed between different devices. The fact that the devices with different FP length (L_{FP}=0, 1, 3, and 5μm) showed almost the same breakdown characteristics with respect to L_{GD} implies that the virtual gate extension by surface charge trapping during off state does not govern the electric field distribution of the device. Therefore, it is reasonable to conclude that uniformly distributed negative polarization charges on the AlGaN surface are responsible for establishing such field distribution between gate and drain, as suggested by the natural super-junction model [11].

Characterization of dynamic R_{on} was carried out by on-wafer pulsed measurements, where the gate voltage was switched from off-state (V_{GS}=-5 V, below the threshold voltage of -3.7 V) to on-state (V_{GS}=1 V), while applying a drain bias voltage (V_{DS}) up to 200 V. The load resistance (R_L) was connected in series with the tested device and was adjusted so that R_{on} was reasonably measured in the linear region, i.e., below 1/4 of the maximum drain current. The on-state duration time (t_{on}) and the off-state duration time (t_{off}) were fixed at 1 μs and 10 ms, respectively. To represent the magnitude of current collapse quantitatively, we have defined the current collapse, where the R_{on} value measured at t_{on}=1 μs was normalized

by its static value. Figure 5.5 shows the current collapse as a function of V_{DS} with V_{GS}=1 V for devices without FP electrode. For devices without FP, the normalized dynamic R_{on} was gradually increased from 190 to 320 with increasing L_{GD} from 5 to 20 μm. Current collapse was increased with increasing V_{DS}. Hence, higher drain bias voltages lead to enhancement of trapped electrons [12].

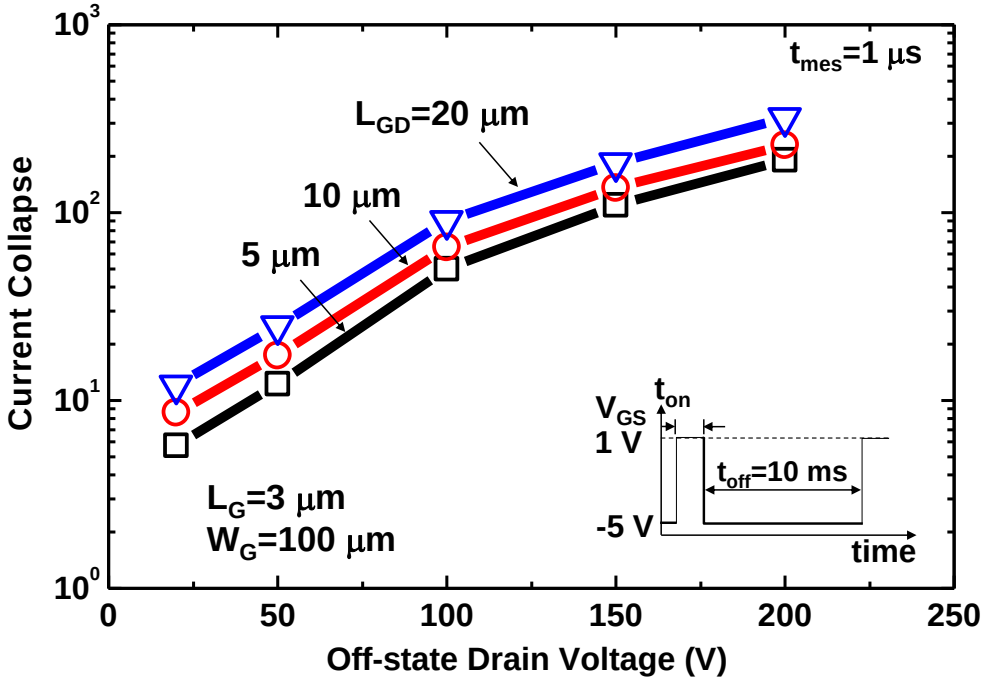


Fig. 5.5. Current collapse as a function of off-state drains bias voltage for AlGaN/GaN HEMTs without FP electrode.

In power switch applications, high breakdown voltage is required. Devices with longer L_{GD} meet the requirement of high breakdown voltages. However, longer L_{GD} devices have large current collapse for AlGaN/GaN HEMTs without FP, leading to increase power loss in switching devices. Therefore, a trade-off is needed between current collapse and breakdown. This is a key challenge for GaN-based power switching devices. Device with FP electrode is one of the solutions to solve this issue. Next dynamic behaviors of devices with FP have been discussed.

Figure 5.6 shows measured time-dependent waveforms of the drain current and the drain voltage (insert) of devices with and without FP. A constant R_L of 15 kΩ was used at V_{GS}=1 V and V_{DS}=200 V. Although the drain current waveform exhibited an oscillatory response in the early stage (up to 200 ns), our setup was able to stably measure the drain current response with a time constant of more than 300 ns. The device without FP exhibited seriously degraded drain current response with a long time constant (more than 1 ms), while the drain current recovery was much faster for the FP device. The dynamic R_{on} measured at t_{on}=1 μs was as large as 2220 Ωmm for the device without FP, while that for the FP device (L_{FP}=5 μm) was only 45 Ωmm. More interestingly, the drain current recovery became faster as L_{FP} was increased, indicating that the gate-FP structure with reasonably long L_{FP} is effective to reduce dynamic R_{on}.

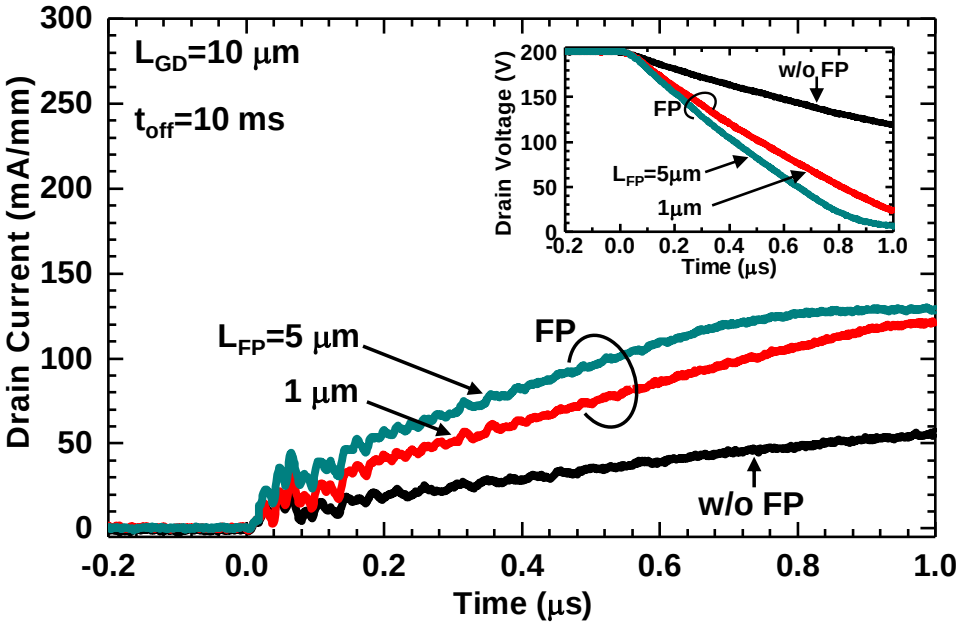


Fig. 5.6. Transient drain current of AlGaN/GaN HEMTs with and without FP. Pulsed mode is operated with 15 kΩ load line with off-state drain bias voltage of 200 V and on-state gate voltage of 1 V. Inset shows transient drain voltage.

5.4 Effect of gate field-plate length

Figure 5.7 shows the current collapse as a function of off-state V_{DS} for AlGaN/GaN HEMTs with different FP length. It is obvious that the dynamic R_{on} increases with increasing

V_{DS}. Note that the current collapse for the FP device is lowered by 1 or 2 orders of magnitude compared to the device without FP, demonstrating a primary advantage of FP to suppress current collapse. To our knowledge, this is the first report showing experimental evidence of current collapse suppression by using gate FP, where the dynamic R_{on} was compared among devices with essentially the same breakdown voltages. Figure 5.8 shows current collapse as a function of V_{DS} with different V_{GS}. For the device without FP, the normalized dynamic R_{on} was increased with increasing V_{DS}, approaching more than 200 at V_{DS}=200 V. This behavior was almost independent of the on-state V_{GS} between -1 and +1 V. On the other hand, for the FP device, V_{GS} dependence was clearly observed, where normalized dynamic R_{on} was significantly reduced by increasing on-state V_{GS} from negative to positive values due to generation of capacitively-induced additional channel charge (on the order of 10^{11} cm^{-2}) in the early stage of on state (up to t_{on}=1 μs). Note that the normalized dynamic R_{on} of the FP device with V_{GS}=-1 V is approaching to that for the device without FP, indicating that FP electrode becomes less effective on dynamic R_{on} when on-state V_{GS} was set at negative values under high V_{DS} conditions.

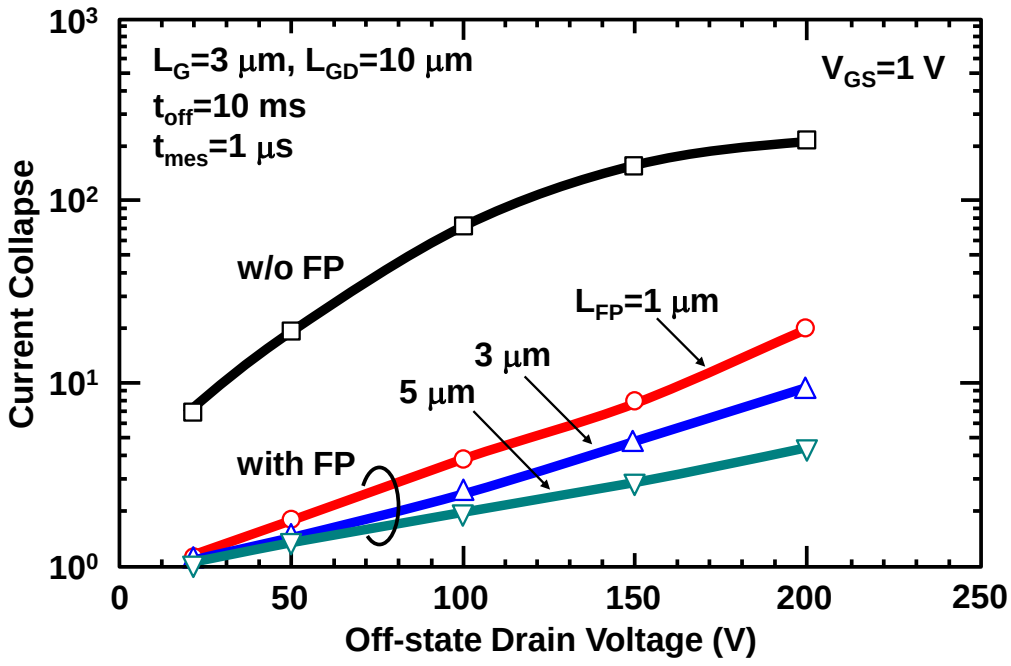


Fig. 5.7. Current collapse as a function of off-state drain bias voltage for AlGaN/GaN HEMTs with different FP length.

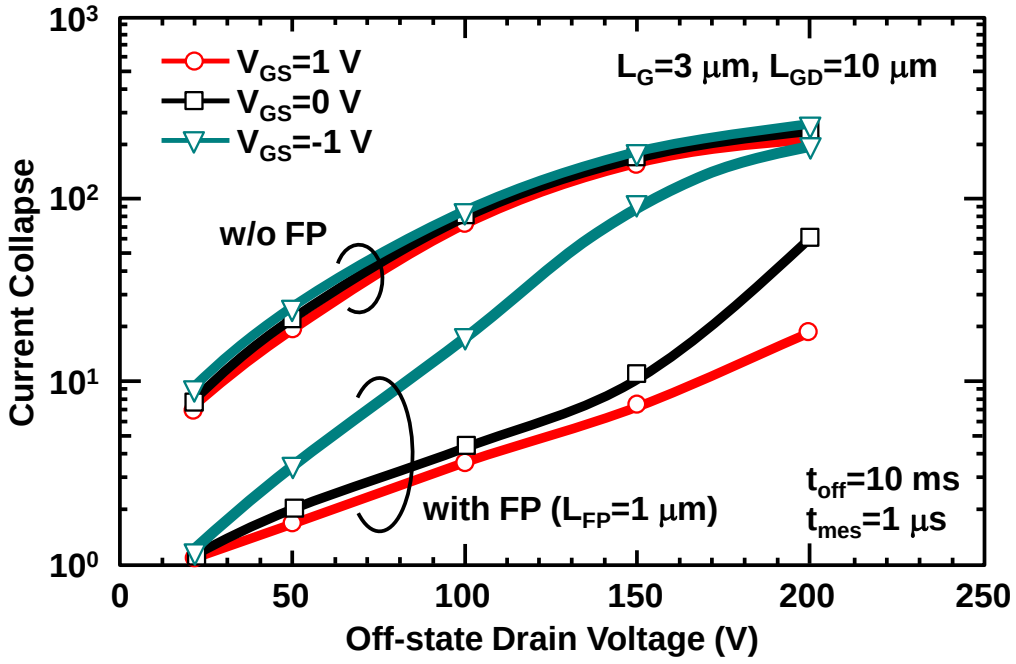


Fig. 5.8. Current collapse as a function of off-state drain bias voltage for AlGaN/GaN HEMTs with different gate bias voltage.

5.5 Mechanism of current collapse suppression

Figure 5.9 shows the schematic diagram of device operation under on states for AlGaN/GaN HEMTs with and without FP. During the off state with V_{GS}=-5 V, both devices are considered essentially the same, where channel 2DEG electrons are fully depleted under

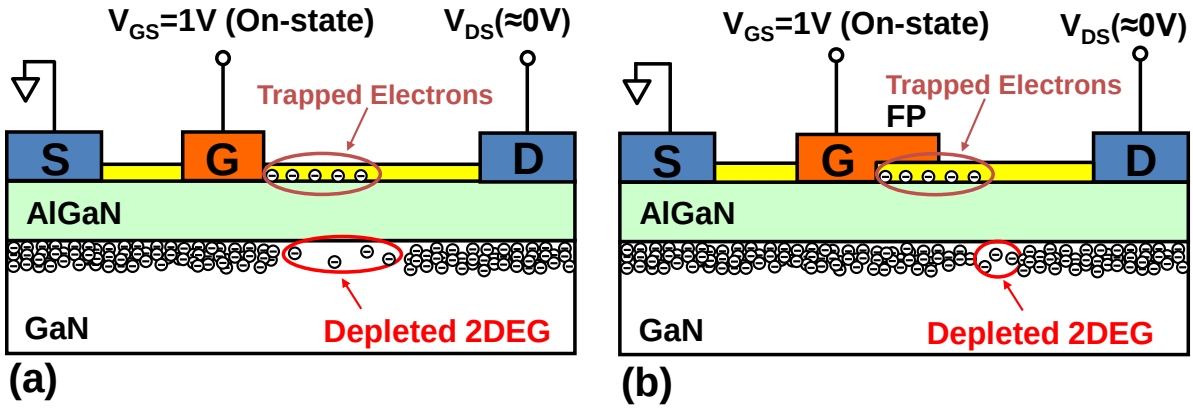


Fig. 5.9. Schematic diagrams of on state device operation for AlGaN/GaN HEMTs (a) without FP and (b) with FP.

the gate. Due to strong reverse electric fields between gate and drain during off state, electrons are injected from the gate edge as leakage currents and are assumed to be trapped at the AlGaN/SiN interface. Those trapped electrons contribute to partly deplete the channel 2DEG electrons near the gate edge in the drain side. Next the gate voltage is switched to on state (V_{GS}=1 V), resulting in quick generation of electron accumulation under the gate. However, emission of captured electrons does not occur within a short period of time (i.e., less than 1 μs). Hence it takes rather a long time before steady state condition is reached for the device without FP (see Fig. 5.9 (a)). This is the main reason for causing the current collapse. On the other hand, the situation for the FP device is quite different, as shown in Fig. 5.9 (b). Since the AlGaN surface near the gate is covered with FP, the partial depletion of 2DEG electrons can be instantly recovered by the field effect of the positively-biased FP electrode. Therefore, the recovery of channel electrons is much faster for the FP device, leading to more enhanced improvements in dynamic performance during on state with more positive gate biases, as shown in Fig. 5.8.

5.6 Summary

The effect of gate FP on current collapse for a series of AlGaN/GaN HEMTs having essentially the same breakdown voltage but with different FP lengths have studied here. By applying a more positive on-state gate bias voltage, pronounced recovery in the dynamic on-resistance was observed for the FP device, whereas no significant gate-bias effects were observed for the device without FP. The mechanism responsible for the improved current collapse was proposed, where field-effect charge control by FP resulted in the quick recovery of partial channel depletion in the gate-to-drain access region. Figure 5.10 shows current collapse as function of L_{GD} for AlGaN/GaN HEMTs with different FP length. Although all devices with same L_{GD} have almost same breakdown voltage, current collapse suppressed more than one order of magnitude by introducing FP electrode. These results indicate that current collapse is one of the solutions for suppression of current collapse.

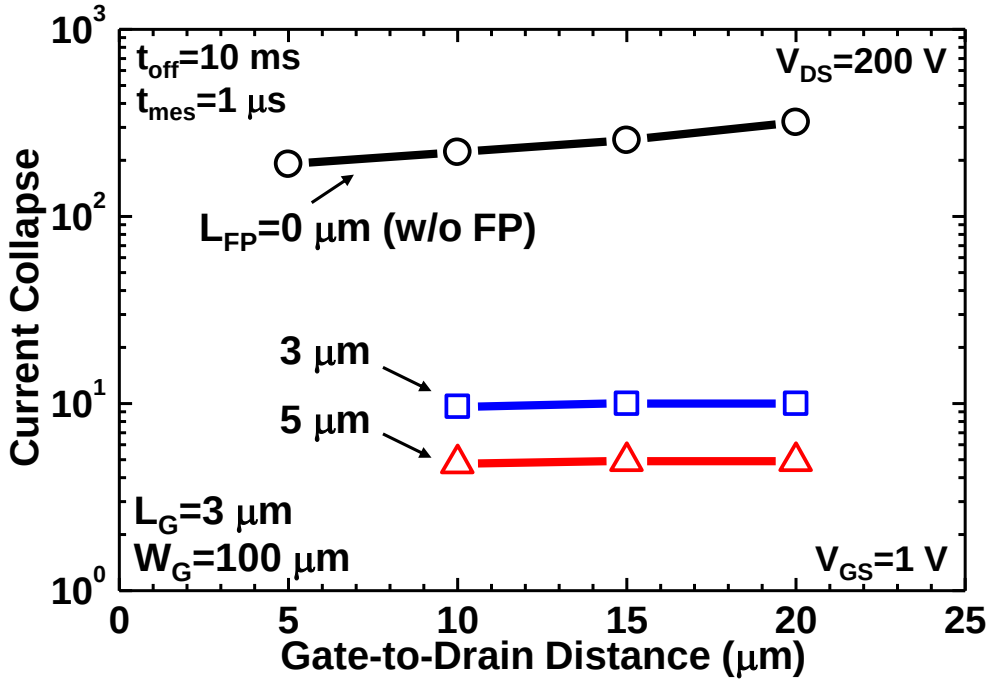


Fig. 5.10. Current collapse as a function of L_{GD} for AlGaN/GaN HEMTs with different FP length.

References

[1] S. C. Binari, K. Ikossi, J. A. Roussos, W. Kruppa, D. Park, H. B. Dietrich, D. D. Koleske, A. E. Wickenden, and R. L. Henry, "Trapping effects and microwave power performance in AlGaN/GaN HEMTs," IEEE Trans. Electron Devices, vol. 48, no. 3, pp. 465–471, Mar. 2001.

[2] R. Chu, A. Corrion, M. Chen, R. Li, D. Wong, D. Zehnder, B. Hughes, and K. Boutros, "1200-V normally off GaN-on-Si field-effect transistors with low dynamic ON-resistance," IEEE Electron Device Lett., vol. 32, no. 5, pp. 632–634, May 2011.

[3] R. Vetury, N. Q. Zhang, S. Keller, and U. K. Mishra, "The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs," IEEE Trans. Electron Devices, vol. 48, no. 3, pp. 560–566, Mar. 2001.

[4] W. Saito, T. Nitta, Y. Kakiuchi, Y. Saito, K. Tsuda, I. Omura, and M. Yamaguchi, "Suppression of dynamic On-resistance increase and gate charge measurements in high-voltage GaN-HEMTs with optimized field-plate structure," IEEE Trans. Electron Devices, vol. 54, no. 8, pp. 1825–1830, Aug. 2007.

[5] B. M. Green, K. K. Chu, E. M. Chumbes, J. A. Smart, J. R. Shealy, and L. F. Eastman, "The effect of surface passivation on the microwave characteristics of undoped AlGaN/GaN HEMTs," IEEE Electron Device Lett., vol. 21, no. 6, pp. 268–270, Jun. 2000.

[6] T. Kikkawa et al, "Surface charge controlled AlGaN/ GaN-power HEFT without current collapse and G_m," in IEDM Tech. Dig., 2001, pp. 25.4.1 - 25.4.4.

[7] Y. Ando, Y. Okamoto, H. Miyamoto, T. Nakayama, T. Inoue, and M. Kuzuhara, "10-W/mm AlGaN–GaN HFET with a field modulating plate," IEEE Electron Device Lett., vol. 24, no. 5, pp. 289–291, May 2003.

[8] Y. Wu, A. Saxler, M. Moore, R. P. Smith, S. Sheppard, P. M. Chavarkar, T. Wisleder, U. K. Mishra, and P. Parikh, "30W/mm GaN HEMTs by field plate optimization," IEEE Electron Device Lett., vol. 25, no. 3, pp. 117–119, Mar. 2004.

[9] W. Saito, Y. Kakiuchi, T. Nitta, Y. Saito, T. Noda, H. Fujimoto, A. Yoshioka, T. Ohno, and M. Yamaguchi, "Field-plate structure dependence of current collapse phenomena in high-voltage GaN-HEMTs," IEEE Electron Device Lett., vol. 31, no. 7, pp. 659–661, Jul. 2010.

[10] A. Brannick, N. A. Zakhleniuk, B. K. Ridley, J. R. Shealy, W. J. Schaff, and L. F. Eastman, "Influence of field plate on the transient operation of the AlGaN/GaN HEMT," IEEE Electron Device Lett., vol. 30, no. 5, pp. 436–438, May 2009.

[11] H. Ishida, D. Shibata, M. Yanagihara, Y. Uemoto, H. Matsuo, T. Ueda, T. Tanaka, and D. Ueda, "Unlimited high breakdown voltage by natural super junction of polarized semiconductor," IEEE Electron Device Lett., vol. 29, no. 10, pp. 1087–1089, Oct. 2008.

[12] Z. Tang, S. Huang, Q. Jiang, S. Liu, C. Liu, and K.J. Chen, "High-voltage (600-V) low-leakage low-current-collapse AlGaN/GaN HEMTs with AlN/SiN_x passivation," IEEE Electron Device Lett., vol. 34, no. 3, pp. 366–368, Mar. 2013.

Chapter 6
Conclusions

Nowadays, AlGaN/GaN high-electron-mobility transistors (HEMTs) are interesting for their high-power performance capabilities. However, current collapse, i.e., dispersion of drain current or increased dynamic on-resistance (R_{on}), is the prime issue which limits microwave output power and switching performances in AlGaN/GaN HEMTs. Although there have been remarkable improvements in growth and device technologies, it is still essential to understand mechanism of current collapse and ways to get rid of it. In this work, I have been investigated the mechanism of current collapse in AlGaN/GaN HEMTs. We have also been proposed a solution for current collapse suppression.

This work has been focused on characterization of the dynamic behavior in AlGaN/GaN HEMTs with different passivation films. The maximum drain current was increased by around 25% for SiN passivated devices at t_{on}=1 μs as compared to its static value, while it was reduced by around 56% for Al_2O_3 passivated devices. The drain current was decreased with increasing t_{on} and was increased with increasing t_{off} for SiN passivated devices, while Al_2O_3 passivated devices showed vice versa. The drain current transient was very slow for Al_2O_3 passivated devices, i.e., rather long time (ms order) to reach steady-state condition. Interface (insulator/AlGaN) traps are responsible for these slow drain current transient. These results indicate that the trap density at Al_2O_3/AlGaN is comparatively higher than that of SiN/AlGaN. Both passivated devices are suffered with buffer associated traps during small on-state duration time.

The effect of SiN-deposition temperature on dynamic R_{on} has been investigated. Current collapse (i.e., normalized dynamic R_{on}) was increased with increasing off-state drain bias voltage and was decreased with increasing SiN-deposition temperature. It was also decreased with increasing post-annealing temperature. These results indicate that the SiN/AlGaN interface trap density is reduced with increasing both SiN-deposition and post-annealing temperatures.

We have studied the effect of gate FP on current collapse for a series of AlGaN/GaN HEMTs having essentially the same breakdown voltage but with different FP lengths. By applying a more positive on-state gate bias voltage, pronounced recovery in the dynamic on-resistance was observed for the FP device, whereas no significant gate-bias effects were observed for the device without FP. The mechanism responsible for the improved current collapse was proposed, where field-effect charge control by FP resulted in the quick recovery of partial channel depletion in the gate-to-drain access region.

The above studies indicate that the current collapse is suppressed by good passivation film and longer FP with more positive on-state gate biases in AlGaN/GaN HEMTs for future high-power applications.

Acknowledgement

First and foremost, I would like to express my deepest gratitude to my research advisor Professor Masaaki Kuzuhara. It was one of my luckiest events in my life to become his student. Had it not been for his deep insight and patience throughout the course of his guidance, I would have never finished this journey. Not only in technical point of view but also in many other aspects, I believe that in the future I will greatly benefit from all the experiences that I had with him and from all his teachings.

I also would like to thank Dr. Hirokuni Tokuda, a visiting professor in our laboratory, for giving me intuition and invaluable advice to solve my challenging problems. His helpful discussion makes my research easy.

I was fortunate to have Professor Akihiro Hashimoto, Professor Kazutoshi Fukui, and Professor Toshio Katsuyama in the thesis approval committee. Thanks them for accepting to be on the jury of this dissertation.

Thanks to Professor Akio Yamamoto, Professor Ashraful Ghani Bhuiyan, Professor Md. Rafiqul Islam, and Eiichi Kobayashi for the interesting discussions about research and for being always kind and available to help me. All the graduate and undergraduate students of my laboratory have provided different kinds of support during not only my research but also my stay at Fukui. It is my pleasure to acknowledge their kind help.

I am indebted to my beloved elder sister Mimi, younger brother and sisters, Santa, Tareq, and Tania for their hearting support. Special thanks to my wife Shoshi who gave me a lot of motivation, spirit, inspiration, and energy to move forward. Last but definitely not least, I am entirely thankful to my loving parents who have been encouraging me from the other side of the earth. Without their endless support and love, I could not have reached this far. I love you all.

Finally, I would like to acknowledge the financial support from the Ministry of Education, Culture, Sports, Science, and Technology (MEXT) of the Japanese Government through the award of a Monbukagakusho Scholarship which made this work and my experience in Japan possible. Without their support, understanding, patience, and sacrifices I would not have reached this educational goal.

Author

Curriculum Vitae

Md. Tanvir Hasan

Education

Bachelor of Science (B. Sc.) in Electrical and Electronic Engineering, Khulna University of Engineering & Technology (KUET), Khulna, Bangladesh, February 2006.

Master of Science (M. Sc.) in Electrical and Electronic Engineering, Khulna University of Engineering & Technology (KUET), Khulna, Bangladesh, December 2007.

Doctor of Philosophy (Ph. D.) in Electrical and Electronics Engineering, University of Fukui, Japan, September 2013.

Publications

Journal Papers

[1] **Md. Tanvir Hasan**, Hirokuni Tokuda, and Masaaki Kuzuhara, "Surface barrier height lowering at above 540 K in AlInN/AlN/GaN heterostructures", **Appl. Phys. Lett.** vol. 99, no. 13, p.132102, 2011.

[2] **Md. Tanvir Hasan**, Ashraful G. Bhuiyan, and Akio Yamamoto, "Two dimensional electron gas in InN-based heterostructures: Effects of spontaneous and piezoelectric polarization", **Solid-State Electronics**, vol. 52, no. 1, pp.134-139, 2008.

International Conference Papers

[3] **Md. Tanvir Hasan**, Takashi Asano, Hirokuni Tokuda, and Masaaki Kuzuhara, "Effect of field plate on dynamic ON-resistance in AlGaN/GaN HEMTs", **ISCS 2013**, Kobe, Japan, 2013, 312-ISCS2013TuC4-3.

[4] **Md. Tanvir Hasan**, Toshikazu Kojima, Hirokuni Tokuda, and Masaaki Kuzuhara, "Effect of sputtered SiN passivation on current collapse of AlGaN/GaN HEMTs", **CS MANTECH 2013**, New Orleans, Louisiana, USA, 2013, pp. 131-134.

Domestic Conference Papers

[5] **Md. Tanvir Hasan**, Hirokuni Tokuda, and Masaaki Kuzuhara, "Effect of passivation on drain current dispersion for AlGaN/GaN HEMTs", **IEICE Technical Report**, vol. 112, no. 327, Osaka, Japan, 2012, pp.45-50.

[6] **Md. Tanvir Hasan**, Hirokuni Tokuda, and Masaaki Kuzuhara, "Surface barrier height lowering at above 540 K in AlInN/AlN/GaN heterostructures", **IEICE Technical Report**, vol. 112, no. 327, Kyoto, Japan, 2011, pp.29-33.

Other Journal Papers

[1] Md. Mottaleb Hossain, Md.Abdullah-Al-Humayun, **Md. Tanvir Hasan**, Ashraful G. Bhuiyan, and A. Yamamoto, "Theoretical Design of 1.55 μm Quantum Dot Heterostructure Laser using InN", **IEICE Trans. Electron.**, vol. E95-C, no.2, pp. 255-261, 2012.

[2] **Md. Tanvir Hasan**, Md. Rejvi Kaysir, Md. Sherajul Islam, Ashraful G. Bhuiyan, Md. Rafiqul Islam, A. Hashimoto, and Akio Yamamoto, "Properties of 2DEG in InN/InGaN/InN Double Channel HEMTs", **Phys. Status Solidi C**, vol. 7, no. 7–8, pp.1997–2000, 2010.

[3] **Md. Tanvir Hasan**, Md. Jahirul Islam, Rajib-ul Hasan, Md. Sherajul Islam, Shahrina Yeasmin, Ashraful G. Bhuiyan, Md. Rafiqul Islam, and Akio Yamamoto, "Design and Performance of 1.55 μm Laser Using InGaN", **Phys. Status Solidi C**, vol. 7, no. 7–8, pp.1825– 1828, 2010.

[4] Md. Sherajul Islam, Sakib M. Muhtadi, **Md. Tanvir Hasan**, Ashraful G. Bhuiyan, Md. Rafiqul Islam, A. Hashimoto, and A. Yamamoto, "AlInN/InN Metal Oxide Semiconductor Heterostructure Field Effect Transistor", **Phys. Status Solidi C**, vol. 7, no. 7–8, pp.1983–1987, 2010.

[5] Md. Rafiqul Islam, **Md. Tanvir Hasan**, Ashraful G. Bhuiyan, M. R. Islam, and A. Yamamoto, "Design and performance of $In_xGa_{1-x}N$-based MJ solar cells", **IETECH Journal of Electrical Analysis**, Vol. 2, No. 4, pp.237 – 243, 2008.

Others International Conference Papers

[6] **Md. Tanvir Hasan**, Ashraful G. Bhuiyan, K. Sasamoto, A. Hashimoto, A. Yamamoto "A novel high performance GaN-based Rectangular Patch Antenna", **International Workshop on Nitride semiconductors (IWN 2010)**, Florida, U.S.A., 2010.

[7] **Md. Tanvir Hasan**, M. Majharul Haque, Ashraful G. Bhuiyan, Akio Yamamoto," Effects of Cap Layer on 2DEGs in InN-Based Heterostructures", 6th International Conference on Electrical & Computer Engineering (**ICECE 2010**), Dhaka, Bangladesh, IEEE catalogue number: CFP0868A-CDR, ISBN: 978-1-4244-6277-3, pp.120-122.

[8] **Md. Tanvir Hasan**, Md. Monibor Rahman, A.N.M. Shamsuzzaman, Md. Sherajul Islam, and Ashraful G. Bhuiyan, "InN-based Dual Channel High Electron Mobility Transistor", 5th International Conference on Electrical & Computer Engineering (ICECE 2008), Dhaka, Bangladesh, IEEE catalogue number: CFP0868A-CDR, ISBN: 978-1-4244-2015-5, pp. 452-55,

[9] **Md. Tanvir Hasan**, M. Azim Ullah, Md. Asaduzaman, and Ashraful G. Bhuiyan, "Design of 1.55 μm Laser Using InN-based Quantum Well Heterostructures", 5th International Conference on Electrical & Computer Engineering (**ICECE 2008**), Dhaka, Bangladesh, IEEE catalogue number: CFP0868A-CDR, ISBN: 978-1-4244-2015-5, pp. 946-48.

[10] **Md. Tanvir Hasan**, Md. Fahimul Islam, Ashraful G. Bhuiyan, M. R. Islam, and A. Yamamoto,"Piezoelectrically Induced Polarization and Charge in InN-based Heterostructures", 4th International Conference on Electrical & Computer Engineering (**ICECE 2006**), Dhaka, Bangladesh, IEEE catalogue number: 06EX1362, pp. 245-49.