Topologically Minimal Realization of a Negative Resistor Using Nullors and Positive Resistors

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Abstract— Although it is heuristically well-known that a negative resistor can be realized with nullors and positive resistors, the minimal realization of it have not been discussed systematically in detail. In this paper, based upon the general fundamental properties of linear active networks, it is proved systematically that nullors not less than one (two) and positive resistors not less than three (one, respectively) are necessary to realize a negative resistor and there exist only two circuits for the topologically minimal realization disregarding the labelling of nullors and resistors.

1. INTRODUCTION

It has been already known that negative resistors can be realized by means of positive resistors and nullors (where "nullor" is the abbreviation of a pair of a nullator and a norator which from now on are denoted by Nu or 5, and No or 6, respectively) [1]. It seems that none of papers consider the topologically minimal realization of a negative resistor on the basis of the given port characteristics and the general fundamental properties of the nullor-model network. Furthermore, it seems also that the variety in the nullor-model representations of other functional circuits results in the fact that there exist the circuits not less than one for the topologically minimal realization of a negative resistor [2], [3]. Then, it is considered significant to systematize all the topologically minimal realization circuits of a negative resistor from the above viewpoints [4].

In this paper, based upon the general fundamental properties of linear active networks, the least number of elements needed for the topologically minimal realization of a negative resistor and all the topologically minimal realization circuits of it are found systematically.

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2. PRELIMINARIES

(1) One port considered in this paper consists of nullors and positive resistors and contains no independent sources. Suppose that one port has no redundancy corresponding to the following Lemmata 1 and 2 [5].

[Lemma 1] The following transformations guarantee that the values of all the branch variables in N port remain unchanged before and after the transformations:

(I) If a loop (cut-set) consists of only nullators, replace an arbitrary one of them by an open (a short, respectively) circuit.

(II) Suppose that there exists a loop (cut-set, respectively) which consists of nullators more than one and y-branch. If y-branch is a norator, replace it by a short (an open, respectively) circuit and further repeat the transformation (I). If y-branch is a regular branch, replace it by an open (a short, respectively) circuit.

[Lemma 2] The following transformations guarantee that the values of all the branch variables in N port remain unchanged before and after the transformations except for the current (voltage) values of branches which are included in each loop (cut-set, respectively) :

(III) If a loop (cut-set) consists of only norators, or of norators and independent voltage (current) sources, replace an arbitraly one of the norators by an open (a short, respectively) circuit.

(IV) Suppose that there exists a loop (cut-set, respectively) which consists of norators more than one and y-branch. If y-branch is a nullator, replace it by a short (an open, respectively) circuit and further repeat the transfomation (III). If y-branch is a regular branch, replace it by an open (a short, respectively) circuit.

(2) In the graph G_o for N port consisting of nullors and positive resistors, let G_v (G_i) be the voltage (current) graph which is obtained from the graph G_o by replacing all nullators (norators) and all norators (nullators, respectively) by short circuits and open circuits , respectively, where the port branches are dealt with in the same way as the resistive branches. Let a common tree $\mathcal{T}_c$ be a set of branches which is a tree of both G_v and G_i . Furthermore, let $\mathcal{T}_c^v$ ($\mathcal{T}_c^i$) be a tree of the graph G_o such that some port tree branches of $\mathcal{T}_c$, conductive tree branches of $\mathcal{T}_c$ and nullators (norators) branches are taken as the tree branches of the graph G_o and the other port co-tree branches of $\mathcal{T}_c$, resistive co-tree branches of $\mathcal{T}_c$, and norators (nullators, respectively) branches, as the co-tree branches of the graph G_o .

(3) If the values of resistors in the network are independent algebraically and all the network variables are uniquely determined for the arbitrary input waveforms, the network is called the non-trivial one in a topological sense. In realizing the active circuit, it is called the

topologically minimal realization when the circuit is realized on the basis of the above topological conditions and moreover each element of the realized circuit is essential to specify the given port characteristics.

(4) The statement that one port is topologically non-trivial is equivalent to each of the following statements [6]:
Statement 1: There exists a common tree $\mathcal{T}_c$ in the graphs G_v and G_i.
Statement 2: There exist $\mathcal{T}_c^v$ and $\mathcal{T}_c^i$ in the graph G_o.
Statement 3: Matrices $\underset{\sim}{F}_{56}$ and $\underset{\sim}{F}_{65}$ are nonsingular*.

(5) Since negative resistors have finite immittances and it is assumed in the minimal realization of a negative resistor that there is no redundancy in the network structures, the following assumptions are valid for the realization of a negative resistor without loss of generality:
(i) The graphs G_v and G_i for the negative resistor are connected graphs.
(ii) Neither G_v nor G_i for the negative resistor consists of only tree branches or only co-tree branches.
(iii) The port branch of one port is always chosen as a tree branch of $\mathcal{T}_c^v$ and $\mathcal{T}_c^i$ in the graph G_o.

(6) Now, provided that the port branch is chosen as a tree branch of $\mathcal{T}_c^i$ in the graph G_o, let us get the general expression of a negative resistor in terms of the explicit network structures [7]. Suppose from now on that the reference directions for all the branch voltages and all the branch currents including the port branch variables are the associated reference directions [8]. Then, applying KVL and KCL to one port on the basis of $\mathcal{T}_c^i$ of the graph G_o, we have

$$\underset{\sim}{v}^l = -\underset{\sim}{F}\,\underset{\sim}{v}^t \qquad \text{and} \qquad \underset{\sim}{i}^t = \underset{\sim}{F}^T \underset{\sim}{i}^l , \tag{1}$$

where $\underset{\sim}{v}^l \triangleq [\ \underset{\sim}{v}_5^T,\ \underset{\sim}{v}_R^T\ ]^T$, $\underset{\sim}{i}^l \triangleq [\ \underset{\sim}{i}_5^T,\ \underset{\sim}{i}_R^T\ ]^T$, $\underset{\sim}{v}^t \triangleq [\ v_P,\ \underset{\sim}{v}_6^T,\ \underset{\sim}{v}_G^T\ ]^T$, $\underset{\sim}{i}^t \triangleq [\ i_P,\ \underset{\sim}{i}_6^T,\ \underset{\sim}{i}_G^T\ ]^T$, and
$\underset{\sim}{v}^l$ ($\underset{\sim}{i}^l$): the co-tree branch voltage (current, respectively) vector,
$\underset{\sim}{v}^t$ ($\underset{\sim}{i}^t$): the tree branch voltage (current, respectively) vector,
$\underset{\sim}{v}_5$ ($\underset{\sim}{i}_5$): the nullator-branch voltage (current, respectively) vector,
$\underset{\sim}{v}_6$ ($\underset{\sim}{i}_6$): the norator-branch voltage (current, respectively) vector,
$\underset{\sim}{v}_G$ ($\underset{\sim}{i}_G$): the conductive branch voltage (current, respectively) vector,
$\underset{\sim}{v}_R$ ($\underset{\sim}{i}_R$): the resistive branch voltage (current, respectively) vector,
v_P (i_P): the port-branch voltage (current, respectively) scalar,

*: The matrix $\underset{\sim}{F}_{56}$ is the square matrix defined by eq. (2) and the matrix $\underset{\sim}{F}_{65}$ is the square matrix defined for $\mathcal{T}_c^v$ in the graph G_o in the same way as the matrix $\underset{\sim}{F}_{56}$ for $\mathcal{T}_c^i$. From now on, the symbols "$\underset{\sim}{A}$" and "A" denote the matrix and the scalar, respectively.

and furthermore, $\underset{\sim}{F}$ denotes the principal submatrix of the fundamental loop matrix and $\underset{\sim}{F}^T$ denotes the transpose of it. The matrix $\underset{\sim}{F}$ is defined in detail by the following equation:

$$\underset{\sim}{F} = \begin{matrix} \\ Nu \\ R \end{matrix} \begin{matrix} \begin{matrix} P & No & G \end{matrix} \\ \begin{bmatrix} \underset{\sim}{F}_{5P} & \underset{\sim}{F}_{56} & \underset{\sim}{F}_{5G} \\ \underset{\sim}{F}_{RP} & \underset{\sim}{F}_{R6} & \underset{\sim}{F}_{RG} \end{bmatrix} \end{matrix}, \tag{2}$$

where the submatrix $\underset{\sim}{F}_{\alpha\beta}$ denotes the $|\alpha| \times |\beta|$ matrix which shows whether the fundamental loop with respect to the α co-tree branch contains the β tree branch or not and $|\alpha|$ and $|\beta|$ denote the number of set α and that of set β, respectively. Furthermore, the branch characteristics are as follows:

$$\left.\begin{array}{l} \underset{\sim}{v}_R = \underset{\sim}{R}\underset{\sim}{i}_R\ , \quad \underset{\sim}{i}_G = \underset{\sim}{G}\underset{\sim}{v}_G\ , \quad \underset{\sim}{v}_5 = \underset{\sim}{0}\ , \quad \underset{\sim}{i}_5 = \underset{\sim}{0}\ , \quad \underset{\sim}{v}_6 = \text{the arbitrary vector}, \\ \text{and } \underset{\sim}{i}_6 = \text{the arbitrary vector}, \end{array}\right\} \tag{3}$$

where $\underset{\sim}{R}$ and $\underset{\sim}{G}$ are the $|R| \times |R|$ positive diagonal matrix and the $|G| \times |G|$ positive diagonal matrix, respectively. Provided that the following matrix $\underset{\sim}{K}_R$ is nonsingular, which is guaranteed by the property stated in (7) of the preliminaries, the port characteristics of one port is expressed from eqs.(1), (2), and (3) by the following equation:

$$i_P = \underset{\sim}{F}_{RP}^T \underset{\sim}{K}_R^{-1} (\underset{\sim}{F}_{R6} \underset{\sim}{F}_{56}^{-1} \underset{\sim}{F}_{5P} - \underset{\sim}{F}_{RP})\ v_P \tag{4}$$

where $\underset{\sim}{K}_R = \underset{\sim}{\mathcal{R}} - \underset{\sim}{F}_{R6} \underset{\sim}{F}_{56}^{-1} \underset{\sim}{F}_{5G} \underset{\sim}{G}^{-1} \underset{\sim}{F}_{R6}^T$ and $\underset{\sim}{\mathcal{R}} = \underset{\sim}{R} + \underset{\sim}{F}_{RG} \underset{\sim}{G}^{-1} \underset{\sim}{F}_{RG}^T$.

Consequently, considering that the reference directions of the port branch variables are the associated reference directions, the condition that eq.(4) satisfies the port characteristic of the negative resistor is obtained as follows:

$$\underset{\sim}{F}_{RP}^T \underset{\sim}{K}_R^{-1} (\underset{\sim}{F}_{R6} \underset{\sim}{F}_{56}^{-1} \underset{\sim}{F}_{5P} - \underset{\sim}{F}_{RP}) > 0. \tag{5}$$

If there is no conductive tree branches in the graph G_0, eqs.(4) and (5) are rewritten as the following eqs.(4') and (5'), respectively:

$$i_P = \underset{\sim}{F}_{RP}^T \underset{\sim}{R}^{-1} (\underset{\sim}{F}_{R6} \underset{\sim}{F}_{56}^{-1} \underset{\sim}{F}_{5P} - \underset{\sim}{F}_{RP})\ v_P \tag{4'}$$

and

$$\underset{\sim}{F}_{RP}^T \underset{\sim}{R}^{-1} (\underset{\sim}{F}_{R6} \underset{\sim}{F}_{56}^{-1} \underset{\sim}{F}_{5P} - \underset{\sim}{F}_{RP}) > 0. \tag{5'}$$

(7) Note that it is derived from eq.(5) that the graph G_0 of a negative resistor, that is, one port must contain at least one resistive co-tree branch, and note that the necessary and sufficient condition for the existence of one port is equal to the following: (i) there exist $\mathcal{T}_c^v$ and $\mathcal{T}_c^i$ in the graph G_0 with the port branch chosen as the tree branch or the co-tree branch and (ii) the fundamental loop matrix of the resistor subnetwork of one port, $\underset{\sim}{K}_R$ is nonsingular [7].

3. NECESSARY AND SUFFICIENT CONDITION FOR THE NUMBER OF ELEMENTS NEEDED FOR THE MINIMAL REALIZATION OF A NEGATIVE RESISTOR

In this section, on the basis of the above preliminaries stated in the section 2, the number of nullors and positive resistors needed for the minimal realization of a negative resistor is discussed in detail.

In order to make it clear, first of all, the necessary condition is given in the next theorem.

[Theorem 1] If negative resistors are realized by means of nullors and positive resistors, n_n is not less than one and n_r is not less than three, or n_n is not less than two and n_r is not less than one, where n_n and n_r denote the number of nullors and the number of positive resistors, respectively.

Proof:

Let us prove this by the contraposition. Then, we shall prove that any negative resistor cannot be realized in each of the following four cases: case(1) $n_n = 0$ and $n_r \geq 1$, case(2) $n_n \geq 1$ and $n_r = 0$, case(3) $n_n = 1$ and $n_r = 1$, and case(4) $n_n = 1$ and $n_r = 2$.

Cases (1) and (2): It is clear that any negative resistor can not be realized in the cases (1) [8] and (2) [5].

Case (3): Consider eqs.(2) and (4) which are expressed on the basis of $\mathcal{T}_c^i$, in which the tree branches are the port branch and a norator branch, and the co-tree branches are a nullator branch and a resistive branch. Then, considering in eq.(2) of this case (3) that there is no redundancy corresponding to Lemmata 1 and 2, we have $F_{5P} \neq 0$, $F_{RP} \neq 0$, $F_{R6} \neq 0$, and moreover $F_{56} \neq 0$ because the nonsingular matrix $\underset{\sim}{F}_{56}$ is the 1×1 matrix. Furthermore, since the principal submatrix of the fundamental loop matrix defined by eq.(2) is the totally unimodular matrix, without loss of generality, it is assumed that $F_{56} = F_{5P} = F_{RP} = F_{R6} = 1$.

If the above conditions are substituted into eq.(4), the coefficient of v_p in the right-hand side of eq.(4) becomes

$$F_{RP}^{T} R^{-1} (F_{R6} F_{56}^{-1} F_{5P} - F_{RP}) = 0 ,$$

where R denotes the scalar positive resistance of a resistive co-tree branch. However, since the above equation contradicts the requirement of eq.(5), it is concluded that any negative resistor can not be realized in this case (3).

Case (4): In this case, both G_v and G_i consist of three branches including the port branch. Since the port branch and a resistive branch must be chosen as a tree branch and a co-tree branch, respectively, of the common tree $\mathcal{T}_c$ in G_v and G_i, the other branch may be chosen as a tree branch or a co-tree branch of $\mathcal{T}_c$. Then, without loss of generality, this case (4) is divided into the following two cases: (i) $n_c = 2$ and (ii) $n_c = 1$, where n_c denotes the number of the common tree branches of $\mathcal{T}_c$ in G_v and G_i. Case (4-i) $n_c = 2$: Consider eqs.(2) and (4) which are expressed on the basis of $\mathcal{T}_c^i$, in which the tree branches are the port branch, a norator branch, and a conductive branch, and the co-tree branches are a nullator branch and a resistive branch. Then, considering in eq.(2) of this case (4-i) that there is no redundancy corresponding to Lemmata 1

and 2, we obtain $F_{R6} \neq 0$, $F_{RP} \neq 0$, $F_{RG} \neq 0$, and moreover $F_{56} \neq 0$ because the nonsingular matrix $\underset{\sim}{F}_{56}$ is the 1×1 matrix in this case (4-i). Furthermore, since the principal submatrix of the fundamental loop matrix defined by eq.(2) is the totally unimodular matrix, without loss of generality, we can assume that $F_{56} = F_{R6} = F_{RP} = F_{RG} = 1$. Substituting the above conditions into eq.(5), we have

$$\left\{R + G^{-1}(1 - F_{5G})\right\}^{-1}(F_{5P} - 1) > 0, \tag{6}$$

namely

$$R + G^{-1}(1 - F_{5G}) > 0 \text{ and } F_{5P} > 1 \tag{7}$$

or

$$R + G^{-1}(1 - F_{5G}) < 0 \text{ and } F_{5P} < 1, \tag{8}$$

where R and G denote the scalar positive resistance of a resistive co-tree branch and the scalar positive conductance of a conductive tree branch, respectively. However, the condition of $F_{5P} > 1$ in eq.(7) and that of $R + G^{-1}(1 - F_{5G}) < 0$ in eq.(8) contradict the fact that each of F_{5P} and F_{5G} is one of the elements of the totally unimodular matrix $\underset{\sim}{F}$ defined by eq.(2). Therefore, it is concluded that any negative resistor can not be realized in this case (4-i). Case (4-ii) $n_c = 1$: Consider eqs.(2) and (4) which are expressed on the basis of $\mathcal{T}_c^i$, in which the tree branches are the port branch and a norator branch, and the co-tree branches are two resistive branches. Then, considering in eq.(2) of this case (4-ii) that there is no redundancy corresponding to Lemmata 1 and 2, we have the following conditions; $F_{5P} \neq 0$, $\underset{\sim}{F}_{R6} (\in \mathbb{R}^{2\times 1})^* \neq \underset{\sim}{0}$, each element of $\underset{\sim}{F}_{RP} (\in \mathbb{R}^{2\times 1})$ is non-zero, and moreover $F_{56} \neq 0$ because the nonsingular matrix $\underset{\sim}{F}_{56}$ is the 1×1 matrix in this case (4-ii). Furthermore, since the principal submatrix of the fundamental loop matrix defined by eq.(2) is the totally unimodular matrix, without loss of generality, it is assumed that $F_{5P} = F_{56} = 1$ and $\underset{\sim}{F}_{RP}^T = [\,1,\ 1\,]$. Let $\underset{\sim}{F}_{R6}^T = [\,a\ ,b\,] \neq \underset{\sim}{0}$ and $\underset{\sim}{R} = \mathrm{diag}(R_1\ ,\ R_2)$, where R_1 and R_2 denote the scalar positive resistances of two resistive co-tree branches, and at least one of a and b is non-zero scalar. Then, substituting the above conditions into eq.(5), we have

$$(a - 1)R_1^{-1} + (b - 1)R_2^{-1} > 0. \tag{9}$$

However, eq.(9) contradicts the fact that the elements of the matrix $\underset{\sim}{F}$, that is, a and b must be ones of the totally unimodular matrix $\underset{\sim}{F}$ defined by eq.(2). Therefore, it is also concluded that any negative resistor can not be realized in this case (4-ii).

The proof of the case (4) is completed by those of the cases (4-i) and (4-ii). Then, the proof of this theorem is completed by those of the cases (1), (2), (3), and (4). Q.E.D.

[Theorem 2] The number of elements needed for the minimal realiza-

*: $\mathbb{R}^{n\times m}$ denotes the $n \times m$ matrices of real numbers.

tion of a negative resistor is $n_n = 1$ and $n_r = 3$, or $n_n = 2$ and $n_r = 1$.

Proof:

The necessity is proved by the theorem 1, while the sufficiency is clearly proved from the fact that each of the circuits shown in Fig.1 (a) and (b) is the negative resistor. Q.E.D.

4. ALL THE MINIMAL REALIZATION CIRCUITS OF A NEGATIVE RESISTOR

The least number of elements needed for the minimal realization of a negative resistor was given by the theorem 2. In this section, all the minimal realization circuits of a negative resistor with the above least number of elements are found systematically.

[Theorem 3] The minimal realization circuits of a negative resistor by means of nullors and positive resistors are only the two circuits shown in Fig.1 (a) and (b).

Proof:

Sufficiency: It is obvious that each of the circuits of Fig.1 (a) and (b) is the minimal realization circuit of a negative resistor.

Necessity: Case (1): Let us prove that the minimal realization circuit of a negative resistor by means of a nullor and three positive resistors is only the circuit shown in Fig.1(a). In this case, both G_v and G_i consist of four branches, and the port branch and at least one resistive branch should be chosen as a tree branch and a co-tree branch, respectively, of the common tree $\mathcal{T}_c$ in G_v and G_i. Then, each of the other two resistive branches may be chosen as a conductive tree branch or a resistive co-tree branch of $\mathcal{T}_c$, so this case (1) is divided into the following three cases: (i) $n_c = 3$, (ii) $n_c = 2$, and (iii) $n_c = 1$, where n_c denotes the number of the common tree branches. Case (1-i) $n_c = 3$: In this case, from the above statements, it is evident that we can select the tree $\mathcal{T}_c^i$ which consists of the port tree branch, a norator tree branch, two conductive tree branches, a nullator co-tree branch, and a resistive co-tree branch. Then, considering eq.(2) on the basis of the above $\mathcal{T}_c^i$ and the fact that

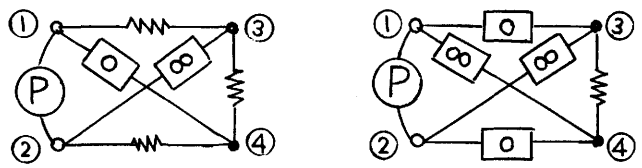

Fig.1. All minimal realization circuits of a negative resistor. In each figure in this paper, o and ∞ show a nullator and a norator, respectively.

in eq.(2) of this case (1-i) there is no redundancy corresponding to Lemmata 1 and 2, we obtain the following conditions; $F_{56} \neq 0$, $F_{RP} \neq 0$, all elements of $\underset{\sim}{F}_{RG}$ ($\in \mathbb{R}^{1\times 2}$) are non-zero, and moreover F_{56} ($\in \mathbb{R}^{1\times 1}$) $\neq 0$ because the nonsingular matrix $\underset{\sim}{F}_{56}$ is the 1×1 matrix in the case (1-i). Furthermore, since the principal submatrix of the fundamental loop matrix defined by eq.(2) is the totally unimodular matrix, without loss of generality it is assumed that $F_{56} = F_{RG} = F_{RP} = 1$, and $\underset{\sim}{F}_{RG} = [1,1]$. Let $\underset{\sim}{F}_{5G} = [a,b]$ and $\underset{\sim}{G} = \mathrm{diag}(G_1, G_2)$, where G_1 and G_2 denote the scalar positive conductances of two conductive tree branches. Then, substituting the above conditions into eq.(5), we have

$$\left\{ R + (1-a)G_1^{-1} + (1-b)G_2^{-1} \right\} (F_{5P} - 1) > 0, \tag{10}$$

namely

$$R + (1-a)G_1^{-1} + (1-b)G_2^{-1} > 0 \text{ and } F_{5P} > 1 \tag{11}$$

or

$$R + (1-a)G_1^{-1} + (1-b)G_2^{-1} < 0 \text{ and } F_{5P} < 1, \tag{12}$$

where R denotes the scalar positive resistance of a resistive co-tree branch. However, the condition of $F_{5P} > 1$ in eq.(11) and that of $R + (1-a)G_1^{-1} + (1-b)G_2^{-1} < 0$ in eq.(12) contradict the fact that F_{5P}, a, and b are the elements of the totally unimodular matrix $\underset{\sim}{F}$. Therefore, it is concluded in the case (1-i) of $n_c = 3$ that any negative resistor can not be realized.

Case(1-ii) $n_c = 2$: In this case, from the same reason as the case (1-i), it is evident that we can select the tree $\mathcal{T}_c^i$ which consists the port tree branch, a conductive tree branch, a nullator co-tree branch, and two resistive co-tree branches. Since the graph G_0 is assumed to be connected and the number of tree branches of $\mathcal{T}_c^i$ is three, the number of all nodes in the nullor-model network is four. In consideration of the bilaterality of the negative resistor, no mutual couplings between the branches in the nullor-model network, and no distinction between nullators and norators, it can be assumed that the network structure of the negative resistor seen at the port branch is symmetric. Consider eq.(2) on the basis of the above tree $\mathcal{T}_c^i$ and let $\underset{\sim}{F}_{RP}^T = [a_1, a_2]$, $\underset{\sim}{F}_{RG}^T = [b_1, b_2]$, and $\underset{\sim}{F}_{R6}^T = [c_1, c_2]$ for the simplicity of the explanation. Considering in eq.(2) of this case (1-ii) that there is no redundancy corresponding to Lemmata 1 and 2, we can assume that at least one element of each pair of (F_{5P}, F_{5G}), (a_1, b_1), (a_2, b_2), (a_1, a_2), (b_1, b_2), and (c_1, c_2) is non-zero.

From the above stated, first of all, the port branch, a nullator branch, and a norator branch can be fixed as shown in Fig.1 (a) without loss of generality. Since the nonsingular matrix $\underset{\sim}{F}_{56}$ is the 1×1 matrix in this case (1-ii) and is the submatrix of the totally unimodular matrix $\underset{\sim}{F}$, without loss of generality we obtain $F_{56} = 1$. Then, a conductive tree branch must be inserted between the node ③ and the node ④ in Fig.1 (a) because the fundamental loop associated with the nullator co-tree branch

in $\mathcal{T}_c^i$ must contain a norator tree branch. Hence, we have $F_{5P} = F_{55} = 1$. Secondly, it is assumed that the fundamental cut-set associated with the port tree branch in $\mathcal{T}_c^i$ must contain at least one resistive co-tree branch because of no redundancy corresponding to Lemmata 1 and 2 in the graph G_0. In consideration of the above stated and the elimination of the apparent redundancy (namely, the each parallel connection of a nullator branch and a resistive branch, a norator branch and a resistive branch, and a conductive branch and a resistive branch) in the graph G_0, it is assumed that two resistive co-tree branches must be inserted only between the node ① and the node ③, and the node ② and the node ④, respectively. Consequently, in this case (1-ii) of $n_c = 2$, the circuit in Fig. 1 (a) is obtained uniquely.

Case (1-iii) $n_c = 1$: In this case, from the same reason as the case (1-ii), it is evident that we can select the tree $\mathcal{T}_c^i$ which consists of the port tree branch, a norator tree branch, a nullator co-tree branch, and three resistive co-tree branches. Then, considering eq.(2) on the basis of the above tree $\mathcal{T}_c^i$ and the fact that there is no redundancy correspoding to Lemmata 1 and 2, we have the followings; $F_{5P} \neq 0$, all elements of $\underset{\sim}{F}_{RP}$ ($\in \mathbb{R}^{3\times 1}$) are non-zero, $\underset{\sim}{F}_{R6}$ ($\in \mathbb{R}^{3\times 1}$) $\neq \underset{\sim}{0}$, and moreover $F_{56} \neq 0$ because the non-singular matrix $\underset{\sim}{F}_{56}$ is the 1×1 matrix in this case (1-iii). Furthermore, since the principal submatrix of the fundamental loop matrix defined by eq.(2) is the totally unimodular one, without loss of generality, it is assumed that $F_{56} = F_{5P} = 1$ and $\underset{\sim}{F}_{RP}^T = [\ 1,1,1\ ]$. Let $\underset{\sim}{F}_{R6}^T = [a,b,c\ ]$ and $\underset{\sim}{R} = \mathrm{diag}(R_1, R_2, R_3)$, where R_1, R_2, and R_3 denote the scalar positive resistances of three resistive co-tree branches. Then, substituting the above conditions into eq.(5), we have

$$(a - 1)R_1^{-1} + (b - 1)R_2^{-1} + (c - 1)R_3^{-1} > 0. \tag{13}$$

However, eq.(13) contradicts the fact that a, b, and c are the elements of the totally unimodular matrix $\underset{\sim}{F}$. Therefore, it is concluded in this case (1-iii) of $n_c = 1$ that any negative resistor cannot be realized.

Case (2): Let us prove that the minimal realization circuit of a negative resistor by means of two nullors and a positive resistor is only the circuit shown in Fig. 1 (b). In this case, it is evident from the property (4) in the preliminaries that both G_v and G_i consist of the parallel connection of the port tree branch and a resistive co-tree branch. Therefore, consider eq.(2) on the basis of $\mathcal{T}_c^i$ which consists of the port tree branch, two norator tree branches, two nullator co-tree branches, and a resistive co-tree branch. Then, considering in the eq.(2) of this case (2) that there is no redundancy corresponding to Lemmata 1 and 2, we have the followings; $F_{RP} \neq 0$ and all elements of $\underset{\sim}{F}_{5P}$ ($\in \mathbb{R}^{2\times 1}$) and $\underset{\sim}{F}_{R6}$ ($\in \mathbb{R}^{2\times 1}$) are non-zero. Furthermore, since the principal submatrix of the fundamental loop matrix is totally unimodular, without loss of generality

it is assumed that $\underset{\sim}{F}_{5P}^{T} = [1,1]$, $F_{RP} = 1$, and $\underset{\sim}{F}_{R6} = [1,1]$. If there exists any one row vector with all non-zero elements in the row vectors of $\underset{\sim}{F}_{56}$ ($\in \mathbb{R}^{2\times 2}$), then the tree path formed by the nullator co-tree branch corresponding to the row vector is equal to that formed by the resistive co-tree branch. Hence, it is clear that there exists redundancy of the parallel connection of the nullator branch and the resistive branch in the graph G_o. Therefore, all the elements of each row vector of $\underset{\sim}{F}_{56}$ should not be non-zero. Similarly all the elements of each column vector of $\underset{\sim}{F}_{56}$ should not be non-zero. Then, without loss of generality, it is assumed that the 2x2 nonsingular matrix $\underset{\sim}{F}_{56}$ is the diagonal one.

From the above mentioned, all the elements of the principal submatrix $\underset{\sim}{F}$ of the fundamental loop matrix are determined and the matrix $\underset{\sim}{F}$ becomes

$$\underset{\sim}{F} = \left[\begin{array}{c|cc} \underset{\sim}{F}_{5P} & \underset{\sim}{F}_{56} \\ \hline F_{RP} & \underset{\sim}{F}_{R6} \end{array}\right] = \left[\begin{array}{c|cc} 1 & * & 0 \\ 1 & 0 & * \\ \hline 1 & 1 & 1 \end{array}\right], \tag{14}$$

where the symbol " * " denotes the non-zero element. By synthesizing the nullor-model network in accordance with eq.(14), the circuit of Fig.1(b) is uniquely obtained.

The proof of necessity was completed by the proofs of the cases (1) and (2).

Q.E.D.

5. IMPLEMENTATIONS

Although it has been already known that the negative resistor can be effectively realized by using operational amplifiers, even all the implementations of the minimal realization circuits in Fig.1 with operational amplifiers are not well-known. In this section, the implementations of the minimal realization circuits using operational amplifiers are considered. First of all, the implementation of the nullor using operational amplifiers is shown in Fig.2. The circuit of Fig.2(a) is a conventional operational amplifier with floating input port and unfloating output port and has widely been put to practical use, while the circuit of Fig. 2(b) is an operational amplifier with floating input and output ports, and had not been almost made practicable to be on the general market. However, the monolithic integrated nullor corresponding to the circuit of Fig.2(b)* has been recently developed by the integrated circuit tech-

*: The availability of such universal active elements makes it possible to minimize the number of active elements and passive precision elements in implementations of analog system functions, for example, as shown in Fig.3.

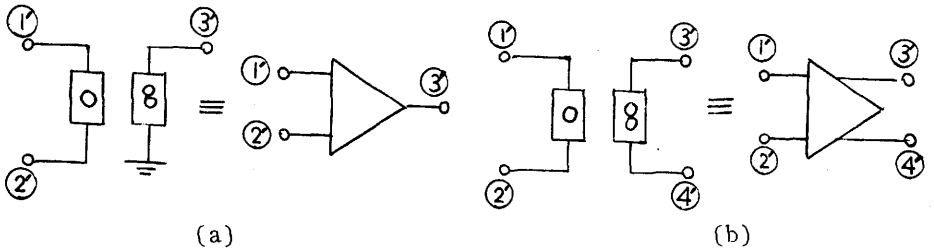

Fig.2. Implementations of a nullor using operational amplifiers. (a) A nullor with floating input port and unfloating output port. (b) A nullor with floating input and output ports.

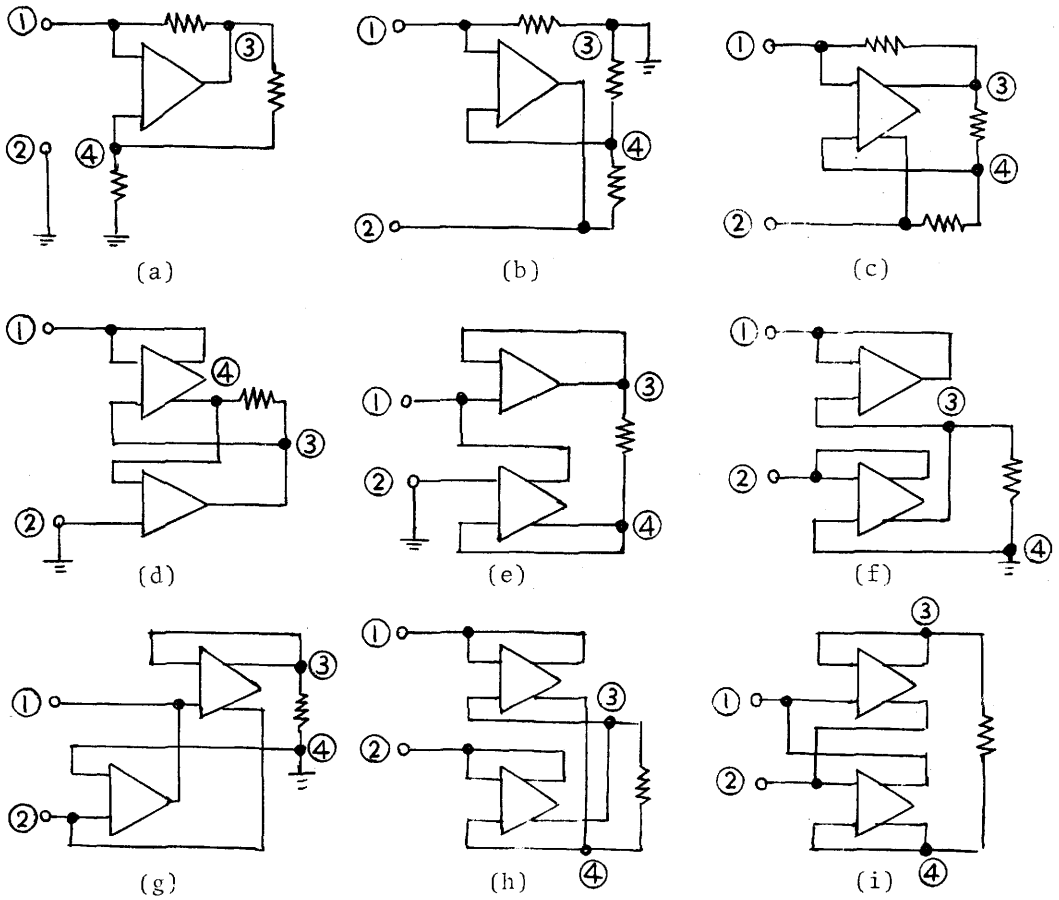

Fig.3. Implementations of the minimal realization circuits of a negative resistor using operational amplifiers. All the nodes ①, ②, ③, and ④ shown in Fig.3 correspond to those shown in Fig.1. Although the polarity of the input terminals in each operational amplifier is omitted, it should be selected by considering the stability of each circuit.

nique [9]. Therefore, it is considered significant to find all the implementations of the minimal realization circuits of a negative resistor in consideration of the existence of the circuit shown in Fig.2(b) in addition to that of the circuit shown in Fig.2(a).

The results of these implementations are easily obtained as shown in Fig.3, in which the circuits of (a), (b), and (c) are derived from that of Fig.1(a) and the circuits of (d), (e), (f), (g), (h), and (i), from that of Fig.1(b). Furthermore, it is to be noted in Fig.3 that the circuits of (b), (c), (f), (g), (h), and (i) are the floating negative resistors in contrast with those of (a), (d), and (e), and that only the circuits of (a) and (b) have been put to practical use. Therefore, we can expect much from the applications of the circuits of Fig.3(c)~ (i) to the active network synthesis.

6. CONCLUSIONS

This paper has strictly discussed the necessity of the Theorem 3 and guaranteed that all the topologically minimal realization circuits of a negative resistor are only the two circuits shown in Fig.1. Furthermore, all the usefull implementations of the minimal realization circuits by means of operational amplifiers are shown in Fig.3.

Finally, the following fact must be also noted. If the concept of " the chain bond between ports for the active N-port including one port" which gives the necessary and sufficient condition of the existence of transmission path between ports [10] is introduced, the Theorems 1,2, and 3 will be proved more easily and systematically. This will be appeared in detail elsewhere.

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