MEMOIRS OF THE FACULTY OF ENGINEERING
FUKUI UNIVERSITY
VOL. 29 NO. 2 1981

Noise and Transient Response Characteristics of Phase-Locked Loops

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(Received Aug. 31, 1981)

In designing a phase-locked loop to be used as a demodulator for PM or PSK signals two important criteria include short acquisition time and high accuracy. The settling time of phase step response and the steady-state phase error variance of a loop may be considered as measures of the acquisition time and the accuracy of the loop respectively. We have established relationships between the settling time of phase step response and the steady-state phase error variance for both of the first and second order loops. With this, it is a simple matter to find proper filter parameters for a satisfactory or nearly optimum loop performance with a short settling time and a small phase error variance.

I. INTRODUCTION

When we design a phase-locked loop (PLL) to be used as a demodulator for angle modulated or phase-shift-keyed (PSK) signals, there exist two important criteria that we must take into consideration. The first one is that the phase-locked loop should follow the change of phase of incoming signal as quickly as possible, and the second is that its steady-state mean square phase error should be kept as small as possible. Obviously these are contradictory requirements that cannot be satisfied simultaneously. Therefore, we have to make a compromise between fast response and small steady-state phase error variance. For this purpose it is necessary to investigate the relationships between phase step response and steady-state phase error characteristics of PLLs.

In this paper we will consider the PLL shown in Fig. 1 and specifically be concerned with relationships between the steady-state phase error variance and the settling time of phase step response of

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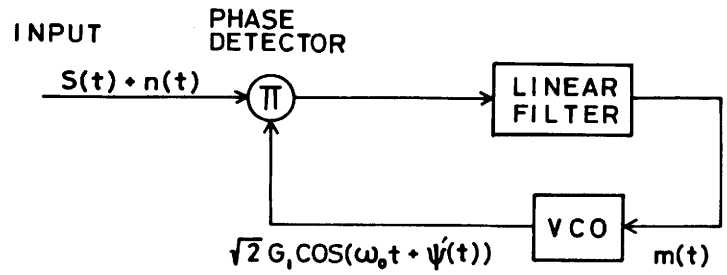


Fig. 1 Block diagram of phase-locked loop.

the PLL. The settling time may be considered as a control-theoretic measure of the loop's acquisition time, while the phase error variance gives an indication of the accuracy of the loop. The relationship will lead to a solution of the problem: what loop filter is to be placed in the loop or what filter parameters are to be chosen for a given loop in order to obtain a satisfactory performance of the loop.

II. PHASE STEP RESPONSE

In Fig. 1, the input to the PLL is the sum of a signal

$$s(t) = \sqrt{2}\, A \sin\{\omega_0 t + \psi(t)\} \tag{1}$$

and white Gaussian noise $n(t)$ of spectral density $N_0/2$. The output of voltage-controlled oscillator (VCO) is assumed to be $\sqrt{2}\, G_1 \cos\{\omega_0 t + \psi'(t)\}$.

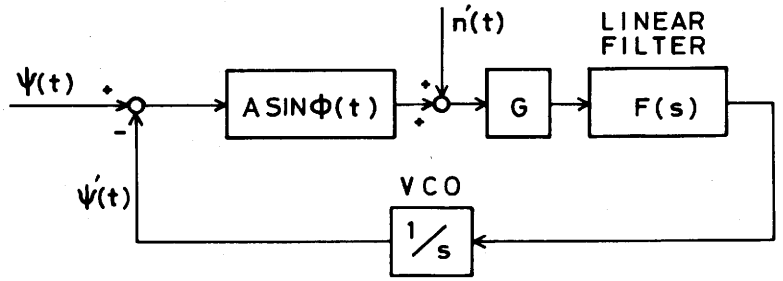


Fig. 2 Equivalent model for the PLL.

The block diagram depicted in Fig. 2 is a well-known equivalent model for the PLL system. It has been shown [1)-3)] that system operation may be described by the stochastic differential equation

$$\dot{\phi}(t) = \dot{\psi}(t) - G\, F(s)\{A \sin\phi(t) + n'(t)\};\ s = \frac{d}{dt}. \tag{2}$$

Here $\phi(t) = \psi(t) - \psi'(t)$ is the instantaneous phase error of the VCO with respect to the input signal $s(t)$, and $F(s)$ is the transfer function of the loop filter in operator form. The noise $n'(t)$ is Gaussian and essentially white at least over the frequency region up to ω_0, and its spectral density is $N_0/2$. The loop gain is given by $G = G_1 G_2$, where G_1 is the rms value of the VCO output and G_2 is a constant representing the sensitivity of the VCO; i.e., $\dot{\psi}'(t) = G_2 \cdot m(t)$.

In the following we shall consider the phase step response of the PLL for some typical loop filters. The loop is assumed to be noise-free.

For the first-order loop with phase step input, $F(s) = 1$ and $\dot{\psi}(t) = 0$, and (2) reduces to

$$\frac{d\phi(\tau)}{d\tau} = - \sin \phi(\tau), \tag{3}$$

where τ is time variable normalized with AG, i.e., $\tau = AGt$. The solution of (3) can be found to be

$$\tau = - \ln \left| \tan \frac{\phi}{2} \right|. \tag{4}$$

The equation (4) gives the transient response of the first-order loop to phase step input.

For the second-order noise free loop with a loop filter whose transfer function is $F(s) = 1 + (k/s)$, (2) becomes

$$\frac{d^2\phi(\tau)}{d\tau^2} + \cos \phi(\tau) \frac{d\phi(\tau)}{d\tau} + k' \sin\phi(\tau) = 0, \tag{5}$$

where $k' = k/AG$. Solving the second-order differential equation (5) numerically, we can obtain the transient response of the second-order loop to phase step input.

The third loop we will consider is the second-order loop with imperfect integrator. The transfer function of loop filter is given by $F(s) = (s + k)/(s + \Delta)$. For this loop (2) becomes

$$\frac{d^2\phi(\tau)}{d\tau^2} + \{\Delta' + \cos\phi(\tau)\} \frac{d\phi(\tau)}{d\tau} + k' \sin\phi(\tau) = 0, \tag{6}$$

where $\Delta' = \Delta/AG$. The equation (6) gives the phase step response of the particular second-order loop when solved numerically.

For the second-order loop with RC filter whose transfer function is $F(s) = a/(s + a)$, (2) becomes

$$\frac{d^2\phi(\tau)}{d\tau^2} + a' \frac{d\phi(\tau)}{d\tau} + a' \sin\phi(\tau) = 0, \tag{7}$$

where $a' = a/AG$.

For various choices of filter parameters and initial conditions, (5)-(7) have been solved numerically to obtain transient responses of the loops to phase step input. The settling time to characterize those responses has been defined as follows: the settling time τ_s of phase step response is defined as the value of τ for $|\phi(\tau)|$ to decrease to and stay within 5 or 10 per cent of $|\phi(0)|$.

III. SETTLING TIME VS. PHASE ERROR VARIANCE CHARACTERISTICS

As mentioned before, the settling time is a measure of the acquisition time of PLL, while the steady-state phase error variance gives an indication of the accuracy of the loop disturbed by the noise at the input.

The steady-state phase error variance σ_ϕ^2 is known to be given by [1)-3)]

$$\sigma_\phi^2 = \frac{\pi^2}{3} + \sum_{n=1}^{\infty} \frac{(-1)^n 4 I_n(\alpha)}{n^2 I_0(\alpha)}, \tag{8}$$

where α is the signal-to-noise ratio (SNR) in the bandwidth of the loop, and is given by

$$\alpha = \begin{cases} \frac{4A}{GN_0} & \text{(the first-order loop)}, \\ \frac{4A}{GN_0} \frac{1}{1+k'} & \text{(the second-order loop)}, \\ \frac{4A}{GN_0} \frac{1+\Delta'}{1+k'} & \text{(the second-order loop with imperfect integrator)}, \\ \frac{4A}{GN_0} & \text{(the second-order loop with RC filter)}. \end{cases} \tag{9}$$

The steady-state phase error variance and the settling time of phase step response are both related to loop filter parameters and loop gain. Therefore, the phase error variance can be related to the settling time through loop filter parameters.

Figure 3 shows relations between the magnitude of phase step and the settling time for the first-order loop. From this figure we can obtain the settling time $\tau_s = AGT_s$ of the first-order loop for any combination of the magnitude of phase step and the value of AG. Here T_s is a settling time in second corresponding to τ_s.

Figure 4 indicates relation between the SNR $\alpha = 4A/GN_0$ and the

steady-state phase error variance σ_ϕ^2 for the first-order loop. As α decreases, σ_ϕ^2 increases as expected.

In Fig. 5 the phase error variance is shown as a function of the settling time for the second-order loop with various initial conditions and SNRs. As is apparent from the definition of the SNR, i.e., $\alpha = (4A/GN_0)/(1+k')$, the phase error variance of the second-order loop approaches that of the first-order loop as k' decreases. Observe that, as k' is increased, the phase error variance increases, while the settling time decreases for small k'. But it starts to swing back and forth as k' is increased further. This may be explained as follows: As k' increases, α decreases and as a result the phase error variance increases. On the other hand, as we can expect from the fact that the damping coefficient of the linearized second-order loop is equal to $1/2\sqrt{k'}$, the loop becomes less damped and the step response tends to be more oscillatory as k' increases. This results in the swinging behavior of the settling time.

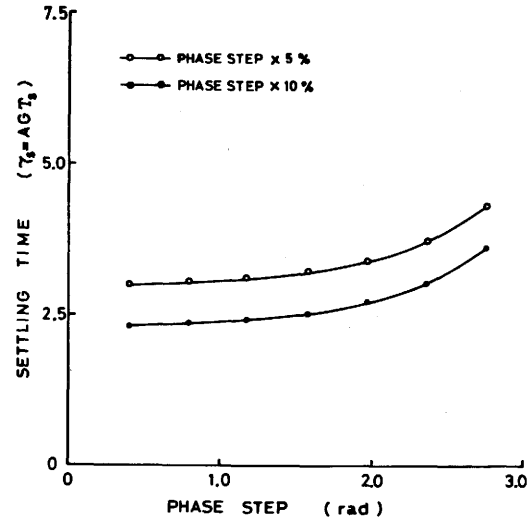


Fig. 3 Relations between magnitude of phase step and settling time for first-order loop.

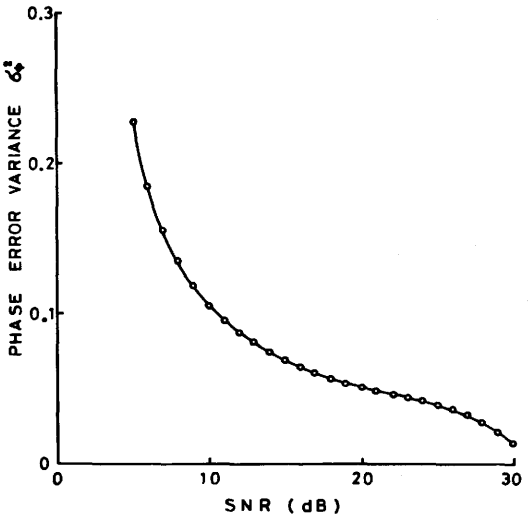


Fig. 4 Relation between SNR and steady-state phase error variance for first-order loop.

There is another observation besides the above. The value of k' which minimizes the settling time tends to decrease as the magnitude of phase step increases. This is illustrated in Fig. 6, which shows relations between the shortest attainable settling time and the phase error variance for various magnitudes of the phase step. This

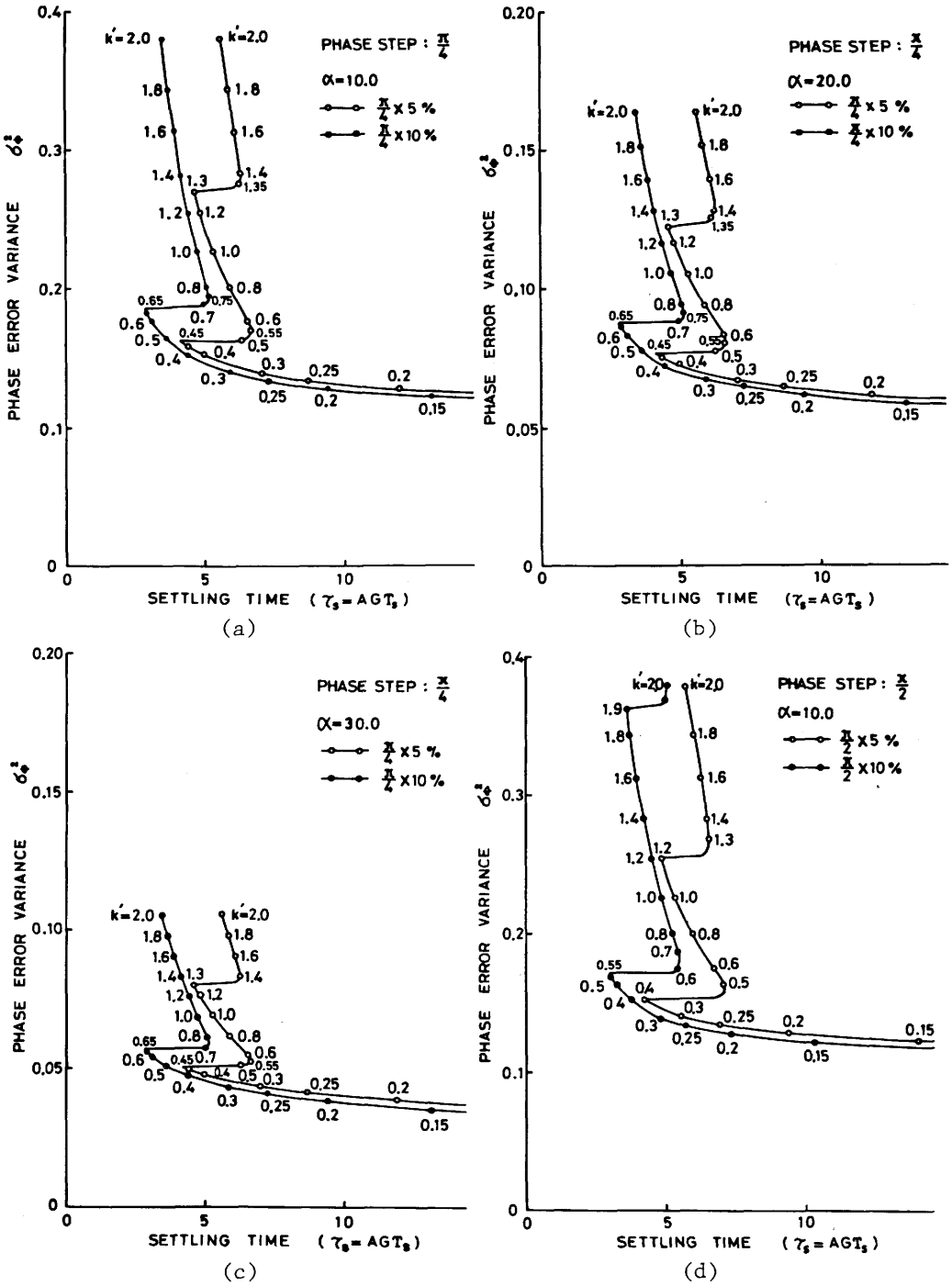


Fig. 5 Settling time vs. phase error variance characteristics of second-order loop.

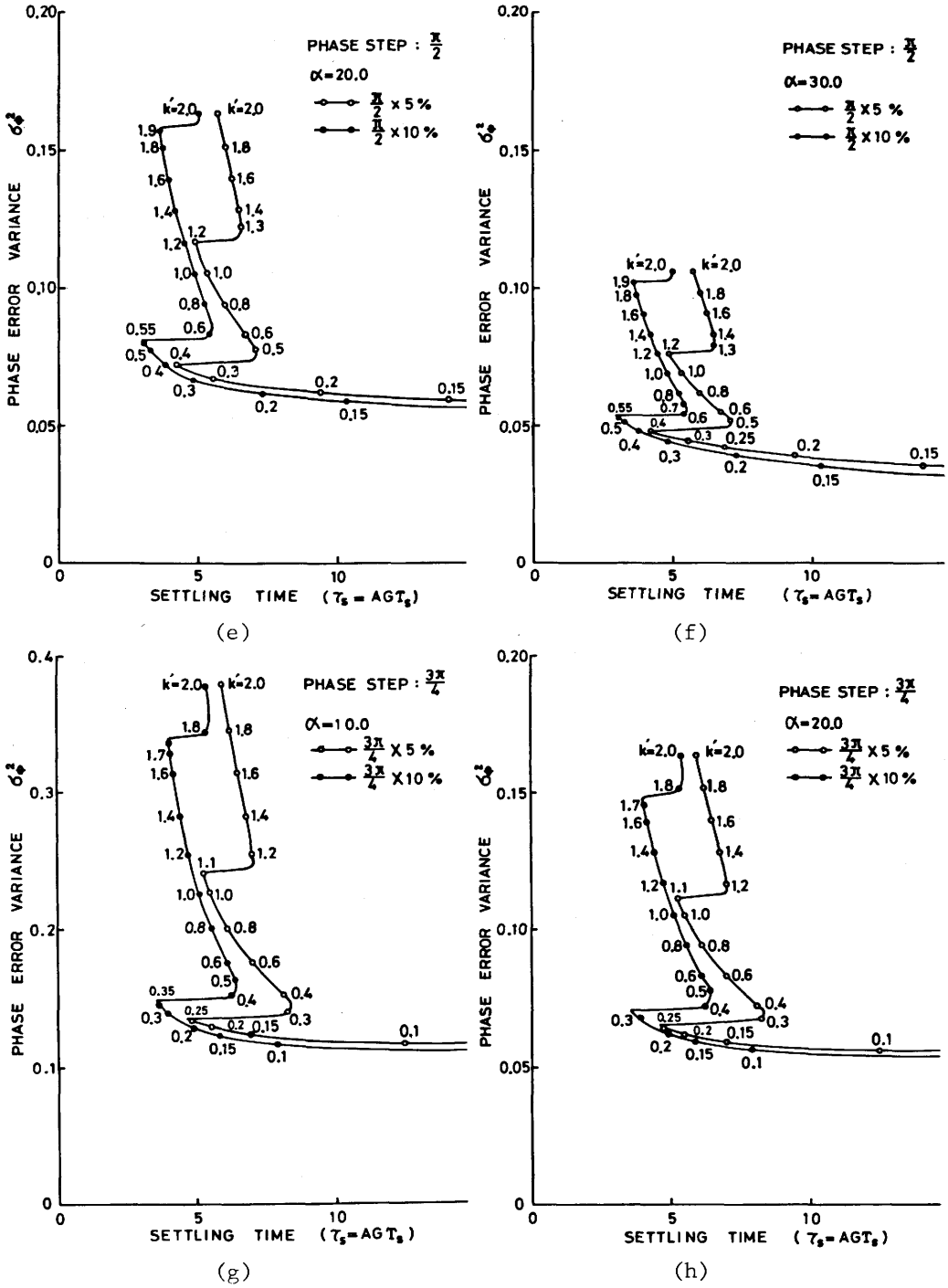
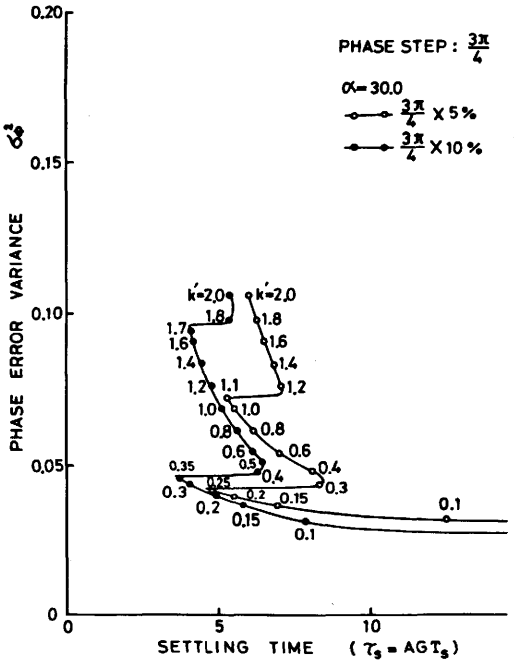


Fig. 5 (Continued)



(i)

Fig. 5 (Continued)

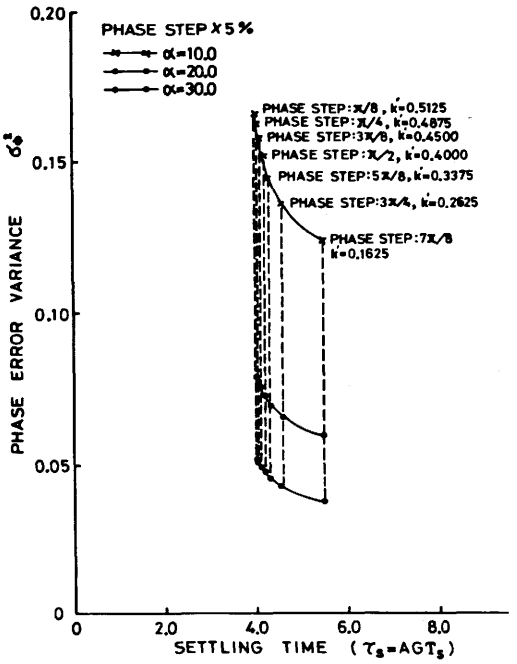


Fig. 6 Relations between shortest attainable settling time and phase error variance for second-order loop.

observation tells us a fact that in order to obtain a fast acquisition it is necessary to make the loop less damped as the magnitude of phase step increases.

Figure 7 shows the settling time vs. phase error variance characteristics of the second-order loop with imperfect integrator. Observe that the phase error variance for the particular loop is slightly less than that for the second-order loop. This agrees with the fact that the SNR for the second-order loop with imperfect integrator is $(1 + \Delta')$ times as large as the SNR for the second-order loop as is obvious from (9). Here Δ' is arbitrarily chosen to be 0.1.

Figure 7 can be of use for finding a proper value of k' which will make both of the settling time and the phase error variance small.

Figure 8 shows the shortest attainable settling time vs. the phase error variance characteristics for the second-order loop with imperfect integrator.

The phase error variance of the second-order loop with RC filter

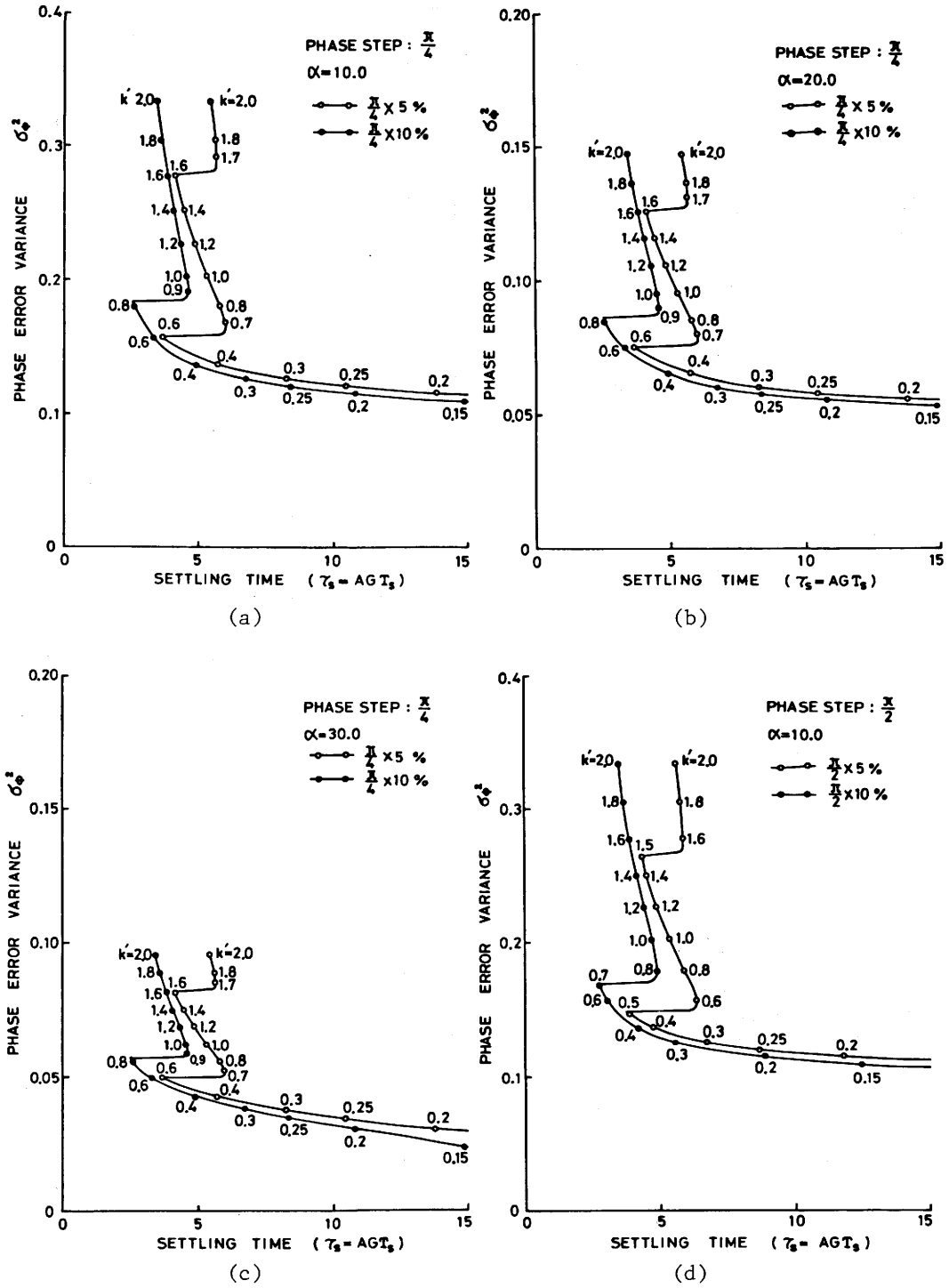
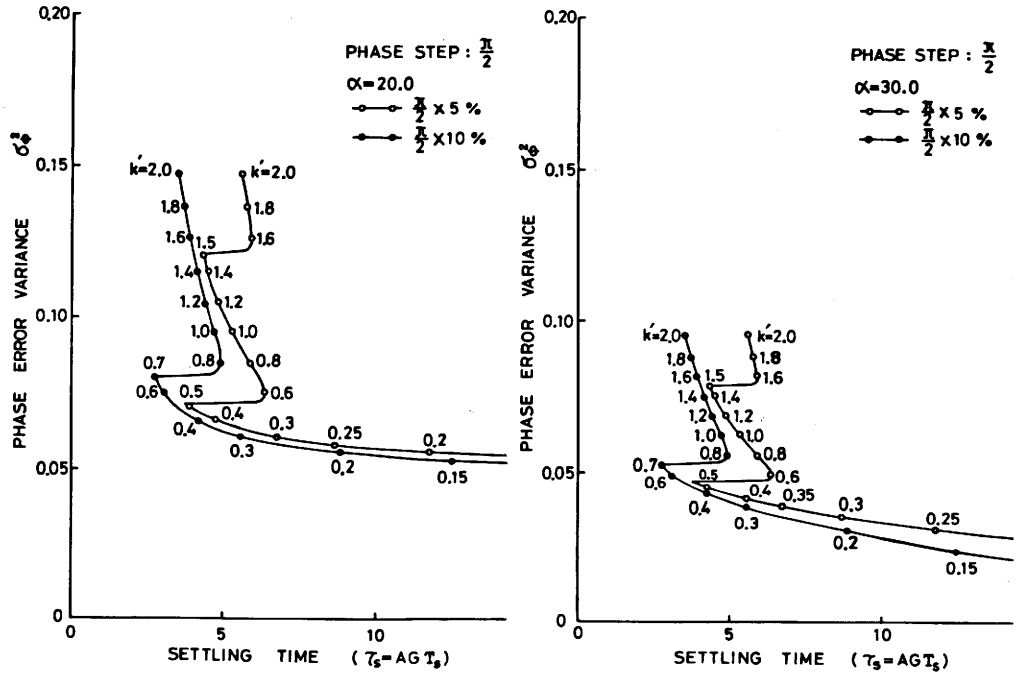


Fig. 7 Settling time vs. phase error variance characteristics of second-order loop with imperfect integrator.



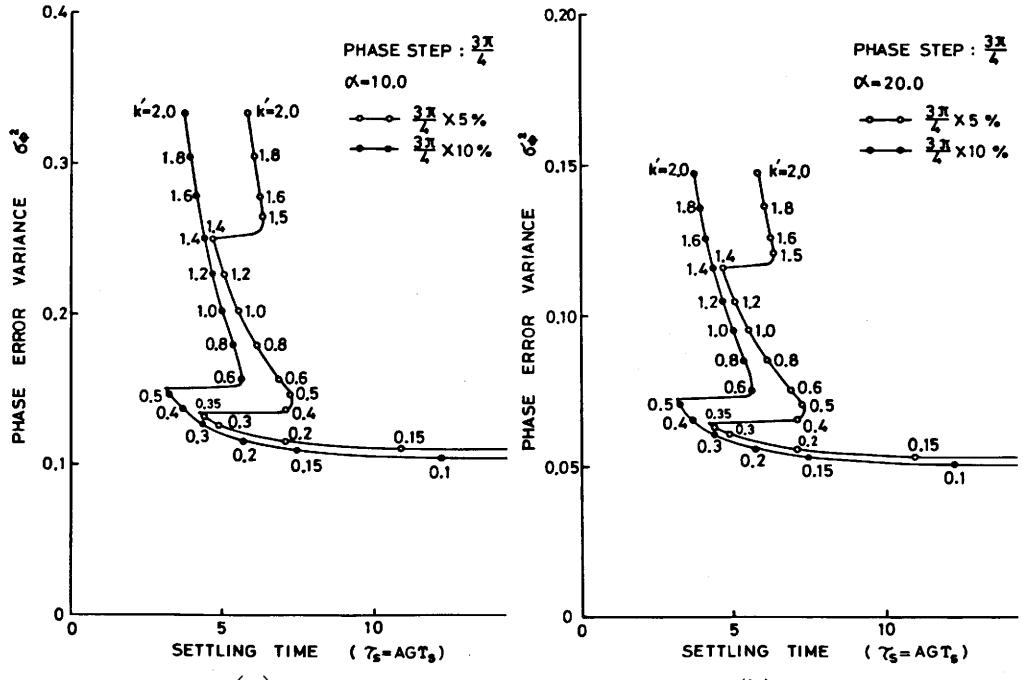
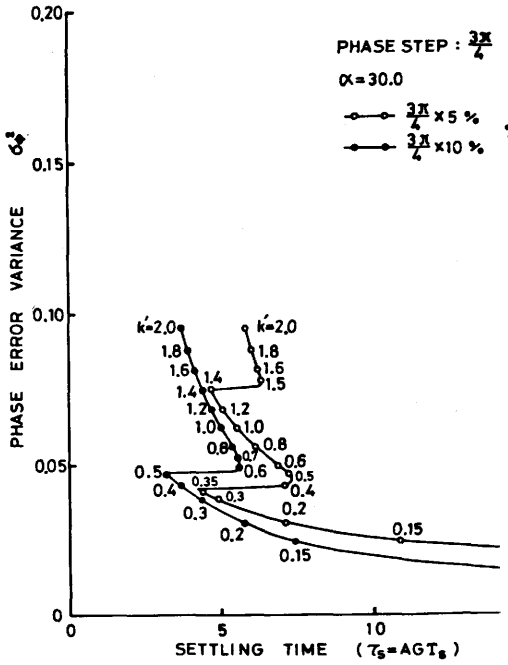


Fig. 7 (Continued)



(i)

Fig. 7 (Continued)

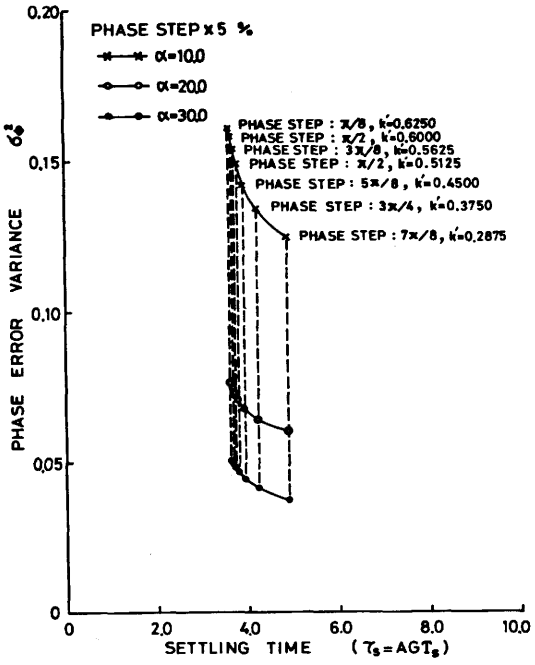


Fig. 8 Relations between shortest attainable settling time and phase error variance for second-order loop with imperfect integrator.

is the same as that of the first-order loop irrespective of the value of a'. However, its settling time is longer than that of the first-order loop. For example, it is nearly four times as long as that of the first-order loop when a' = 0.5.

For phase step input, the shortest settling time and the smallest phase error variance are attained by the first-order loop. However, this does not necessarily imply the unconditional superiority of the first-order loop over higher order loops. If the quiescent frequency of the VCO is caused to change from ω_0 to any other frequency ω by the change of power supply voltage or ambient temperature or by any other extraneous disturbance, the first-order loop will not be able to correct the frequency error $\omega - \omega_0$ by itself and a steady-state phase error of $(\omega - \omega_0)/AG$ will remain.

On the other hand the second-order loop has not only the shortest settling time and the smallest phase error variance among all the second-order loops but also a capability of correcting frequency error. In view of this the second-order loop may be considered to be

most preferable as a demodulator for PM or PSK signals.

The other second-order loops will also have nonzero steady-state phase error, if the quiescent frequency of VCO is different from the carrier frequency ω_0 of incoming signal. The steady-state phase error for the second-order loop with imperfect integrator is $(\Delta/k)(\omega - \omega_0)/AG$, which is less than that of the first-order loop when $k > \Delta$.

With the help of the result given above it is possible for us to find a proper loop filter and its parameters for a satisfactory loop performance, when the loop is used as a demodulator for PM or PSK signals.

IV. CONCLUSIONS

We have established relationships between the settling time of step response and the steady-state phase error variance for both of the first and second-order loops. With this, it is a simple matter to find proper filter parameters for a satisfactory or nearly optimum loop performance with a short settling time and small offset and steady-state phase error variance which imply a short acquisition time and a high accuracy respectively.

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