

WARP, a Unified Wireless Network Testbed for Education and Research

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Abstract

In this paper, we introduce the Wireless Open-Access Research Platform (WARP) developed at CMC lab, Rice University. WARP provides a scalable and configurable platform mainly designed to prototype wireless communication algorithms for educational and research oriented applications. Its programmability and flexibility makes it easy to implement various physical and network layer protocols and standards. Moreover, the online open-access WARP repository is used to document and share different wireless architectures and cross-layer designs developed at educational and research centers. This repository is a fast and easy solution for students and researchers with a wide range of backgrounds in hardware implementation and algorithm development to collaborate and initiate multi-disciplinary system designs.

1 WARP Platform Architecture

Rice University's WARP [2] is a scalable, extensible and programmable wireless platform, built from the ground up, to prototype wireless networks. The platform architecture consists of four key components: custom hardware, platform support packages, open-access repository and research applications; all together providing a reconfigurable wireless testbed for students and faculty. Figure 1 shows the WARP board along with four daughtercards.

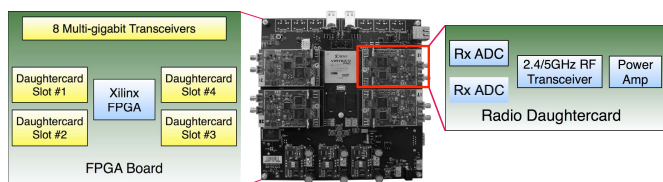


Figure 1. WARP board with radio daughtercards.

1.1 Custom Baseband Hardware

To balance the computational needs of wireless systems operating at hundreds of Mbits/sec with the flexibility and programmability needed for wireless systems, we choose Xilinx Virtex-II Pro FPGAs as the primary communication processor on the main board. The PowerPC processors embedded in the FPGAs provide a complete embedded programming environment for MAC and network layer design. The dedicated multi-gigabit transceivers (MGTs) provide high speed board-to-board connections which make the WARP platform scalable and extendable.

One of the main features of WARP hardware, which makes it distinguishable from other similar boards designed for educational purposes, is its four daughtercard slots that can be used to connect radio boards. These radio boards, designed fully by Rice University students, can be attached to the main board so that up to a 4×4 multiple-input multiple-output (MIMO) system can be built. The availability of a multi-antenna radio testbed results in broader educational experiences and opportunities that enable students to understand various aspects of wireless systems such as coding, synchronization, modulation and RF IQ imbalances.

1.2 Development Tools

For physical layer design, the platform supports different levels of design flows from low level VHDL/Verilog RTL coding to system level MATLAB modeling. Xilinx "System Generator" is one of the system-level modeling tools integrated in MATLAB that provides abstractions for building and debugging high-performance DSP systems in MATLAB/Simulink using the Xilinx Blockset. Moreover, the WARP board supports Simulink "hardware co-simulation" that expedites the simulation and debugging steps.

For MAC and network layer design, the WARP platform supports "C" based applications on the PowerPC while interfacing the physical layer implementations in the FPGA fabric. The Xilinx "Platform Studio" tool is an integrated programming environment that is used to control both the physical layer and MAC layer implementations.

1.3 Online Open-Access Repository

One of the most important educational features of the WARP platform is its open-access repository [3]. Accessible from the Internet, the repository is the central archive for all source codes, models, platform support packages, application building blocks, research applications, design documents and hardware design files associated with WARP. The contents of the repository are verified by the project administrator at Rice University. The students can ask questions and exchange ideas about different algorithmic and hardware implementation subjects on the WARP forum, through the repository webpage.

2 Prototyping Designs and Algorithms

WARP provides a unique platform to develop, implement and test advanced wireless algorithms. Physical (PHY) and Media Access Control (MAC) layer designs, developed at the Rice University CMC lab and available in the online repository, have been implemented and tested on WARP as examples to show the flexibility of the platform.

The embedded PowerPC core in the Xilinx FPGA has been programmed using the C language to implement a flexible medium access development framework, WARPMAC [4]. This framework is in fact a set of software routines that can be used by network students and researchers to develop various advanced MAC and networking protocols, e.g. multi-hop and relay networks, while abstracting away the physical layer.

The Xilinx FPGAs deployed in WARP boards provide significant processing resources to implement and test complicated physical (PHY) layers. Currently, two different PHY have been implemented and fully verified in over-the-air tests [3]. The single-input single-output (SISO) Orthogonal Frequency Division Multiplexing (OFDM) transceiver uses the FPGA for all the baseband processing. The up-conversion to the RF band is carried out using one radio daughtercard [6] in each WARP node. Furthermore, a 2×2 MIMO OFDM transceiver, i.e. two daughtercard radio boards for each WARP node, has been designed and is currently in the process of being tested on the WARP hardware.

In order to study the effects of exploiting novel wireless algorithms and techniques, they have been tailored to fit in the WARP architecture, e.g. [5], while using the MAC layer framework described earlier in this section. Sphere detection and LDPC decoding are currently in the process of being incorporated in the MIMO OFDM PHY developed for WARP.

3 Educational Courses and Workshops

Flexibility and programmability makes WARP suitable for different educational applications. For instance, in

courses such as High Speed Embedded System Design, ELEC 424 at Rice University, students may design various daughtercards, e.g. video boards, 4 channel A/D conversion and etc., that fit into the WARP board to extend the functionality of the board. In general, WARP can be potentially used in courses that involve design and implementation of wireless communications, e.g. Architecture for Wireless Communications [1], where students can design and implement different blocks of a communication link; Advanced VLSI Design course, ELEC 522, where the final projects are the design and implementation of a 4×4 matrix QR decomposition block as well as various FIR filters. From a network layer perspective, this platform can be used in networking courses/labs to implement and test different well-studied MAC layer algorithms, and verify their performance.

A number of workshops have been held at Rice University as well as other universities and research centers, e.g. National Chiao Tung University and IIT Delhi, to further expand the use of the WARP platform. Additional workshops are scheduled for 2007 and 2008.

4 Conclusion

In this paper, we introduced WARP as a platform that can be used for educational and research applications to prototype various wireless communications algorithms. The simplicity of the design flow and the flexibility of the platform make WARP a suitable solution that can be extensively used by researchers and students with different backgrounds in computer engineering, communications and networking. Also, the online open-access repository, a major part of WARP, distributes the designs and contributions of each user to all other users.

5 Acknowledgement

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