A Family of PFC Voltage Regulator Configurations with Reduced Redundant Power Processing

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***Abstract*—This paper discusses a systematic method for deriving basic converter configurations that achieve power factor correction (PFC) and voltage regulation. The discussion begins with a general three-port representation of power supplies that provide PFC and voltage regulation. Based on this representation and a power flow consideration, a systematic procedure is derived to generate all possible minimal configurations. Among these configurations, only a few have been known previously and used in practice. It is found that the efficiency of PFC voltage regulators can be improved by reducing the amount of redundant power to be processed by the constituent converters. A systematic circuit synthesis procedure is proposed for creating PFC voltage regulators with reduced redundant power processing. Experimental measurements verify the improved efficiency.**

***Index Terms*—Circuit synthesis, power factor correction, switching converters, topologies.**

I. Introduction

HIGH power factor and low input-current harmonics are becoming mandatory design criteria, in addition to a tight output voltage regulation, for switching power supplies with input power exceeding 75 W. Recently, there have been numerous attempts in combining a power-factor-correction (PFC) switching stage with a conventional dc/dc converter to form a high-power-factor voltage regulator which converts power from the ac line to the load. The PFC stage is typically a switching converter operating in discontinuous conduction mode (DCM) or under a special current-mode control scheme. Of much research interest is, moreover, the amalgamation of two stages to form the required PFC voltage regulator [1]–[9]. The basic requirement of the afore-described combined system, to which we simply refer as *PFC regulator*, is the presence of an energy storage element which buffers the difference between the instantaneous input power and the output power [6], [10]. In the case of a PFC regulator having unity input power factor and perfect output regulation, the input power is $2P_o \sin^2 \omega_m t$, where P_o is the output power and ω_m is the line angular frequency. The instantaneous power buffered by the storage is thus given by $P_o(1-2\sin^2 \omega_m t)$ or $P_o \cos 2\omega_m t$, which varies at twice the line frequency.

Since a low-frequency energy storage is mandatory in a voltage regulator with PFC capability, the general configuration may be represented by a three-port network terminating in an input voltage, a low-frequency storage element and an output load, as shown in Fig. 1. Based on this three-port model, a number of minimal practical PFC voltage regulator configurations are derived in this paper. These circuit configurations are then compared, first of all, in terms of their efficiency. A particularly illuminating result of this study is that efficient PFC regulators can be constructed by selecting appropriate configurations that can prevent the power processed by one converter from being re-processed entirely by another converter within the PFC regulator. This leads to the idea of *reduced redundant power processing* (R^2P^2). Our main focus is the derivation of a practical circuit synthesis process for creating R^2P^2 PFC regulators. Finally, we present experimental evidence of the enhanced efficiency of a chosen R^2P^2 PFC regulator.

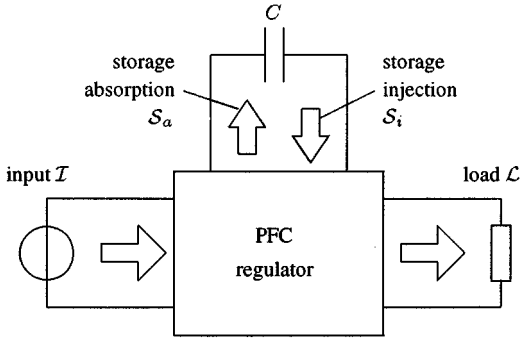

Fig. 1. Three-port model of a PFC switching regulator.

II. Configurations of PFC Regulators Based on Power Flow Graphs

Since the primary objective of a PFC regulator is to transfer power from the input port to the load port with low-frequency buffering in the storage element, we begin with the basic process of power flow between the three ports of a PFC regulator.

We first introduce, for ease of presentation, *power flow graphs* for describing the way in which power is transferred among the three ports. The branches in a power flow graph denote the paths through which power is being transferred, and the arrows on the branches indicate the direction of power flow. One or more branches form a *power flow sub-graph*, or simply *sub-graph*. For a three-port network, it is clear that only three types of sub-graphs can be used to connect the ports:

Type I: Power is transferred from one port to another port [Fig. 2(a)].

Type II: Power is transferred from two ports to one port [Fig. 2(b)].

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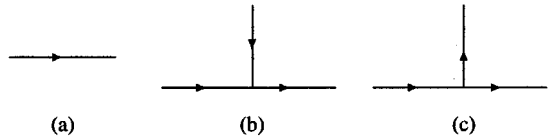

Fig. 2. Power flow sub-graphs. (a) Type I. (b) Type II. (c) Type III.

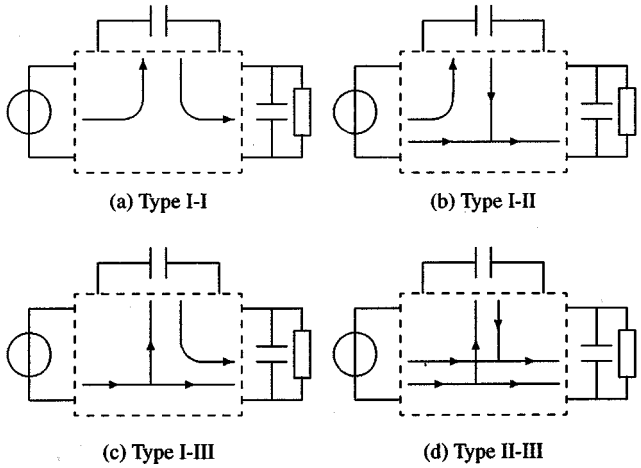

Fig. 3. Power flow graphs for PFC regulators. (a) Type I-I. (b) Type I-II. (c) Type I-III. (d) Type II-III.

Type III: Power is transferred from one port to two ports [Fig. 2(c)].

Now we can construct the complete power flow graph for a PFC regulator using the three types of sub-graphs of Fig. 2. Clearly, there are only four possible constructions, each comprising two sub-graphs. For ease of reference, we denote the complete power flow graph by Type I-I if it involves two Type I sub-graphs. For a power flow graph that involves one Type I sub-graph and one Type II sub-graph, we refer to it as Type I-II. Likewise, we also have Type I-III and Type II-III power flow graphs, as shown in Fig. 3.

Finally, since the minimal configuration requires two simple converters, we complete the derivation by putting two converters in the appropriate paths of the power flow graph. In particular we consider putting one converter to each sub-graph in order to take full control of power flow to and/or from each port. Also, for each Type II and Type III sub-graph, we have three possible ways of placing a converter. Hence, *sixteen configurations of PFC regulators are possible.* For simplicity, we denote them as Configuration I-I, Configuration I-IIA, Configuration I-IIB, Configuration I-IIC, Configuration I-IIIA, Configuration I-IIIB, Configuration I-IIIC, etc., as shown in Fig. 4.

Based on these configurations, we can construct actual circuits using two simple converters. For the cascade configuration, i.e., Configuration I-I, many topologies have been proposed previously [2]–[4]. The well-known BIFRED circuit is an example of Configuration I-IIIB. In García *et al.* [8], a practical circuit was proposed again for Configuration I-IIIB, but with two duty-cycle control for achieving PFC and output regulation. In Jiang *et al.* [3], yet another circuit of Configuration I-IIIB was proposed. Table I lists some previously reported circuits and their respective configurations. Instead of studying these circuits individually, our focus in this paper is to derive a systematic method for generating practical PFC regulators, and specifically those which can reduce the amount of redundant power processed by the constituent converters.

III. Comparison of Efficiency

Intuitively, the cascade configuration, i.e., Configuration I-I, has a poor efficiency since the input power is processed by the two converters "serially" before reaching the load. If η_1 and η_2 are the efficiencies of the two converters, the overall efficiency of Configuration I-I is given by $\eta_{I\text{-}I} = \eta_1\eta_2$.

For Configuration I-IIA, the efficiency is expected to be higher than $\eta_1\eta_2$ since part of the input power goes through only one converter stage. Suppose the input power is split, in a ratio of k to $1-k$, into converters 1 and 2, as shown in Fig. 4(b). The efficiency in this case is

$$\begin{aligned}\eta_{\text{I-IIA}} &= k\eta_1\eta_2 + (1-k)\eta_2 \\ &= \eta_1\eta_2 + (1-k)\eta_2(1-\eta_1) \\ &> \eta_1\eta_2 \qquad \text{for all } 0 < k < 1. \end{aligned} \tag{1}$$

For Configuration I-IIC, we assume that the input power is split, in a ratio of k to $1-k$, into converters 1 and 2, as shown in Fig. 4(c). The efficiency is given by

$$\begin{aligned}\eta_{\text{I-IIB}} &= k\eta_1 + (1-k)\eta_2 > \min\{\eta_1, \eta_2\} \\ &\qquad \text{for all } 0 < k < 1 > \eta_1\eta_2. \end{aligned} \tag{2}$$

Likewise, the efficiencies of the other configurations can be found, as tabulated in Table II. It is readily shown that Configurations I-IIA through IIC-IIIC all have a higher efficiency than Configuration I-I. In other words, *the lower bound of the efficiency of a PFC regulator, η, is theoretically equal to $\eta_{I\text{-}I}$, i.e., $\eta \le \eta_1\eta_2$.*

The above theoretical efficiency calculation does highlight a possible way to the design of inherently efficient PFC regulators, which is to minimize redundant power processing of the two constituent converters.

IV. Derivation of Practical PFC Regulator Circuits With Reduced Redundant Power Processing

In Section II, sixteen basic configurations of PFC regulators have been derived, each of which is composed of two basic switching converters. One of these is the conventional cascade configuration in which a PFC stage is cascading with a dc/dc converter stage [4]–[7]. The other fifteen have noncascading structures which, as shown above, have a higher efficiency compared to the cascade configuration. The improved efficiency can be attributed to the *reduced-redundant-power-processing* feature of the noncascading structures. However, not all fifteen configurations can be readily implemented in practical forms. Upon close inspection of these configurations, we can readily conclude that out of the fifteen configurations, four permit simple interconnections and transformer isolation, namely, configurations I-IIA, I-IIB, I-IIIA and I-IIIB [Fig. 4(b), (c), (e) and (f)]. In the following, we present a systematic procedure for synthesizing PFC regulator circuits that arise from these four basic configurations.

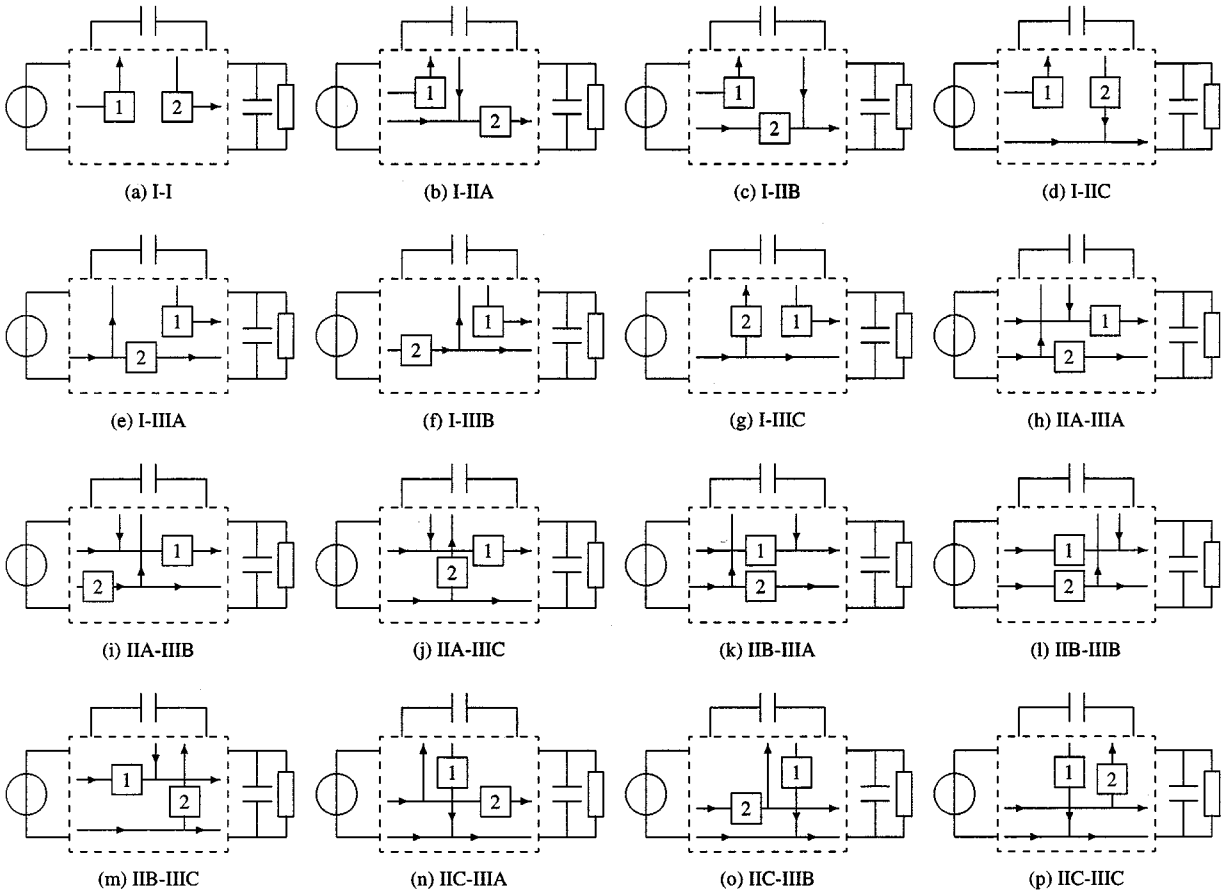

Fig. 4. Configurations of PFC regulators in terms of power flow. Solid square boxes denote simple converters.

TABLE I
PREVIOUSLY REPORTED PFC REGULATOR CIRCUITS

PFC regulator circuit	Configuration
Ćuk, SSIPP [4], BIBRED [2]	I-I
Zeta	I-IIA
SEPIC, BIFRED [2]	I-IIIB
PPFC [3]	I-IIIB
García circuit [8]	I-IIIB

A. Transformation of Power Flow Graphs into Equivalent Circuits

Since the input and load are voltage terminated, the use of voltage converters and capacitive storage becomes a convenient choice. The basic voltage converters are shown in Fig. 5. In general, an R^2P^2 circuit can be realized by two voltage converters connecting the input, storage and load ports. The crucial question is how to connect the ports with two converters, such that the power flow configuration concerned can be realized.

In transforming the power flow representations of Fig. 4(b), (c), (e) and (f) into practical circuits, the following basic connection rules should be observed:

1) Since the ports are voltage terminated, connection of any two ports simultaneously to a converter should be realized by a *series circuit connection.*
2) Connection of a port with the inputs (or outputs) of two converters should be realized by a *parallel circuit connection.*

Based on these rules and Fig. 4, we can develop equivalent circuit representations for the four basic configurations of R^2P^2 PFC regulators, as shown in Fig. 6.

B. Placement of Constituent Basic Converters

The next logical step in the synthesis process is to place converters appropriately in the rectangular boxes of Fig. 6, paying attention to the polarity markings of the input and output terminals of the converters. In general, referring to Fig. 5, power flows through a converter from terminals X^+X^- to Y^+Y^-. Thus, in order to ensure power flows in the appropriate directions, we place converters in the circuits of Fig. 6 in such a way that terminals X^+X^- and Y^+Y^- of the basic converters of Fig. 5 match those in the R^2P^2 PFC regulator circuits. However, the choice of basic converters to be placed in the R^2P^2 PFC regulator circuits is not arbitrary, as will be discussed in the next subsection.

C. Constraints on the Choice of Basic Converters

We now consider using nonisolated basic converters for realizing converters 1 and 2, and examine the constraints in the choice of converters. We first observe that all nonisolated converters have a direct short-circuit path between input and output terminals, during the entire or part of a switching period.

TABLE II
THEORETICAL EFFICIENCIES (WHERE $0 < k < 1$ AND $0 < m < 1$). EXPRESSIONS ARRANGED FOR EASY COMPARISON WITH $\eta_1\eta_2$

Config.	Efficiency	
I-I	$\eta_1\eta_2$	
I-IIA	$\eta_1\eta_2 + (1-k)\eta_2(1-\eta_1)$	where $(1-k)\eta_2(1-\eta_1) > 0$
I-IIB	$k\eta_1 + (1-k)\eta_2$	where $k\eta_1 + (1-k)\eta_2 > \min\{\eta_1, \eta_2\} > \eta_1\eta_2$
I-IIC	$\eta_1\eta_2 + (1-k)(1-\eta_1\eta_2)$	where $(1-k)(1-\eta_1\eta_2) > 0$
I-IIIA	$k\eta_1 + (1-k)\eta_2$	same as I-IIB
I-IIIB	$\eta_1\eta_2 + (1-k)\eta_2(1-\eta_1)$	same as I-IIA
I-IIIC	$\eta_1\eta_2 + (1-k)(1-\eta_1\eta_2)$	same as I-IIC
IIA-IIIA	$k\eta_1 + (1-k)\eta_2$	same as I-IIB
IIA-IIIB	$\eta_1\eta_2 + m(1-k)\eta_2(1-\eta_1) + k\eta_1(1-\eta_2)$	where $m(1-k)\eta_2(1-\eta_1) + k\eta_1(1-\eta_2) > 0$
IIA-IIIC	$\eta_1\eta_2 + m(1-k)(1-\eta_1\eta_2) + k\eta_1(1-\eta_2)$	where $m(1-k)(1-\eta_1\eta_2) + k\eta_1(1-\eta_2) > 0$
IIB-IIIA	$\eta_1\eta_2 + \eta_1\eta_2\left[\frac{km}{\eta_1}\left(\frac{1}{\eta_2}-1\right) + \left(\frac{(1-k)\eta_1+k\eta_2}{\eta_1\eta_2}-1\right)\right]$	where $(1-k)\eta_1 + k\eta_2 > \eta_1\eta_2$ (see I-IIB)
IIB-IIIB	$k\eta_1 + (1-k)\eta_2$	same as I-IIB
IIB-IIIC	$\eta_1\eta_2 + \eta_1\eta_2\left[\frac{km}{\eta_1}\left(\frac{1}{\eta_2}-1\right) + \left(\frac{(1-k)\eta_1+k\eta_2}{\eta_1\eta_2}-1\right)\right]$	where $(1-k)\eta_1 + k\eta_2 > \eta_1\eta_2$ (see I-IIB)
IIC-IIIA	$\eta_1\eta_2 + \eta_1\eta_2\left[\frac{(1-k)\eta' + k\eta_1\eta_2}{(\eta_1\eta_2)\eta'} - 1\right]$	where $\eta' = \frac{\eta_1\eta_2}{(1-m)\eta_1 + m\eta_2}$ and $(1-k)\eta' + k\eta_1\eta_2 > \eta_1\eta_2\eta'$
IIC-IIIB	$\eta_1\eta_2 + \eta_1\eta_2\left[k + \left(\frac{(1-k)\eta_2 + k\eta''}{\eta_2\eta''} - 1\right)\right]$	where $\eta'' = \eta_1\eta_2$ and $(1-k)\eta_2 + k\eta'' > \eta_2\eta''$
IIC-IIIC	$\eta_1\eta_2 + (1-km)(1-\eta_1\eta_2)$	where $(1-km)(1-\eta_1\eta_2) > 0$

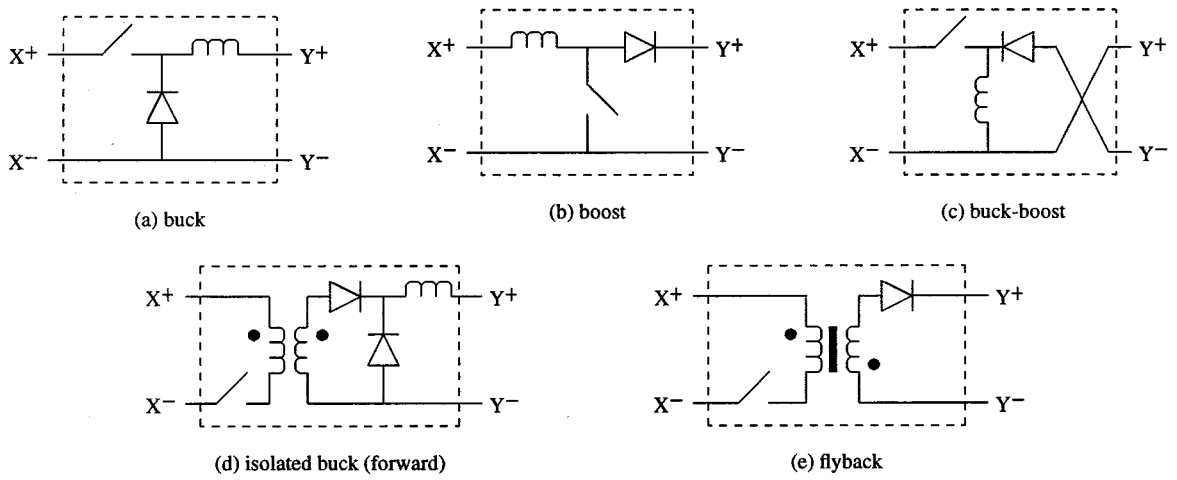

Fig. 5. Basic voltage converter circuits: (a)–(c) nonisolated, (d)–(e) isolated.

- For the nonisolated buck and boost converters, regardless of how the switch, diode and inductor are re-arranged, there is a short-circuit path either between X^+ and Y^+, or between X^- and Y^-.
- For the nonisolated buck-boost converter, regardless of how the switch, diode and inductor are re-arranged, there is a short-circuit path either between X^+ and Y^-, or between X^- and Y^+.

Clearly, in choosing a nonisolated basic converter for placement in an R^2P^2 circuit, care should be taken to ensure that the short-circuit paths imposed by the basic converters do not affect the intended connections. The allowable short-circuit paths can be readily found by inspection of the R^2P^2 circuits of Fig. 6.

1) For Configuration I-IIA, short-circuit paths are allowed between
   a) X^+ and Y^- of converter 1;
   b) any X and Y terminal of converter 2.
2) For Configuration I-IIB, short-circuit paths are allowed between
   a) X^- and Y^- of converter 1;
   b) X^- and Y^+ of converter 2.
3) For Configuration I-IIB, short-circuit paths are also allowed between
   a) X^+ and Y^- of converter 1;
   b) X^+ and Y^+ of converter 2.
4) For Configuration I-IIIA, short-circuit paths are allowed between
   a) X^- and Y^+ of converter 1;
   b) X^+ and Y^+ of converter 2.
5) For Configuration I-IIIA, short-circuit paths are also allowed between
   a) X^- and Y^- of converter 1;
   b) X^+ and Y^- of converter 2.

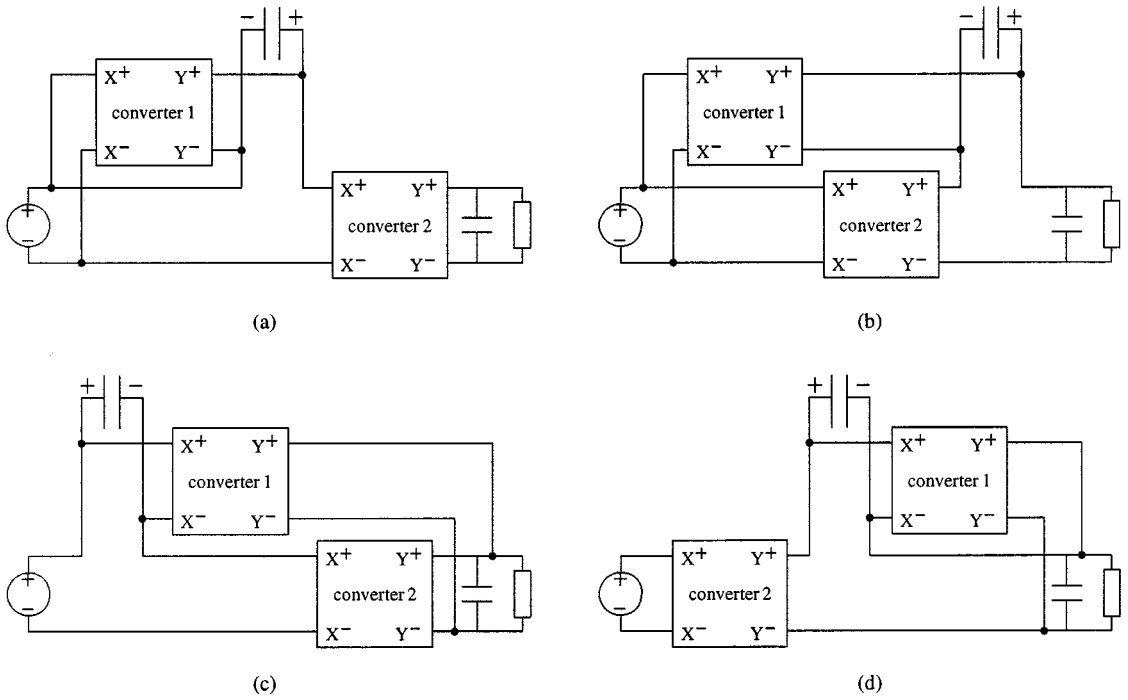

Fig. 6. Equivalent circuits of the simplest *reduced redundant power processing* (R^2P^2) configurations. Rectangular blocks denote converters. (a) I-IIA; (b) I-IIB; (c) I-IIIA; and (d) I-IIIB.

6) For Configuration I-IIIB, short-circuit paths are allowed between
   a) X^- and Y^+ of converter 1;
   b) any X and Y terminal of converter 2.

From the above observations and the earlier observations regarding the presence of short-circuit paths in the basic nonisolated converters, we can deduce the type of basic nonisolated converters that can be used for converters 1 and 2 in a nonisolated R^2P^2 PFC regulator. The main results are stated as follows and summarized in Table III, along with some previously reported circuits.

- For Configuration I-IIA, converter 1 can only be a buck-boost converter, and converter 2 can be any converter.
- For Configuration I-IIB, two cases are possible. If converter 1 is a buck or a boost converter, converter 2 can only be a buck-boost converter. If converter 1 is a buck-boost converter, converter 2 can be a buck or a boost converter.
- For Configuration I-IIIA, two cases are possible. If converter 1 is a buck-boost converter, converter 2 can only be a buck or a boost converter. If converter 1 is a buck or a boost converter, converter 2 can only be a buck-boost converter.
- For Configuration I-IIIB, converter 1 can only be a buck-boost converter, and converter 2 can be any converter.

TABLE III
POSSIBLE CHOICE OF CONVERTERS FOR NON-ISOLATED R^2P^2 PFC REGULATOR TOPOLOGIES

Configuration	Conv. 1	Conv. 2	Reported
I-IIA	buck-boost	buck	Zeta Chow *et al.*[10]
I-IIA	buck-boost	buck-boost	–
I-IIA	buck-boost	boost	–
I-IIB	buck	buck-boost	–
I-IIB	boost	buck-boost	–
I-IIB	buck-boost	buck	–
I-IIB	buck-boost	boost	–
I-IIIA	buck-boost	buck	–
I-IIIA	buck-boost	boost	–
I-IIIA	buck	buck-boost	–
I-IIIA	boost	buck-boost	–
I-IIIB	buck-boost	buck	–
I-IIIB	buck-boost	buck-boost	García *et al.* [8]
I-IIIB	buck-boost	boost	SEPIC BIFRED [1]

D. Requirement for Isolation Between Input and Load

The requirement of isolation between the input and load necessitates the use of transformer-isolated converters for either or both constituent converters. The simplest implementation for Configurations I-IIA and I-IIIB is to have only converter 2 isolated, and in any such implementation, converter 1 must be a buck-boost converter while converter 2 can be any isolated converter. Of course, if converter 1 is also isolated (though not necessary), any combination of converter types is possible.

Moreover, Configurations I-IIB and I-IIIA would require transformer isolation for both converters 1 and 2, and hence can employ any combination of basic isolated converters.

V. CIRCUIT SYNTHESIS EXAMPLES

In this section we will apply the afore-described synthesis procedure to construct practical R^2P^2 PFC voltage regulators.

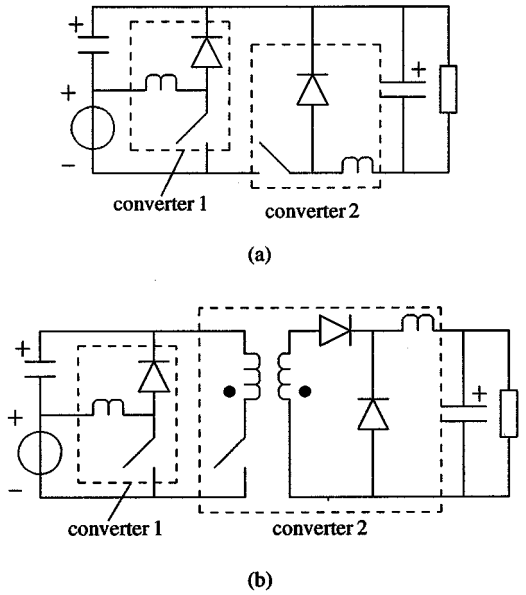

Fig. 7. (a) A possible implementation for Configuration I-IIA using a buck-boost and a buck converter for converters 1 and 2; (b) isolated version using a buck-boost and a transformer-isolated forward converter for converters 1 and 2. Core reset arrangement omitted for brevity.

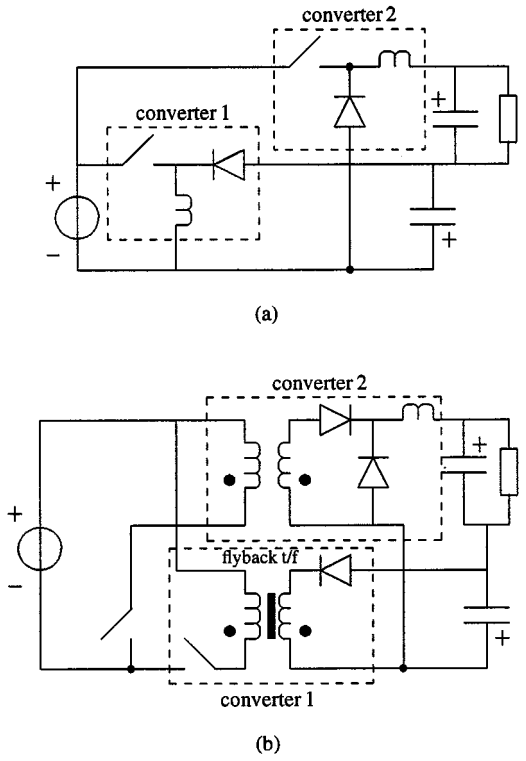

Fig. 8. (a) A possible implementation for Configuration I-IIB using a buck-boost and a buck converter for converters 1 and 2; (b) isolated version using a flyback and a forward converter for converters 1 and 2. Core reset arrangement omitted for brevity.

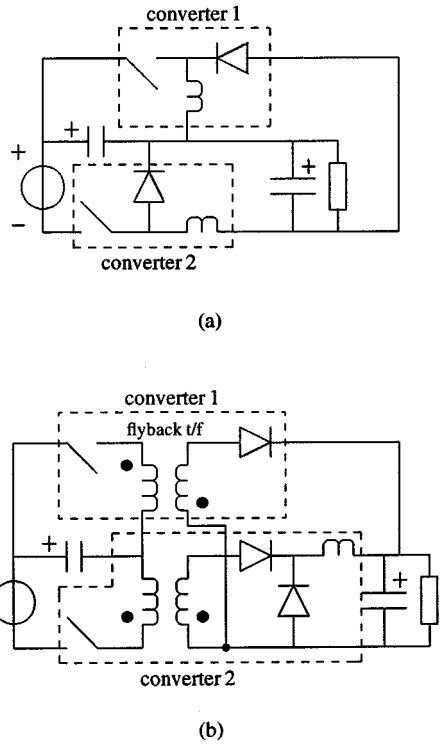

Fig. 9. (a) A possible implementation for Configuration I-IIIA using a buck-boost and a buck converter for converters 1 and 2; (b) isolated version using a flyback and a forward converter for converters 1 and 2. Core reset arrangement omitted for brevity.

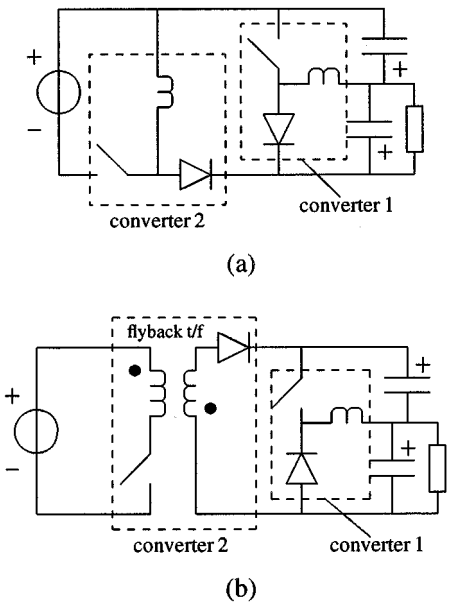

Fig. 10. (a) A possible implementation for Configuration I-IIIB using buck-boost converters for converters 1 and 2; (b) isolated version using a flyback and a forward converter for converters 1 and 2.

Example 1: Realization of Configuration I-IIA: As mentioned before, the simplest way to provide isolation between the input and the load for Configuration I-IIA is to use an isolated converter for converter 2. Note that converter 1 need not be isolated. Thus, we can employ any isolated converter for converter 2, but necessarily use a buck-boost converter for converter 1 (to avoid having to use an isolated converter for converter 1). Let us choose a buck converter for converter 2. Placing the two converters appropriately in the equivalent circuit of Configuration I-IIA shown in Fig. 6, we obtain the circuit shown in Fig. 7(a). The transformer isolated version is shown in Fig. 7(b).

Example 2: Realization of Configuration I-IIB: We consider Configuration I-IIB. Suppose we employ a buck-boost and a buck converter for converters 1 and 2 respectively. Similar to

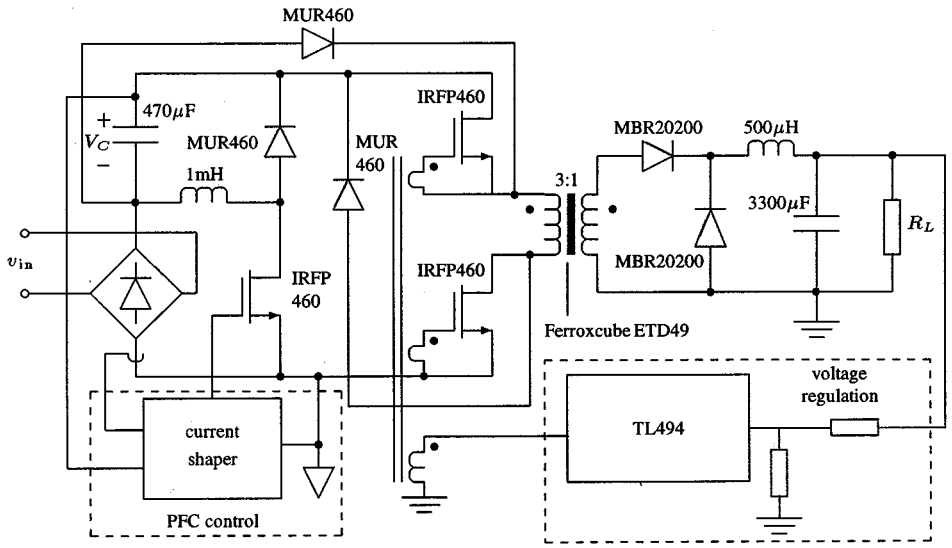

Fig. 11. Schematic of experimental R^2P^2 PFC regulator. Note that the two-switch forward topology and the choice of MOSFET's are immaterial to this experiment since the aim is to verify the improved efficiency of the noncascade structure based on the same set of constituent converters. Comparisons are relative, not absolute.

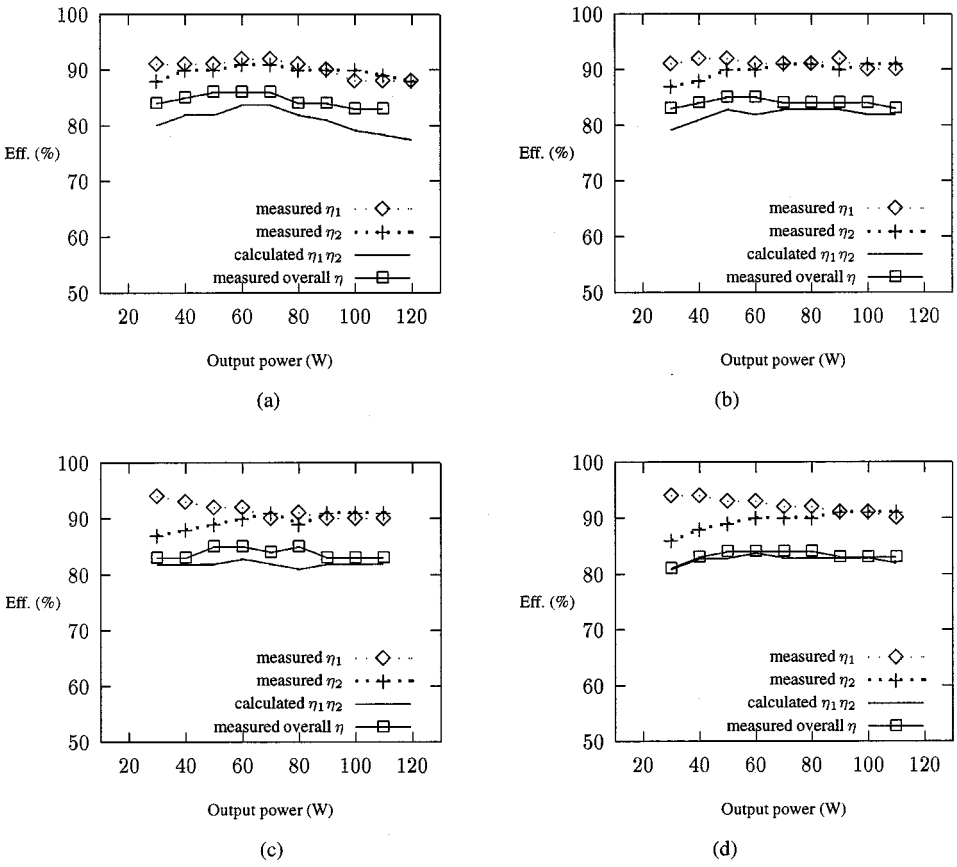

Fig. 12. Efficiency comparison of Configuration I-IIA circuit [Fig. 4(b)], showing improved overall efficiency over a cascade structure for (a) $V_C = 160$ V; (b) $V_C = 190$ V; (c) $V_C = 200$ V and (d) $V_C = 230$ V.

Example 1, we obtain an R^2P^2 PFC regulator, as shown in Fig. 8. Note that both isolation is required of both converters 1 and 2 in order to provide isolation for the R^2P^2 PFC regulator.

Example 3: Realization of Configuration I-IIIA: Consider Configuration I-IIIA. Suppose we employ a buck-boost and a buck converter for converters 1 and 2 respectively. Likewise, we obtain a new PFC regulator, as shown in Fig. 9.

Example 4: Realization of Configuration I-IIIB: Like Configuration I-IIA, isolation can be achieved for Configuration I-IIIB by employing an isolated converter for converter 2, and there is no need for converter 1 to be isolated. Thus, we can employ any isolated converter for converter 2, but necessarily use a buck-boost converter for converter 1 (to avoid having to use an isolated converter for converter 1). Fig. 10 shows a possible

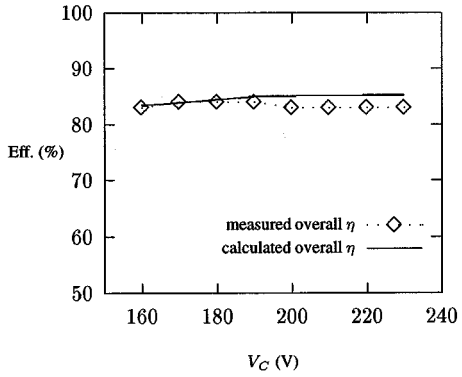

Fig. 13. Efficiency versus V_C at 100 W for Configuration I-IIA circuit [Fig. 7(b)], confirming the efficiency formula; calculated curve is based on efficiency formula and measured values of η_1 and η_2; experimental curve is from direct measurement of the overall efficiency.

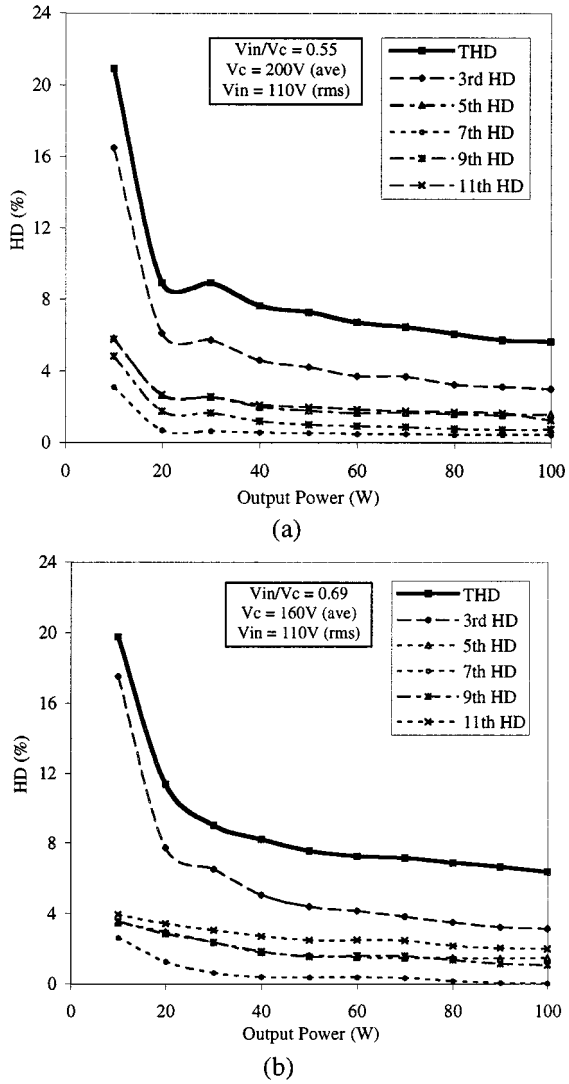

Fig. 14. Measured harmonic distortions versus output power. (a) $V_{\rm in}/V_c = 0.55$; (b) $V_{\rm in}/V_c = 0.69$.

R^2P^2 PFC regulator circuit arising from Configuration I-IIIB. This circuit has been tested experimentally by García [8].

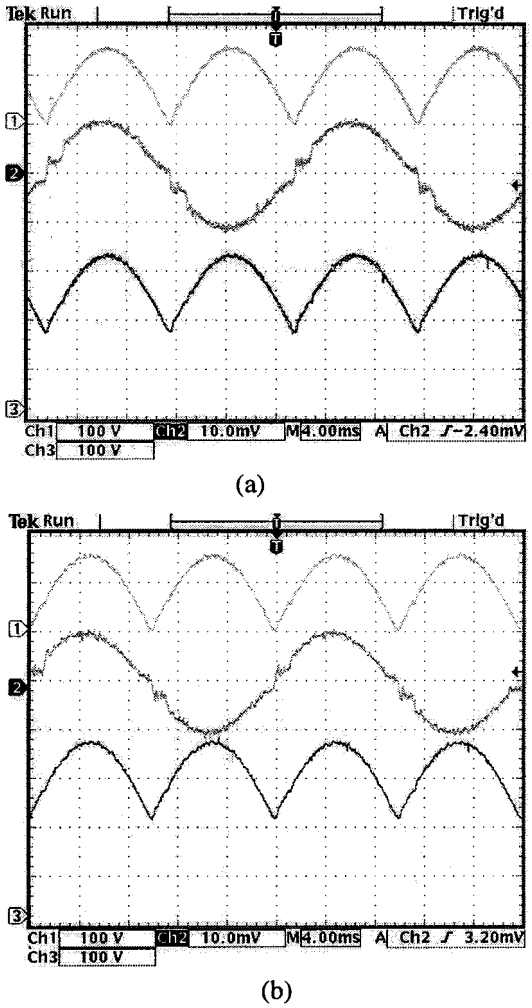

Fig. 15. Measured waveforms of input voltage (trace 1), input current (trace 2), capacitor voltage (trace 3). (a) $V_c = 160$ V; (b) $V_c = 200$ V. Scale: 100 V/div, 1 A/div and 4 ms/div.

VI. Experimental Tests

In this section we attempt to demonstrate the advantage of R^2P^2 PFC regulators experimentally. We choose in particular the circuit of Fig. 7(b) (Configuration I-IIA) for the purpose of illustration. The two constituent converters are a buck-boost converter and a forward converter. Fig. 11 shows the schematic of the circuit. The two extra diodes connecting the primary side of the power transformer are for core reset purposes. The control consists of a simple TL494 control chip applied to the forward converter for regulating the output voltage, and a simple feedback circuit applied to the buck-boost converter for shaping the input current. The circuit is tested over a power range from 20 W to 120 W.

Since our purpose is to verify the function of reduced redundant power processing, we specifically measure the efficiencies of the two constituent converters and compare their product with the measured overall efficiency, under the same voltage stress for each power level. For example, Fig. 12 compares the efficiencies for V_C at 160 V, 190 V, 200 V and 230 V. Similar tests were performed for other values of V_C. Fig. 13 shows a plot of efficiency versus V_C at 100 W output power. From Fig. 12, we see that the efficiency of the converter is generally improved

over that of a cascade structure consisting of the same two constituent converters. Also, for a lower value of V_C, the overall gain in the efficiency is higher, as shown in Fig. 13. This agrees with the efficiency formula given previously, i.e.,

$$\eta_{\text{I-IIA}} = \eta_1\eta_2 + (1-k)\eta_2(1-\eta_1) \tag{3}$$

where η_1 and η_2 are the efficiency of the buck-boost stage and of the forward stage, respectively, and k is the ratio at which the input power is split into the storage and the forward converter. For the circuit of Fig. 7, k is

$$k = \frac{V_C}{V_C + V_{\text{in}}}. \tag{4}$$

Finally, to verify the PFC function, the harmonic distortions are measured for different V_C and output power levels, as shown in Fig. 14, and some measured waveforms are shown in Fig. 15.

Remarks: It is worth noting that the efficiency advantage gradually becomes less significant when V_C becomes large, as clearly shown Fig. 12. This can be easily understood because we are actually having more power re-processed as V_C increases (k increases). In the extreme case of V_C tending to infinity, the circuit simply reduces to Configuration I-I.

VII. Conclusion

Although a number of PFC regulator topologies have been reported recently, they represent isolated cases of innovative circuit design, and very little formal work has been performed on the basic procedure for deriving the required circuit configurations that can shed light on the creation of new circuit topologies for such applications [11], [12]. This paper derives the basic configurations of converters for achieving PFC and voltage regulation. Specifically, based on a power flow consideration, we have derived sixteen possible configurations, from which PFC regulators can be constructed systematically. Since the main purpose is to present a systematic procedure for creating circuits, we focus on the general connection structure rather than specific circuit analysis. By comparing the theoretical efficiencies of these basic configurations, one can appreciate that the way in which power is processed plays a crucial role in determining the overall efficiency of a PFC regulator. A particularly illuminating result, which turns out to be intuitive, is that the overall efficiency can be improved if the power processed by one converter is not re-processed totally by the other converter within the PFC regulator. This leads to the idea of reduced-redundant-power-processing PFC regulators which has been the subject of this paper. It is hoped that this study will provide useful reference for engineers to create "new" efficient PFC regulators.

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