Fundamental Considerations of Three-Level DC–DC Converters: Topologies, Analyses, and Control

Xinbo Ruan, *Senior Member, IEEE*, Bin Li, *Member, IEEE*, Qianhong Chen, *Member, IEEE*, Siew-Chong Tan, *Member, IEEE*, and Chi K. Tse, *Fellow, IEEE*

***Abstract*—This paper discusses the basic family of three-level (TL) dc–dc converters. The origin of TL converters and their basic topological variations are described. Systematic procedures leading to improved and simplified circuit topologies are discussed. A feedforward control scheme that ensures the proper functioning of these converters is proposed. Moreover, the virtues and drawbacks of these converters as compared to conventional converters are highlighted. In particular, the advantages of TL converters include reduced voltage stress of the switches, reduced filter size, and improved dynamic response. It is shown that TL converters are highly suitable for high input/output voltage and medium-to-high-power dc–dc power conversions.**

***Index Terms*—DC–DC power conversion, feedforward control, full-bridge (FB) converter, interleaved control, three-level (TL) converter.**

I. Introduction

THE IDEA of having circuits that generate three-level (TL) voltage waveforms can be traced back to two U.S. patents granted in the early 1960s [1], [2]. These TL circuits were invented for computer applications with the intention of transforming conventional computation methodology from binary logic form to ternary form.

Later, Nabae *et al.* [3] and Baker[1] [4] reported a different form of TL circuits specific to power conversion application in 1980 and 1981, respectively. The circuit is named the neutral-point-clamped (NPC) inverter. In contrast to conventional power inverter, the phase leg of this inverter can output not only the positive and negative bus voltages but also the neutral-point voltage. As a result, the output voltage of the NPC inverter has lower harmonics as compared to that of traditional inverters [5]. This allows the use of a smaller output filter. Since the phase leg provides three levels of voltages, the NPC inverter is also called TL inverter. An additional advantage of the TL inverter is that the voltage stress of the switches is reduced to half of the input voltage, which makes it suitable for high input voltage power conversions [6].

This technique has been applied to dc–dc converters by Pinheiro and Barbi [7], [8] to reduce the voltage stress of the switches. It should be emphasized that the application of the technique does not create a TL voltage state in the case of dc–dc converters. Nevertheless, since the phase leg of this dc–dc converter is similar to that of the TL inverter, i.e., having four switches, two dividing capacitors at the input, and two clamping diodes, this dc–dc converter was named TL converter. However, it will be shown in the following section that the so-called TL converter is essentially a half-bridge (HB) converter. To differentiate it from other TL derived converters, in this paper, we will refer to it as the HB TL converter.

Until now, several soft-switching types of HB TL converters have been proposed for industrial considerations [7]–[16]. Although the design of these converters has been presented at the operational level, some fundamental issues such as topologies, analyses, and control have not been thoroughly studied. In this paper, the basic HB TL topology is first presented. This is followed by the derivation of a systematic method of generating TL converter topologies, leading to the derivation of a family of TL converters with improvement and simplification for better functionality and practicality. The resulting TL family of converters inherits the important advantage of having a reduction in the switch voltage stress. In addition, for some of the TL converters, the advantages also include a reduction in the size of the storage elements. In order to ensure the proper functioning of the TL converters, a feedforward control scheme is proposed to ensure that the dividing capacitors' voltages are equal. It is hoped that the results of this paper will lead to better understanding of the fundamental problems associated with the design and analysis of TL converters, thereby facilitating the further development and innovation into new types of TL converters for various practical requirements.

II. Origin of TL DC–DC Converters

The HB TL converter shown in Fig. 1(c) is derived from the conventional HB converter shown in Fig. 1(a). The voltage stress of the switches in the conventional HB converter is originally the input voltage $V_{\rm in}$. To reduce the voltage stress, each switch of this converter is replaced by a switching device that is made up of two series-connected switches, i.e., Q_A is replaced

Manuscript received November 26, 2007; revised April 21, 2008. First published June 17, 2008; current version published December 12,2008. This work was supported in part by the National Natural Science Foundation of China under Award 50177013 and in part by the Delta Power Electronics Science and Education Development Fund. This paper was recommended by Associate Editor E. Alarcon.

X. Ruan is with the College of Electrical and Electronics Engineering, Huazhong University of Science and Technology, Wuhan 430074, China (e-mail: ruanxb@mail.hust.edu.cn).

B. Li is with EMC Information Technology Research & Development (Shanghai) Company, Ltd., Shanghai 200433, China.

Q. Chen is with the Aero-Power Sci-tech Center, College of Automation Engineering, Nanjing University of Aeronautics and Astronautics, Nanjing 210016, China.

S. C. Tan and C. K. Tse are with the Department of Electronic and Information Engineering, The Hong Kong Polytechnic University, Kowloon, Hong Kong.

Digital Object Identifier 10.1109/TCSI.2008.927218

[1]The U.S. patent was filed by Baker on August 2, 1979 [4].

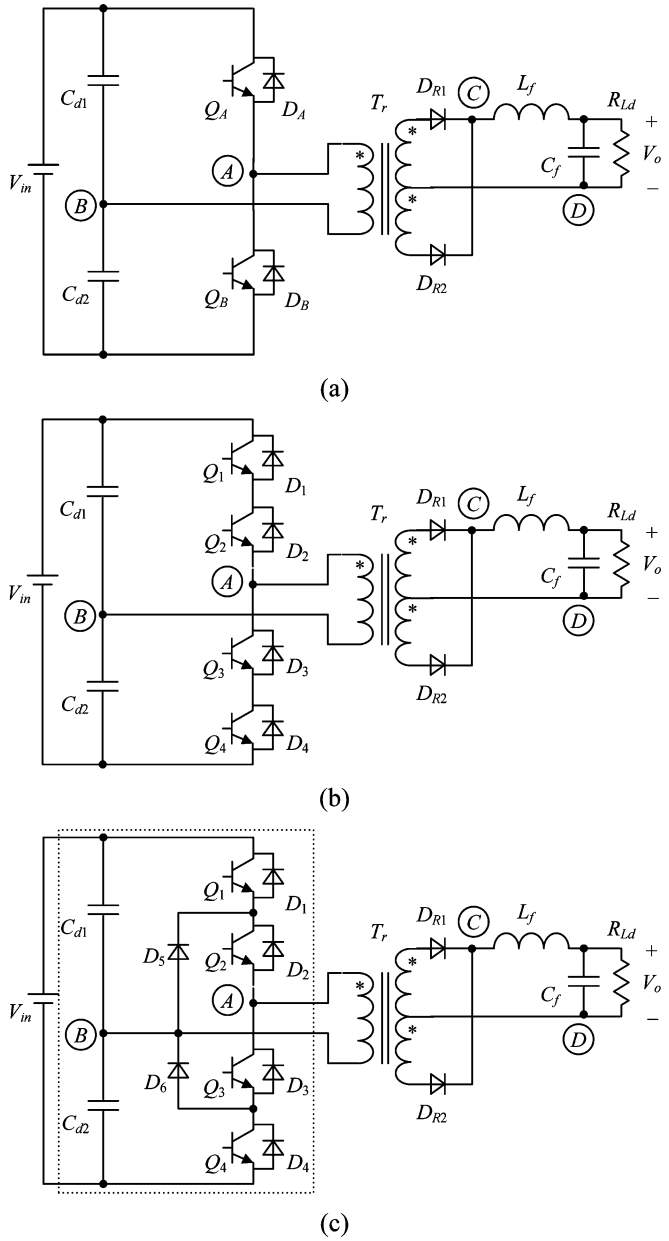


Fig. 1. Derivation of the HB TL converter. (a) HB converter. (b) HB converter with two switches replacing each original switch. (c) HB TL converter.

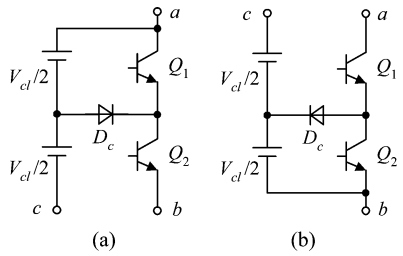


Fig. 2. TLSCs. (a) Anode. (b) Cathode.

by Q_1 and Q_2 and Q_B is replaced by Q_3 and Q_4. This transforms the converter to that given in Fig. 1(b). Ideally, with the series-connected switches (e.g., Q_1 and Q_2) being identical, the voltage stress across each individual switch would be $V_{\rm in}/2$. However, since there is always slight differences in the characteristics as well as the driving circuits of the two series switches, there will always be an imbalance in the voltage stress of the two series switches.

To resolve this problem, it is proposed to have two clamping diodes D_5 and D_6 inserted into the converter to counteract the imperfections of the switching actions, as shown in Fig. 1(c). With this arrangement, the series-connected switches will each suffer a voltage stress of $V_{\rm in}/2$ despite the switches' nonideality. Interestingly, the circuit in the dashed block represents one phase leg of a TL inverter [3]. Hence, the name TL converter has been conveniently adopted to represent this kind of converters (see Fig. 1(c)). To be precise, this converter should be known as HB TL converter.

Obviously, the use of two switches (instead of one switch) in each switching connection of the converter would result in the doubling of the required switches, which leads to a doubling of the switching devices' cost, and also the penalty of having more switching complications and losses. However, such tradeoffs for a lower voltage stress return are often necessary when it comes to developing converters performing high-voltage medium-to-high-power dc–dc conversion. This is because, with the type of switches that the semiconductor industry currently offers, the overall cost of using two low-voltage-rated switches is much lower than the overall cost of using a single high-voltage-rated switch for such kind of operating condition. In extreme cases, the application of this technique represents the only means of achieving a very high-voltage dc–dc conversion, which is otherwise unachievable with existing switches.

Following this discussion, it will be shown how the method of deriving the HB TL converter can be extended to all types of dc–dc converters. With that, a family of TL converters for the following topologies will be introduced: 1) nonisolated topologies: buck, boost, buck–boost, Cuk, SEPIC, and Zeta, and 2) isolated topologies: forward, flyback, push–pull, HB, and full-bridge (FB).

III. TLSCs

From the derivation of the HB TL converter, it is known that in order to reduce the voltage stress of the switches, two switches connected in series are used to replace a single switch, and the clamping diodes and voltage sources are introduced to maintain an equal voltage stress distribution among the two series switches despite the presence of intrinsic devices' imperfections. It can be seen that with such an arrangement, the clamping voltage source will be equal to the voltage stress magnitude of the basic converter, which is half of the original voltage stress applied on the switches.

Careful study into the circuit shows that from the way in which the clamping diode D_c and clamping voltage source $V_{\rm cl}$ are connected, two kinds of TL switch cells (TLSC) can be extracted from the converter, as shown in Fig. 2. Fig. 2(a) shows the first type of which the anode of $V_{\rm cl}$ is connected to the collector of switch Q_1, and the anode of D_c is connected to the center point of $V_{\rm cl}$. We call this cell arrangement anode TLSC (A-TLSC). Fig. 2(b) shows the second type of which the cathode of $V_{\rm cl}$ is connected to the emitter of the switch Q_2, and the

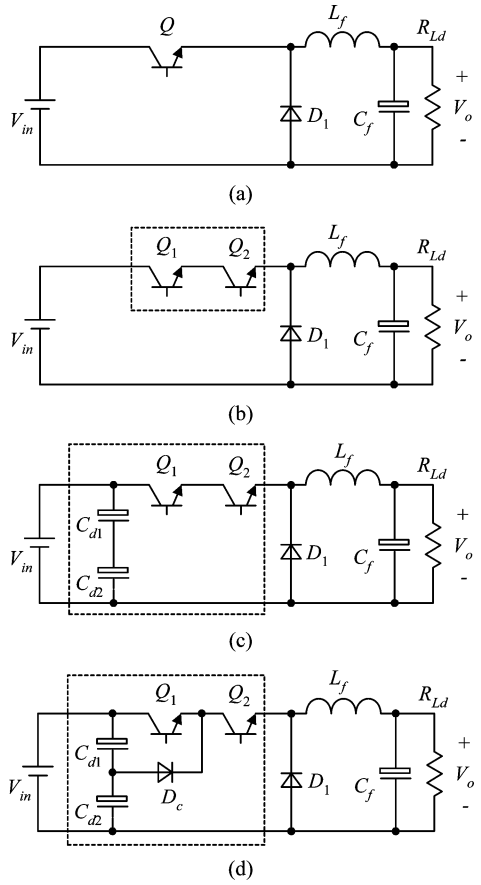


Fig. 3. Derivation of the buck TL converter.

cathode of D_c is connected to the center point of $V_{\rm cl}$. We call this cell arrangement cathode TLSC (C-TLSC).

To ensure the proper functioning of the operation in balancing the voltage stress of the two switches, the switch in the closed loop must always be turned off prior to the turning off of the remaining switch. For example, in the case of A-TLSC, Q_1 must first be turned off while Q_2 remains on. When this occurs, the current flowing through Q_1 will be transferred to the path of D_c. This concurrently clamps the voltage stress of Q_1 at $V_{\rm cl}/2$. Then, when Q_2 is turned off, its voltage stress will also be clamped at $V_{\rm cl}/2$. On the other hand, if Q_2 is turned off before Q_1, the voltage stress of Q_2 will be $V_{\rm cl}$. This turn-off sequence is similar for the C-TLSC. Q_2 should be turned off prior to the turning off of Q_1.

IV. Derivation of TL Converters

A. Derivation of the Buck TL Converter

Through the concept of TLSC, the method of deriving the HB TL converter can be extended to all types of dc–dc converters. As an example, it will be demonstrated in the following how a buck converter, as shown in Fig. 3(a), can be transformed to a buck TL converter, as shown in Fig. 3(d).

Step 1) Replace the switch Q of the buck converter in Fig. 3(a) with two series switches Q_1 and Q_2 to obtain the converter shown in Fig. 3(b).

Step 2) Next, find or build a clamping voltage source in the converter. If there exists a voltage source which equals the magnitude of the voltage stress of the switch Q in the converter, it can be readily used as the clamping voltage source. Otherwise, it is necessary to build one. For the buck converter, the voltage stress of Q is existing in the form of the input voltage $V_{\rm in}$. So, it can be used as the clamping voltage source through simple modification. This can be easily done by splitting $V_{\rm in}$ into two separate voltage sources equally (with voltage level of $V_{\rm in}/2$ each) by connecting two series capacitors in parallel to $V_{\rm in}$. This transforms the converter to that shown in Fig. 3(c). Note that the function of the two series input capacitors is similar to that of the input split capacitors in conventional HB converters.

Step 3) Finally, introduce a clamping diode D_c into the converter to connect the center point of the two voltage sources to the center point of the two series switches. The direction of the clamping diode can be determined using the switch-cell analysis given in the previous section. Since the buck converter shown in Fig. 3(c) basically represents an A-TLSC, the direction of the clamping diode is therefore provided. The completed form of the buck TL converter using the A-TLSC is shown in Fig. 3(d).

Remark: It should be mentioned that the TL converters derived in this paper are based on the diode-clamped TL inverter. However, it is possible to derive a different family of TL converters using the concept of capacitor-clamped TL inverter proposed by Meynard and Foch [17]. Interested readers are referred to [17] and [18].

B. Family of TL Converters

Based on the approach developed for deriving the buck TL converter, an entire family of TL converters for various topologies can be derived. Fig. 4 shows the derived family of six nonisolated TL converters based on the buck, boost, buck–boost, Cuk, SEPIC, and Zeta topologies. For the boost converter, the voltage stress of the switch is the output voltage V_o. Therefore, V_o is employed as the clamping voltage source. For the buck–boost, SEPIC, and Zeta converters, the voltage stress of the switch is $V_{\rm in}+V_o$. However, since such a voltage source is not readily available in the circuit, it is necessary to develop one. Knowing that the potential level between points A and B is equivalently $V_{\rm in}+V_o$, two identical capacitors connected in series are introduced in shunt with these points to form the clamping voltage sources [see Fig. 4(c), (e), and (f)]. As for the Cuk converter, the voltage stress of the switch is also $V_{\rm in}+V_o$, and such a voltage source can be found in the energy transfer capacitor. Hence, this capacitor can be split into two series capacitors C_{b1} and C_{b2}, which are then employed as the clamping voltage source [see Fig. 4(b)].

Fig. 5 shows the derived family of isolated TL converters based on the forward, flyback, push–pull, HB, and FB topologies. For the forward converter, if the winding numbers of the reset winding and the primary winding are equal, the voltage stress of the switch will be $2V_{\rm in}$. Therefore, the input voltage

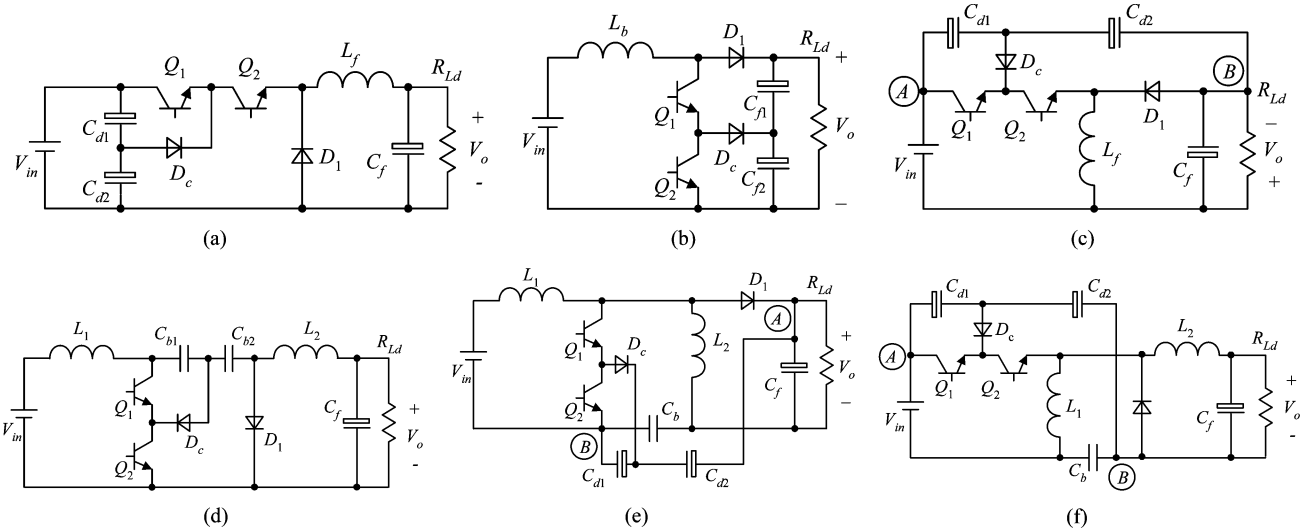


Fig. 4. Six nonisolated TL converters. (a) Buck. (b) Boost. (c) Buck–boost. (d) Cuk. (e) SEPIC. (f) Zeta.

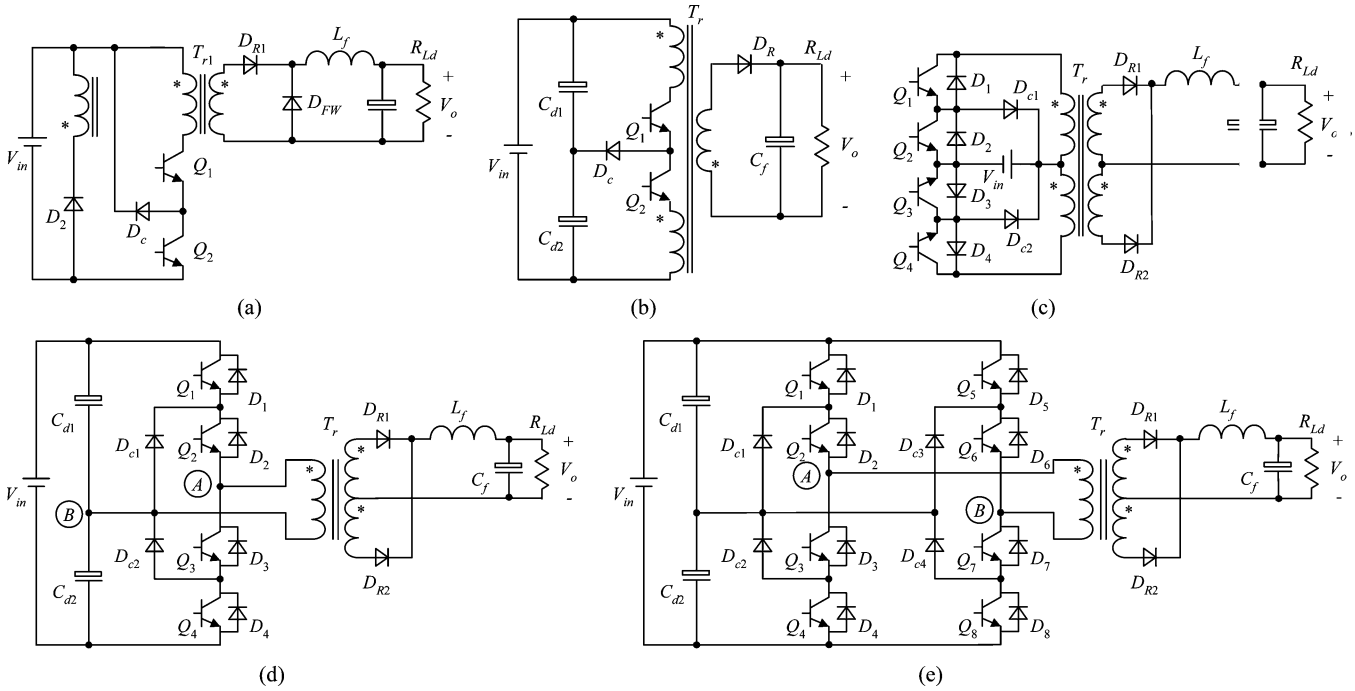


Fig. 5. Isolated TL converters. (a) Forward. (b) Flyback. (c) Push–pull. (d) HB. (e) FB.

source can be directly employed as the clamping voltage source [see Fig. 5(a)]. For the flyback converter, the original primary winding can be split into two separate windings and can be used as the clamping voltage source [see Fig. 5(b)]. For the push–pull converter, the input voltage source is employed as the clamping voltage source [see Fig. 5(c)]. Finally, the FB converter uses the same clamping voltage source as the HB TL converter [see Fig. 5(d) and (e)].

V. Improvement and Simplification of TL Converters

The TL converters introduced in the previous section are obtained directly from the application of the TLSC. This section discusses how they can be further improved and simplified for better performance and practicality.

A. Improvement of Nonisolated TL Converters

Refer to the buck TL converter shown in Fig. 6(a). If both the switches of this converter are turned on and off simultaneously, the voltage across the *LC* filter will be the same as that of the basic buck converter, as shown in Fig. 7(a). In this case, the following two voltage levels are possible: $(+1)V_{\rm in}$ and $(0)V_{\rm in}$. Now, consider that the same buck TL converter is operated such that Q_3 is always on while Q_1 follows the PWM control. Then, the waveform of the voltage across the *LC* filter will be similar to that shown in Fig. 7(b). In this case, the two voltage levels are $(+1)V_{\rm in}$ and $(+1/2)V_{\rm in}$. Obviously, if the input and output voltages of both the buck converter and the buck TL converter are identical, the high-frequency content of the latter will be lower than that of the former. With that, a smaller filter inductance

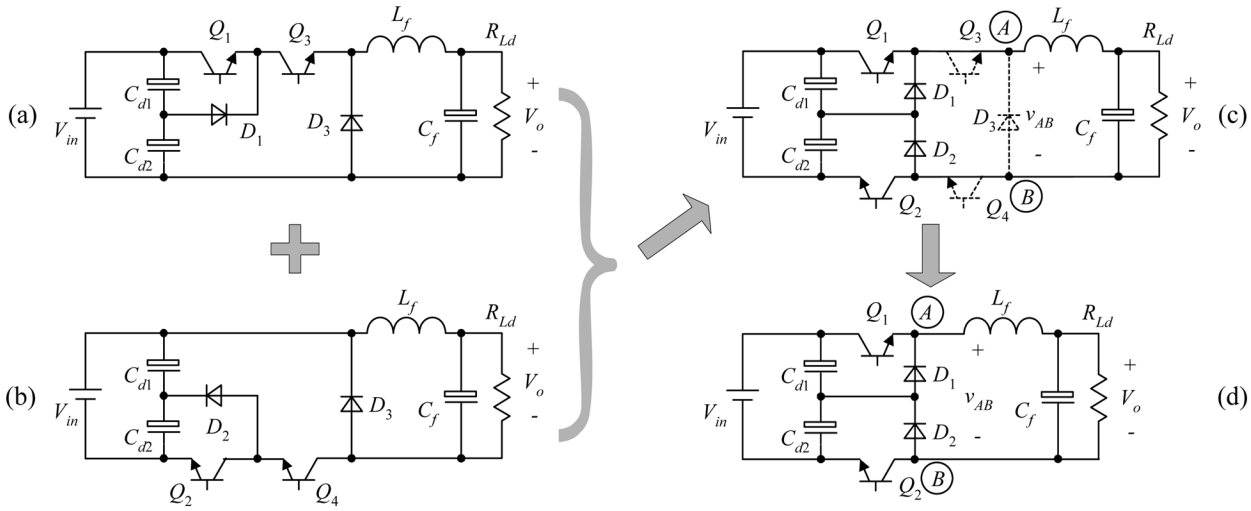


Fig. 6. Improvement of the buck TL converter.

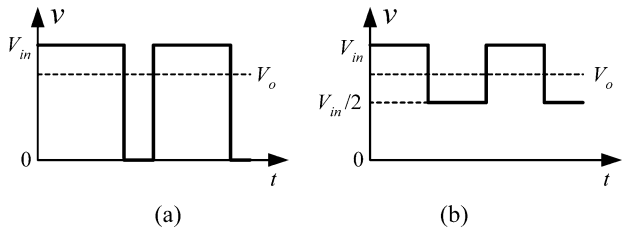


Fig. 7. Voltage across the filter. (a) Buck converter. (b) Buck TL converter.

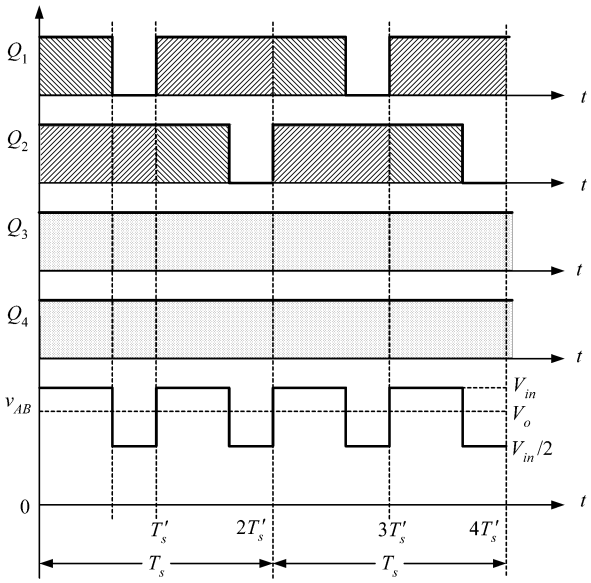


Fig. 8. Control strategy of the buck TL converter.

is required for the buck TL converter as compared to the buck converter. As a result, the former will have a faster dynamic response as compared to the latter.

However, such a control strategy of having one switch turned on while the other switch is operating under the PWM control will result in an imbalance in the voltage level of the two dividing capacitors C_{d1} and C_{d2}. This is because, in the duration when both Q_1 and Q_3 conduct, both capacitors provide energy to the load. However, in the duration when Q_1 is turned off, only C_{d2} provides energy to the load. Therefore, in a switching period, C_{d2} will provide more energy to the load than C_{d1}, and its voltage will become lower while the voltage of C_{d1} becomes higher. Accumulated over time, the voltage of C_{d1} will saturate at $V_{\rm in}$, and the voltage of C_{d2} will be null. Thus, the buck TL converter shown in Fig. 6(a) cannot be operated normally under the described control strategy.

As discussed in Section II, there are two available types of TLSC, namely, the A-TLSC and the C-TLSC. Recall that the buck TL converter shown in Fig. 6(a) is derived using the A-TLSC. It is also possible to obtain a buck TL converter using the C-TLSC, as shown in Fig. 6(b). Here, if the TL converter is operated such that Q_4 is always on while Q_2 follows the PWM control, the waveform of the voltage across the filter will be identical to that in Fig. 7(b). The use of such a control strategy results in C_{d1} providing more energy to the load than C_{d2} over time. This consequence is opposite to that of the buck TL converter in Fig. 6(a) under the same control strategy. Now, if both the buck TL converters in Fig. 6(a) and (b) are integrated into one with common input dividing capacitors, as shown in Fig. 6(c), the voltage of the dividing capacitors can be balanced.

Fig. 8 shows the control strategy of the combined buck TL converter shown in Fig. 6(c). In the first switching period T_s', switches Q_2, Q_3, and Q_4 will be turned on while Q_1 is PWM controlled. In this duration, C_{d2} will provide more energy to the load than C_{d1}. In the second switching period, switches Q_1, Q_3, and Q_4 will be turned on while Q_2 is PWM controlled. In this duration, C_{d1} will provide more energy to the load than C_{d2}. Thus, by rotating the energy provision burden between both capacitors through adjacent switching periods, the two dividing capacitors will provide, on average, an equal amount of energy to the load. This allows them to maintain a balance voltage over time.

Although functioning, the buck TL converter proposed in Fig. 6(c) is overtly complicated. To make it practically more appealing, it would be necessary to reduce the converter into a simpler form. First, since Q_3 and Q_4 are always on, they can be

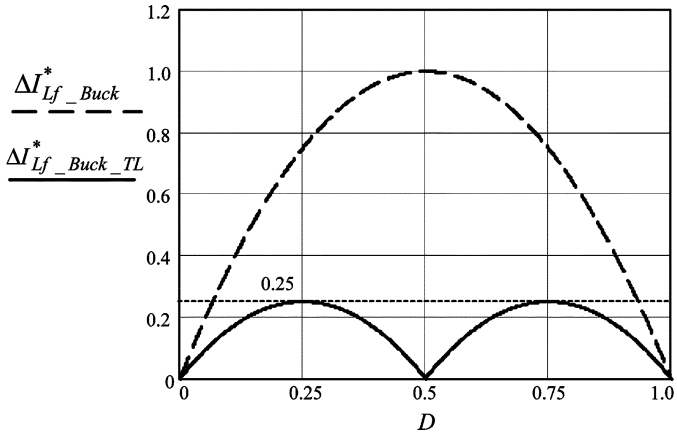


Fig. 9. Comparison of the ripple current of the filter inductance of the buck converter and the buck TL converter.

replaced by a direct conduction path. Second, the freewheeling diode D_3 is parallel to D_1 and D_2. It is therefore redundant and removable. With that, the simplified buck TL converter can be obtained, as shown in Fig. 6(d).

Note that, in Fig. 8, the drive signal of Q_1 for two adjacent switching periods, i.e., $2T_s'$, is connected and can be considered as one period. This means that the switching frequency of Q_1 is equivalently half the original switching frequency. This is similar for the drive signal of Q_2. An examination of Q_1 and Q_2 shows that a time difference of $T_s/2$ exists between them. This is obvious since Q_1 and Q_2 are interleaved switched. Hence, for a switching frequency $f_s(= 1/T_s)$, the ripple frequency of the voltage across the *LC* filter would be $2f_s$.

Fig. 9 shows the normalized ripple current of the filter inductances of a buck converter and a buck TL converter with the same filter inductance and switching frequency. The equations for plotting the graphs are given as

$$\Delta I^*_{Lf\_\mathrm{Buck}\_TL} = \Delta I_{Lf\_\mathrm{Buck}\_TL}/\Delta I_{Lf\_\mathrm{Buck}\_\mathrm{max}} \quad (1)$$

$$\Delta I^*_{Lf\_\mathrm{Buck}} = \Delta I_{Lf\_\mathrm{Buck}}/\Delta I_{Lf\_\mathrm{Buck}\_\mathrm{max}}. \quad (2)$$

It can be seen from the figure that the maximum ripple current of the filter inductance of the buck TL converter is only one-fourth of that of the buck converter. On the other hand, if both their ripple currents are equal, the filter inductance of the buck TL converter will be one-fourth of that of the buck converter. Such a merit is obtained from the following two facts: 1) The voltage waveform across the filter of the buck TL converter has lower high-frequency content than that of the buck converter, and 2) the ripple frequency of the voltage across the filter is twice the switching frequency. Furthermore, as the ripple frequency of the filter inductance of the buck TL converter is twice that of the buck converter, if the ripple currents are equal, the filter capacitor of the buck TL converter can be reduced to half that of the buck converter if the output voltage ripples of the two converters are equal.

Similar to the improvement performed on the buck TL converter, other nonisolated TL converters can be improved using the same approach. The improved version of these converters is shown in Fig. 10.

B. Simplification of the Forward TL Converter

Unlike the nonisolated TL converters, the derived isolated TL converters shown in Fig. 5 are properly functional in its current form. It is noted, however, that the forward TL converter can be further simplified with the steps shown in Fig. 11. First, the positions of Q_1 and the transformer can be exchanged, as shown in Fig. 11(b). With this arrangement, when Q_2 is turned off while Q_1 remains on, D_1 will conduct. This makes the primary voltage of the transformer zero, and the voltage of Q_2 will be clamped at V_{in}. Then, when Q_1 is turned off, D_c will conduct, and the transformer will be reset via the reset winding. Since the primary winding and reset winding have equal turns number, the voltage of the primary winding will be V_{in}, and the voltage potential level of point "*" will be zero. Thus, point "*" can be shorted to the ground. To do that without affecting the normal operation of the converter, diode D_2 is introduced, as shown in Fig. 11(c). As a result, the primary winding can be used to perform the resetting function of the transformer. This makes the branch of the reset winding with D_c redundant and can therefore be removed. Fig. 11(c) shows the simplified forward TL converter, which is the well-known double-switch forward converter.

VI. Derivation of the H-FB TL Converter

In Fig. 3, a buck TL converter is derived using the A-TLSC. If a transformer is introduced to isolate its input from its output, a buck TL converter of the form shown in Fig. 12(a) can be obtained. If this converter is operated with a primary winding waveform similar to Fig. 7(b), the following two problems will occur: 1) The voltage of the dividing capacitors will be unequal, and 2) the magnetic field of the transformer cannot be reset. Fortunately, this can be resolved by incorporating this converter with an isolated form of the buck TL converter that is derived using C-TLSC, as shown in Fig. 12(b). Due to their opposing directions, the combination of these converters [see Fig. 12(c)] will ensure that the energy provision of the dividing capacitors is equal and that the magnetic field of the transformer will be bidirectional. This is similar to that of the HB and FB converters. Note that two switches Q_5 and Q_6 have been introduced to prevent a short circuit. Finally, this converter can be redrawn by including the secondary windings of the transformer, the full-wave rectifier, and the *LC* filter, as shown in Fig. 12(d). Here, six diodes D_1–D_6 are introduced in parallel to Q_1–Q_6, respectively.

The derived converter in Fig. 12(d) is fundamentally an FB TL converter. However, it is different from the FB TL converter shown in Fig. 5(e). As it has two phase legs (one is the TL leg and the other is the two-level leg), we name it the hybrid FB (H-FB) TL converter. It is found that the H-FB TL converter can perform zero-voltage switching (ZVS) for the TL leg, and ZVS or zero-current switching for the two-level leg. The detail of the analysis and results are reported in [14], [15].

VII. Possibility of Obtaining TL Waveform

The original objective of proposing the use of two series-connected switches in lieu of a single switch is to reduce the voltage

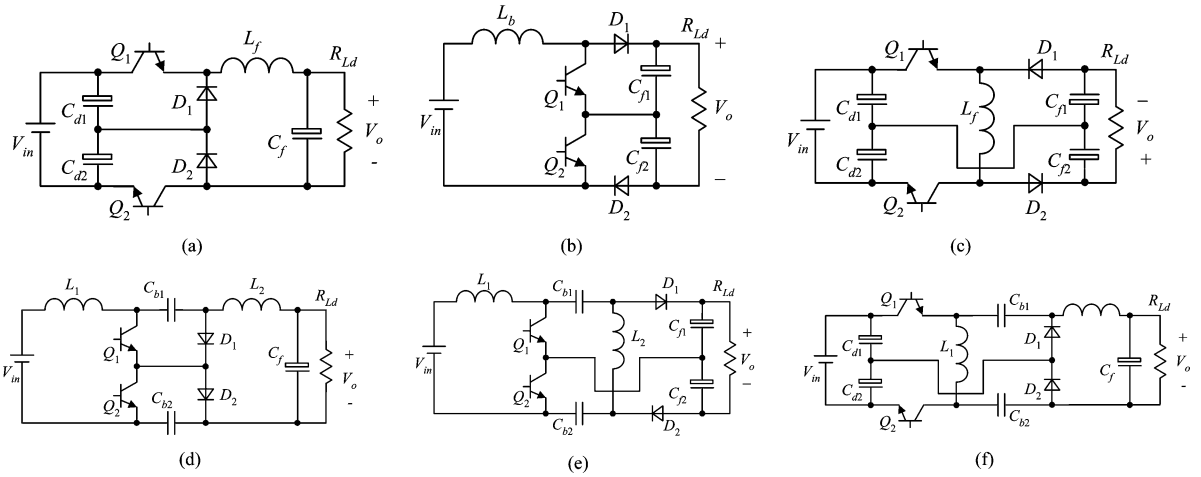


Fig. 10. Improved six basic TL converters. (a) Buck. (b) Boost. (c) Buck–boost. (d) Cuk. (e) SEPIC. (f) Zeta.

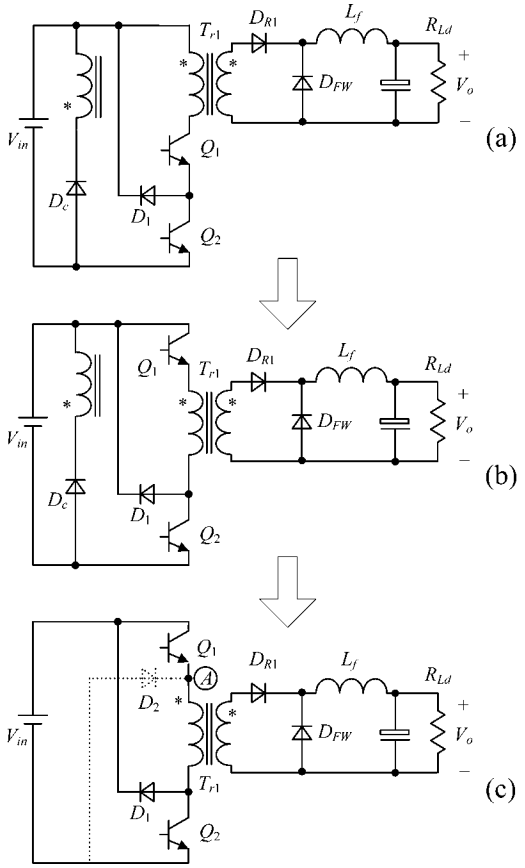


Fig. 11. Simplification of the forward TL converter.

stress of the switches of the converters used in high-voltage application. It is intriguing to know that besides such an advantage, the derived buck TL converter can be operated in a way such that its filter can be significantly reduced. This draws the immediate question as to whether all TL converters can be operated such that the size requirement of their filters can be reduced. This is important since the reduction of filter size can significantly improve the dynamic response of the converter, which is a critical issue in current electronic systems [19], [20].

To answer the aforementioned question, it is necessary to consider how such an operation can be achieved. First, the reduction of filter size is possible due to the reduction of the high-frequency content of the voltage applied to the filter, as that shown in Fig. 7(b). To obtain such a waveform, two dividing capacitors are needed to support the switching operation. For part of a switching period, both capacitors will power the load simultaneously. For the remaining duration of the switching period, only one of the capacitors will power the load. This task of having only the capacitors supplying energy to the load will be alternately carried out between the two capacitors.

With that, it is now possible to check if all TL converters can be operated such that the size of their filters can be reduced. For the family of nonisolated TL converters, the two dividing capacitors can be operated to meet this condition. Furthermore, the filter voltage waveforms with frequency that is twice the switching frequency can be obtained. Hence, the size of their filters can be reduced.

For the family of isolated TL converters, only the FB TL converter and the H-FB converter can have filter voltage waveforms with frequency that is twice the switching frequency. Thus, only these isolated TL converters can have reduced filter. As for the forward, flyback, push–pull, and HB TL converters, either they have only one capacitor or only one of the dividing capacitors is used to power the load. Hence, the frequency of their filter voltage waveforms cannot be twice the switching frequency.

VIII. Feedforward Control Scheme for the TL Converters

As mentioned before, when the TL converters are operating with reduced filter size, the dividing capacitors will be operated to alternately supply energy to the load. Theoretically, such an operation will produce an ideal waveform as that shown in Fig. 7(b). However, in actual implementation, this is not so straightforward. Due to the nonideality and variations of the driver and controller circuits between the switches, i.e., a slight difference in the control signals for the switches, there will be a difference in the amount of energy provided by each dividing capacitor to the load. In other words, the dividing capacitors

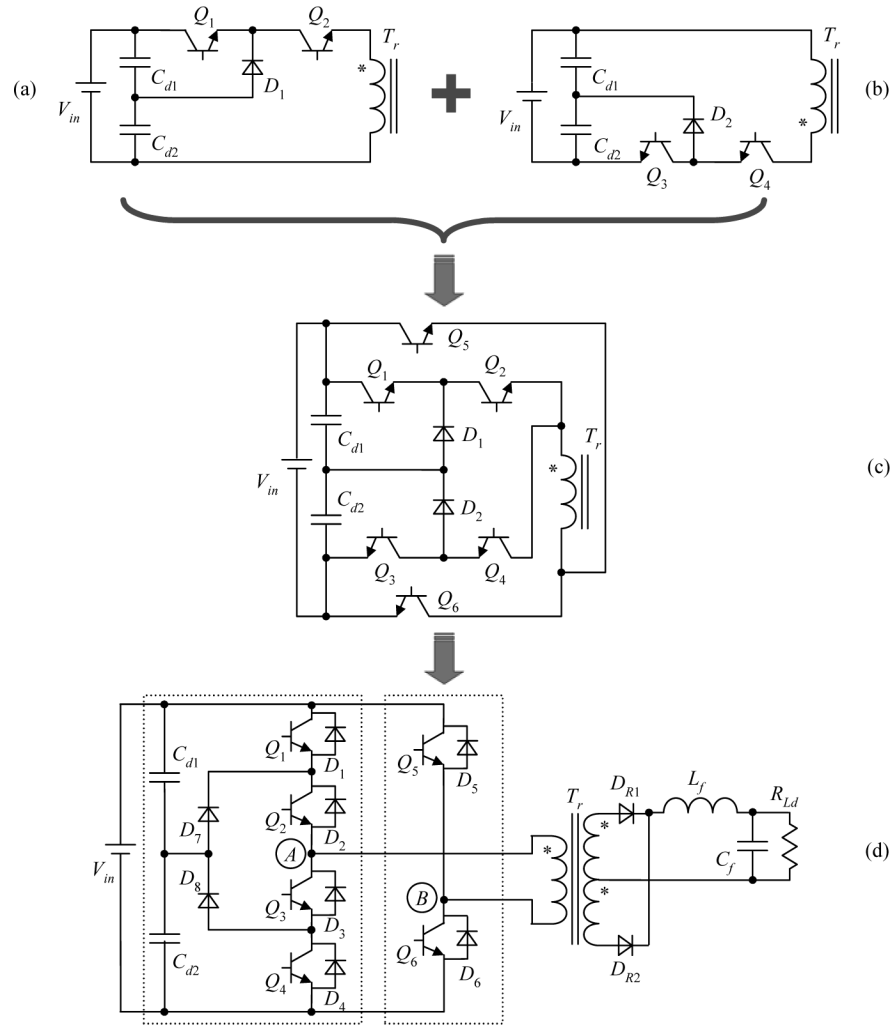


Fig. 12. Derivation of the H-FB TL converter.

will have unequal voltages. If this happens, the voltage waveform across the filter will be asymmetrical. This also means that the filter size of the TL converter has to be larger than ideally required to attain the same current ripple specification [21], [22].

To resolve this issue, we propose to incorporate a feedforward control scheme that adjusts the voltage level of the dividing capacitors, such that voltage equality is achieved, into the existing feedback controller. Recall that the function of the feedback controller is to regulate the output voltage of the TL converters. On the other hand, the task of the feedforward control scheme is to monitor the voltage across the dividing capacitors and to appropriately reduce or increase their switching durations such that their voltages can be balanced. Even though there is a correlation in how the switch is turned on or off between the two schemes, there is no conflict in their copresence. Hence, such a scheme is practically viable.

Fig. 13 shows how the proposed feedforward control scheme can be incorporated into the feedback controller for the buck TL converter. The operating mechanism of the overall controller can be understood as follows.

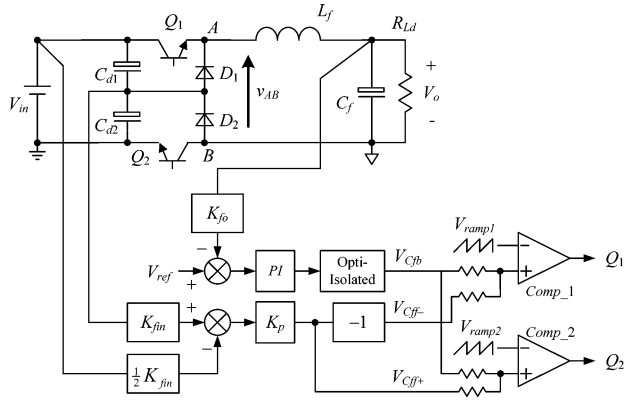


Fig. 13. Feedforward control of the buck TL converter.

A. Feedback Control Mechanism

The feedback control mechanism of this controller is similar to that of the conventional controller for TL converters. The output voltage V_o is sensed through a feedback network $K_{\rm fo}$. The signal is then compared to the reference voltage $V_{\rm ref}$ where

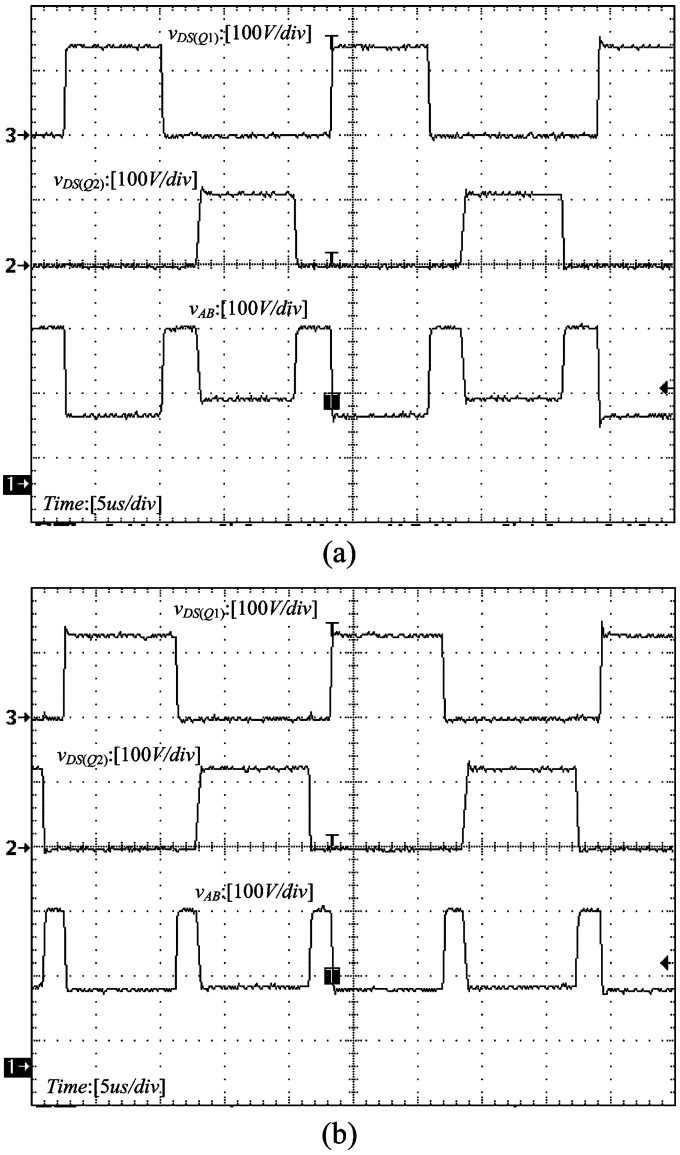


Fig. 14. Experimental waveforms of the buck TL converter. (a) Without the feedforward control. (b) With the feedforward control.

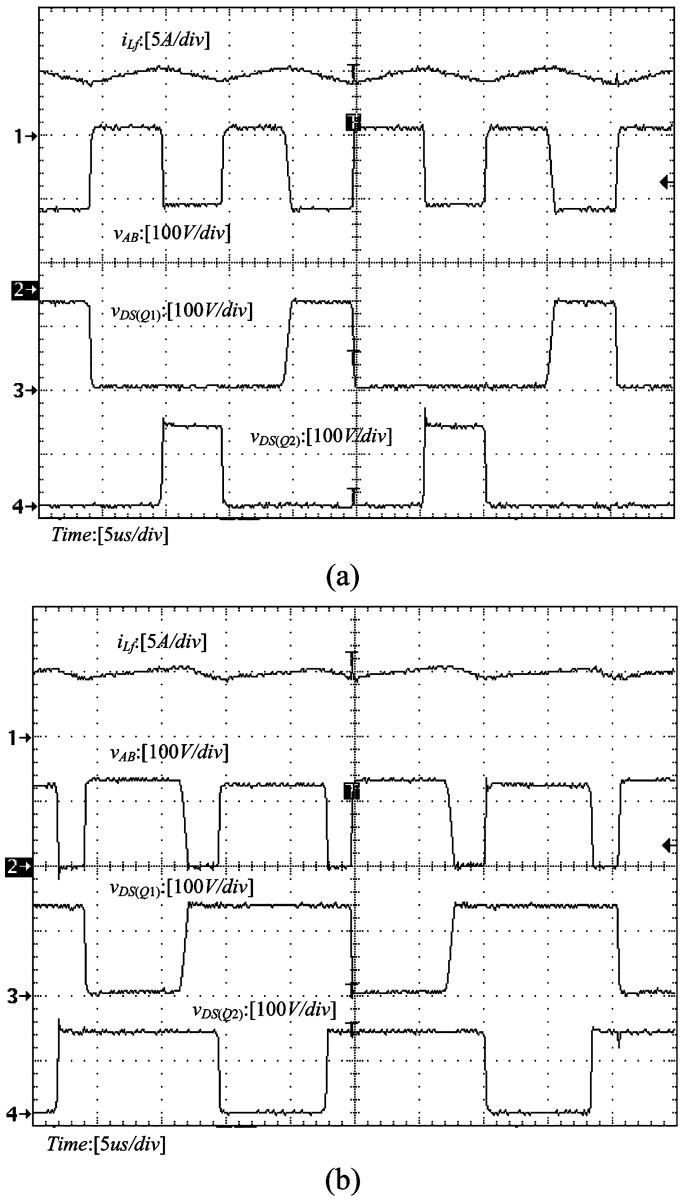


Fig. 15. Experimental waveforms of the buck TL converter operating with (a) $D > 0.5$ and (b) $D < 0.5$.

the error is amplified through a proportional–integral (PI) gain amplifier. This signal is then passed through an isolation device to achieve common ground with the control signal processed from the feedforward loop, i.e., $V_{\mathrm{Cff}-}$ and $V_{\mathrm{Cff}+}$. The feedback control signal after electrical isolation, i.e., V_{Cfb}, is passed through the PWM comparators Comp_1 and Comp_2. The ramp signals fed into Comp_1 and Comp_2 are sawtooth carriers with a shifted phase of $T_s/2$, where T_s is the switching period to generate alternative switching between Q_1 and Q_2.

B. Feedforward Control Mechanism

The feedforward control mechanism begins with the sensing of the input voltage V_{in} and the voltage of capacitor C_{d2}, i.e., V_{Cd2}. The amplitude of V_{in} is scaled down with a ratio of 0.5 K_{fin}, and the amplitude of V_{Cd2} is scaled down with K_{fin}. Recall that the overall feedforward control objective is to set V_{Cd2} to half of the input voltage V_{in}. Hence, this accounts for why the sensing ratio of V_{in} is half of the sensing ratio of V_{Cd2}. With that, the signals 0.5 $K_{\mathrm{fin}}V_{\mathrm{in}}$ and $K_{\mathrm{fin}}V_{Cd2}$ serve as the reference and the tracking signal for the feedforward control, respectively. The difference of these two signals is then amplified through a K_P gain amplifier. This signal is then divided into two paths as follows—one which directly feeds Comp_2, i.e., $V_{\mathrm{Cff}+}$, and the other which is multiplied by -1 before feeding to Comp_1, i.e., $V_{\mathrm{Cff}-}$. At the PWM comparator stage, these feedforward control signals ($V_{\mathrm{Cff}+}$ and $V_{\mathrm{Cff}-}$) are added to the feedback control signal V_{Cfb} to achieve regulation in both the output voltage and the input capacitors' voltage. As an example, if the voltage V_{Cd2} goes above half the input voltage, i.e., $V_{\mathrm{Cd2}} > 0.5V_{\mathrm{in}}$, $V_{\mathrm{Cff}+}$ will be positive, and $V_{\mathrm{Cff}-}$ will be negative. When summed with V_{Cfb} and passed through the PWM comparators, the PWM signal to Q_1 will have a smaller duty ratio than that of Q_2. In other words, Q_2 will have a longer turn on duration than Q_1, therefore prompting more energy being discharged from C_{d2}

than C_{d1}. This reduces the voltage of C_{d2} and increases the voltage across C_{d1}. On the other hand, if voltage V_{Cd2} falls below half the input voltage, the reverse happens.

Note that this feedforward scheme is different from the conventional feedforward scheme which is used for improving the dynamic performance of the converter [23], [24]. The proposed scheme can also be easily adopted for other TL converters. Future work on such aspect may include the large-signal modeling [25] and the nonlinear control [26] of the TL converters.

To verify the effectiveness of the proposed feedforward control scheme, an experiment is performed on a buck TL converter. Fig. 14 shows the experimental waveforms of the buck TL converter with and without the feedforward control. In the figures, Traces 2 and 3 show the voltages across the drain and the source of switches Q_2 and Q_1, respectively. From Fig. 14(a), it can be seen that without the feedforward control, the magnitude of both the waveforms (Trace 2 and Trace 3) is different. This is due to the unequal voltage of the dividing capacitors. On the other hand, from Fig. 14(b), it can be seen that with the feedforward control, the magnitude of the waveforms is almost similar. This is due to the effect of the feedforward control which is ensuring a balance voltage between the dividing capacitors. The significance of this result is further reflected on the waveform of v_{AB}, which represents the voltage across the filter. Without the feedforward control, the waveform of v_{AB} is irregular, and with the feedforward control, the waveform is regular. As discussed, this affects the size requirement of the filter.

An experiment is also performed to evaluate the performance of the proposed scheme under different conversion ratios. Figs. 15(a) and (b) shows the experimental waveforms of the same buck TL converter with the feedforward control scheme operating with duty ratios $D > 0.5$ and $D < 0.5$, respectively. It is demonstrated that the proposed feedforward control scheme performs satisfactorily in maintaining the voltage level of the dividing capacitors for different conversion ratios.

IX. Conclusion

This paper discusses several fundamental issues related to the topological derivation, analysis, and control of TL dc–dc converters. It has been shown, from the derivation of the basic HB TL converter, how TLSCs, namely, the A-TLSCs and the C-TLSCs, are formulated. Based on the concept of TLSCs, a family of TL converters has been derived. It has been shown theoretically that all the nonisolated TL converters that are improved with the use of the A-TLSC and the C-TLSC can operate with reduced filter sizes. However, for the family of isolated TL converters, only the FB and H-FB TL converters can be operated with reduced filter sizes. Furthermore, it has been experimentally demonstrated that the proposed feedforward control scheme works well in maintaining an equal voltage among the dividing capacitors used in the converters.

References

[1] K. M. Trampel, "Three-level inverter circuit," U.S. Patent 3 060 330, Oct. 23, 1962.

[2] A. J. Gruodis, L. K. Lange, and W. H. Mcanney, "Three level converter," U.S. Patent 3 155 845, Nov. 3, 1964.

[3] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-clamped PWM inverter," in *Conf. Rec. IEEE IAS Annu. Meeting*, 1980, pp. 761–766.

[4] R. H. Baker, "Bridge converter circuit," U.S. Patent 4 270 163, May 26, 1981.

[5] D. Czarkowski, D. V. Chudnovsky, G. V. Chudnosky, and I. W. Selesnick, "Solving the optimal PWM problem for single-phase inverters," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 49, no. 4, pp. 465–475, Apr. 2002.

[6] E. E. H. Ismail, M. M. A. Al-Saffar, and A. A. J. Sabzali, "High conversion ratio DC–DC converters with reduced switch stress," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 7, pp. 2139–2151, Aug. 2008.

[7] J. R. Pinheiro and I. Barbi, "The three-level ZVS PWM converter—A new concept in high-voltage DC-to-DC conversion," in *Proc. IEEE IECON*, 1992, pp. 173–178.

[8] J. R. Pinheiro and I. Barbi, "Wide load range three-level ZVS-PWM DC-to-DC converter," in *Proc. IEEE PESC*, 1993, pp. 171–177.

[9] F. Canales, P. M. Barbosa, J. M. Burdió, and F. C. Lee, "A zero-voltage-switching three-level DC/DC converter," in *Proc. CPES*, 2000, pp. 366–371.

[10] F. Canales, P. M. Barbosa, and F. C. Lee, "A zero-voltage and zero-current-switching three level DC/DC converter," *IEEE Trans. Power Electron.*, vol. 17, no. 6, pp. 898–904, Nov. 2002.

[11] X. Ruan, L. Zhou, and Y. Yan, "Soft-switching PWM three-level converters," *IEEE Trans. Power Electron.*, vol. 16, no. 5, pp. 612–622, Sep. 2001.

[12] X. Ruan, D. Xu, and Y. Yan, "Zero-voltage-switching PWM three-level converter with two clamp diodes," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 790–799, Aug. 2002.

[13] T. Song, N. Huang, and A. Ioinovici, "A family of zero-voltage and zero-current-switching (ZVZCS) three-level DC–DC converters with secondary-assisted regenerative passive snubber," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 11, pp. 2473–2481, Nov. 2005.

[14] X. Ruan, Z. Chen, and W. Chen, "Zero-voltage-switching PWM hybrid full-bridge three-level converter," *IEEE Trans. Power Electron.*, vol. 20, no. 2, pp. 395–40, Mar. 2005.

[15] X. Ruan and B. Li, "Zero-voltage and zero-current-switching PWM hybrid full-bridge three-level converter," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 213–220, Feb. 2005.

[16] S. Bai, N. Huang, and A. Ioinovici, "Small-signal modeling and dynamic analysis of a novel ZVZCS three-level converter," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 9, pp. 1958–1965, Sep. 2006.

[17] T. A. Meynarda and H. Foch, "Multi-level conversion: High voltage choppers and voltage-source inverters," in *Proc. IEEE PESC*, 1992, pp. 397–403.

[18] V. Yousefzadeh, E. Alarcon, E. , and D. Maksimovic, "Three-level buck converter for envelope tracking applications," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 549–552, Mar. 2006.

[19] K. H. Chen, H. W. Huang, and S. Y. Kuo, "Fast-transient DC–DC converter with on-chip compensated error amplifier," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 12, pp. 1150–1154, Dec. 2007.

[20] N. A. Keskar and G. A. Rincon-Mora, "A fast, sigma–delta ($\Sigma\Delta$) boost DC–DC converter tolerant to wide *LC* filter variations," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 55, no. 2, pp. 198–202, Feb. 2008.

[21] I. Nuez and V. Feliu, "On the voltage pulse-width modulation control of *L–C* filters," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 47, no. 3, pp. 338–349, Mar. 2000.

[22] Y. Shrivastava, S. Y. Hui, S. Sathiakumar, H. S. H. Chung, and K. K. Tse, "Harmonic analysis of nondeterministic switching methods for DC–DC power converters," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 47, no. 6, pp. 868–884, Jun. 2000.

[23] M. K. Kazimierczuk and A. Massarini, "Feedforward control of DC–DC PWM boost converter," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 44, pp. 143–148, Mar. 1997.

[24] M. K. Kazimierczuk and L. A. Starman, "Dynamic performance of PWM DC–DC boost converter with input voltage feedforward control," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 46, no. 12, pp. 1473–1482, Dec. 1999.

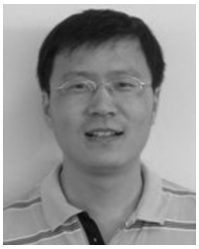
[25] K. Natarajan and M. Yektaii, "Modeling of DC–DC buck converters for large-signal frequency response and limit cycles," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 8, pp. 712–716, Aug. 2006.

[26] S. C. Tan, Y. M. Lai, and C. K. Tse, "A unified approach to the design of PWM-based sliding-mode voltage controllers for basic DC–DC converters in continuous conduction mode," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 8, pp. 1816–1827, Aug. 2006.

Xinbo Ruan (M'97–SM'02) was born in Hubei, China, in 1970. He received the B.S. and Ph.D. degrees in electrical engineering from Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 1991 and 1996, respectively.

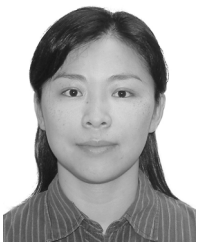
In 1996, he was a Faculty Member with the Electrical Engineering Teaching and Research Division, NUAA, where he became a Professor with the College of Automation Engineering in 2002, teaching and researching in the field of power electronics. From August to October 2007, he was a Research Fellow with the Department of Electronic and Information Engineering, The Hong Kong Polytechnic University, Kowloon, Hong Kong. Since March 2008, he has been with the College of Electrical and Electronics Engineering, Huazhong University of Science and Technology, Wuhan, China. He is also a Guest Professor of Beijing Jiaotong University, Beijing, China, and Hefei University of Technology, Hefei, China. He has published over 100 technical papers in journals and conferences and also published three books. His main research interests include soft-switching dc/dc converters, soft-switching inverters, power factor correction converters, converter modeling, power electronics system integration, and renewable energy generation system.

Dr. Ruan is a Senior Member of the IEEE Power Electronics Society. He was recognized as the Delta Scholar by the Delta Environment and Education Fund in 2003 and the Special Appointed Professor of the Chang Jiang Scholars Program by the Ministry of Education, China, in 2007.



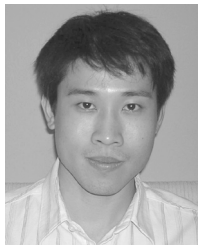
Bin Li (M'02) received the B.S. and M.S. degrees in electrical engineering from Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 1997 and 2002, respectively.

From 2002 to 2004, he was with the Bel Power (Hangzhou) Engineering Center as a Senior Developing Engineer, focusing on low-power dc/dc power module product development. From 2004 to 2007, he was with Tyco Electronics Power Systems Research & Development (Shanghai) Company, Ltd., Shanghai, China, as an Engineer Leader, focusing on telecom standard and customer design ac/dc power module product development. He is currently a Senior Power System Engineer with EMC Information Technology Research & Development (Shanghai) Company, Ltd., Shanghai.



Qianhong Chen (M'06) was born in Hubei, China, in 1974. She received the B.S., M.S., and Ph.D. degrees in electrical engineering from Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 1995, 1998, and 2001, respectively.

In 2001, she was a Faculty Member with the Electrical Engineering Teaching and Research Division, NUAA, where she is currently an Associate Professor with the Aero-Power Sci-Tech Center, College of Automation Engineering. Her research interests include soft-switching dc/dc converters, application of integrated magnetics, and contactless resonant converters.



Siew-Chong Tan (S'00–M'06) received the B.Eng. (with honors) and M.Eng. degrees in electrical and computer engineering from the National University of Singapore, Singapore, Singapore, in 2000 and 2002, respectively, and the Ph.D. degree from The Hong Kong Polytechnic University, Kowloon, Hong Kong, in 2005.

He worked briefly as a Research Associate and then as a Postdoctoral Fellow with the Department of Electronic and Information Engineering, The Hong Kong Polytechnic University, where he is currently a Lecturer. His research interests include motor drives and power electronics.

Chi K. Tse (M'90–SM'97–F'06) received the B.Eng. (Hons.) degree (with first-class honors) in electrical engineering and the Ph.D. degree from the University of Melbourne, Melbourne, Australia, in 1987 and 1991, respectively.

He is currently a Chair Professor and the Head of the Department of Electronic and Information Engineering, The Hong Kong Polytechnic University, Kowloon, Hong Kong. He is also a Guest Professor with Wuhan University, Wuhan, China, Nanjing University of Aeronautics and Astronautics, Nanjing, China, and Southwest University, Chongqing, China. He is the author of *Linear Circuit Analysis* (Addison-Wesley, 1998) and *Complex Behavior of Switching Power Converters* (CRC Press, 2003) and the coauthor of *Chaos-Based Digital Communication Systems* (Springer-Verlag, 2003) and *Chaotic Signal Reconstruction with Applications to Chaos-Based Communications* (TUP, 2005). He is a coholder of a U.S. patent and two pending patents. His research interests include power electronics, complex networks, and nonlinear systems.

In 1987, he was the recipient of the L.R. East Prize by the Institution of Engineers, Australia, the IEEE TRANSACTIONSON POWER ELECTRONICS Prize Paper Award in 2001, and the International Journal of Circuit Theory and Applications Best Paper Award in 2003. In 2007, he was awarded the Distinguished International Research Fellowship by the University of Calgary, Calgary, Canada. While with The Hong Kong Polytechnic University, he received twice the President's Award for Achievement in Research, the Faculty's Best Researcher Award, the Research Grant Achievement Award, and a few other teaching awards. From 1999 to 2001 and since 2007, he was/has been an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS PART I: FUNDAMENTAL THEORY AND APPLICATIONS, and since 1999, he has been an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS. In 2005, he was an IEEE Distinguished Lecturer. He is currently the Editor-in-Chief for the IEEE CIRCUITS AND SYSTEMS SOCIETY NEWSLETTER; an Associate Editor for the *International Journal of Systems Science*, the IEEE CIRCUITS AND SYSTEMS MAGAZINE, and the *International Journal of Circuit Theory and Applications*, and a Guest Editor of a few other journals.