Failure Analysis and Stress Simulation in Small Multichip BGAs

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Abstract—This paper examines one of the common modes of structural failure in multichip ball grid arrays (BGAs), determines its locations within the package structure, relates it to the stresses generated in the reliability tests under which it occurs, and by Finite Element simulations, determines an explanation for the failure, and finally proposes a method to avoid this failure mechanism.

Several designs of multichip BGA substrates were manufactured and production silicon assembled into them. These were all 14 mm × 22 mm 119 ball PBGA. These were subjected to a set of package reliability tests, until some units failed electrical test. The failed units were analyzed and the physical location and shape of the failure was determined in many cases. From this information, the mechanical mode of failure for each unit was determined. In addition there was sufficient information in some of the analyses to provide definite suggestions as to the mechanism of failure.

Meanwhile, finite element analysis was performed using simplified representations of the multichip BGAs, in order to find the locations of highest stress, and the expected modes of failure. This data was matched to the failure modes found in the physical analysis. Some novel failure analysis techniques were used to expose the damage in the failed units.

A particular failure mode occurred frequently in temperature cycle, and the sites of failure were located by failure analysis. The failure was due to open circuit in the copper tracks in the top layer of the substrate caused by cracking in the solder resist directly underneath the edge of the die attach fillet. Finite element analysis was carried out and the location of the actual failures was found to be a local zone of high tensile stress in the solder resist.

Index Terms—BGA, die attach, failure analysis, finite element analysis, multichip, solder resist, thermomechanical stress.

I. BACKGROUND

This work arose from the challenges of qualifying multichip ball grid array (BGA) products. A desire to combine the functions of several different integrated circuits into a single package as quickly as possible set the requirement for a multichip assembly. Several successful two-chip products in leadframe packages existed but this approach could not meet the high number of interconnections needed for present designs. The 14 mm × 22 mm BGA package was evaluated for two-chip and three-chip proposals.

Little was found in the literature about structural integrity of the BGA package; most studies were focused on solder joint reliability. However, McCluskey et al. [1] had examined substrate damage in IR reflow, while Egan et al. [2] and Garrett [3] had examined the attributes of BGA package warpage from different perspectives.

The first assemblies proved successful electrically, but when reliability tests were undertaken many weaknesses came to light. One by one the causes of failures were diagnosed and package improvements were introduced. It will be shown in this paper that thermomechanical stresses are the root cause of the damage; finite element analyses have been carried out and have yielded a partial understanding of the sources of the failures. This paper reports on one of the failure mechanisms observed, and the explanations elicited by FEA.

II. PHYSICAL DESCRIPTION OF THE PACKAGE

The focus of this paper is on the PBGA package, JEDEC outline MS-028 (formerly MO-163), with body size of 14 mm × 22 mm, and 119 balls in a matrix of 17 × 7. The substrate is glass reinforced Bismaleimide Triazine (BT) resin with four layers of copper conductors. The mold-cap is 12 mm × 20 mm at its interface with the substrate, and the relief angle is 30°.

The arrangement in Fig. 1 has three chips encapsulated within the mold-cap. The chips are in line, in a single column, with the greater dimension of each chip across the narrow dimension of the package. This arrangement allows a large proportion of the encapsulated area of the package to be occupied by silicon, and in this instance the silicon to package ratio is 36% by area.

Chip A was positioned nearest to the molding gate. Its horizontal edge was 1.5 mm from the top edge of the encapsulant. The inter-chip space was 1.5 mm approximately, and the space between Chip C and the lower edge of the encapsulant was again 1.5 mm. Normally a BGA needs a minimum clearance between edge of die and edge of encapsulant of 1.5 mm.

Consequently this design was right on the design rule limit for both short ends of the package; the resultant stress exceeded the capabilities of the package. Several failure modes came to light in reliability testing of assemblies using the first design of the substrate. All failure modes, the corrective actions taken, and the resultant improvement in reliability are detailed in Moore and Jarvis [4].

This present paper will focus on one failure mode only. It will describe it in detail, and then present an FEA examination of the
failed region and thereby explain the cause of the failure. Finally it will discuss how the failure mode might be avoided.

III. VERTICAL CRACKING AT EDGE OF DIE-ATTACH

The vertical cracking was discovered in temperature cycle after 500 cycles; it occurred in a total of four instances across three lots each of 45 units at -65 °C to +150 °C. Failure analysis found open-circuits on one or more traces relating to bond-pads on the outer edge of chip A. Acoustic microscopy did not show any delamination. By 1000 cycles, the number of such failures had risen to 22 out of the total of 135 units.

Electrical probing found the traces on the bottom of the substrate to be intact as far as the vias. This confirmed that the open circuit lay in the top copper layer of the substrate. It also enabled the approximate location of defective traces to be determined—close to the related bond-pads. This was possible because the relevant top layer traces were short in length and the electroplating traces were nearby on the same layer, available to be used in electrical probing.

The mold compound and die-attach material were removed without damaging the solder resist (the technique is described later) and a crack was visible which followed the periphery of the die-attach paste around 80% of the perimeter of Die A. A photograph of a portion of this crack is shown in Fig. 2.

Contact points were exposed on the copper trace which was open circuit and it was confirmed that the break in the copper circuit lay precisely underneath the crack in the solder resist.

Fig. 3 is a pair of SEM photographs; note the openings in the solder resist to expose copper for contacting. The right-hand photo shows the curve of the crack as it follows the edge of the die-attach paste around a corner of the chip. This same shape is also evident in the photograph in Fig. 2.

Further investigation of these cracks was carried out using focused ion beam equipment (FIB) and the nature of the crack was explored in detail by this means. The FIB was used to cut an incision in the substrate, and the profile of the crack was examined (see Fig. 4). The cracking occurred at the interface of three different materials, viz. molding compound, die-attach adhesive and solder resist. These have substantially differing mechanical properties and give rise to a high level of stress at the die-attach edge. It was concluded that unless chip A was relocated, the stress-induced damage was unavoidable.

A variety of material changes were considered as potential cures. However, there was not a material available of greatly differing properties which had the potential for eliminating the problem. Instead it was decided to make the design more rugged, and make the circuit insensitive to substrate cracking at the edge of die-attach. This was achieved by rerouting all top-layer traces which passed beneath the edge of any chip.
Fig. 4. FIB incision in substrate; solder mask removed, crack in copper and BT resin.

Fig. 5. (a) Original layout—traces pass beneath edge of die-attach. (b) New rugged layout—only vias underneath die-attach edge.

Sample top-layer traces beneath the sensitive segment of chip A are shown in Fig. 5—with “before” and “after” images to show how rerouting was accomplished.

IV. FINITE ELEMENT SIMULATION

The PRO/Mechanica p-version finite element software was used to investigate the thermomechanical stresses in the PBGA shown in Fig. 1. P-type elements were chosen because they allow rapid changes in mesh density and their insensitivity to element distortion makes them particularly suitable for modeling thin layers, Schiermeier and Szabo [5]. They also converge rapidly, and allow error estimates to be easily incorporated (see Szabo [6]).

With conventional h-type elements the order of the polynomial trial solution used is fixed, usually at either first or second order. Consequently if the accuracy of the results needs to be improved a finer mesh must be used. With p-type elements the order of the trial solution is variable usually from first to ninth order. So if the accuracy of the results from a first or second order analysis needs to be improved the mesh remains unaltered, and the order of the trial solution is incremented automatically until the error measures show the desired accuracy. This automatic improvement of the results to the desired accuracy is termed p-adaptive refinement. Since p-elements are designed to use high order trial solutions, the meshes can be much coarser than the h-element mesh of comparable accuracy.

The 2-D plane strain model of the three-chip PBGA shown in Fig. 1 was built since Kelly [7] showed that this gives a better correlation with a 3-D model than plane stress. The section taken was along the centerline parallel to the 22 mm dimension, and the geometry for the model is shown in Fig. 6. A labeled schematic is shown in the detail in Fig. 8. Global-x ran horizontally from left to right; Global-y was vertically upwards. Global origin was at the lower left hand corner of the model. The model was also divided vertically along the line $x = 11$ mm (i.e., half way along the BT Laminate) in order to apply displacement constraints (two points constrained in $x$ only, and one point constrained in $y$ only). The line $x = 11$ mm is shown in Figs. 6 and 7, and it is clear that the center of chip B is offset from the centerline of the structure. There are no other constraints.

The model consisted of three 0.280 mm thick silicon die, three 0.020 mm thick die-attach layers, a 0.7 mm thick layer of molding compound, and a 0.660 mm BT Laminate layer which incorporated a 0.028 mm top layer of solder resist. Each die-attach layer extended beyond the edge of the silicon die by 0.175 mm, and was terminated with a fillet of 0.2 mm radius. These fillets can be seen in Figs. 6 and 7, and are numbered fillet1 to fillet6 from left to right in Fig. 7.

Except for the BT substrate, all materials were taken as isotropic and temperature independent, with properties shown in Table I. In reality these properties vary with temperature; however the approximations used enabled a simpler analysis to be made without impairing the validity of the findings.

The BT properties are shown in Table II, and were measured by TMA testing of a substrate of similar design and include the contribution of the copper layers.

The mesh used is shown in Fig. 7 above; it contained 800 2-D plane strain elements. Fig. 8 shows a die-attach fillet in detail. As mentioned earlier, three single point constraints were placed on the line $x = 11$ mm shown in Fig. 6. The section of the silicon die for Chip B which lies on this line was constrained from moving horizontally, whilst the lowest point on the top solder resist layer was constrained from moving vertically. The model was assumed stress free at 170 °C (the molding temperature) and the temperature of the entire model was reduced to −65 °C.

The deformation caused by the uniform temperature drop is shown in Fig. 9. The left and right sides of the BT Laminate both contracted horizontally by 30 μm. Negligible warping of the BT Laminate occurred for a central region extending for a third of the way along chip A on the left and a third of the way along chip C on the right. The warping which occurred to the left and right of this central region included the regions below fillet1 on the left and fillet6 on the right.

This warping resulted in both the left and right hand corner points at the extremities of the BT Laminate/solder resist junction dipping by 4.7 μm. This value is consistent with that found on manufactured product at Incoming QA.
In investigating the vertical cracking of the solder resist outlined earlier, attention was focused on any high tensile or shear interface stresses since these could initiate delamination, and provide a site for crack growth. The regions of highest maximum principal stress and highest in-plane shear over the whole model were found to be in the die attach fillet regions. Each of the six fillet regions showed very similar stress distributions with similar stress magnitudes.

The failure analysis work had also drawn attention to the die-attach fillet region as a possible area of high stress. Cracking was found in most exposed areas of solder resist, and it was considered that the failure mechanism was general rather than local. The following analyses focus on the region of fillet6 because this is where the failed traces susceptible to open-circuit were located.

Fig. 10 shows a fringe plot of $\sigma_1$ for the fillet whilst Fig. 13 shows a fringe plot for $\sigma_2$. $\sigma_1$ ranges from 9 N/mm$^2$ to 111 N/mm$^2$ and is tensile whilst $\sigma_2$ ranges from $-162$ N/mm$^2$ to $+39$ N/mm$^2$. Fig. 13 shows that $\sigma_2$ is positive (i.e., tensile) for a large portion of the fillet, so that, taken with $\sigma_1$ being tensile everywhere shows that a large portion of the fillet is in biaxial tension. This arises because the fillet is prevented from contracting by the silicon and the mold compound, both of which have a much lower coefficient of thermal expansion than the die-attach; and both have a high elastic modulus.

However the solder resist has a low elastic modulus, and is pulled upwards as a result of this biaxial tension as shown in Figs. 12 and 13. The deformed shapes are shown in Fig. 14.

It can be seen that the deformed shape of the bottom of the die-attach fillet is accommodated by a corresponding deformation of the solder resist. The die and molding compound remain relatively undeformed, and a slight bowing of the BT resin is also discernible.

Fig. 15 shows how the magnitudes and directions of $\sigma_1$ and $\sigma_2$ vary over the fillet. Along its boundary with the molding com-
pound, and also with the solder resist there are significant portions where $\sigma_2$ is tensile and directed normal to the boundary. This “peeling” stress may cause delamination if adhesion between the materials is weak.

Experience has shown that delamination between the die attach fillet and the mold compound often occurs, indicating that the adhesion between the two materials is poor. Thus the bi-axial tension in the fillet together with the peeling stresses outlined above are likely to cause separation of the fillet from the molding compound and result in a crack tip at point C.

**B. The Stresses at Point C in the Solder Resist**

Point C on the fillet is at the junction of three materials, and is thus a point of material singularity. Accordingly it is essential to check whether the stresses are bounded at this point.

Table III lists the number of degrees of freedom generated by the adaptive model during each of the eight passes, and indicates how the model was automatically refined until convergence had been reached. Fig. 16 shows convergence curves for the principal stresses $\sigma_1$ and $\sigma_2$ for each of the three materials meeting at point C. The stresses in all materials at this point are bounded despite the material singularity. This demonstrates that the material singularity does not create infinite stresses at point C and therefore the results of the analysis are valid at this location.
The principal stress vectors for the region around point C in the solder resist are shown in Fig. 17. There is clearly a distinctive zone around point C where $\sigma_1$ is tensile and directed longitudinally. This zone arises in the solder resist due to tensile stresses in the die-attach fillet near point C directed horizontally from right to left. $\sigma_1$ for this solder resist zone ranged from 20 to 41 N/mm². The manufacturer has determined that the ultimate tensile strength of the solder resist is 27–30 N/mm²—substantially lower than the tensile stress in the local region within 10 or 15 μm of point C.

Any crack in the solder resist which forms at point C will clearly be opened by such a stress field. Even without a crack tip at C these tensile stresses may initiate failure of the solder resist in this region (see Fig. 18).

### V. SUMMARY OF FAILURE ANALYSIS TECHNIQUES

The purpose of this investigation was to examine defects in the package construction, so failure analysis work had to avoid adding damage whenever possible. The destructive decapsulation procedure used for leaded packages has the distinct disadvantage that the chemicals attack the copper traces in the substrate, and it is virtually impossible to expose all die in a multichip BGA assembly without damaging some copper traces. This causes great difficulty in any further electrical analysis. The alternative methodology used is described below.

#### A. Use of Electroplating Traces for Continuity Checks

An examination of plots of the substrate layers showed that several of the damaged circuits were connected to top-layer plating escapes. This enabled continuity checks to be made directly to the relevant bondfinger. Undamaged continuity to the bond-finger was proven and the device was found to be fully functional when accessed through the plating escape.

In these circuits the routing was short; the path in the top layer ran underneath the die for about 1 to 1.5 mm directly to the via. The via went straight to the bottom layer. From the underside it was shown in each case that the routing between the via and the ball was intact. It was also confirmed that the via cross section in the plane of the bottom layer was intact.

This allowed the failure analysis to focus on the possibility of either top layer damage, or horizontal breakage across the via, perhaps in the plane of an inner layer.
The machine-shop surface grinders in toolmaker shops have high precision worktable motions. Vertical motion can be indexed in steps of 0.5 \( \mu \text{m} \), and positional accuracy is better than 2 \( \mu \text{m} \) cumulative at any point in its vertical travel. Since the thicknesses of the substrate layers are ten to twenty times this value the machine is well suited for the controlled depth of grinding required for this failure analysis.

Firstly the device was mounted on the grinder with the balls facing upwards, and the balls were dressed to make them co-planar, in a plane parallel to the top surface of the BGA. The package was turned right side up, and aligned in the grinder vise. Finally the vise was given a slight tilt by placing a 625 \( \mu \text{m} \) (25 mils) shim underneath one end of its 100 mm long base. This resulted in a tilt across the 12 mm dimension of the substrate of 75 \( \mu \text{m} \), equivalent to the thickness of the die-attach layer plus the solder resist layer plus the copper layer. Moore and Jarvis [4] contains several photographs which illustrate the simultaneous exposure of several thin layers by grinding a slightly inclined substrate.

This made it possible to observe and control the progress of removal of each layer. The controlled tilt allowed estimation of the remaining thickness of the exposed layer at any location with acceptable accuracy. The key objective in this work was to expose the top solder mask layer, while leaving the underlying copper layer intact in the area where damage was suspected. The method was effective.

C. Use of Laser to Make Probe Opes in the Solder Resist

The solder resist was exposed in the area of interest, and the next step was to find the location of the open circuit. There was a risk that if the surface grinding were continued in order to remove the solder resist and expose the copper, then the crack in the copper could become smeared over by the action of the grinder. Accordingly it was decided to make small openings in the solder resist which would expose the copper in local regions only.

Several options were evaluated, and the results obtained by blasting the solder resist with a neodymium–ion doped Yttrium Aluminum Garnet (Nd: YAG) laser—commonly known as a green laser—were found to be acceptable. Several examples of these openings are evident in the SEM photographs in Fig. 3. The opening size is approximately 100 \( \mu \text{m} \) across.

The technique used was to make two openings close by each other on one side of the open-circuit location, both positioned over the open-circuit track, and to prove continuity of the contacts between them. A similar pair of openings was made over the same track some distance away and continuity verified there also. The continuity was then tested between one contact in each pair to determine the open circuit. Additional openings were made, progressively closer to the suspected site of the defect, until the location of the open circuit was determined to within 100 \( \mu \text{m} \) of the crack.

D. Use of FIB for Cross-Sectioning of the Cracks

Once the open-circuit was located and confirmed to lie at the crack in the solder resist, it became necessary to examine the crack in cross-section. Although conventional laboratory cross-sectioning and polishing apparatus could probably have been
used it was found to be simple and convenient to use Focused Ion Beam equipment both for making the cross-section and for examining it afterwards.

In every case, the crack started as a separation in the vertical plane, and gradually tended to an angle of approximately 45° from the vertical. When it reached the interface with underlying material (e.g., from solder resist to copper, and from copper to BT substrate) the crack became vertical again, and then tended to a 45° angle in the opposite direction to that in the previous layer. In this way the crack tended to maintain its position vertically underneath the edge of the die-attach adhesive.

The pattern of crack was consistent from sample to sample.

VI. CONCLUSIONS

The finite element analysis demonstrated that high stress levels exist in the solder resist at the tri-material point. It identified the high TCE of the die-attach and the low tensile strength of the solder resist as the primary factors in this failure mechanism. It explained how the cracks found during testing came to exist.

Under a large temperature drop, a very localized tensile stress arises in the solder resist, exactly at the outer edge of the die-attach fillet. This stress is high enough to cause cracking of the solder resist around the entire periphery of the die. This crack can propagate into the underlying copper and cause the copper to become open circuit. The crack does not appear to continue past the glass fiber reinforcement of the substrate.

With existing material sets, the stress is unavoidable. A solution is to reroute the top-layer traces so that no trace passes across the edge of the die-attach fillet. This has been demonstrated to be effective in practice. Design rules for substrate layout for BGAs are needed to ensure that safe layout of substrate traces is implemented as a matter of good design.

VII. RECOMMENDATIONS

The solution implemented in this particular instance was a work-around which did not eliminate the destructive stresses. There is scope for a number of studies which might be fruitful. Firstly, the possibility of eliminating the die-attach fillet and its effect on stresses within the structure could be studied. Secondly, the possible changes in stress distribution from increasing the thickness of the solder resist may point toward reliability improvements. And thirdly, a combination of thicker solder resist coupled with a die-attach adhesive having significantly lower coefficient of thermal expansion (even with a much higher modulus of elasticity), could lead to a more durable construction for this type of package.

Work is under way with real-life assemblies and finite element simulations to explore these variables. Meanwhile a root cause of reliability failures in BGAs has been identified and a practical work-around solution is offered herein.

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REFERENCES


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