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Issue Date	2014-06
URL	http://hdl.handle.net/10228/5782
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Ultra-fast Lateral 600 V Silicon PiN Diode Superior to SiC-SBD

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***Abstract*—Ultra-fast silicon PiN diode is proposed by lateral structure with traps using silicon on insulator (SOI) substrate as shown in Fig. 1. The proposed lateral SOI silicon PiN diode achieved ultra-fast reverse recovery without waveform oscillation successfully. The proposed lateral SOI structure with traps will contributes to performance improvement of all of bipolar power devices including IGBT.**

I. BACKGROUND

Efficiency improvement and prevalence of power electronics apparatus are key factors for efficient energy usage in the more electric society. Standing on this point of view, role of power electronics as nega-watt was examined. Energy saving by highly efficient power electronics apparatuses and systems is equivalent to electrical energy generation. Using this concept, nega-watt cost concept is introduced [1, 2].

For the nega-watt cost reduction, the demands of fast switching, low forward voltage drop and low cost are required for power semiconductor devices. That's because the fast switching and the low forward voltage drop increase the saved energy. And the fast switching, the low forward voltage drop and the low cost reduce the system cost.

In order to meet the demands, power semiconductor devices have made remarkable progress in the last decade and many technologies have been continuously researched to enables the next generation power electronics. The technologies are roughly divided into three areas, namely, "More Silicon (Breakthrough in silicon power technology)", "Beyond Silicon (Heterogeneous integration technology)" and "More than Silicon (Wide-band-gap power technology)".

Silicon devices are superior to wide-band-gap power devices in the aspect of mass-production technology. On the other hand, it has thought that the further fast switching of the silicon devices is difficult by the physical property. Therefore, authors try to research ultra-fast reverse recovery and propose a novel diode structure in the silicon power technology.

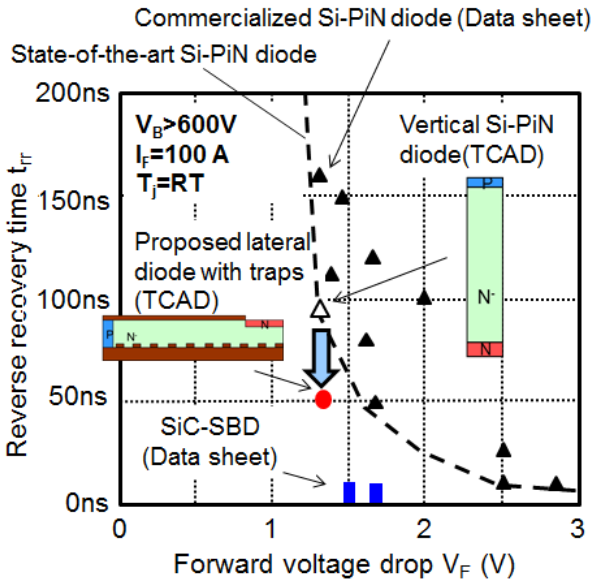


Fig. 1. Performance of proposed lateral SOI PiN diode and benchmarks (Plotted diodes by TCAD don't generate waveform oscillation).

II. POTENTIAL AND PLOBLEM FOR FASTER REVERSE RECOVERY

Reverse recovery speed and forward voltage drop are main characteristics in diode performance. The forward voltage drop of silicon PiN diode (Si-PiN) is determined by the sum of the built-in potential at PN junction and the voltage drop in low resistance N- layer with stored carrier. In contrast, the forward voltage drop of silicon carbide schottky-barrier diode (SiC-SBD) is determined similarly by the sum of the schottky-barrier height at metal-silicon junction and the voltage drop in thin drift layer. When Si-PiN is compared with SiC-SBD, the forward voltage drop is almost the same, but reverse recovery speed is extremely slow by the time for sweeping stored carrier out of N- layer.

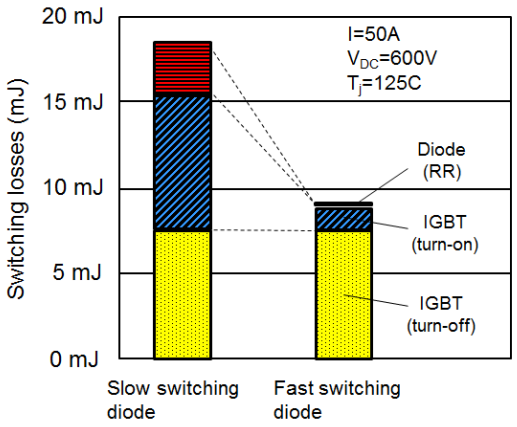


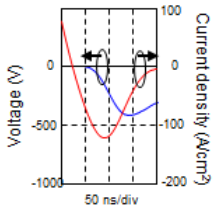
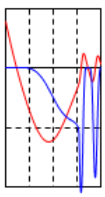
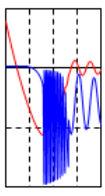
Fig. 2. Switching loss on power devices in experiment [3].

Fast reverse recovery has a large impact to not only diode but also switching device because reverse recovery carrier path through switching device during turn-on and increase turn-on loss. The turn-on loss is dramatically reduced with reverse recovery loss reduction by using fast recovery diode in experiment as shown in Fig. 2 [3].

Authors analytically calculate the reverse recovery speed by bipolar device model and revealed that there is a big room for faster reverse recovery [4, 5]. The calculated speed became many times faster than state-of-the-art Si-PiN by adapting thin N- layer. On the other hand, it's also revealed by TCAD simulation that thin N- Si-PiN beyond the state-of -the-art Si-PiN induces strong waveform oscillation during reverse recovery as shown in table 1. That's why it was impossible to realize ultra-fast Si-PiN until now.

The trigger of the oscillation was clarified from previous works [6-9]. When the carrier injection of the diode is stopped, the stored carrier is carried away from both sides of the diode. At the same time, the high electric field regions expand from the both sides and finally reach the other high electric field. The phenomenon is the trigger of the oscillation and called "dynamic punch-through". In contrast, thick N- layer doesn't generate dynamic punch-through, so the waveform is not oscillated.

TABLE 1. Simulated reverse recovery waveforms of conventional vertical diodes with different N- layer width [5].

Si-PiN Structure	P, 100 µm, N-, N	90 µm	40 µm
t_{rr} (ns)	150	130	110
V_F (V)	1.85	1.71	1.13
Reverse recovery waveform (L_S=100nH, V_B>600V, T_j=RT))			

The previously-proposed diode structures for the oscillation suppression are roughly divided into two types; one prompts reinjection of carrier by partial doping layer and another avoids hard dynamic punch-through by middle doping layer in N- layer [7, 10-14]. However, the both structures cannot achieve dramatic fast reverse recovery because the reinjection carrier increases reverse recovery loss and the middle doping layer worsen trade-off between reverse recovery loss and forward voltage drop by longer current pass. If the middle doping layer is made by thin layer with slightly high doping, the thin layer causes dynamic punch-through.

III. Proposed Ultra-fast Silicon Diode by Lateral SOI Structure with Traps

It is obvious that prevention of dynamic punch-through is required to suppress the oscillation. However, the prevention with fast reverse recovery beyond state-of-the-art diode is difficult for conventional vertical PiN diode as mentioned in chapter 3. From the aspect of dynamic punch-through, the authors propose lateral SOI diode with traps as shown in Fig. 3. The traps act as an electric field stopper without higher doping layer in the n-layer. The thickness of silicon and buried SiO_2 are 10 µm and 5 µm respectively. And the trap pitch is 5 µm and the trap height is 0.5 µm. The traps are designed by electric field distribution.

The conventional vertical diode forms the lineally-sloped electric field distribution corresponding to doping concentration of N- layer as shown in Fig. 4. Therefore, the vertical diode is easy to generate dynamic punch-through on the high voltage like surge voltage. Lateral SOI diode has two electric field peaks at the borders of layers. So the electric field is changed and dynamic punch-through is suppressed a little. The lateral SOI diode with traps also has the two electric field peaks with lower electric field near N layer. Eventually, the dynamic punch-through of the proposed diode is most suppressed in these three diodes by strong suppression of electric field penetration in N- layer using trapped hole as shown in Fig. 5.

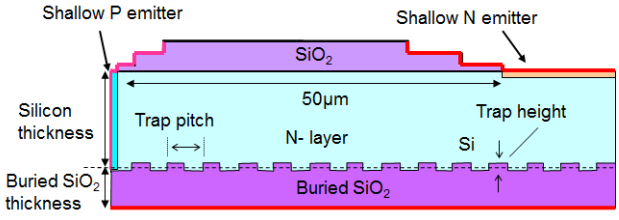
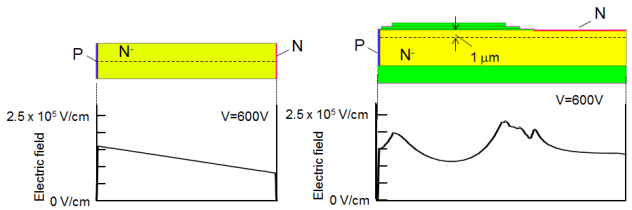
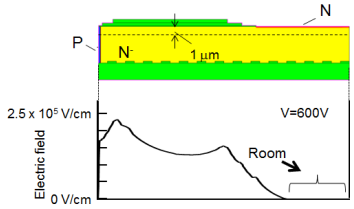


Fig. 3. Structure of proposed lateral SOI PiN diode.



(a) Conventional vertical Si-PiN

(b) Lateral SOI Si-PiN



(c) Proposed lateral SOI Si-PiN with traps

Fig. 4. Diode structures and corresponding electric field along dotted line by TCAD simulation.

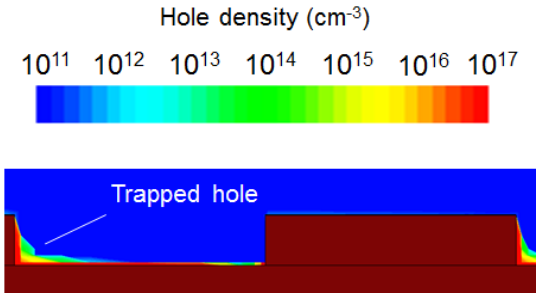
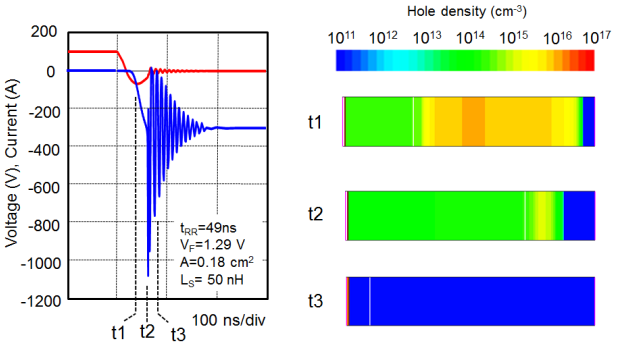


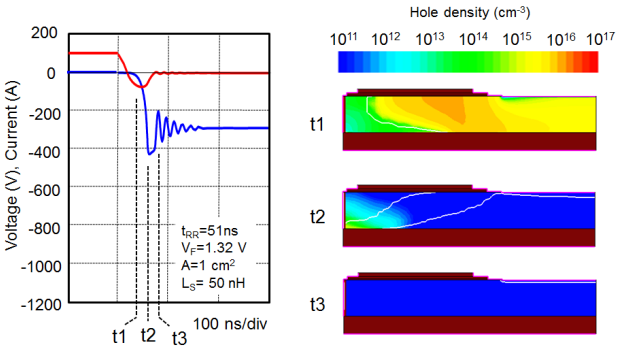
Fig. 5. Trapped hole in buried SiO_2 corresponding with Fig. 4. (c).

The trap concept was introduced in previous works to higher the breakdown voltage on power devices with trapped carrier [15-21]. For example, concavo-convex-shaped oxide film or dish-shaped oxide film is used for lateral devices and vertical devices respectively. The point of trap concept is the suppression of electric filed penetration. Therefore the authors thought the trap concept can be utilized to prevent dynamic punch-through with thin N- layer.

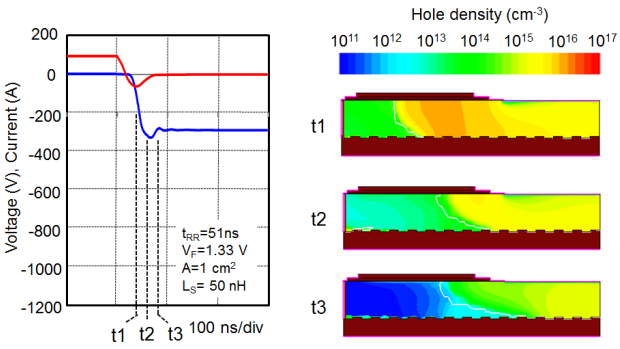
The oscillation of proposed lateral diode is successfully suppressed by the trap concept as shown in Fig. 6. Stored carrier remains throughout the reverse recovery time and dynamic punch-through is not generated as expected. On the other hand, the strong oscillation is generated by dynamic punch-through on the conventional diode and lateral SOI diode. The proposed lateral Si-PiN successfully achieves ultra-fast reverse recovery to one-half compared to state-of-the-art vertical Si-PiN without the oscillation as shown in Fig. 1. The hole density of the proposed diode gradually eliminated as shown in Fig. 7. The design of the proposed diode was discussed by the height of hole traps as shown in Fig.8. Since trapped hole is increased along with increasing trap height, the oscillation suppression effect is improved.



(a) Conventional structure of vertical Si-PiN



(b) Lateral SOI Si-PiN



(c) Proposed lateral SOI Si-PiN with traps

Fig. 6. Waveform during reverse recovery and corresponding to hole density by TCAD simulation.

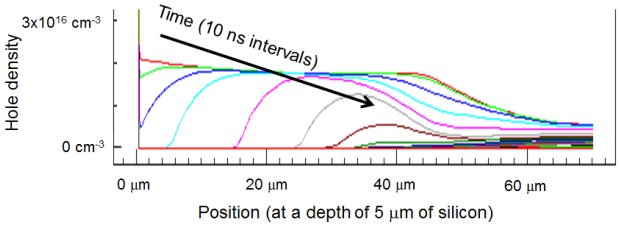


Fig. 7. Hole density change during reverse recovery corresponding to Fig. 6 (c) by TCAD simulation.

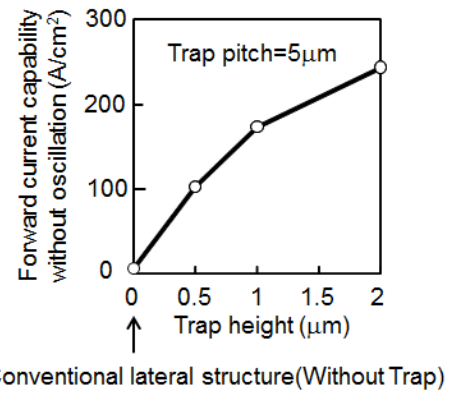


Fig. 8. Design dependence of maximum current capability without waveform oscillation..

The proposed lateral SOI structure achieves a major breakthrough on the performance improvement barrier of the oscillation. The proposed structure will contributes bipolar power device design including IGBT.

IV. CONCLUSION

For the nega-watt cost reduction, the fast switching, the low forward voltage drop and the low cost are required for power semiconductor devices. Especially, fast reverse recovery (fast switching) has a large impact to not only diode but also switching device because reverse recovery carrier path through switching device at turn-on and increase turn-on loss.

Authors analytically calculate the reverse recovery speed by bipolar device model and revealed that there is a big room for faster reverse recovery. On the other hand, it's also revealed by TCAD simulation that thin N- Si-PiN beyond the state-of-the-art Si-PiN induces strong oscillation during reverse recovery.

The authors propose lateral SOI Si-PiN with traps and achieved the ultra-fast reverse recovery without the oscillation. The proposed lateral SOI structure with traps will contributes to all of bipolar power devices including IGBT.

REFERENCES

[1] "The research for green electronics technologies which efficiently utilize electric power and enable the lowest-energy-consumption in the year 2050 (20090000000868)," NEDO Research Report, 2007.

[2] Hiromichi Ohashi, "Power devices now and future, strategy of Japan Role of power electronics for a low carbon society," Proc. of ISPSD, pp. 9-12, 2012.

[3] Masanori Tsukuda, Ichiro Omura, Wataru Saito, Tomokazu Domon and Masakazu Yamaguchi, "Power Loss Estimate for 2 Level 3 Phase Inverter using 1200 V-Class Si-IGBT and 1200 V-Class SiC-SBD," (in Japanese) Proc. of IEEJ, Issues 4, pp. 5-6, 2005.

[4] Ichiro Omura, Wataru Saito, Tomokazu Domon and Kunio Tsuda, "Gallium Nitride Power HEMT for High Switching Frequency Power Electronics," Proc. of IWPSD, pp. 781-786, 2007.

[5] M. Tsukuda, K. Kawakami, K. Takahama, I. Omura, ""Design for EMI" approach on power PiN diode reverse recovery," Microelectronics Reliability Vol. 51, Issues 9-11, pp. 1972-1975, 2011.

[6] Masanori Tsukuda, Ichiro Omura, Yoko Sakiyama, Masakazu Yamaguchi, Ken'ichi Matsushita and Tsuneo Ogura, "Critical IGBT Design Regarding EMI and Switching Losses," Proc. of ISPSD, pp. 185-188, 2008.

[7] Masanori Tsukuda, Yoko Sakiyama, Hideaki Ninomiya and Masakazu Yamaguchi, "Dynamic Punch-Through Design of High-Voltage Diode for Suppression of Waveform Oscillation and Switching Loss," Proc. of ISPSD, pp. 128-131, 2009.

[8] Kenichi Takahama and Ichiro Omura, "Numerical study on very high speed silicon PiN diode possibility for power ICs in comparison with SiC-SBD," Proc. of ISPSD, pp. 169-172, 2010.

[9] Josef Lutz, Heinrich Schlangenotto, Uwe Scheuermann and Rik De Doncker, "Semiconductor Power Devices: Physics, Characteristics, Reliability," Springer, 2011.

[10] M. Mori, Y. Yasuda, N. Sakurai and Y. Sugawara, "A NOVEL SOFT AND FAST RECOVERY DIODE (SFD) WITH THIN P-LAYER FORMED BY AIS ELECTRODE," Proc. of ISPSD, pp. 113-117, 1991.

[11] K. T. Kaschani and R. Sittig, "How to avoid TRAPATT Oscillation at the Reverse-Recovery of Power Diodes," Proc. of CAS'95, pp. 571-574, 1995.

[12] K. Satoh, K. Morishita, Y. Yamaguchi, N. Hirano, H. Iwamoto and A. Kawakami, "A Newly Structured High Voltage Diode Highlighting Oscillation Free Function In Recovery Process," Proc. of ISPSD, pp. 249-252, 2000.

[13] M. Nemoto, T. Naito, A. Nishiura and K. Ueno, "MBBL Diode : A Novel Soft Recovery Diode," Proc. of ISPSD, pp. 433-436, 2004.

[14] F. Hille, M. Bassler, H. Schulze, E. Falck, H.P. Felsl, A. Schieber, A. Mauder, "1200V Emcon4 freewheeling diode - a soft alternative," Proc. of ISPSD, pp. 109-112, 2007.

[15] Robert Plikat, Dieter Silber and Wolfgang Wondrak, ""Very High Voltage Integration" in SOI Based on a New Floating Channel Technology," Proc. of IEEE International SOI Conference, pp. 59-60, 1998.

[16] Ichiro Omura and Akio Nakagawa, "Silicon on Insulator semiconductor device with increased withstand voltage," United States Patent, 6,049,109, April 11, 2000.

[17] Holger Kapels, Robert Plikat and Dieter Silber, "Dielectric Charge Traps: A New Structure Element for Power Devices," Proc. of ISPSD, pp. 205-208, 2000.

[18] Ichiro Omura and Akio Nakagawa, Japanese Patent, No. 3950105, 2007.

[19] Ichiro Omura and Akio Nakagawa, Japanese Patent, No. 3959125, 2007.

[20] Xiaorong Luo, Bo Zhang, Zhaoji Li, Yufeng Guo, Xinwei Tang, and Yong Liu, "A Novel 700-V SOI LDMOS With Double-Sided Trench," IEEE Electron Device Lett., vol. 28, No. 5, pp. 422-424, May 2007.

[21] Satoshi Shiraki, Yoichi Ashida, Shigeki Takahashi, and Norihito Tokura, "Analysis of Transient Characteristics of Lateral IGBTs and Diodes on Silicon-on-Insulator Substrates with Trenched Buried Oxide Structure," Proc. of ISPSD, pp. 261-264, 2010.