MEMOIRS OF THE FACULTY OF ENGINEERING
FUKUI UNIVERSITY
VOL.29 No.2 1981

Noise and Transient Response Characteristics of Digital Phase-Locked Loops

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(Received Aug. 31, 1981)

In designing a digital phase-locked loop two important criteria include short acquisition time and high accuracy. The settling time of step response and the steady-state phase error variance of a loop may be considered as measures of the acquisition time and the accuracy of the loop respectively. We have established relationships between the settling time of step response and the steady-state phase error variance for the first and second-order loops. With this, it is a simple matter to find proper filter parameters for a desirable or nearly optimum loop performance with a short settling time and a small phase error variance.

I. INTRODUCTION

In recent years the performance of digital phase-locked loop (DPLL) has been investigated by a number of authors. In particular, Weinberg and Liu [1] considered discrete time analyses of first and second-order loops for phase step and frequency step inputs. Gill and Gupta [2] analyzed higher order loops and investigated the problem of optimizing loop filter for minimum mean square error.

In designing PLL, digital or analog, there exist two important criteria that must be taken into consideration. The first one is that PLL should follow the change of phase or frequency of incoming signal as quickly as possible, and the second is that its steady-state mean square phase error should be kept as small as possible. Obviously these are contradictory requirements that cannot be satisfied simultaneously. Thus we have to make a compromise between fast response and small steady-state phase error variance. For this purpose it is necessary to investigate the relationships between transient response and steady-state phase error characteristics of PLLs.

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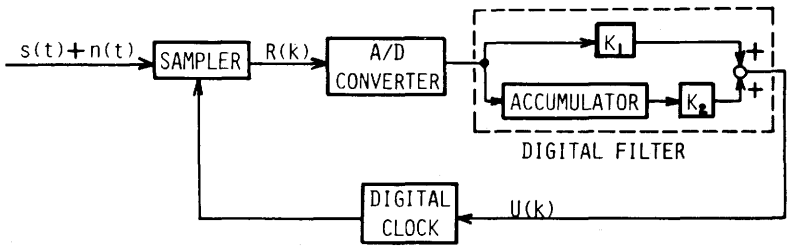
None of the previous papers seem to have considered this sort of problem.

In this paper we will consider a DPLL shown in Fig. 1 and specifically be concerned with relationships between the steady-state phase error variance and the settling time of step response of the DPLL. The settling time may be considered as a control-theoretic measure of the loop's acquisition time, and the phase error variance gives an indication of the accuracy of the loop. The relationships will lead to a solution of the problem: what loop filter is to be placed in the loop or what filter parameters are to be chosen in order to obtain a satisfactory performance of the loop.



($K_2 = 0$ for first-order filter)

Fig. 1 Block diagram of digital phase-locked loop.

II. TRANSIENT RESPONSE

The DPLL shown in Fig. 1 tracks the zero crossings of incoming signals, and hence is characterized by nonuniform sampling intervals.

The input to the DPLL is assumed to be the sum of a signal

$$s(t) = A \sin\{\omega_0 t + \theta(t)\} \tag{1}$$

and white Gaussian noise $n(t)$. The input is sampled at time instants $t(k)$ determined by the digital clock.

The value of the kth sample is denoted by $R(k)$, i.e.,

$$R(k) = A \sin\{\omega_0 t(k) + \theta(k)\} + n(k), \tag{2}$$

where $\theta(k) = \theta\{t(k)\}$, $n(k) = n\{t(k)\}$. Let $I(k)$ denote the time between the $(k-1)$th and the kth sampling instants. The sequence $\{R(k)\}$ is passed through the A/D converter and the digital filter whose output, $\{U(k)\}$, is used to control the period of the DPLL ac-

cording to the relationship

$$I(k) = T - U(k-1), \tag{3}$$

where $T = 2\pi/\omega_0$ is the nominal clock period.

Without loss of generality we can assume that $t(0) = 0$. Therefore it follows from (3) that

$$t(k) = \sum_{j=1}^{k} I(j) = kT - \sum_{j=0}^{k-1} U(j). \tag{4}$$

From Fig. 1, $U(j)$ is given by

$$U(j) = K_1 R(j) + K_2 \sum_{i=0}^{j} R(i). \tag{5}$$

From (2), (4), and (5) we obtain

$$\theta(k+1) - \theta(k) = \phi(k+1) - \phi(k) + \omega_0(K_1 + K_2)\{A \sin\phi(k) + n(k)\} + \omega_0 K_2 \sum_{j=0}^{k-1} \{A \sin\phi(j) + n(j)\}; \tag{6}$$

where $\phi(k)$ is the phase error at $t(k)$ and is given by

$$\phi(k) = -\omega_0 \sum_{j=0}^{k-1} U(j) + \theta(k). \tag{7}$$

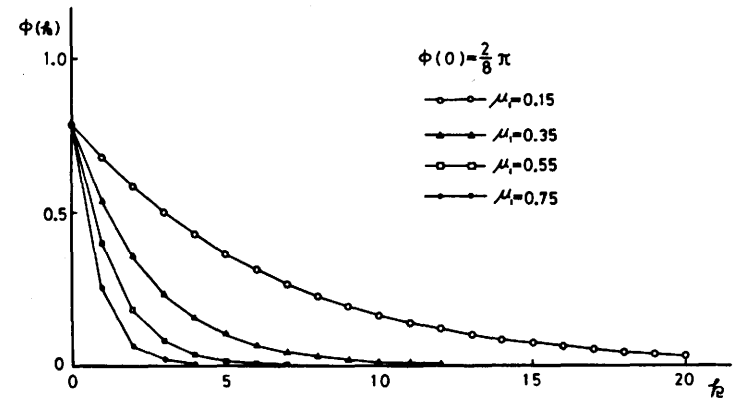
First, the response of the first-order loop to phase step input is considered. The loop is assumed to be noise-free. For the first-order loop with phase step input, $K_2 = 0$ and $\theta(k+1) = \theta(k)$, and (6) reduces to

$$\begin{aligned} \phi(k+1) - \phi(k) &= -\omega_0 K_1 A \sin\phi(k) \\ &= -\mu_1 \sin\phi(k), \end{aligned} \tag{8}$$

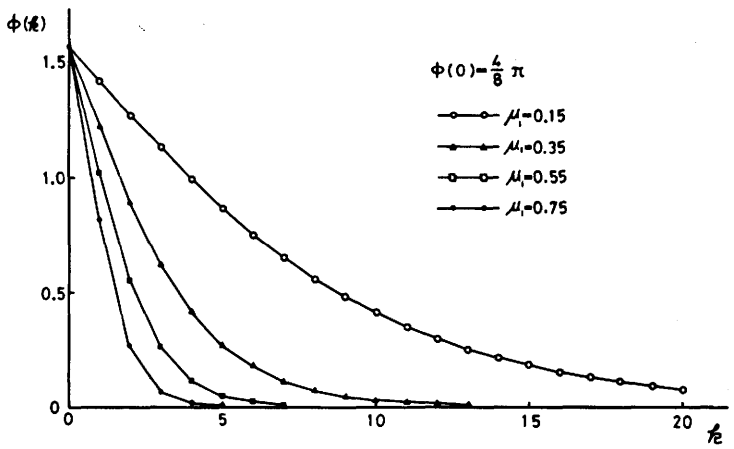
where

$$\mu_1 = \omega_0 K_1 A. \tag{9}$$

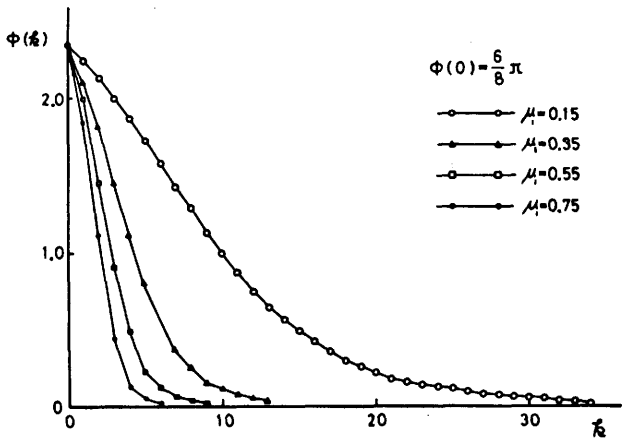
Solving the difference equation (8) numerically, the transient responses of the first-order loop to phase step input have been obtained for several values of the loop gain μ_1. Some of the result is shown in Fig. 2.



(a)



(b)



(c)

Fig. 2 Responses of first-order loop to phase step input

For the second-order noise-free loop with frequency step input, (6) reduces to

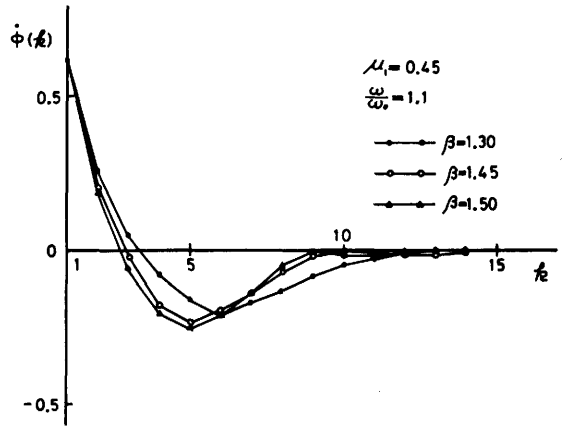
$$\phi(k+1) - 2\phi(k) + \phi(k-1) = \lambda_1 \sin\phi(k-1) - \beta\lambda_1 \sin\phi(k), \tag{10}$$

where

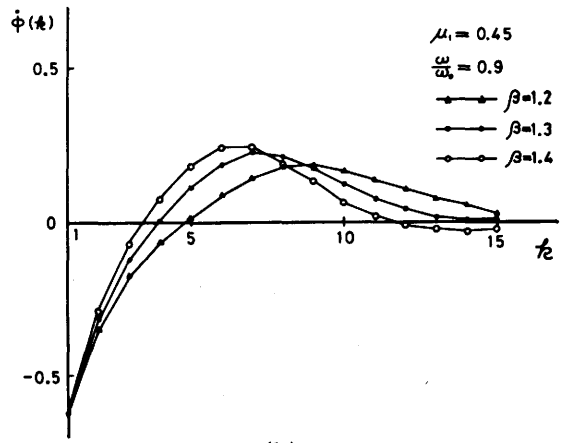
$$\lambda_1 = \omega K_1 A = \mu_1 \omega/\omega_0, \tag{11}$$

$$\beta = (K_1 + K_2)/K_1. \tag{12}$$

For various choices of filter parameters and initial conditions, the difference equation (10) has been solved to obtain transient responses and incremental phase plane plots, some of which are shown in Figs. 3 and 4. In those figures $\dot{\phi}(k)$ represents $\phi(k)-\phi(k-1)$.



(a)



(b)

Fig. 3 Responses of second-order loop to frequency step input.

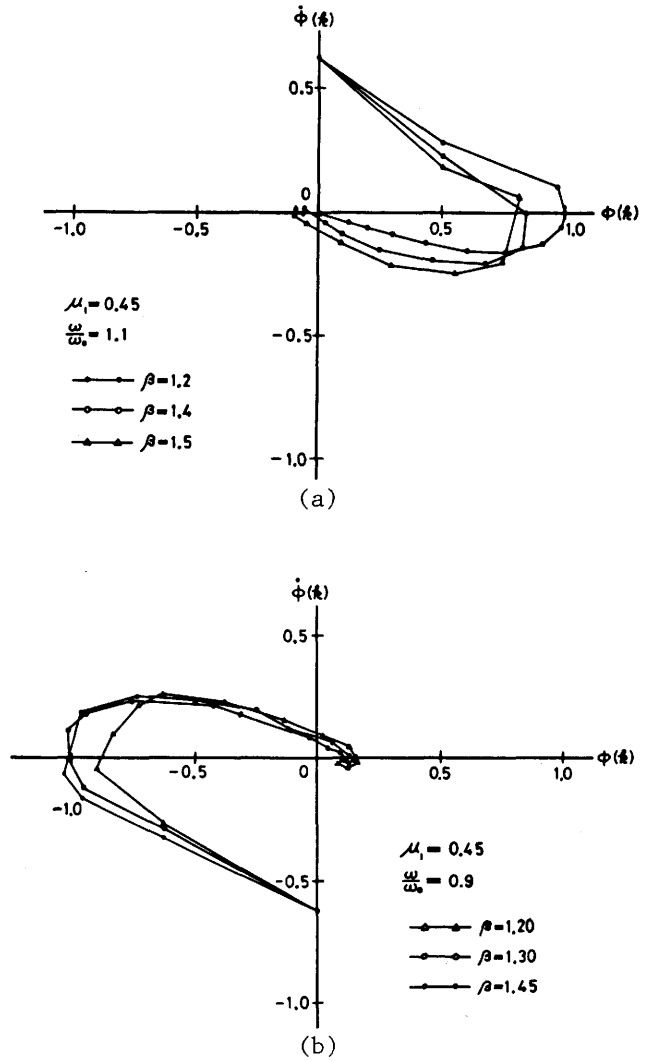


Fig. 4 Incremental phase plane plots of second-order loop for frequency step input.

The settling time to characterize these responses is defined as follows:

For the first-order loop with phase step input, the settling time T_{s1} is defined as the value of k required for $|\phi(k)|$ to decrease to and stay within 10 per cent of $|\phi(0)|$.

For the second-order loop with frequency step input, the settling time T_{s2} is defined as the value of (k+1) required for $|\phi(k+1)-\phi(k)|/\omega_0 T$ to decrease to and stay within 5 per cent of $|\omega-\omega_0|/\omega_0 = |\phi(1)-\phi(0)|/2\pi$.

Figure 2 clearly shows that the settling time T_{s1} is shortened by increasing the loop gain μ_1. This is the same with the settling time T_{s2} of the second-order loop, as long as the value of μ_1 remains below a certain upper limit. The upper limit is known to be $(\omega_0/\omega)(4/1+\beta)$ [1]. Concerning the other filter parameter β, we can roughly conclude from Figs. 3 and 4 that the settling time T_{s2} becomes short as the value of β increases.

III. SETTLING TIME VS. PHASE ERROR VARIANCE CHARACTERISTICS

As mentioned before, the settling time is a measure of the acquisition time of the DPLL, while the steady-state phase error variance gives an indication of the accuracy of the loop disturbed by the noise at the input.

In the past, several authors analyzed the first and second-order loops for phase step and frequency step plus noise inputs [1),3)]. A way to do this is to apply Gram-Charlier series expansion to the Smoluchowski equation associated with phase error probability density of the DPLL [3].

In the present work, steady-state phase error variances for the first and second-order loops have been obtained by the analytical method mentioned above, and to justify the results the digital simulation of (6) has also been performed. The analytical results have been found to be in good agreement with the simulation results.

The steady-state phase error variance and the settling time of step response are both related to loop filter parameters. Therefore, the phase error variance can be related to the settling time through loop filter parameters.

In Fig. 5 the phase error variance is shown as a function of the settling time for the first-order loop with various initial conditions and inverse signal-to-noise ratios (ISNs). The ISN is defined as $\overline{n^2(t)}/A^2$. Figure 6 shows the similar relation between the settling time and the phase error variance for the second-order loop.

In the first-order loop, as the loop gain μ_1 increases, the loop's ability to correct phase error is improved, and as a result the settling time decreases. On the other hand, as μ_1 increases noise power in the loop also increases, and this increases the phase error variance.

Basically this is the same with the second-order loop. However, the problem is not so simple as in the case of the first-order loop, since the step response becomes oscillatory for large loop gain. In the case of the second-order loop there is another parameter which

we are allowed to choose, i.e., β. It is possible for the second-order loop to have a satisfactory or nearly optimum performance by a proper choice of the filter parameters, μ_1 and β, since the phase error variance is not sensitive to the change of the settling time for small μ_1 and β as we can observe in Figs. 6(a) and 6(b).

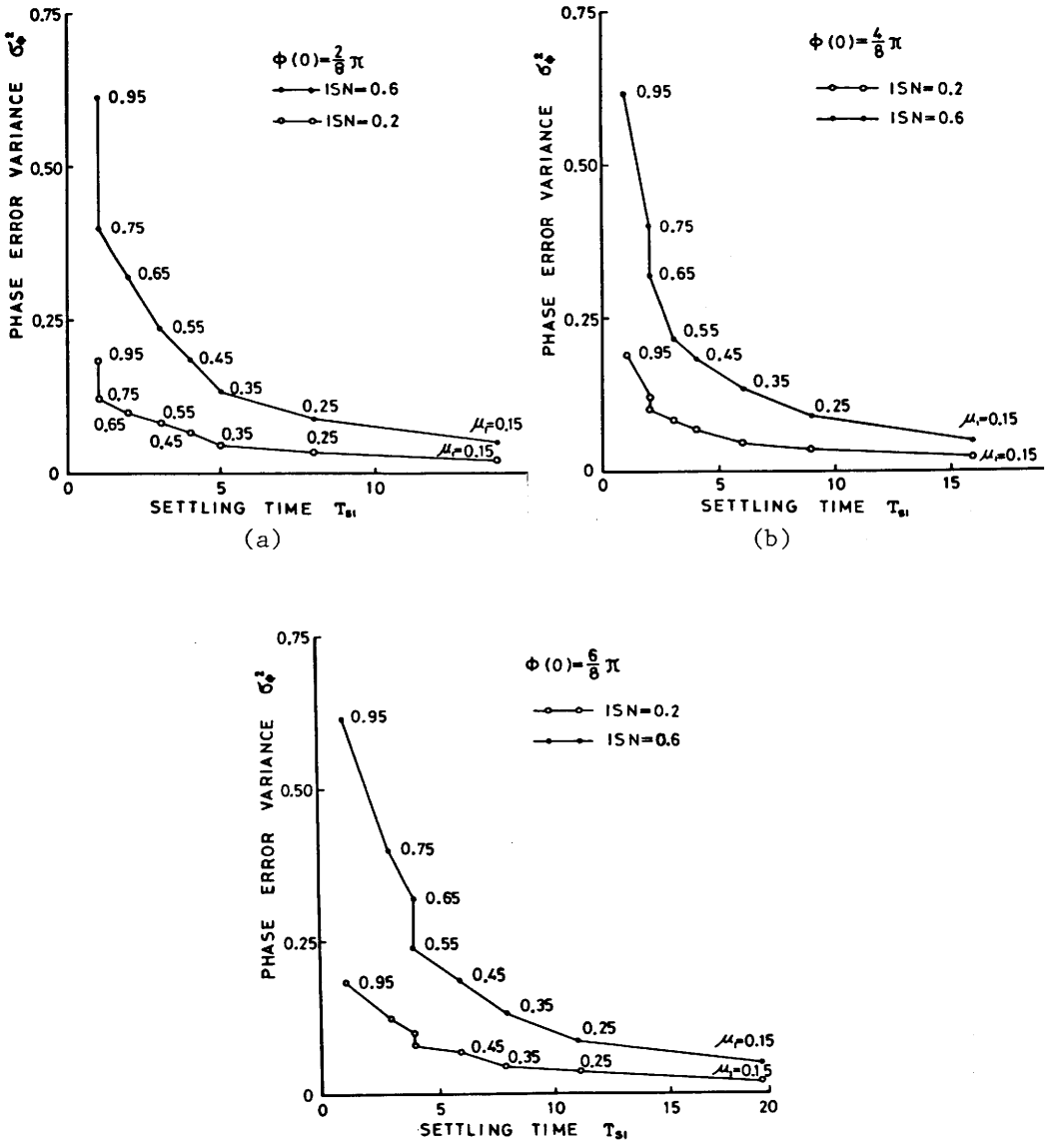


Fig. 5 Settling time vs. phase error variance characteristics of first-order loop.

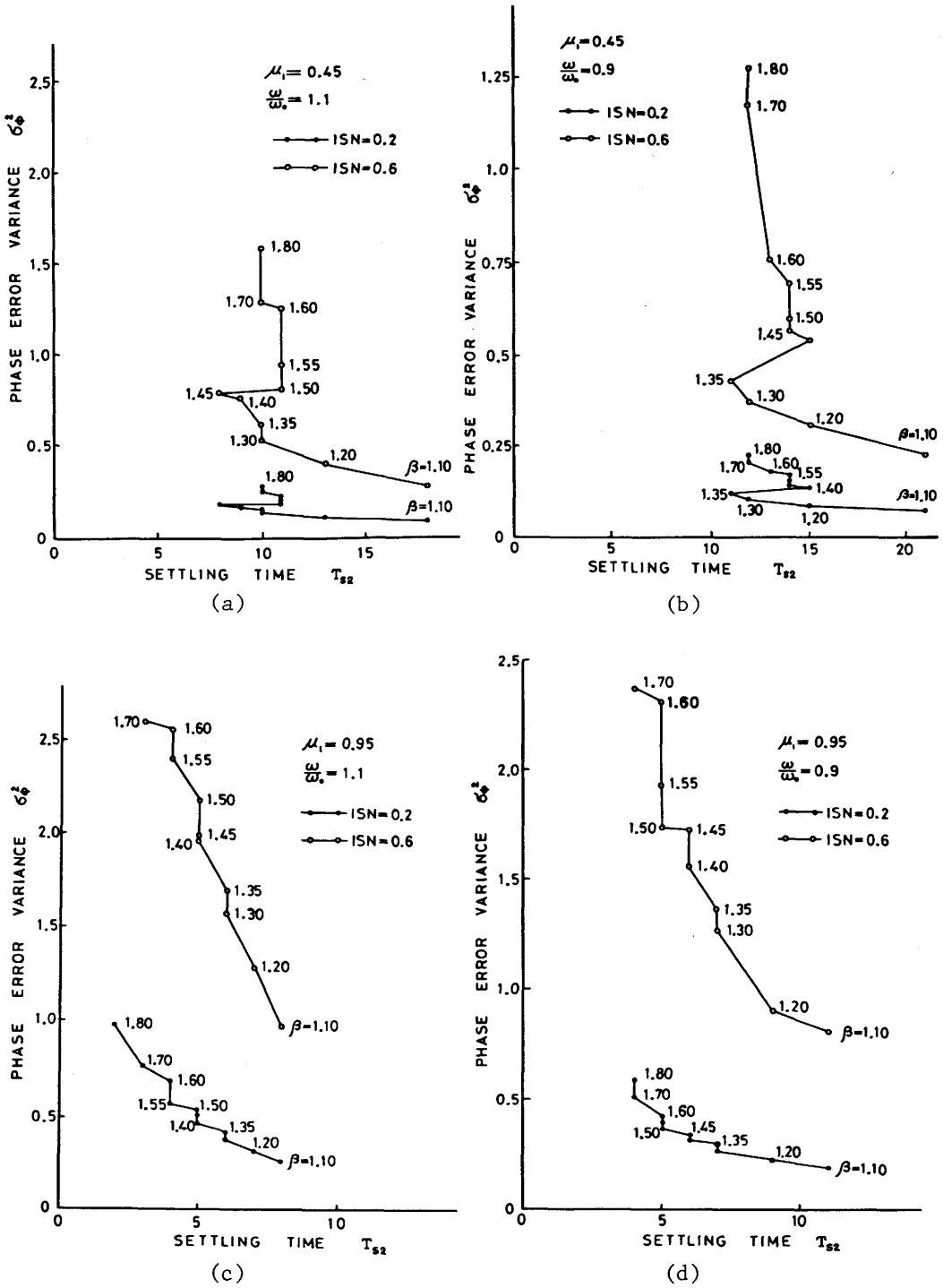


Fig. 6 Settling time vs. phase error variance characteristics of second-order loop.

IV. CONCLUSIONS

We have established relationships between the settling time of step response and the steady-state phase error variance for both of the first and second-order loops. With this, it is a simple matter to find proper filter parameters for a satisfactory or nearly optimum loop performance with a short settling time and a small steady-state phase error variance which imply a short acquisition time and a high accuracy respectively.

Here we have considered only the first and second-order loops, but certainly the analysis can be extended to higher order loops. A similar analysis of the third-order loop will be a problem for study in the future.

REFERENCES

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