

Multiple-Hop Routing in Ultrafast All-Optical Packet Switching Network Using Multiple PPM Routing Tables

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Abstract—In this paper we present the modeling and simulation of multiple-hop routing in ultrafast all-optical packet switching based routers employing multiple pulse position modulation (PPM) formatted routing table. In multiple PPM routing tables (PPRTs) with reduced entry length, only a subset of the header address is converted into a PPM format in order to reduce the packet header recognition time. Packet header address correlation is carried out using only a single optical AND gate to improve the processing time. We show that the proposed scheme offers unicast/multi-cast/broadcast transmitting capabilities. The simulation results for the optical signal-to-noise ratio (OSNR) at each hop are presented and compared with the theoretical calculations.

Index Terms— Packet switching, pulse position modulation, address correlation, optical switch, OSNR.

I. INTRODUCTION

Rapidly growing internet traffic volume necessitates the need for ultra-wideband networks. Photonic networks with all-optical packet routing are one such a network where packet header processing is entirely carried out in the optical domain [1, 2]. By replacing the slow optical/electrical/optical (O/E/O) conversion modules with optical processors a higher data throughput and lower power consumption can be achieved. Recently, the development of ultra high-speed Boolean logic gates [3-5] (such as AND, OR and XOR) with operating data rates higher than 40 Gbit/s have become the key enabling technology for realizing all-optical packet routing. At present packet header processing is carried out by sequentially correlating the incoming packet header address with each entry of a local routing table. For a small size network this is viable provided the routing table size is not too large. However, for a large size network with a routing table with hundreds or thousands of entries, the cost and complexity become a real issue. In addition a larger size routing table will lead to a conspicuous increase in packet header processing time at each router. In [6] it has been shown that packet header processing time (i.e. correlation time) can be considerably reduced by adopting PPM signal format for both the header address bits and the routing table entries. In this scheme the routing table entries contain multiple header address, thus considerably reducing its size.

In this paper we propose and investigate multiple PPM

based routing table with reduced entry length, where only a subset of the header address is converted into a PPM format. To avoid the low response-time of all-optical logic gates as in [6], a single bitwise AND gate is used to carry out header address correlation. The proposed scheme also offers multiple transmitting modes (unicast, multi-cast and broadcast) capability in an optical layer. In addition, we also investigate the multiple-hop routing in terms of the OSNR performance. The paper is organized as follows: after introduction, the principle of the multiple PPRTs, the $1 \times M$ node architecture and the analysis of multiple-hop OSNR are outlined in Section 2. In Section 3 simulation results and discussions are presented. Finally, Section 4 will conclude the paper.

II. ALL-OPTICAL ROUTER WITH MULTIPLE PULSE POSITION ROUTING TABLES

A. Optical Core Network

An all-optical network is composed of K edge nodes and L core nodes, see Fig. 1 with $K = 32$. Each edge node has its own specific address. Incoming low-speed electrical packets at a source edge node with the same destination (i.e. same target edge node) are combined and converted into a high speed optical packet. Optical packets are then routed to their destination via the core-network. When a packet arrives at proposed router (i.e. a core node), its header address is processed and correlated with all entries of the local multiple PPRTs in order to switch the packet to the correct output port. Depending on the network configuration and the local

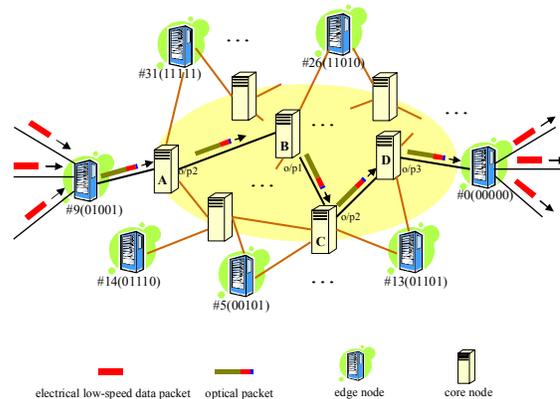


Fig. 1. An optical core network with 32 edge nodes.

multiple PPRTs, the packet may propagate through a number of core routers before reaching its targeted edge node. In Figure 1, an illustration of a four-hop routing path is presented.

B. Multiple Pulse Position Routing Tables

Assuming that the packet header has N bits address $[a_{N-1} a_{N-2} \dots a_2 a_1 a_0]$, where a_{N-1} is the most significant bit (MSB), the conventional routing table (RT) will have a maximum of 2^N entries. In the worst case scenario i.e. checking all entries, the router will perform 2^N N -bitwise correlations. Table I illustrates a routing table for $N = 5$, where 32 possible addresses are grouped into M groups based on the intended output ports. Here $M = 3$ representing the number of output ports. If a packet address match a pattern in a group, then it is switched to relevant output port, see the 1st and 2nd columns. The 3rd column shows the PPRT entries E_i ($i = 1, 2, 3..$) of length $2^N \times T_s$ for each group of address bits, where T_s is the slot duration. The locations of the short pulses correspond to the decimal values of address patterns in i^{th} group. Note that the number of entries is reduced to 3 from 32 for the conventional RT. Further downsizing of PPRT could be accomplished by splitting each PPRT entry into sub-groups of E_{ij} ($i = 1, 2, 3..$, and $j = A, B, C..$) with a reduced length of $2^{N-X} \times T_s$. $N-X$ is the number of bits in the subset of packet header address, see the 4th column in Table I, and A, B, C and D represent address

TABLE I
THE CONVERSION OF CONVENTIONAL RT TO SINGLE PPRT AND MULTIPLE PPRTs

Address patterns ($N=5$)	Output port	PPRT entries with 32 slots ($N=5$)	4 Multiple PPRT entries with 8 slots ($N=5, X=2$)
00000 00001 00011 00101 01001 01101 10000 10011 10101 11000 11100 11110	1	Decimal values 0 1 3 5 9 13 16 19 21 24 28 30 PPM pulses E_1	E_{1D} (0 1 3 5), E_{1C} (9 13), E_{1B} (16 19 21), E_{1A} (24 28 30)
00000 00001 00010 00110 01010 01100 10111 10010 10111 11010 11101	2	Decimal values 0 1 2 6 10 12 15 18 23 26 29 PPM pulses E_2	E_{2D} (0 1 2), E_{2C} (6 10 12 15), E_{2B} (18 23), E_{2A} (26 29)
00000 00100 00111 01000 01011 01110 10001 10100 10110 11001 11011 11111	3	Decimal values 0 4 7 8 11 14 17 20 22 25 27 31 PPM pulses E_3	E_{3D} (0 4 7 8), E_{3C} (11 14), E_{3B} (17 20 22), E_{3A} (25 27 31)

← Conventional RT ← Single PPRT ← Multiple PPRTs

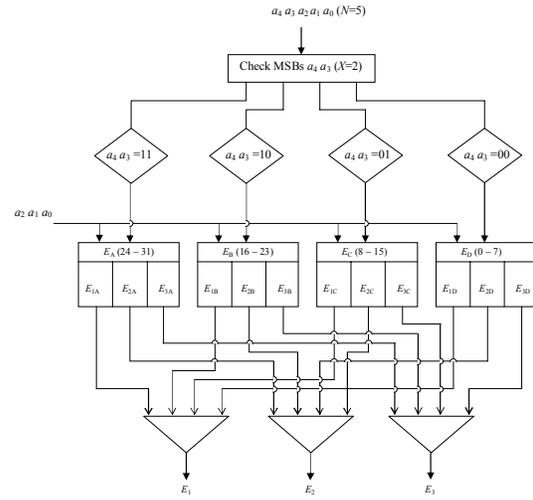


Fig. 2. A block diagram of multiple PPRT ($E_{1A}, E_{2A}, E_{3A}, \dots, E_{3D}$) for 5-bit packet header address.

patterns with decimal metrics in ranges of (24-31), (16-23), (8-15) and (0-7), respectively. E.g., for $N = 5$ the PPRT entry length is reduced from $32 \times T_s$ to $8 \times T_s$ when $X = 2$. The process is best explained with reference to Figure 2 ($N = 5, X = 2$). The two MSBs a_4 and a_3 of 5-bit header address are first checked to identify PPRT entry. Based on a_4 and a_3 pattern, E_{ij} is generated from the remaining $a_2 a_1 a_0$ bits, which are then combined to generate E_1, E_2 and E_3 . E_{ij} s are then applied to the AND gates to carry out header address correlation [7].

C. Node Architecture

The router based on the multiple PPRT with M -output ports

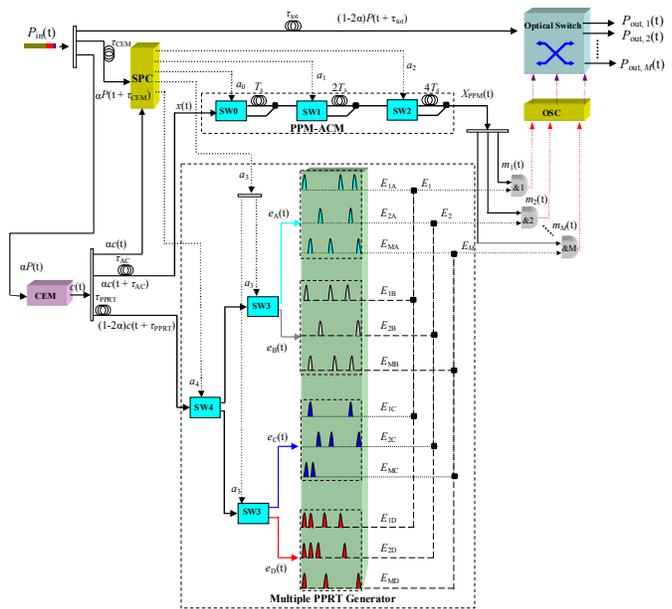


Fig. 3. A node structure with multiple PPRTs for 5-bits packet header address ($N=5, X=2$).

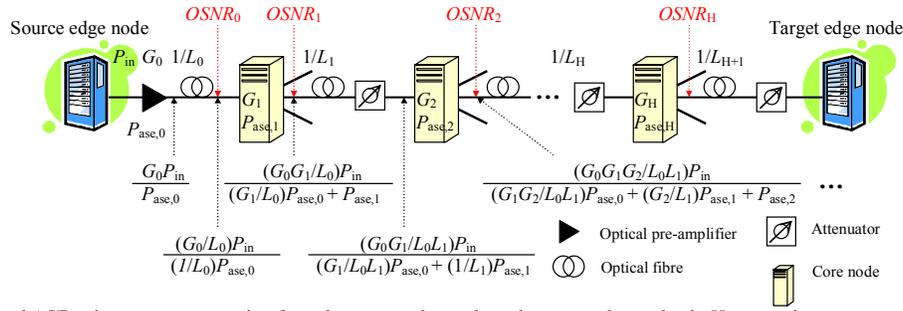


Fig. 4. Signal and ASE noise power propagation from the source edge node to the target edge node via H core nodes.

is composed of a number of main modules based on symmetric Mach-Zehnder (SMZ) including a clock extraction module (CEM), a PPM address conversion module (PPM-ACM), a serial-to-parallel converter (SPC), a multiple PPRT generator, AND gates, all-optical switches (OS), an OS control module (OSC), and a number of 1×2 high extinction ratio optical switches (SW) [6], see Figure 3. The incoming packet $P(t)$ is split and applied to the CEM, SPC and OS with the delays of 0, τ_{CEM} (required time for clock extraction) and τ_{tot} (total required time for PPM header processing), respectively. The extracted clock pulse $c(t)$ with delays of 0, τ_{AC} and τ_{PPRT} is applied to the SPC [6-7], PPM-ACM and SW4, respectively. N -bit packet header addresses are extracted at the output of SPC. The PPM-ACM with the output defined by:

$$x_{\text{PPM}}(t) = x\left(t + \sum_{i=0}^{N-3} a_i \times 2^i \times T_s\right), \quad a_i \in \{0, 1\} \quad (1)$$

where $x(t) = \alpha c(t + \tau_{\text{AC}})$ and α is the splitting factor. SW4 is used to check a_4 . for “1” or “0”. If a_4 is “1” then the first two groups E_A and E_B of multiple PPRTs are selected. Further selection of E_A and E_B is made using SW3. If a_3 is “1” or “0” then E_A or E_B is selected, respectively. PPRTs with the same i^{th} index are combined together and applied to the optical AND gates for address correlation. For example a header address of “11100” converted into a PPM format shows a pulse located at the 4th position (i.e. decimal value of “100”) within an 8-slot PPM frame. The two MSBs (“11”) are used to select one of the multiple PPRTs for correlation. Note that, only one multiple PPRT is used for correlation with an incoming packet header address. The outputs of the multiple PPRTs, see Figures 2 and 3, are given as [7]:

$$E_k(t) = E_{kA}(t) + E_{kB}(t) + E_{kC}(t) + E_{kD}(t) \quad (2)$$

Where each d_k element corresponds to the decimal values of header address bits (first $(N-2)$ -bit) assigned to the node output k^{th} ($k = 1, 2, \dots, M$).

The optical AND gates are based on the SMZ switches [8] with the logical outputs given by:

$$m_k(t) = x_{\text{PPM}}(t) \times E_k(t) = \begin{cases} 1 & \text{if } d_k = \sum_{i=0}^{N-1} a_i \times 2^i \quad \forall k \\ 0 & \text{if } d_k \neq \sum_{i=0}^{N-1} a_i \times 2^i \quad \forall k \end{cases},$$

$$k = 1, 2, \dots, M \quad d_k \in \{0 \sim (2^N - 1)\} \quad (3)$$

The matching pulse $m_k(t)$ is subsequently applied to the OSC module to ensure that incoming packets $P_{\text{in}}(t)$ are switched to the correct output ports. The signal at the output of switch is given as:

$$P_{\text{out},k}(t) = P_{\text{in}}(t) \times m_k(t) = \begin{cases} G_{\text{OS}} \times (1 - 2\alpha) \times P_{\text{in}}(t + \tau_{\text{tot}}) & \text{if } m_k(t) = 1 \\ 0 & \text{if } m_k(t) = 0 \end{cases}$$

$$k = 1, 2, \dots, M \quad (4)$$

where G_{OS} is the optical switch gain.

If more than one pulse is located at the same position in more than one (or all) PPRT entries, then the packet is broadcasted to multiple outputs (i.e. multicast) or all outputs (i.e. broadcast), respectively.

D. Multiple-hop OSNR

Figure 4 illustrate the path across the optical core network for packets with the average power P_{in} from source to the destination. The packet signal is first amplified and passed through a fiber span before being applied to a node.

The SOA unpolarized amplified spontaneous emission (ASE) noise is generally computed by [9]:

$$P_{\text{ase},i} = 2n_{\text{sp},i}hf_0(G_{\text{OS},i} - 1)B_0, \quad i = 0, 1, \dots, H \quad (5)$$

where $n_{\text{sp},i}$ and G_i are the spontaneous-emission factor and the gain, respectively, of the amplifier, where $i = 0$ represents the pre-amplifier and $i > 0$ denotes the SOA in OS modules. hf_0 and B_0 are the product of the Planck constant and the operating optical frequency, and the optical bandwidth of the system (i.e. filter optical bandwidth), respectively and H is the number of core nodes.

The OSNR at the target node is given as [6]:

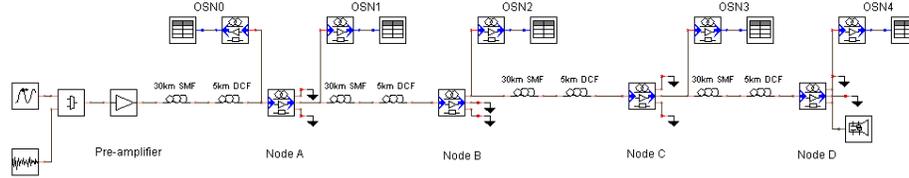


Fig. 5. The VPI simulation setups for four-hop routing.

$$OSNR_H = \frac{\left(G_H \prod_{h=0}^{H-1} (G_h / L_h) \right) P_{in}}{\sum_{h=0}^{H-1} \left(P_{ase,h} \prod_{k=h+1}^H (G_k / L_{k-1}) \right) + P_{ase,H}} \quad (6)$$

where L_h is the total loss incurred between any two core nodes.

III. RESULTS AND DISCUSSIONS

A. Simulation Setup

The proposed router is simulated and its system performance is investigated by using the Virtual Photonics simulation package (VPITM). Table II shows the main

simulation parameters and Figure 5 depicts the simulation setup diagrams for multi-hop routing and an individual router. Six optical packets with addresses of #0, #1, #4, #12, #20 and #28 (decimal values) are transmitted sequentially at 80 Gb/s with 1 ns inter-packet guard interval. Each packet is composed of a 1-bit clock, a 5-bit address, and a 53-byte payload (ATM cell size) [10]. The input packet, with an average power of 3.5 mW, is amplified to compensate for the link loss (fibre attenuation and coupling losses). Each fibre span (link) comprises of 30 km single-mode fibre (SMF) and 5 km dispersion-compensating fibre (DCF). Note that PPRT for of the node A is given in Table I. Similarly, for nodes B, C, and D, the PPRT entries are $E_1 \in \{0, 1, 2, 6, 10, 12, 15, 18, 23, 26, 29\}$, $E_2 \in \{0, 1, 3, 5, 9, 13, 16, 19, 21, 24, 28, 30\}$, and $E_3 \in \{0, 4, 7, 8, 11, 14, 17, 20, 22, 25, 27, 31\}$, respectively.

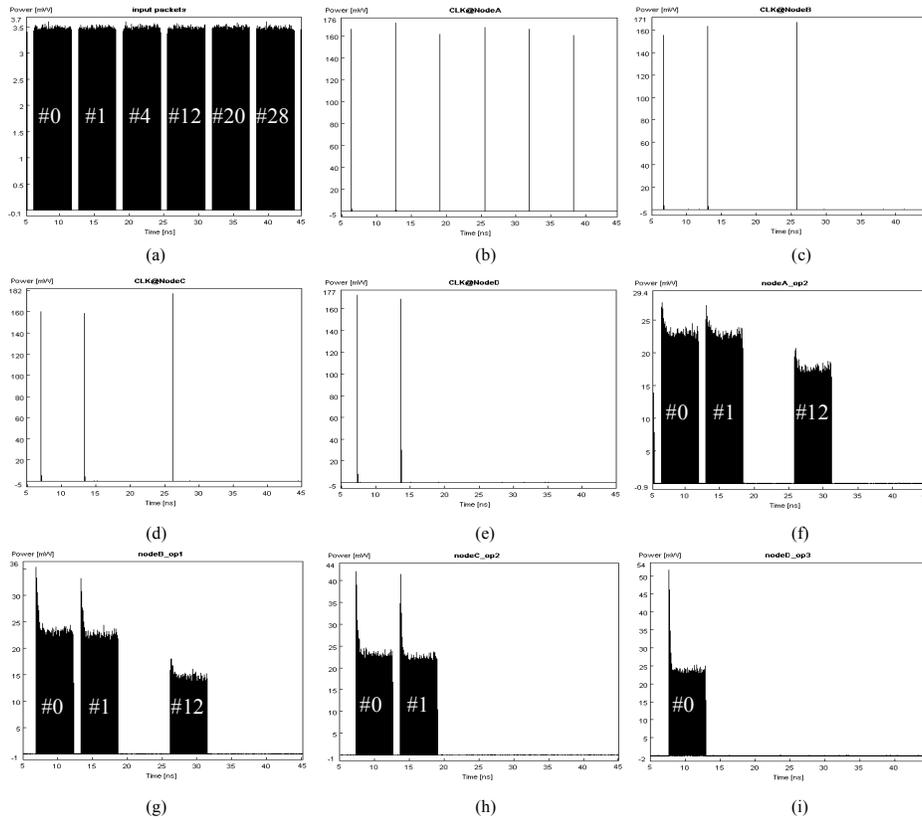


Fig. 6. Time waveforms; (a) input packet at node A, (b)-(e) extracted clock at nodes A, B, C, and D, and (f)-(i) switched packets at nodes A – output2, B – output1, C – output2, and D – output3.

TABLE II
SIMULATION PARAMETERS

Parameter and description	Value
Data packet bit rate – $1/T_b$	80 Gb/s
Packet payload length	53 bytes (424 bits)
Wavelength of data packet	1554 nm
Data & control pulse widths – FWHM	2 ps
PPM slot duration $T_s (=T_b)$	12.5 ps
Average transmitted power P_m	3.5 mW
Average power of $C_s(t)$	165 mW
Optical bandwidth B_o	300 GHz
$G_h (h = 1, 2, \dots, H)$	20 dB
Total loss of a hop $1/L_h (h = 1, 2, \dots, H)$	-7 dB
Pre-amplifier gain G_0	7 dB
First span loss $1/L_0$	-7 dB
Pre-amplifier n_p	2
SOA length	500 μm
SOA n_{sp}	2
Inject current to SOA	150 mA
Splitting factor α	0.4

B. Results and Discussions

The time waveforms of six input packets and their switched versions at the outputs of four nodes (A, B, C and D) are illustrated in Figure 6. Figure 6(a) shows the input packets, whereas the extracted clock pulses observed at nodes A, B, C and D are presented in Figures 6(b)-(e), respectively, showing small intensity variations. At each hop, depending on the node's PPRT, the input packets are switched to their corresponding output ports. Packets with the target address of #0 are subsequently switched to the output ports of 2, 1, 2 and 3 of nodes A, B, C and D, respectively, as shown in Figures. 6(f), (g), (h) and (i). The intensity overshoot observed at the start of switched packets is due to the gain saturation of the SOA within the OS when injected with a number of input packets, where the proceeding bits will experience a lower amplification gain. This can be minimized by decreasing the power of the input packet. Figure 7 depicts the theoretical and simulation for the OSNR against the number of hops. The disparity between the results is mainly due to the accumulated noise associated with matching pulses $m_k(t)$ as in our simulation model. In the theoretical model, the accumulated noise due to the CEM and PPRT has not been considered. It is shown that ~ 2 dB drop on the OSNR, after each hop is due to the accumulated ASE noise.

IV. CONCLUSION

In this paper, the node architecture, operation principle and the OSNR performance analysis of the proposed router with multiple pulse position routing tables were presented. In multiple PPRTs, the number and the length of entries are significantly shorter than the traditional RTs and PPM based RTs, respectively. As a result, the proposed router offers a faster processing time especially for packets with long address bits. The paper also presented simulation results to

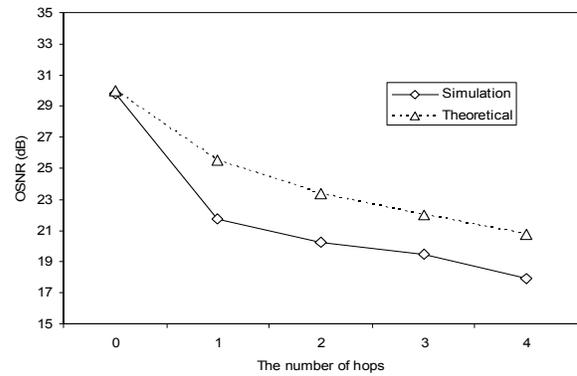


Fig. 7. OSNR vs. the number of hops.

demonstrate the routing operation. It was shown that the OSNR decreases by ~ 2 dB after each hop. The proposed router also is capable of operating in the unicast, multicast and broadcast transmission modes.

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