

# Ultra-fast All-optical Packet-switched Routing with a Hybrid Header Address Correlation Scheme

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**Abstract**—The paper presents a new node architecture for an all-optical packet router employing multiple pulse position modulation (PPM) routing table with a hybrid packet header correlation scheme. Most existing routing tables within a node contain a large number of entries, thus resulting in a long packet header address correlation time before delivering the incoming packet to its destination. In the proposed multiple PPM routing tables (PPRTs) the packet header address is based on the binary and PPM formats which leads to a much reduced routing table size. The packet header address correlation is carried out using only a single optical AND gate, thus offering reduced system complexity. It is also shown that the proposed scheme offers unicast/multi-cast/broadcast transmitting capabilities. The propose scheme is simulated and its characteristics are investigated. The output inter-channel crosstalk (CXT) of up to -18 dB and output packet power fluctuation of 2 dB have been achieved, which largely depend on the guard time between the arriving packets.

**Index Terms**— Packet switching, pulse position modulation, address modulation, address correlation, optical switch.

## I. INTRODUCTION

In high-speed all-optical packet routing it is advantageous to replace packet header processing based on the slow optical/electrical/optical (O/E/O) conversion modules with an entirely optical scheme to achieve a higher data throughput and lower power consumption [1, 2]. In recent years we have seen the development of Boolean logic gates [3-5] (such as AND, OR and XOR) with the operating data rates higher than 40 Gbit/s have become the key enabling technology for realizing all-optical processing, data storing (flip-flop) and

packet routing. Common packet header processing is carried out by sequentially correlating the incoming packet header address with each entry of a local routing table. For a small size network this is viable provided the routing table size is small. However, for a large size network with a routing table with hundreds or thousands of entries, the cost, complexity and packet header processing become a real issue. In [6] it has been shown that packet header processing time (i.e. correlation time) can be significantly reduced by adopting a multiple PPM routing table where only a subset of the header address is converted into a PPM format. To generate a PPM format in each node will require a serial to parallel converter (SPC), an array of 1×2 optical switches, and fibre delay lines. However, to convert a long header address, a large number of optical switches and delay lines are required, thus resulting in deterioration of the extinction in the PPM-converted address [7].

In this paper, we propose a simple hybrid header address correlation scheme with no PPM address conversion module, offering a number of advantageous including (i) significantly reduced routing table entries, (ii) considerably reduced correlation processing time by using merely a single bitwise AND gate instead of a large number of gates with a low response-time, and (iii) unicast, multi-cast and broadcast transmission modes embedded in the optical layer. The proposed scheme offers reduced complexity compared with a previous correlation scheme due to exclusion of the PPM address conversion module [6]. The paper is organized as follows: after the introduction, the format of the hybrid header address and the principle of the multiple PPRTs are illustrated in Section 2. The proposed node architecture is outlined in Section 3. In Section 4 simulation results and discussions are presented. Finally, Section 5 will conclude the paper.

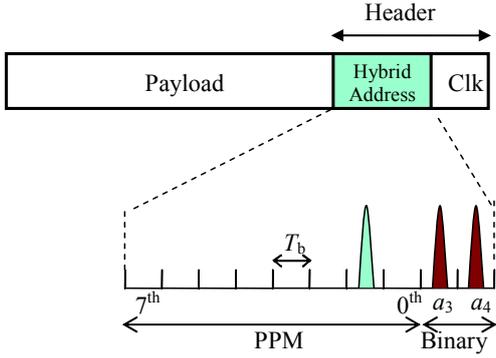


Fig. 1. An optical packet with a hybrid header address format equivalent to  $N$ -bit conventional address pattern ( $N=5$ ),  $T_b$  is the bit duration.

## II. HYBRID HEADER ADDRESS CORRELATION

### A. Hybrid Address

A typical packet is composed of a header (clock and address) and a payload. The clock signal, normally the first bit within the packet header, is used for synchronization within the router. In contrast to the conventional header address

format, which is binary, here we have adopted a hybrid binary and PPM formats. Here a packet composed of 3-element is defined by a set  $S = \{S_C, S_A, S_P\}$ , where the elements representing the clock, address, and payload, respectively is given as:

$$S_C = 1,$$

$S_A = \{S_{A1}, S_{A2}\}$ , where  $S_{A1}$  and  $S_{A2}$  represent the most significant bits and a PPM format given as:

$$S_{A1} = \{a_{N-1}, a_{N-2}, \dots, a_{N-X}\}, \forall S_{A1} \in \{0, 1\}$$

$$S_{A2} = \{b_0, b_1, \dots, b_d, \dots, b_{(2^{N-X}-1)}\}, \exists b_d = 1 \text{ representing a PPM pulse and the rest of elements are equal to "0"},$$

where the decimal value of the binary address bits is  $d = \sum_{i=0}^{N-X-1} a_i \times 2^i$ ,

$N$  and  $X$  represent the conventional header length and its two MSBs, respectively

$S_P = \{p_0, p_1, p_2, \dots, p_{l-1}\}, \forall S_P \in \{0, 1\}$ , where  $l$  is the payload bit resolution.

For example, an  $N$ -bit binary address  $\{a_4 a_3 a_2 a_1 a_0\}$  of  $\{11001\}$  in the hybrid format is "110100000", where the first two bits correspond to  $X$  and the remaining bits represent a PPM frame of length  $2^{N-X}$  with a pulse located in position 2 corresponding to the decimal value of  $\{a_2 a_1 a_0\}$ , see Figure 1.

TABLE I

THE CONVERSION OF CONVENTIONAL RT TO SINGLE PPRT

| Address patterns ( $N=5$ )   | Output port | PPRT entries with 32 slots ( $N=5$ )                                    |
|--|-------------|---|
| 00000<br>00001<br>00011<br>00101<br>01001<br>01101<br>10000<br>10011<br>10101<br>11000<br>11100<br>11110 | 1           | Decimal values: 0 1 3 5 9 13 16 19 21 24 28 30<br>PPM pulses:<br>$E_1$  |
| 00000<br>00001<br>00010<br>00110<br>01010<br>01100<br>01111<br>10010<br>10111<br>11010<br>11101          | 2           | Decimal values: 0 1 2 6 10 12 15 18 23 26 29<br>PPM pulses:<br>$E_2$    |
| 00000<br>00100<br>00111<br>01000<br>01011<br>01110<br>10001<br>10100<br>10110<br>11001<br>11011<br>11111 | 3           | Decimal values: 0 4 7 8 11 14 17 20 22 25 27 31<br>PPM pulses:<br>$E_3$ |

TABLE II

THE CONVERSION OF CONVENTIONAL RT TO MULTIPLE PPRTS

| Address patterns ( $N=5$ )  | PPRT entry | 4 Multiple PPRT entries with 8 slots ( $N=5, X=2$ )                        |
|---|------------|--|
| $E_{1D}$ { 00000<br>00001<br>00011<br>00101<br>01001<br>01101<br>10000<br>10011<br>10101<br>11000<br>11100<br>11110 } | $E_1$      | 0 1 3 5 9 13 16 19 21 24 28 30<br><br>$E_{1D}$ $E_{1C}$ $E_{1B}$ $E_{1A}$  |
| $E_{2D}$ { 00000<br>00001<br>00010<br>00110<br>01010<br>01100<br>01111<br>10010<br>10111<br>11010<br>11101 }          | $E_2$      | 0 1 2 6 10 12 15 18 23 26 29<br><br>$E_{2D}$ $E_{2C}$ $E_{2B}$ $E_{2A}$    |
| $E_{3D}$ { 00000<br>00100<br>00111<br>01000<br>01011<br>01110<br>10001<br>10100<br>10110<br>11001<br>11011<br>11111 } | $E_3$      | 0 4 7 8 11 14 17 20 22 25 27 31<br><br>$E_{3D}$ $E_{3C}$ $E_{3B}$ $E_{3A}$ |

### B. Multiple Pulse Position Routing Tables

For a packet with  $N$ -bit header address  $\{a_{N-1} a_{N-2} \dots a_2 a_1 a_0\}$ , where  $a_{N-1}$  is the most significant bit (MSB), the conventional routing table (RT) will have a maximum of  $2^N$  entries. In the worst case scenario i.e. checking all entries, the router will perform  $2^N$   $N$ -bitwise correlations. Table I illustrates a routing table for  $N = 5$  and its equivalent PPM versions. For each output of the node, there exists a single PPM entry with  $2^N$  slots. In this example, the standard PPM has three entries  $E_i$  ( $i = 1, 2, 3$ ) of length 32 slots with duration  $T_s$ . Here  $T_s$  is set to be equal to the bit duration  $T_b$  of 6.25 ps. The locations of the short pulses in each entry correspond to the decimal values of conventional binary address patterns in  $i^{\text{th}}$  group. In multiple PPMs, entry length could be reduced from  $32T_s$  to  $2^{N-X}T_s$  by splitting each PPM entry into sub-groups of  $E_{ij}$  ( $i = 1, 2, 3$ , and  $j = A, B, C, D$ ), see Table II.  $A, B, C$  and  $D$  represent address patterns with decimal metrics in ranges of (24-31), (16-23), (8-15) and (0-7), respectively. For  $X = 2$  and  $N = 5$  the PPM entry length is reduced from  $32T_s$  to  $8T_s$ .

### III. NODES ARCHITECTURE

The proposed router with a multiple PPM and  $M$ -output

ports is composed of a number of main modules including a clock extraction module (CEM), a header address extraction module (HEM), a multiple PPM generator, AND gates,  $1 \times M$  all-optical switch, an optical switch control module (OSC), and a number of  $1 \times 2$  high extinction ratio optical switches (SW) [7], see Figure 2. The received packet  $P_{in}(t)$  after splitting is applied to the CEM, HEM and optical switch modules, respectively. The extracted clock pulse  $c(t)$  having been delayed by  $2T_b$  and 0 is applied to the HEM and SW4, respectively, whereas the outputs of HEM are applied to the SWs 3&4 and the AND gates. The two MSB bits ( $a_4$  and  $a_3$ ) are checked by SWs 4&3 to select the first two groups  $E_A$  and  $E_B$ , and  $E_C$  or  $E_D$  of multiple PPMs, respectively for address correlation. PPMs with the same  $i^{\text{th}}$  index are combined together and applied to the optical AND gates for address correlation. Note that, only one multiple PPM is used for correlation with an incoming packet header address  $X_{PPM}(t)$ . The outputs of the multiple PPMs, see Figures 2, are given as [6]:

$$E_k(t) = E_{kA}(t) + E_{kB}(t) + E_{kC}(t) + E_{kD}(t). \quad (1)$$

Where each  $d_k$  element corresponds to the decimal values of the header address bits assigned to the node output  $k^{\text{th}}$  ( $k = 1, 2, \dots, M$ ).

The SMZ based optical AND gates [7] outputs are given by:

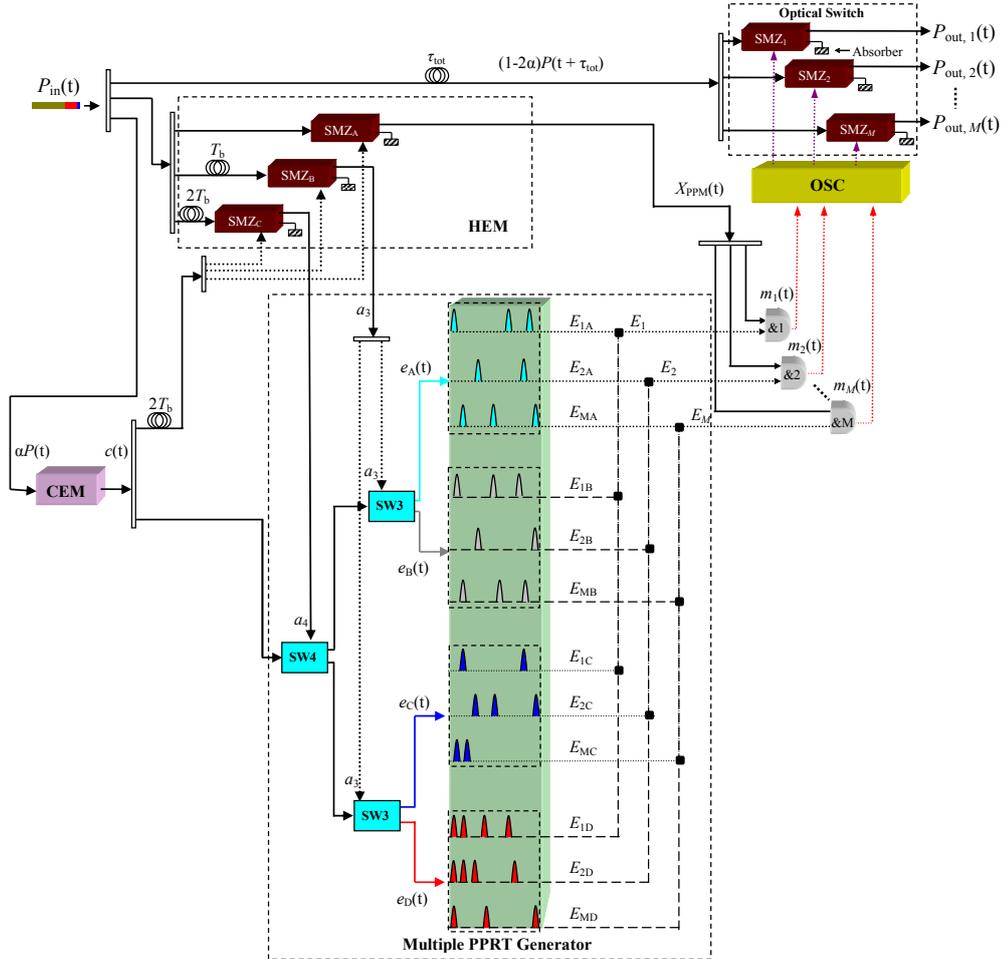


Fig. 2. The node architecture for packets with hybrid header address ( where  $N=5, X=2$ ).

$$m_k(t) = X_{PPM}(t) \times E_k(t) = \begin{cases} 1 & \text{if } d_k = \sum_{i=0}^{N-1} a_i \times 2^i \quad \forall k \\ 0 & \text{if } d_k \neq \sum_{i=0}^{N-1} a_i \times 2^i \quad \forall k \end{cases},$$

$$k = 1, 2, \dots, M \quad d_k \in \{0 \sim (2^N - 1)\}.$$

address correlation) are switched to the correct output ports. The switched packet is given as:

$$P_{out,k}(t) = P_{in}(t) \times m_k(t) = \begin{cases} G_{OS} \times (1 - 2\alpha) \times P_{in}(t + \tau_{tot}) & \text{if } m_k(t) = 1 \\ 0 & \text{if } m_k(t) = 0 \end{cases}$$

$$k = 1, 2, \dots, M \quad (3)$$

$m_k(t)$  are applied to the OSC module to ensure that incoming packets  $P_{in}(t)$  delayed by  $\tau_{tot}$  (total required time for header

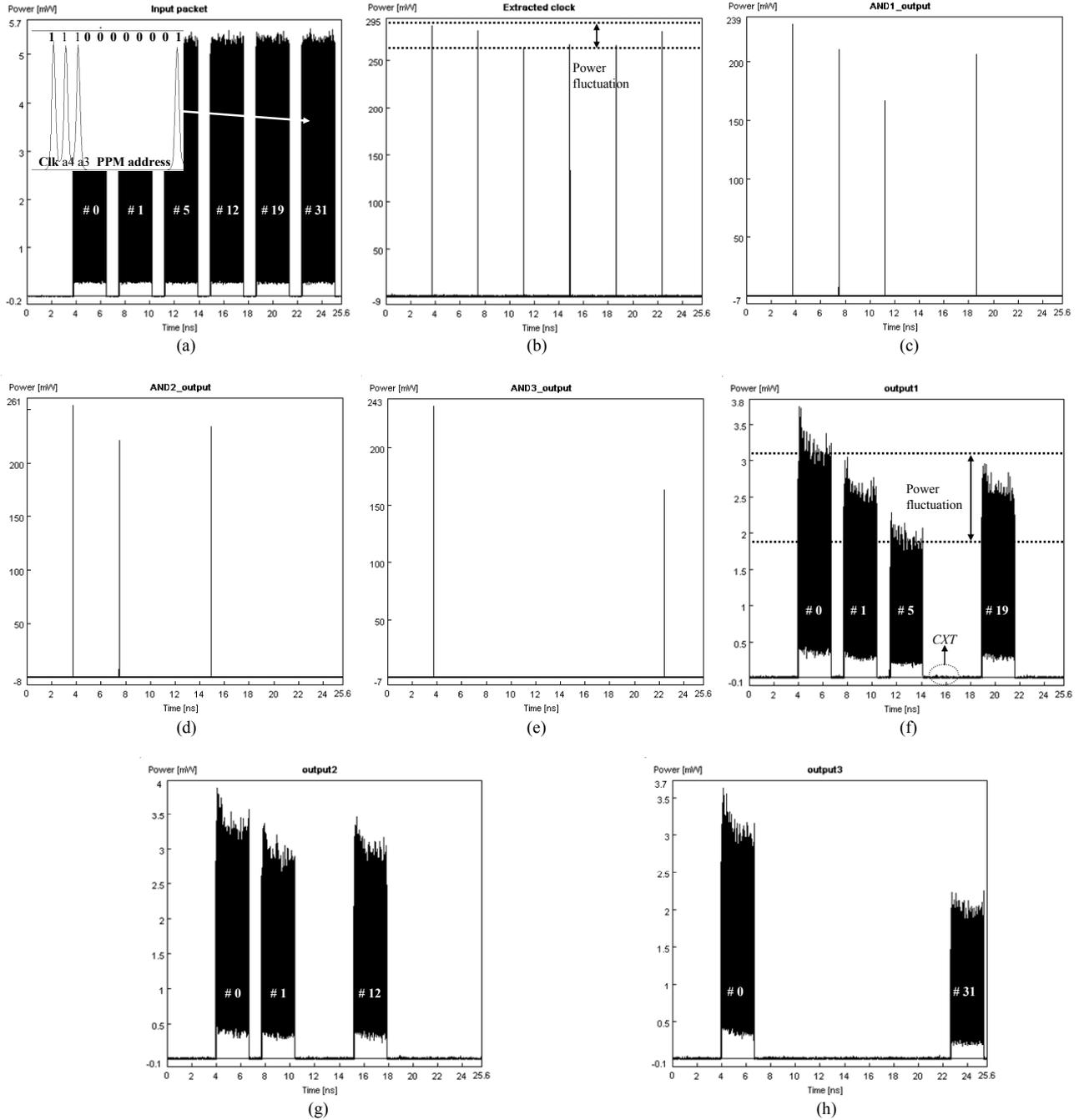


Fig. 3. Time waveforms of (a) input packets, (b) extracted clock signals, (c) matched signals at AND gate 1, (d) matched signals at AND gate 2, (e) matched signals at AND gate 3, (f) switched packets at router's output 1, (g) switched packets at router's output 2, and (h) switched packets at router's output 3.

TABLE III  
SIMULATION PARAMETERS

| Parameter and description          | Value  |
|------------------------------------|--|
| Data packet bit rate – $1/T_b$     | 160 Gb/s   |
| Packet payload length              | 53 bytes (424 bits)                                  |
| Wavelength of data packet)         | 1552.52 nm (193.1 THz)                               |
| Data pulse width – FWHM            | 2 ps   |
| PPM slot duration $T_s (=T_b)$     | 6.25 ps  |
| Average transmitted power $P_{in}$ | 5 mW   |
| Average power of $C_k(t)$          | 270 mW   |
| Optical bandwidth                  | 300 GHz  |
| Splitting factor $\alpha$          | 0.2  |
| Inject current to SOA              | 150 mA   |
| SOA length                         | 500 $\mu\text{m}$                                    |
| SOA width                          | $3 \times 10^{-6}$ m                                 |
| SOA height                         | $80 \times 10^{-9}$ m                                |
| SOA $n_{sp}$                       | 2  |
| Confinement factor                 | 0.15   |
| Enhancement factor                 | 5  |
| Differential gain                  | $2.78 \times 10^{-20}$ m <sup>2</sup>                |
| Internal loss                      | $40 \times 10^2$ m <sup>-1</sup>                     |
| Recombination constant A           | $1.43 \times 10^8$ s <sup>-1</sup>                   |
| Recombination constant B           | $1.0 \times 10^{-16}$ m <sup>3</sup> s <sup>-1</sup> |
| Recombination constant C           | $3.0 \times 10^{-41}$ m <sup>6</sup> s <sup>-1</sup> |
| Carrier density transparency       | $1.4 \times 10^{24}$ m <sup>-3</sup>                 |
| Initial carrier density            | $3 \times 10^{24}$ m <sup>-3</sup>                   |

where  $G_{OS}$  is the optical switch gain.

If more than one pulse is located at the same position in more than one (or all) PPRT entries, then the packet is broadcasted to multiple outputs (i.e. multicast) or all outputs (i.e. broadcast), respectively.

#### IV. RESULTS AND DISCUSSIONS

The router shown in Figure 2 is simulated using the Virtual Photonics simulation software (VPI<sup>TM</sup>). By taking advantage of the hybrid address, the new node architecture could be constructed with reduced complexity due to exclusion of the PPM address conversion module within the router. Table III shows all the main simulation parameters adopted [7]. Six optical packets with addresses of #0, #1, #5, #12, #19 and #31 (decimal values) are transmitted sequentially at 160 Gb/s with 1 ns inter-packet guard time. Each packet contains a 1-bit clock, a 10-bit hybrid address and a 53-byte payload (ATM cell size) [8]. Figure 3(a) shows the time waveforms of the six input packets with the inset illustrating the zoomed-in packet hybrid header with an address decimal metric of #31. The extracted clock pulses are presented in Figure 3(b). Figures 3(c), 3(d), and 3(e) illustrate the time waveforms observed at the outputs of AND gates 1, 2, and 3, respectively. Time waveforms of signals at the output ports 1, 2, and 3 of the router are depicted in Figures 3(f), 3(g), and 3(h), respectively, confirming that the incoming packets with header addresses of #0, #1, #5, #12, #19 and #31 are switched to outputs 1 & 2, 1, 2, 1, and 3, respectively, based on the

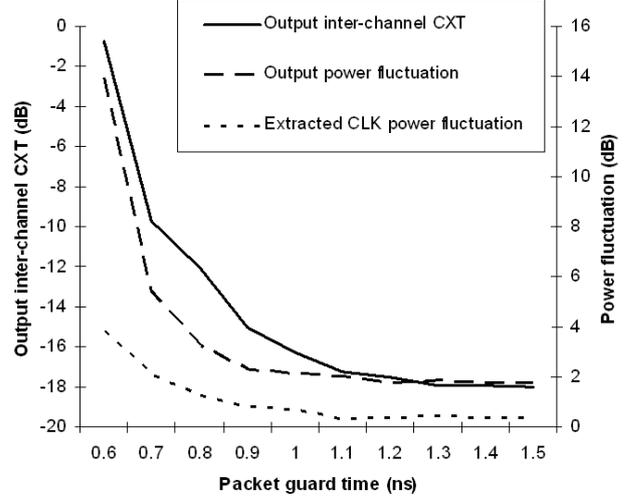


Fig. 4. Packet guard time against the output inter-channel  $CXT$  (left x-axis), output packet power fluctuation (right x-axis) and the extracted clock power fluctuation (right x-axis).

routing information given in Tables I and II. In addition, unicast, multicast and broadcast transmitting capabilities of the router are also demonstrated as packets with addresses of #5, #12, #19, and #31 are switched to one output port of the router, whereas the packets with #1 and #0 addresses are switched to two and all output ports of the router, respectively. Figure 4 investigates the output inter-channel  $CXT$  and power fluctuation against the different packet guard time observed at the output 1. The  $CXT$  is defined as:

$$CXT = 10 \log_{10} (P_{nt} / P_t) \quad (4)$$

where  $P_{nt}$  is the peak output signal power of the undesired packet and  $P_t$  is the average output signal power of the lowest target desired packet. The undesired  $CXT$  is due to the incomplete cut-off edge of the switching window profile induced by the slow gain recovery of the SOA [9].  $CXT$  is high for lower values of the packet guard time, improving significantly by increasing the guard time reaching  $\sim -18$  dB beyond the packet guard time of 1.2 ns. This improvement is due to the switching window being completely closed. However as the guard time increases beyond 1.2 ns, no further improvement is achieved. This is because the  $CXT$  is solely due to the extinction ratio of matched signal  $m(t)$ , see Figure 2.

The power fluctuation of the extracted clock signals and the output packets are defined by the differences between the highest and lowest intensity in decibel, see Figure 3(b) and 3(f), respectively. Figure 4 shows that the minimum power fluctuations of the clock signal and the output packets are 0.3 dB and 2 dB, respectively. The observed power fluctuation of the switched packets is mainly due to the unequal output power of the AND gates, see Figure 3(c)-(e). This is because power fluctuation of the extracted clock signals (see Figure 3(b)) increases after passing through two amplification stages (i.e. SW4 and SW3), thus resulting in an unequal input power at the input of the AND gates. Thus the need for a wider packet guard time of greater than 1ns).

## V. CONCLUSION

The paper has presented an all-optical packet-switched routing scheme with a hybrid header address correlation scheme. The  $1 \times M$  router architecture with the multiple PPRTs is also illustrated, the proposed routing scheme offers a reduced complexity and avoids the speed limitation imposed by the non-linear element based optical AND gates. Header processing and packet routing have been simulated and the results obtained show that this router can operate at 160 Gb/s with the output inter-channel crosstalk (CXT) of up to -18 dB and the margin of output packet power fluctuation is 2 dB largely dependent on the guard time between the packets.

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