Overview of Signal Integrity and EMC Design Technologies on PCB: Fundamentals and Latest Progress

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***Abstract*—This paper reviews the fundamentals and latest progress of modeling, analysis, and design technologies for signal integrity and electromagnetic compatibility on PCB and package in the past decades. Most results in this field are based on the very rich and highly educational literature produced by Prof. C. Paul in his long scientific career. The inclusion of parameters variability effects is also considered, and it is demonstrated how statistical simulations can become affordable by means of recently-introduced stochastic methods. Finally, the necessity of practical training of designers is mentioned, and an experience relying on realistic PCB demonstrators is illustrated.**

***Index Terms*—Circuit demonstrator, crosstalk, differential signaling, eye diagram, macromodeling, mode conversion, paramter variability, PCB, polynomial chaos, practical training, signal integrity, TDR, trace discontinuity.**

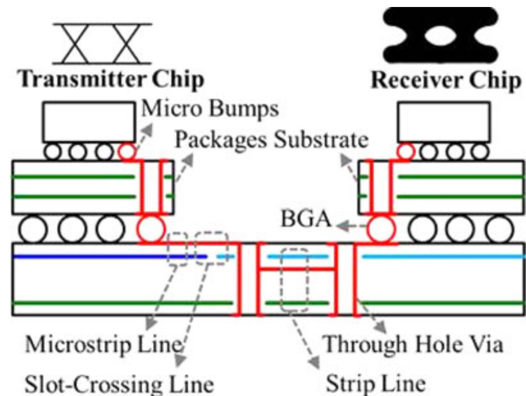

Fig. 1. An example of a link path which starts at a transmitter chip and ends at a receiver chip.

I. Introduction

ELECTROMAGNETIC compatibility (EMC) and signal integrity (SI) are one of the crucial technologies in the future for the electronic product design. The main reasons are high data bandwidth demand for next generation high performance computing (100+ Gbps), cloud communication/computing (50+ Gbps), and client devices (20+ Gbps). EMC and SI technologies on PCB or package will be one of the bottlenecks to achieve such high data bandwidth.

Paul made several pioneering contributions to the field of EMC and SI. He condensed the fundamental theory and required knowledge for EMC and SI design in two masterpiece books [1], [2]; then, in more recent times, he published a series of three books [3]–[5], especially for the design of high-speed digital systems. These references not only guided the direction of EMC and SI research on PCB in past decades and inspired several novel technologies, but are still presently unsurpassed and will impact the development of electronics and systems for many years to come.

In this paper, the fundamentals and latest progress of EMC and SI design technologies on PCB are overviewed. In addition, methods and tools for the simulation of a circuit, with the inclusion of parameters' variability effects on its electrical behavior, are needed to avoid very expensive refabrication. Finally, EMC engineering education is a fundamental step to achieve well-designed and performing devices. "Seeing is believing" particularly applies to the design for EMC, where most effects are felt as "black magic" and teaching using only texts and equations is insufficient. The IEEE EMC education manual [6] proved to be an indispensible tool for teaching practical skills and Paul was a great inspirator for the EMC community also in this respect.

This paper is organized as follows. The link path modeling, analysis, and design technologies are reviewed in Section II, differential signaling design and common-mode noise issues are presented in Section III, discontinuities due to nonideal return paths are treated in Section IV, assessment of parameters variations are discussed in Section V, and an educational experience for PCB design is reported in Section VI.

II. Link-Path Modeling and Analysis

A link path includes a whole electrical interconnect starting from a chip sending a signal and terminating at a chip receiving the signal. The signal integrity could be kept perfect if the link path could behave as a lossless transmission line. In reality, the link path usually consists of several conductive wires in different geometries. Fig. 1 shows an example of a link path. It starts

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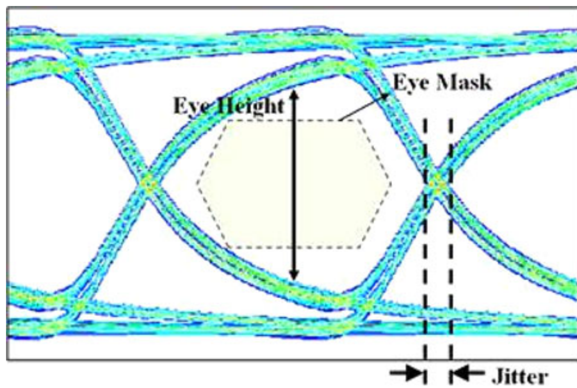

Fig. 2. An example of an eye diagram with the indication of eye height, jitter, and eye mask.

at a transmitter chip, passes through micro bumps, packages substrate, BGA balls, vias, microstrip lines or strip lines on PCB, and ends at a receiver chip. The signals will be distorted both in amplitude and timing due to the nonideal effects of the link path, such as frequency-dependent loss of package and PCB substrate, impedance variance, crosstalk coupling, etc.

An eye diagram is a common way for evaluating the quality of signals propagating on a link path. It is constructed by slicing a long stream of pseudorandom bit sequences (PRBS) and superimposing the different segments of symbols with one or two bits in length. Fig. 2 shows an example of a received eye diagram. Two metrics, eye height and timing jitter, are used to characterize quantitatively the voltage and timing errors, respectively, as shown in Fig. 2. In order to ensure the received signal can be recovered successfully, the jitter must be small enough to provide the receiver a sufficient sampling duration. Also, the eye height must be sufficiently large to ensure the voltage levels meet the threshold region. For some applications, an eye mask representing a forbidden region is defined as a signal quality specification, as shown in Fig. 2. The signal quality will not pass if the eye diagram overlay the mask.

Accurate modeling and characterization of the link path is important for eye diagram behavior prediction. The two books Paul edited at the end of his career [4], [5] provide an excellent summary of the significant developments. He contributed on the fundamental principles of circuit theory and electromagnetics needed to build physically consistent models. Intuitively, the link path can be described by multiport scattering-parameters (S-parameters) or impedance/admittance parameters in frequency domain, which can be obtained from either measurements or full-wave EM simulations [7]. It is sometimes very time-consuming to produce the S-parameters of the overall chip-package-PCB link path by full-wave simulation. Typically, the cascaded S-parameters are employed to take the overall link path into account [8]. However, for transient analysis in digital circuits, some signal processing techniques, such as inverse fast Fourier transform (IFFT) of the link-path S-parameters and a convolution algorithm, are required as an additional approach.

The concept of macromodeling for the partial or full link path has been thus developed to solve such mixed frequency/time domain problems [9]–[16]. The SPICE-compatible macromodels generally produce the same frequency response as the full-wave results in the frequency band of interest, but have no direct relations with the physical structure. The macromodel extraction techniques are based on the rational function approximation for the tabulated S-parameters, that can be implemented in various forms, from the basic vector-fitting [10] to more sophisticated algorithms like Z-domain-based orthonormal vector fitting [16]. However, several intrinsic properties of the original link path may not be preserved by the approximated macromodel, such as stability, causality, or passivity [17]. It has been shown that the overall signal integrity simulation will fail when these fundamental properties are lost because of measurement or simulation errors. Two suggestions are given to avoid the problem. First one is certifying any raw dataset to be self-consistent, causal, and passive before proceeding to further modeling steps. Second, any macromodeling algorithm also has to preserve the properties. On the other hand, it has been shown that passivity is the strongest requirement implying both causality and stability. Approaches for passivity enforcement techniques of macromodeling have also been proposed based on linear or quadratic optimization [18]–[20] or Hamiltonian matrix perturbation [21], [22]. Besides that, a systematic approach has also been proposed for systematically synthesizing the macromodel of interconnects according to the time-domain reflected waveform either measured by time-domain reflectometry (TDR) or simulated by the finite-difference-time-domain method [23]–[26].

As mentioned previously, the worst case eye diagram has to be produced by PRBS input with every possible bit sequence. It is typically time consuming. Another challenging topic for signal integrity modeling on link path regards efficient methodologies to predict the eye diagram properties, such as jitter and eye height [27]–[33]. One of the major reasons for the degradation of the eye diagram is due to the frequency-dependent loss leading to the data-dependent jitter, or so-called intersymbol interference (ISI) [34]. The effect can be caught by the peak distortion analysis [27]. Using the unit pulse or step response of the link path, we can predict the worst case eye height and deterministic jitter. Such approach can be extended for the matched lossy line [28], multireflected line [29]–[31], and lines with crosstalk [32].

Most of those methods are developed based on the linear system assumption for the link path ignoring the nonlinear effect of the driver circuits inside the chip. Latest studies proposed a fast method that could predict the eye diagram considering the interaction between the nonlinear I/O circuits and power distribution network (PDN) noise [33]. Based on the superposition of multiple bit pattern responses (SMBP) concept, an algorithm is developed to fast predict the eye diagram that theoretically captures any nonlinearity in the circuit. As shown in Fig. 3, a test circuit with PDN was constructed to examine the performance of this algorithm. The experiment results, as shown in Fig. 4, indicate a good agreement with the results simulated by long PRBS in HSPICE, for SMBP order higher than two [33].

Passive equalization is still an important topic in SI design of PCB, especially for Gbps signal transmission. Most of the passive equalization techniques are based on a high-pass filter design, such as T-junction [35]–[37], series RL [38], [39], parallel

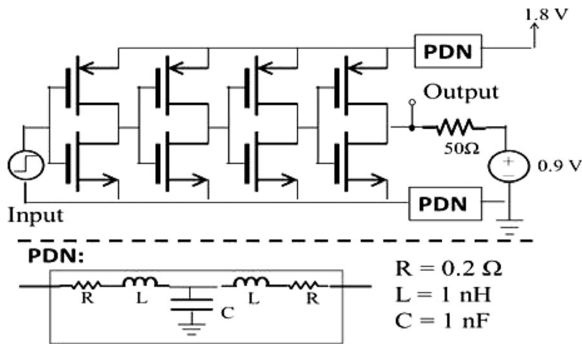

Fig. 3. A test circuit consists of four CMOS inverters as an output driver and two T-model RLC power distribution networks [33].

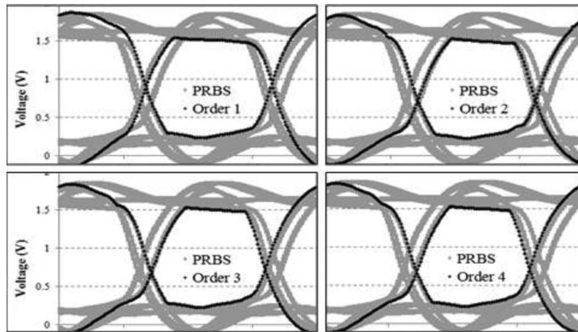

Fig. 4. Four Comparison of eye diagrams between 1000-bit PRBS result (gray line) and SMBP estimations of different orders (black lines). Top left: order 1. Top right: order 2. Bottom left: order 3. Bottom right: order 4 [33].

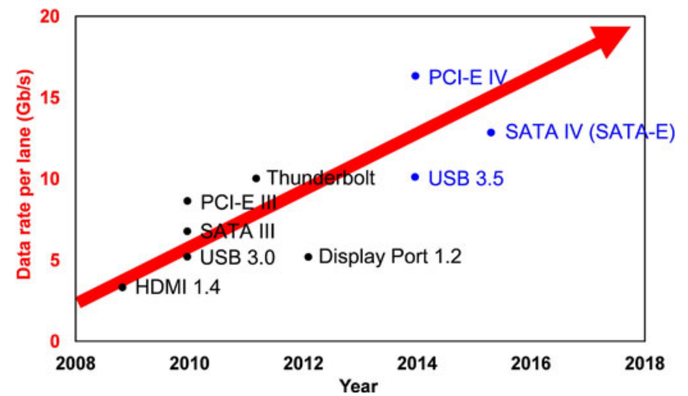

Fig. 5. Summary of latest high-speed I/O interfaces and their evolution. (Specifications with black words are the known information; those with blue words are the anticipation.)

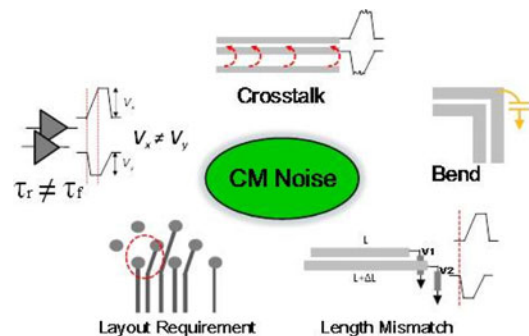

Fig. 6. Root-cause of common-mode noise from a variety of asymmetric geometries in real-world designs.

RC structures [38], implemented by the lumped RLC elements. Coupled traces [40] or defected ground concept [41], [42] on the PCB were recently proposed to replace the *L* element with a lower cost. Several algorithms to accurately find the *RLC* values were also discussed in [38], [43].

Crosstalk is another critical issue that could degrade the SI (or eye diagram) performance. Theoretical deviations and discussions for the crosstalk mechanism through the magnetic or electrical coupling have been well investigated [1], [2], [44]–[46]. Several researchers have discussed the methods to reduce the crosstalk, such as spiral layout scheme [47], serpentine microstrip line method [48], or using guard trace [49]–[51].

III. Differential Signaling

The differential signaling scheme has become required in high-speed digital systems due to its high immunity to noise and high tolerance to link path discontinuities [52], [53]. Fig. 5 shows the data rate trend for differential signals on PCB or cables, such as serial advanced technology attachment (SATA), peripheral component interconnect express (PCI-e), universal serial bus (USB), etc. The projection is far beyond 20 Gbps in the next decade. Typically, a differential (or balanced) line is composed of three conductors (two signal conductors and one ground conductor) that support two fundamental modes, differential (or odd) mode and common (or even) mode [2]. In differential signaling systems, the common-mode signal is usually regarded as the noise, which will degrade the signal integrity or cause EMI problems. Asymmetry in the differential link path is the main reason for exciting the common mode noise. The asymmetry includes the rising/falling time mismatch or amplitude difference in the I/O driver circuit, trace length mismatch between two signal conductors, unavoidable imbalance routing such as bending or via transition, etc. [54], as illustrated in Fig. 6.

With the trend of increasing data rates above several GHz, the discontinuity effect of the differential vias cannot be ignored. Numerical modeling or full-wave simulation based on PEEC [55]–[57], MoM [58], [59], cylindrical wave expansion method [60], etc., is one of the high accuracy ways to understand or predict the electrical behavior of the differential via, though it is time-consuming. Another way is developing equivalent circuit models, which can be linked directly with SPICE or other similar circuit simulators. The equivalent model can be constructed by space-mapping neural network [61], macromodels through time-domain [25], frequency-domain responses [62], [63], or physical models that are related to the via geometry [64]–[66]. In addition, the effective characteristic impedance of differential via transition can also be defined and designed with the help of an equivalent circuit model [67].

Another interesting research direction is on the design of the differential serpentine delay line, which is a common layout technique to equalize the timing delay among different pairs of differential signals. The common-mode noise usually is excited

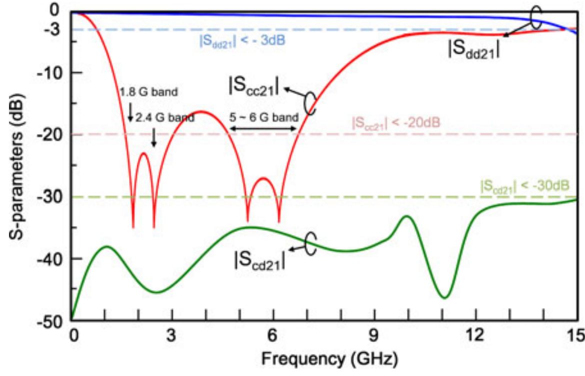

Fig. 7. Typical behavior of a common-mode filter in terms of S-parameters.

TABLE I
CHALLENGING CMF SPECIFICATIONS FOR NEXT GENERATION HIGH-SPEED INTERFACES

Parameters	***Specifications***
Differential mode, $\mid S_{dd21} \mid$	$<$ -3 dB below 15 GHz
Common mode, $\mid S_{cc21} \mid$	$<$ -20 dB for specific bands
Mode conversion, $\mid S_{cd21} \mid$	$<$ -30 dB below 15 GHz
Group delay of differential mode, τ_{dd}	Variation less than 10 %

in the serpentine delay lines due to a plurality of bends, which is one of the imbalance factors to cause the mode conversion. A flat spiral routing scheme was proposed to improve the signal integrity [68]. The common-mode noise could be mitigated by the compensation capacitance, or inductance on the bending corner [69], [70], tightly coupled and tapered lines at partial segment [71], [72]. The phase delay performance of the serpentine differential line can be improved by the shielded structure [73].

On the other hand, connectors and cables are always required for the high-speed interface or peripherals to deliver the signals between devices. Due to the inevitable asymmetry structure, common-mode current on the ground structure combining the PCB, connector, and cables will be excited and result in common-mode radiation [1], [74]–[78]. As the signaling raises up to several GHz, the spectrum of the radiation could cover the wireless communication bands, such 2.4 GHz and 5 GHz of WLAN and 1.5 GHz for GPS. This common-mode radiation, which is commonly called radio-frequency interference (RFI), will degrade signal-to-noise ratio (SNR) or the sensitivity of the transceivers [79]. Suppressing the common-mode noise before entering the connectors by using the common-mode choke (CMC) [80] or common-mode filter (CMF) [81]–[88] is one of the effective ways to solve such an RFI issue. Fig. 7 shows the typical behavior in terms of S-parameters for CMC or CMF. They include the insertion loss for differential mode ($|S_{dd21}|$), stopband for common-mode ($|S_{cc21}|$), mode conversion ($|S_{cd21}|$), and the group delay of differential mode (τ_{dd}). For next generation high-speed interfaces, the challenging specifications, as shown in Table I, are $|S_{dd21}| < -3$ dB from DC to 15 GHz, $|S_{cc21}| < -20$ dB for the specific bands, $|S_{cd21}| < -30$ dB, and τ_{dd} variation is less than 10%. Based on wire winding around ferrite material, CMC is a popular component for the common-mode noise suppression, but the challenge and cost significantly increases for such devices.

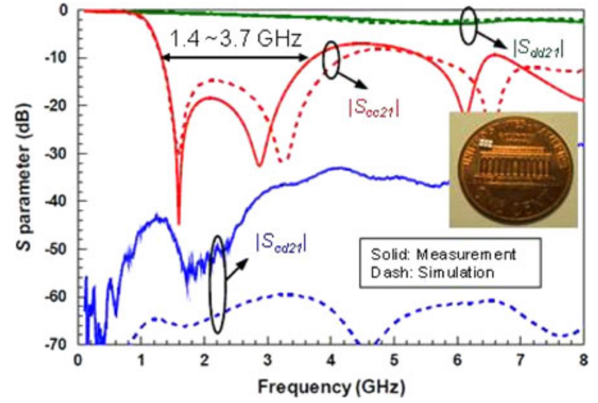

Fig. 8. Compact (much smaller than a 1-cent coin) common-mode filter design based on LTCC substrate, and its performance [88].

Recently, several works were devoted to CMF development based on defect ground structure [81], [82], split ring resonator [83], and metamaterials with negative permittivity [84]. Also, coplanar electromagnetic bandgap structure [85] was proposed to suppress the common-mode noise. These concepts have been demonstrated effective in common-mode noise mitigation without degrading the differential signal quality either on PCB level [86] or component level [87], [88]. Fig. 8 shows a compact-size CMF design based on LTCC substrate, and its S-parameter performance [88].

IV. DISCONTINUITIES

Discontinuities are always inevitable in a practical link path. They lead to discontinuous impedance, result in reflection loss, crosstalk coupling, high-order mode conversion, and dramatic radiated emission, and thus cause significant signal integrity issues. Besides the aforementioned macromodeling method in Section II, analytical or numerical modeling and design techniques for some specific structures have been proposed and will be introduced here. It is worth mentioning a scholar contribution of Paul on loop and partial inductance, summarized in his recent book [3].

One of the common discontinuities in link path is the nonideal return path for slot-crossing signal line. A heterogeneous integration system requires different dc power supplies. One of the layers in PCBs or packages is usually split to accommodate separate power supplies, for example $5, 3.3, 2.5$, or 1.8 V. Splitting of planes also happens when the ground and power planes are located on the same layer. On the other hand, EMC engineers sometimes make use of slot structures to supply inductive impedance on the reference ground and avoid the noise coupling from the noisy digital to the sensitive analog circuits via reference ground. These slits result in incomplete reference planes and nonideal return current paths and cause severe signal degradation and radiated emission. Etching slots on the power/ground planes have been verified to be an effective and low-cost solution to these problems [89]–[92]. All the aforementioned reasons demonstrate that the existence of slot structure is now unavoidable in most system designs. Several EMC issues, including SI [54] and EMI problems [93], arise due to

the slot-crossing traces and need to be investigated. For SI issues, the slotted reference plane results in substantial parasitic effects, which degrade the signal transmission especially for high-frequency components. Meanwhile, the electromagnetic coupling between slot-crossing signal lines is significant in the crossed slotline structure [54]. Moreover, once the frequency of the coupled noise meets the resonant frequency of the slotline, considerable EM radiation will be generated due to the excitation of the antenna-like slotline. This will lead to serious EMI problems and may fail EMC compliance test.

For accurately modeling the EM characteristic of slotline structures, the approximate analysis, transverse method, Galerkin method, and even full-wave numerical simulation have been employed [94]–[96]. Besides, the investigations of slotline discontinuities including the slot-to-microstrip transition, short/open-end effect have both been widely discussed [97]–[99]. Based on the electrical behavior of the slotline, the transmission-line model [100], [101] demonstrates the SI issues induced by signal traces crossing a common slotline. Through the constructed model, the signal distortion and coupled crosstalk can be both quantitatively determined.

Besides using differential signaling, for the case of a single-ended line crossing a gapped reference plane, shorting bridges [102], and stitching capacitors [90] are the most common solutions for providing additional reference paths, which can further be extended to the cases of common-mode noise carried by differential lines. Although placing a shorting bridge underneath the signal lines to connect the split planes is the most intuitive method [102], the use of shorting bridges is not appropriate for two power planes with different voltage levels. In addition, the shorting bridges greatly degrade the isolated efficiency of a slotline at low-frequency [92], which obviously violates the initial purpose of slotted reference planes. Replacing the shorting bridges with decoupling capacitors is now the most predominant technique in industry [90]. This solution can actually avoid those problems induced by shorting bridges and provide return current paths at high frequency. However, its equivalent series inductance significantly dominates the impedance behavior of the decoupling capacitor, which limits its effectiveness to only below the GHz range. In [103], a circuit model has been recently proposed to explain the crosstalk behavior of the signal lines crossing the slotline. A novel solution by using branched reflector, as shown in Fig. 9, shows good capability for reducing the coupled crosstalk. The branched reflector is a slot-crossing open stub with the other end grounded by a via. The crosstalk has been proved to be significantly reduced, as shown in Fig. 10.

Besides the slot-crossing signal lines, the via-plates transition is another discontinuity with nonideal return path. In a multilayer PCB, the increasing integrated components and the complicated layout routing make the via transition through parallel-plate structure inevitable. However, the vertical via transition results in signal distortion and EMI because of excitation of the cavity modes [104]. The modeling of the interaction between the vias and the parallel-plate is thus important. The interaction can be described by an analytical formula for a constrained parallel-plate shape [105], [106] or full-wave simulation with larger computation resources [104], [107]. Recently, a physics-based

Fig. 9. Concept of the branched reflector for a signal passing a slotline.

Fig. 10. Crosstalk reduction by the branched reflector in time domain [103].

via model was proposed with reasonable accuracy and computing efficiency [108]–[112]. This approach combines the parallel-plate impedance based on the cavity model [113], [114] and the via-to-plane capacitance formula [110]. An advantage of the physics-based via model is that it is convenient for producing signal and power integrity cosimulation [112], [115].

V. Assessment of Parameters Variation Effects on PCB Signals

A fundamental step to perform right-the-first-time designs is the availability of efficient methods for the numerical simulation of interconnect structures. Several tools are available, although they are usually deterministic, hence strongly limited whenever manufacturing tolerances or uncertainties on design parameters cannot be neglected. Therefore, stochastic analysis is highly desirable in the early design phase for the prediction of the system performance and for setting realistic design margins. The typical resource allowing to collect quantitative information on the statistical behavior of the circuit response is based on the application of the brute-force Monte Carlo (MC) method [116]. Such an approach, however, is computationally expensive, and this fact prevents us from its application to the analysis of complex realistic structures. Recently, an alternative technique overcoming the previous limitation has been proposed. This methodology is based on the polynomial chaos (PC) theory and on the representation of the stochastic solution of a dynamical systems in terms of orthogonal polynomials [117]. An extension of PC theory to

interconnects described by transmission-line equations [118], and a SPICE implementation of this methodology to lumped circuit elements has been recently provided [119].

A. Stochastic Formulation

In order to account for uncertainties affecting the wave propagation along distributed transmission lines, we refer to the theory of telegraph equations, to which Paul significantly contributed and rigorously and elegantly described in [2]. The transmission line governing equations in the Laplace domain

$$\frac{d}{dz}\begin{bmatrix}\mathbf{V}(z,s)\\ \mathbf{I}(z,s)\end{bmatrix} = -\begin{bmatrix}0 & \mathbf{Z}(s)\\ \mathbf{Y}(s) & 0\end{bmatrix}\begin{bmatrix}\mathbf{V}(z,s)\\ \mathbf{I}(z,s)\end{bmatrix} \tag{1}$$

become stochastic differential equations, leading to randomly varying voltages and currents along the line. In (1), s is the Laplace variable, while $\mathbf{V} = [\ldots, V_i(z,s), \ldots]^T$ and $\mathbf{I} = [\ldots, I_i(z,s), \ldots]^T$ are vectors collecting the voltage and current variables along the multiconductor line (z coordinate). Moreover, $\mathbf{Z} = \mathbf{R} + s\mathbf{L}$ and $\mathbf{Y} = \mathbf{G} + s\mathbf{C}$ are the p.u.l. impedance and admittance matrices, depending on the geometrical and material properties of the structure. When the problem becomes stochastic, we must consider the p.u.l. parameters as random quantities, with entries depending on the random variable ξ. In turn, (1) becomes a stochastic differential equation, leading to randomly varying voltages and currents along the line. Therefore, they also depend on ξ.

Any function H, carrying the effects of variability, can be approximated by means of the following truncated series [120]

$$H(\ldots,\xi) = \sum_{k=0}^{P} H_k(\ldots)\cdot\phi_k(\xi) \tag{2}$$

where $\{\phi_k\}$ are suitable orthogonal polynomials expressed in terms of the random variable ξ. The aforementioned expression is defined by the class of the orthogonal bases, by the number of terms $P+1$ (limited to the range from 2 to 20 for practical applications, depending also on the number of random variables considered) and by the expansion coefficients H_k.

The expansion (2) of the p.u.l parameters and of the unknown voltage and current variables in terms of Hermite polynomials, yields a modified version of (1), whose second row becomes

$$\begin{aligned}&\frac{d}{dz}(\mathbf{I}_0(z,s)\phi_0(\xi) + \mathbf{I}_1(z,s)\phi_1(\xi) + \mathbf{I}_2(z,s)\phi_2(\xi))\\ &= -(\mathbf{Y}_0\phi_0(\xi) + \mathbf{Y}_1\phi_1(\xi) + \mathbf{Y}_2\phi_2(\xi))(\mathbf{V}_0(z,s)\phi_0(\xi)\\ &+ \mathbf{V}_1(z,s)\phi_1(\xi) + \mathbf{V}_2(z,s)\phi_2(\xi))\end{aligned} \tag{3}$$

where a second-order expansion (i.e., $P = 2$) is assumed; the expansion coefficients of electrical variables and of p.u.l. parameters are readily identifiable in the aforementioned equation.

Projection of (3) and of the companion relation arising from the first row of (1) on the first three Hermite polynomials leads to the following augmented system, where the random variable ξ does not appear explicitly, due to integral projection:

$$\frac{d}{dz}\begin{bmatrix}\tilde{\mathbf{V}}(z,s)\\ \tilde{\mathbf{I}}(z,s)\end{bmatrix} = -\begin{bmatrix}0 & \tilde{\mathbf{Z}}(s)\\ \tilde{\mathbf{Y}}(s) & 0\end{bmatrix}\begin{bmatrix}\tilde{\mathbf{V}}(z,s)\\ \tilde{\mathbf{I}}(z,s)\end{bmatrix}. \tag{4}$$

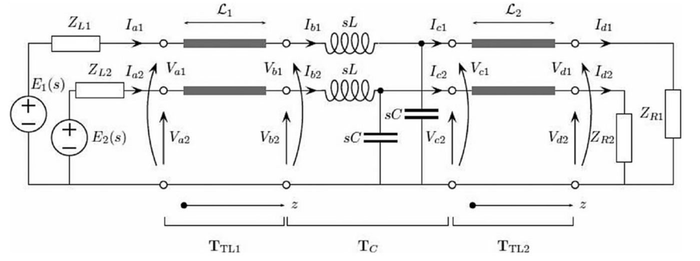

Fig. 11. Example of high-speed data link.

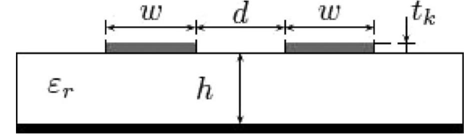

Fig. 12. Microstrip cross section for the transmission lines in Fig. 11.

In the previous equation, vectors $\tilde{\mathbf{V}} = [\mathbf{V}_0, \mathbf{V}_1, \mathbf{V}_2]^T$ and $\tilde{\mathbf{I}} = [\mathbf{I}_0, \mathbf{I}_1, \mathbf{I}_2]^T$ collect the different coefficients of the PC expansion of the voltage and current variables. The new p.u.l. matrix $\tilde{\mathbf{Y}}$ turns out to be

$$\tilde{\mathbf{Y}} = \begin{bmatrix}\mathbf{Y}_0 & \mathbf{Y}_1 & 2\mathbf{Y}_2\\ \mathbf{Y}_1 & (\mathbf{Y}_0 + 2\mathbf{Y}_2) & 2\mathbf{Y}_1\\ \mathbf{Y}_2 & \mathbf{Y}_1 & (\mathbf{Y}_0 + 4\mathbf{Y}_2)\end{bmatrix} \tag{5}$$

and a similar relation holds for matrix $\tilde{\mathbf{Z}}$.

It is worth noting that (4) is analogous to (1) and plays the role of the set of equations of a multiconductor transmission line with a number of conductors that is $(P+1)$ times larger than those of the original line. It should be also remarked that the increment of the equation number is not detrimental for the method, since for small values of P (as typically occurs in practice) the additional overhead in handling the augmented equations is much less than the time required to run a large number of MC simulations.

As far as the solution of the stochastic problem is concerned, the augmented chain parameter matrix, relating the coefficients of the voltage and current variables at the line extremities, becomes

$$\tilde{\mathbf{T}}_{\mathrm{TL}}(\mathcal{L},s) = \mathrm{expm}\left(-\begin{bmatrix}0 & \tilde{\mathbf{Z}}(s)\\ \tilde{\mathbf{Y}}(s) & 0\end{bmatrix}\mathcal{L}\right) \tag{6}$$

where expm denotes the matrix exponential and $\mathcal{L}$ is the line length.

B. Application Example

The proposed technique is applied to the analysis of the structure of Fig. 11, where the transmission lines have lengths $\mathcal{L}_1 = \mathcal{L}_2 = 5$ cm and the cross section of Fig. 12 with the following nominal parameters: $w = 100\,\mu$m, $d = 80\,\mu$m, $h = 60\,\mu$m, $t_k = 35\,\mu$m, and $\varepsilon_r = 3.7$. The depicted scheme provides an exemplification of a typical high-speed data link composed by two transmitters (represented by the Thévenin sources on the left) driving a distributed–possibly multiconductor–interconnect terminated by digital receivers (here assumed linear and simply described by their $Z_{R1,2}$ input impedances). The interconnect

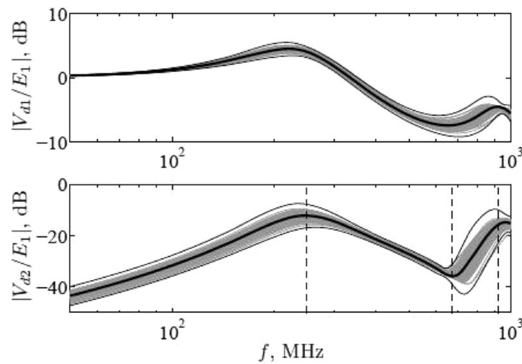

Fig. 13. Magnitudes of $|V_{d1}(j\omega)/E_1(j\omega)|$ and $|V_{d2}(j\omega)/E_1(j\omega)|$ for the variability of substrate parameters and connector capacitance. Solid black thick line—deterministic response, solid black thin line—$\pm 3\sigma$ limits of the third-order PC expansion, gray lines—a sample of responses obtained by means of the MC method (limited to 100 curves, for graph readability).

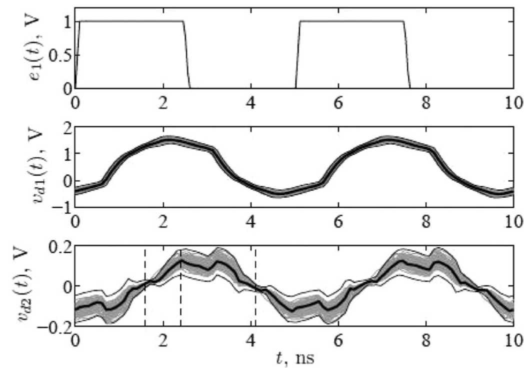

Fig. 14. $v_{d1}(t)$ and $v_{d2}(t)$. Solid black thick line—deterministic response, solid black thin line—$\pm 3\sigma$ limits of the third-order PC expansion, gray lines—a sample of responses obtained by means of the MC method (limited to 100 curves, for graph readability).

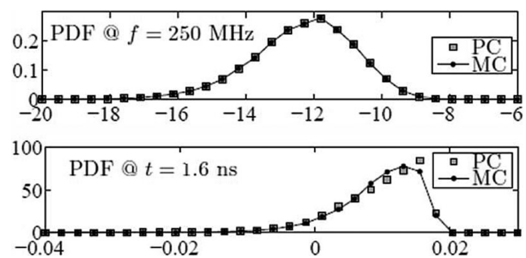

Fig. 15. Probability density function of $|V_{d2}(j\omega)/E_1(j\omega)|$ for 250 MHz (upper panel) and of $v_{d2}(t = 1.6\text{ns})$ (lower panel). The distributions marked MC refer to 40,000 MC simulations, whereas those marked PC refer to the response obtained via a third-order PC expansion.

is supposed to be composed by two identical sections linked by a connector represented by a simple *LC* equivalent. The values of the connector parameters are $L = 3$ nH and $C = 0.4$ pF. The line is excited by ideal linear drivers (one active and one off), whose equivalent series impedances are $Z_{L1} = Z_{L2} = 25\,\Omega$ and $Z_{R1} = Z_{R2} = sC_L$, being $C_L = 10$ pF.

The randomness is provided by the substrate parameters, i.e., h and ε_r, that are considered to be the same for both the transmission lines, as well as by the lumped capacitance C. These parameters are considered as three independent Gaussian random variables with a relative standard deviation of 10%. The total number of terms $P + 1$ (corresponding also to the magnification of the size with respect to the original system) is given by

$$P + 1 = \frac{(p + n)!}{p!n!} \tag{7}$$

where n is the number of random variables and p is the order of accuracy, that represents the maximum degree of the polynomials used for the expansion.

Three augmented models are built for the distributed lines and the intermediate lumped section, which are indicated by their transmission matrices $\mathbf{T}_{\mathrm{TL}1,2}$ and $\mathbf{T}_C$, respectively. Approximate relations were used to numerically compute the PC expansion of the p.u.l. parameters of the coupled microstrips, whereas the expansion of the chain parameter matrix for the lumped block is obtained analytically.

In the first example, the structure is analyzed in frequency domain. Fig. 13 shows the transfer functions between the voltage source and the two right-end terminations. Clearly, the parameter variations lead to a spread in the transfer function, that is well predicted by the estimated 3σ limits.

Fig. 14 shows the results for a time-domain analysis on the same structure. In this case, the time-domain voltage source $e_1(t)$ is a trapezoidal wave with an amplitude of 1 V, rise and fall times of 100 ps, duty cycle 50%, and a total period of 5 ns. Harmonic superposition with $N = 30$ harmonics is considered for the calculations.

Often the knowledge of the standard deviation represents a limited information, since the quantitative information about how the values are distributed is missing. Nonetheless, from the analytical PC model, we can also obtain the probability density function (PDF) of the system responses. Fig. 15 shows the PDF of $|V_{d2}/E_1|$ computed for 250 MHz (upper panel) and the PDF of $v_{d2}(t = 1.6\text{ns})$ (lower panel).

The good agreement between the actual and the predicted PDFs, as shown in Fig. 15, and the accuracy in reproducing the tails and the large variability of non-Gaussian shapes of the reference distributions, confirm the potential of the proposed method. For this example, it is also clear that a PC expansion with order 3 (i.e., $P + 1 = 20$) is already accurate enough to capture the dominant statistical information of the system response. Finally, we observe that the speed-up of PC with respect to MC is over two orders of magnitude.

However, when the number of random variables of interest increases, the efficiency of the PC appraoch tends to decrease, due to the increased number of terms, according to (7). A possible solution consists in performing preliminary tests to identify the most influential variables to be included in the model [121]. Yet, other alternatives less sensitive to the number of random parameters exist. A possible example is the response surface modeling (RSM) approach, based on the fitting of a system response using polynomial terms, whose coefficients are computed in a least-square sense starting from a reduced set of samples. A comparison of PC and RSM applied to the stochastic analysis of a commercial multiconductor flex cable with uncertain parameters described by independent uniform random variables has demonstrated their high efficiency with respect to MC, and

the additional flexibility of RSM, that provided good results for a large number of random parameters [122].

VI. Education for Printed Circuit Board Design

This Section illustrates an experience that one of the Authors[1] started some twenty years ago with the aim of providing practical EMC training for intermediately trained technicians.

In the early times, experiments were focused at cabinet level designs, using demonstrators with wires and sheet metal [123], heavily leaning on the propositions contained in the EMC education manual [6], of which Paul was the inspirer, and on the few available textbooks [124] and [125]. A few years later, PCB designers joined the class and it became apparent that it is vital to provide experiments matching the attendees view of the world. Crosstalk was demonstrated by means of experiments with wires, but the question on how the shown phenomenon relates to PCB structures was always popping up. Hence, all experiments had to be “ported” to PCB versions. To complicate the issues, the level of education had to be lifted from ‘lumped elements” (LE) to “per unit length” (PUL) versions, since the primary reason to educate the PCB designers was a disastrous transition from traditional trace layout craftsmanship to computer aided development (CAD) tools that did not (yet) have transmission line effects on board. These tools were advertised to help with a shorter time to market and savings in terms of reduced PCB production complexity. In order to achieve such results, however, a fast reeducation of the layout engineers was needed on these more elevated subjects and this is where the EMC textbook of Paul came in handy [1]. It also showed the absolute requirement of management awareness in these matters.

The EMC curriculum was then expanded to include “long line” effects using some experimental printed circuit boards already designed using the concepts of ground bounce and partial inductance developed by Paul [1, pp.775–785]. These boards were used for in-company education and the yearly Dutch EMC courses at the Technical University of Eindhoven.

For high-speed work, it is absolutely essential to not only keep signals and return together but also not to disturb the geometry of the interconnection impedance to avoid reflections. Printed circuits are definitely more stable in this respect than their wired counterparts. For the educational demonstrations, however, this posed a challenge to demonstrate the good and the bad approach preferably in one circuit board. A master student was set to work on a consistent set of PCB demonstrations, resulting in an initial set in 2005 [126]. The initial boards are shown in Fig. 16.

These boards were a huge success at sessions with board designers, but a reservation was frequently raised, since these boards did not look like the boards currently manufactured for products. There was apparently a need to give them a more “professional” look in order to make the demonstration boards acceptable for the management-oriented attendees. So, an improved set was built with the help of several students in the 2008–2009 time frame [127] and the preparations for the Kyoto conference paper [131], resulting in

[1]Frits Buesink

Fig. 16. The initial printed circuit board set.

Fig. 17. Selection of the new professional EMC demonstration boards.

sixteen different boards, accompanied by a user manual [128]. A selection of the new boards is shown in Fig. 17.

The EMC Printed Circuit Board Experiments can be performed either in the time domain or in the frequency domain. The former using the TDR approach, the latter using a spectrum analyzer with a tracking generator.

A. Time Domain Experiments

The most challenging audience are the digital high-speed designers. Many of them have had little or no education in analogue phenomena as reflections and crosstalk and the measures

Fig. 18. Home-made time domain reflectometer with scope and generator (Shown with Crosstalk Experiment Board).

to avoid problems. The task for the high-speed digital designers is to transport a critical timing signal from one point to another on a board without distortions. They predominantly think in terms of time. Distortions are created by discontinuities in the transmission line used for the transport, creating partial reflections, or by means of crosstalk from a signal on another trace on the board. The digital designer is usually less interested in the behavior of his or her creation in the frequency domain.

A time domain reflectometer contains a generator to send a fast "zero-to-one" digital transition down a coaxial line, matched to the impedance of the generator, usually 50 Ω. The coaxial line has an open end that is monitored by a fast oscilloscope and also connects to the transmission line under study. Any discontinuity (from the 50 Ω impedance) on this transmission line combination generates a reflection that shows on the monitoring oscilloscope. The location of the discontinuity can be calculated from the time delay between the rising edge and the occurrence of the reflection. An animation of the TDR process is shown on Wikipedia [132], and a short tutorial can be found in [133]. Fig. 18 shows how a TDR can be assembled from a scope and a generator (see also [1], Fig. 4.26).

The resolution of the TDR measurement depends directly on the rise-time of the oscillator transition traveling down the line under study. As a rule of thumb, the smallest discontinuity visible has a length equal to the distance traveled by the wave during the oscillator's rise-time. The PCB experiments at the University of Twente are usually performed by students using the TDR of Fig. 18, assembled from a square wave generator with a $\tau_r = 3$ ns risetime and a 200 MHz bandwidth oscilloscope. The generator is described in [123]. The transmission lines on PCBs are microstriplines having a propagation delay of about $\tau_{PD} = 5$ ns/m. The "resolution" is τ_r/τ_{PD} and equals approximately 60 cm (24 inches). However, it is not enough for the small discontinuities usually encountered on PCB, as shown in Fig. 19. To evaluate those boards in the time domain, a faster TDR is required. Instruments with a signal rise-time under 50 ps, giving a distance resolution of approximately 0.01 m (0.4 in), are required.

The board in Fig. 19 contains a 1.8 mm reference plane gap under a trace. Based on the propagation speed of 5 ns/m for

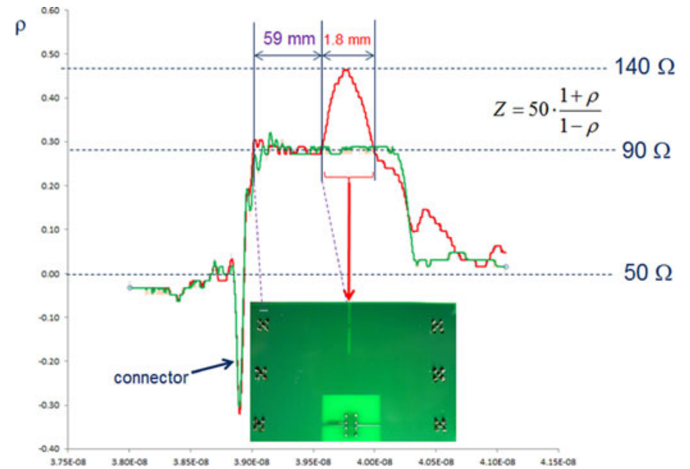

Fig. 19. Effect of trace crossing narrow aperture in ground.

Fig. 20. The board showing Lenz's law.

the trace, the 1.8 mm would be traveled in 9 ps. The actual displayed time is 400 ps, 44 times longer, but still too short to be seen on a 200 MHz oscilloscope that needs a transient of several nanoseconds to make it visible. The effect responsible for this extra delay is the additional induction introduced by the anomaly in the transmission-line geometry. The signal traveling down the transmission line is a specific energy flow, determined by the effective signal voltage and current. When the geometry changes into the large loop formed by the trace and the gap in the ground reference plane, the p.u.l. inductance L_{PUL} of the line suddenly increases while the respective capacitance C_{PUL} goes down. This, in turn, increases the local line characteristic impedance $Z_0 = \sqrt{L_{\mathrm{PUL}}/C_{\mathrm{PUL}}}$. The additional inductance now has to be "filled with magnetic flux" in order to make the line current possible. This process takes time and results in a delay for the pulse propagation.

This *inductive effect* is now explained by the "self-induction" and "Lenz law" demonstration boards. The former is a movable wire over a ground reference plane that can be manipulated to show more or less "spiking" on the TDR (even on the model in Fig. 18). The latter is a board with a U-shaped ground reference strip and seven traces which are layed-out as shown in Fig. 20. Here, the traces cannot be moved and changes on the TDR display are only visible when the TDR signal line is connected to the seven input connectors in sequence. The output connector is not used and normally loaded with 50 Ω.

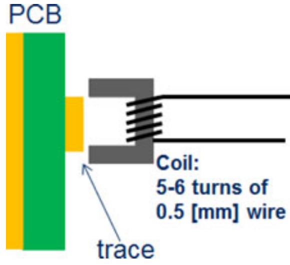

Fig. 21. Small magnetic field probe.

For further demonstrations, a magnetic field probe can be used on the second channel of the oscilloscope/TDR. The probe is made of a small ferrite C-core with a few turns of wire (not critical), as shown in Fig. 21, and it is loaded with 50 Ω.

The probe is used to show where fields are present. For the traces far removed from the reference trace, a high value is measured near the trace and on the edge of the reference strip. If the scope is triggered on the TDR signal feeding the trace, an inverse polarity can be observed. On the rightmost trace (input 7) in Fig. 20, only a small spike is measured if the probe is right on the trace. This demonstrates that, if a return path is available directly under the trace, the return current will prefer to flow there (proximity effect). This demonstrates to the students that currents naturally prefer paths producing as little induction as possible. The field probe of Fig. 21 could also be used on the bottom of the board, on the opposite side of the reference strip to show that the skin effect prevents fields generation from the current in trace 7.

B. Frequency Domain Experiments

Although all boards can be approached either in the time domain or in the frequency domain, there is an effect that can only be shown in the frequency domain. It is a crosstalk experiment with an active trace, escorted by two passive traces: a "20 dB" trace and a "30 dB" trace. The board is shown in Fig. 18, and its trace geometry (cross section) is displayed in Fig. 25. The motivation for this demonstration resides in the fact that digital layout engineers have problems separating their traces. The *signal-to-noise transformation* effect [129] helps with the explanation. In fact, this is the concept of transfer impedance for transmission lines, focused on PCB's. It is defined as the ratio of the noise voltage appearing over the return conductor of a transmission line and the signal voltage transferred over the line. The line is assumed to be terminated in its characteristic impedance. This ratio is shown in Fig. 22. In [129], this "ground lift" voltage is then used as driving voltage to an antenna formed by cables connected to the reference conductor at either side of this section of PCB transmission line. Using the equations for wire antennas, the generated field (e.g., in the far field) is calculated. The interesting aspect is the asymptotic leveling of the ground lift voltage for high frequencies. The level of this asymptote can be calculated from the transmission line geometry.

Analyses and experiments have shown that this same model can be used to calculate the crosstalk between two adjacent PCB traces over a common ground reference plane. Here, too, the crosstalk asymptotically approaches a fixed level, starting at the frequency at which the active transmission line length cor-

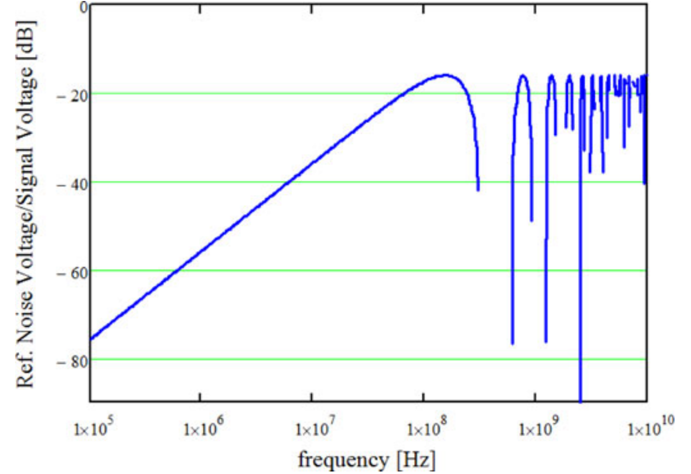

Fig. 22. Signal-to-noise transformation for a PCB transmission line.

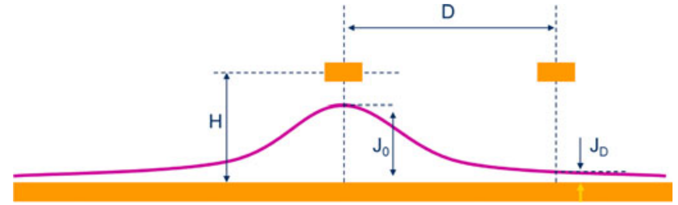

Fig. 23. Geometry of a line with two traces over a reference plane, and current density distribution in the plane.

responds to a quarter wavelength. This is called the "cross-over frequency". The level of the horizontal asymptote for crosstalk is the maximum crosstalk level for the given line geometry for frequencies above the cross over value (determined by the length over which the lines run in parallel and the propagation speed). Obviously, if the original signal on the active line has no components in this frequency range, the actual crosstalk will be lower, thus confirming the basic EMC rule–use no higher frequencies than absolutely necessary. The maximum crosstalk level can be determined using per unit length parameters for the two adjacent lines. Assuming two identical lines, running in parallel at a fixed separation, the ratio of the line inductance, L_{PUL} and the mutual inductance M_{PUL} is needed. This ratio is [130]

$$\frac{M_{\mathrm{PUL}}}{L_{\mathrm{PUL}}} = \frac{J_D}{J_0} \approx \frac{1}{1 + (\frac{D}{H})^2} \tag{8}$$

and Fig. 23 represents the line geometry and the current density distribution in the reference metal plane. The proposition here is to replace the current density J_0 in the ground reference plane under the active trace by the per unit length inductance L_{PUL} of the trace, because the two quantities are proportional. The remaining current density J_D, under the passive trace, is then replaced by the per unit length mutual inductance M_{PUL} between the active and the passive trace.

The asymptotic crosstalk level (referenced to the signal level in the active trace as 0 dB) can be interpreted as an attenuation, depending on the PCB trace configuration, i.e.

$$\text{Attenuation} = 20 \log \frac{L_{\mathrm{PUL}} + M_{\mathrm{PUL}}}{M_{\mathrm{PUL}}} \tag{9}$$

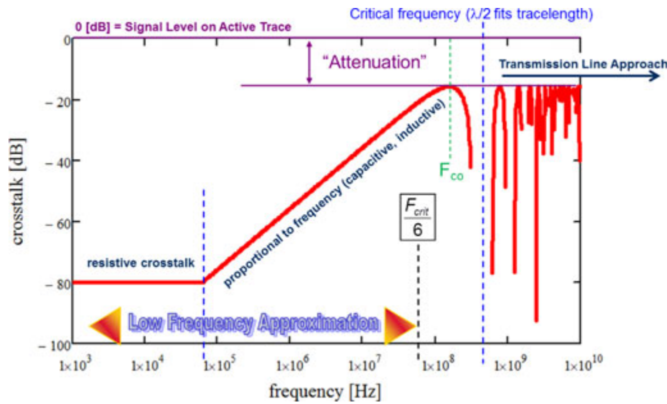

Fig. 24. Crosstalk between two identical terminated PCB traces.

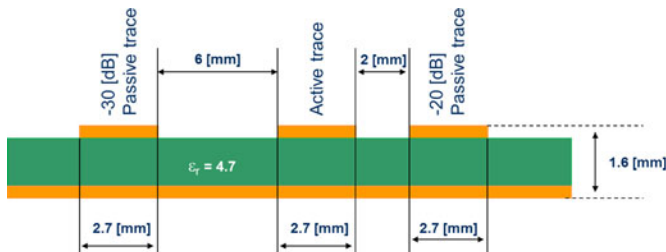

Fig. 25. Trace geometry (cross section) for crosstalk experiment board.

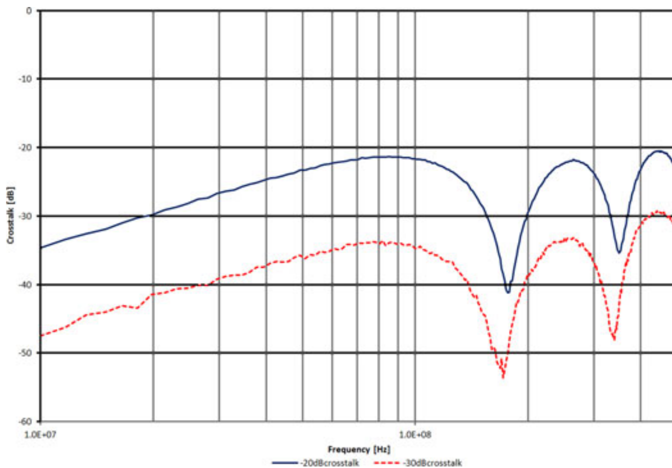

Fig. 26. -20 and -30 dB crosstalk demonstration by measurements on the side traces of the experiment board of Fig. 25.

and is shown in Fig. 24. Using this approach to crosstalk, its envelope in the frequency domain can be easily drawn using the maximum value of (9) for frequencies above F_{CO} and values decreasing proportional to frequency below it. Although the analysis is valid only for properly terminated lines, which is almost never the case in digital boards, at least there is a lot of insight to be gained from this experiment. Fig. 25 illustrates the cross section of the experiment board (2.7 mm-wide traces are needed to achieve a 50 Ω impedance to match the available standard test cabling). The two cases -20 and -30 dB have been designed for the crosstalk board in the experiment set. The experiment is performed using a spectrum analyzer with tracking generator that is first calibrated to 0 dB with the input interconnected to the generator. The result for the two traces is shown in Fig. 26.[2] This demonstration is intended for helping layout engineers to determine their trace separations, once they know how much crosstalk their design can afford. This information can then be extracted from signal levels, susceptibility thresholds and the bandwidth of the system active signals.

VII. Conclusion

In this paper, three main topics (link path, differential signal, and discontinuities) related to SI and EMC for PCB or package have been outlined and reviewed from the points of view of modeling, analysis, and design. The inclusion of parameters variability effects has also been considered, and it has been demonstrated that recently introduced stochastic methods allow simulations of interconnects with several statistical parameters. Finally, an educational experience for PCB design has been illustrated, and a description of a small sample of demonstration boards has been provided. Nevertheless, it should be mentioned that the University of Twente EMC group makes available the boards for whomever wishes to use them, in the spirit of Paul's IEEE EMC education manual and for the promotion of EMC knowledge and of the techniques to achieve it.

In future, further research for the cosimulation and codesign to take signal integrity, power integrity, EMC, RFI into account will be one of the crucial directions that both industry and academia should pursue.

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