

Laplace Transform–based Theoretical Foundations and Experimental Validation – Low Frequency Supercapacitor Circulation for Efficiency Improvements in Linear Regulators

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Abstract- Supercapacitor circulation techniques can be used to improve the end-to-end efficiency of linear regulators based on commercial low drop-out regulators (LDO). In this approach, one or more supercapacitors are used in series and parallel to the input of an LDO IC, and circulated at a very low frequency to increase the end-to-end efficiency by a multiplication factor compared to the efficiency of a linear regulator circuit with the same input-output voltages. This paper presents the essential theory of supercapacitor circulation, together with analytical results and comparisons with experimental measurements from a practical 12V to 5V implementation. The new technique achieved overall end-to end efficiencies in the range of 70 to 80%, compared to the maximum theoretical efficiency of 42% for a 12V-5V linear regulator.

1. Introduction

Low-voltage supercapacitors with capacitances ranging from few farads to several hundred farads are now used in various applications such as electric vehicles, wind energy, surge absorption, battery-supercapacitor hybrids and memory backups [1-6]. Single-cell devices are DC rated from about 2.3V to 5.5V, while supercapacitor modules are available with DC voltage ratings beyond 100V. With the availability of very thin profile supercapacitors from manufacturers such as Cap-XX (Australia) [7] with the capacitance values up to several farads and very low equivalent series resistance (ESR) values, a new approach to enhancing the end-to-end efficiency of linear regulators based on low dropout regulator ICs has been developed [8-14]. The technique is easily applicable to standard cases such as 12V-5V, 5V-3.3V and 5V-1.5V which are common in processor-based electronic systems [15].

In the power conversion area, dominated by switching power supply based DC-DC converter techniques, low dropout regulators (LDO) were introduced to address the requirements of noise-sensitive and fast transient loads in portable devices [16-24]. In an LDO where V_{in} is the unregulated input voltage and V_{out} is the regulated output voltage, if the control circuits consume minimal power compared to the output power, the approximate efficiency is given by,

$$\eta = \frac{V_{out}}{V_{in}} \times 100 \% \quad (1)$$

Most commercial off-the-shelf (COTS) LDOs have their input voltage slightly higher than the desired regulated output for higher efficiency. In many situations, the dropout voltage is on the order of 0.1V to 2V with the control circuits using extremely low power, providing efficiencies around 65% at the lower end, and, much higher for lower dropout voltages. For example, 66% efficiency could be achieved for cases such as 5V to 3.3V converters, and, around 94% for 3.5V to 3.3V LDOs. As LDOs provide adequate transient response with low noise for fast-varying loads, combining LDOs and switch-mode regulators is common in portable products. In commercial systems, this technique is called the point of load (POL) supply [25]. LDOs operate in the same manner as standard NPN regulators apart from the pass transistor being replaced by a single PNP or a PMOS transistor which can hold its output voltage in regulation with much lower voltage differences across the series element [16-18, 26].

Supercapacitor-based energy recovery, a patented technique [11], builds on the simple concept that a very large capacitor placed in the series path of the input acts as a lossless voltage dropper (assuming an ideal capacitor with zero ESR). The capacitor is then discharged in the second phase of the technique, in order to release the accumulated energy to the LDO, so that the net accumulated charge on the capacitor averages to zero over the complete charge-discharge cycle. This technique is different to the classical switched-capacitor converters where the input voltage is converted to a higher voltage or a negative value using capacitor switching, since the new technique uses a very large value capacitor (a supercapacitor) as a simple lossless voltage dropper in the series path, and a linear regulator for output voltage regulation.

The special case of $V_p > 2V_{in(min)}$ is discussed in the paper, where V_p is the unregulated input supply voltage and $V_{in(min)}$ is the minimum required input voltage value for the LDO IC to keep the output regulated. The technique can be easily adapted to other practical applications such as $V_p < 2V_{in(min)}$ and $V_p > 3V_{in(min)}$ configurations, as far as the usability of a linear regulator at the output end is broadly applicable [8, 10]. If the input voltage is lower than the output, classical switched-capacitor

configurations will be required. A 12V-5V regulator requires only a single supercapacitor, while other combinations such as 5V-3.3V and 5V-1.5V converters require supercapacitor arrays [10]. More details are provided in [8-14] with various configurations applicable to different input-output voltage combinations.

In Section 2 a summary of the technique is discussed with practical achievements for the efficiency enhancement. Section 3 provides a summary of four phases of operation and related Laplace transform relationships applicable. In Section 4 we compare the analytical relationships and MATLAB based evaluations with experimental waveforms applicable to a prototype 12V to 5V converter based on the new technique.

2. Basic concepts

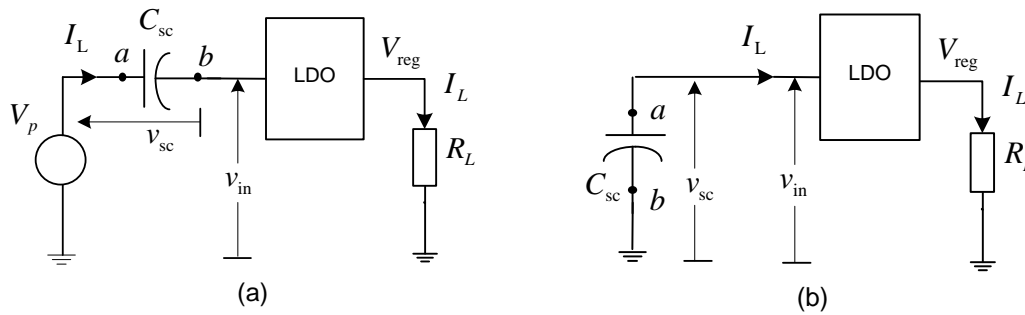


Fig.1: Concept of supercapacitor energy storage and recovery (a) minimizing the series element dissipation and (b) releasing stored energy

Fig. 1 illustrates the concept: a supercapacitor C_{sc} is placed in series with the input of the LDO. Since the series capacitor is large (of the order farads), it will pass current as it charges for a reasonable period of time. Based on this simple principle, a single supercapacitor, can cyclically store and release energy.

As per Fig. 1(a) in the first phase of the operation, due to supercapacitor charging, when the value of LDO input voltage, V_{in} is dropped down to its minimum possible input voltage which is $V_{in(min)}$. At the end of this phase, the supercapacitor is connected in parallel with the input of the LDO as shown in Fig. 1(b) to release the stored energy in the supercapacitor.

Assume the initial voltage across the supercapacitor (C_{sc}) is $V_{sc(0)}$. After charging for a period Δt , the instantaneous voltage across the capacitor v_{sc} is given by,

$$v_{sc}(t) = V_{sc(0)} + \frac{I_L \Delta t}{C_{sc}} \quad (2)$$

where I_L is the load current entering the capacitor from the power supply (We can assume that the load acts as a constant-current sink, and that the bypass current from LDO to ground can be neglected).

The unregulated source voltage V_p , equals the sum of the supercapacitor voltage and the LDO input voltage,

$$V_p = v_{sc}(t) + v_{in}(t) \quad (3)$$

The supercapacitor charges until v_{in} reaches $V_{in(min)}$ while the voltage across the capacitor reaches $V_p - V_{in(min)}$ at the end of the charging time. In order to discharge this supercapacitor at the next stage down to $V_{in(min)}$, the criterion $V_p - V_{in(min)} > V_{in(min)}$ must be satisfied. This creates the condition $V_p > 2V_{in(min)}$.

At the conclusion of charging cycle, the stored energy can be released as shown in Fig. 1(b). Discharging continues until LDO input voltage drops back to $V_{in(min)}$ satisfying the following equation,

$$V_p - 2V_{in(min)} = \frac{I_L \Delta t}{C_{sc}} \quad (4)$$

The circuit draws power from the unregulated input only during half the time of its operating period: during the supercapacitor charging phase the supercapacitor draws current from the unregulated supply, whereas during discharge the supercapacitor delivers power to the LDO keeping the unregulated power supply disconnected from the system, so that the average input current is $I_L/2$. Assuming that the capacitors and switching elements are ideal and neglecting the power consumed by control circuits, approximate end-to-end efficiency for the case $V_p > 2V_{in(min)}$ is given by,

$$\eta = \frac{P_{out}}{P_{in}} = \frac{I_L V_{reg}}{V_p \times I_L / 2} = \frac{2V_{reg}}{V_p} \quad (5)$$

Fig.2 shows the efficiency results: theoretical performance of the supercapacitor technique (upper trace), practical performance of the supercapacitor technique (middle trace) and performance of standard linear regulator (lower trace) for a 12V-5 V regulator.

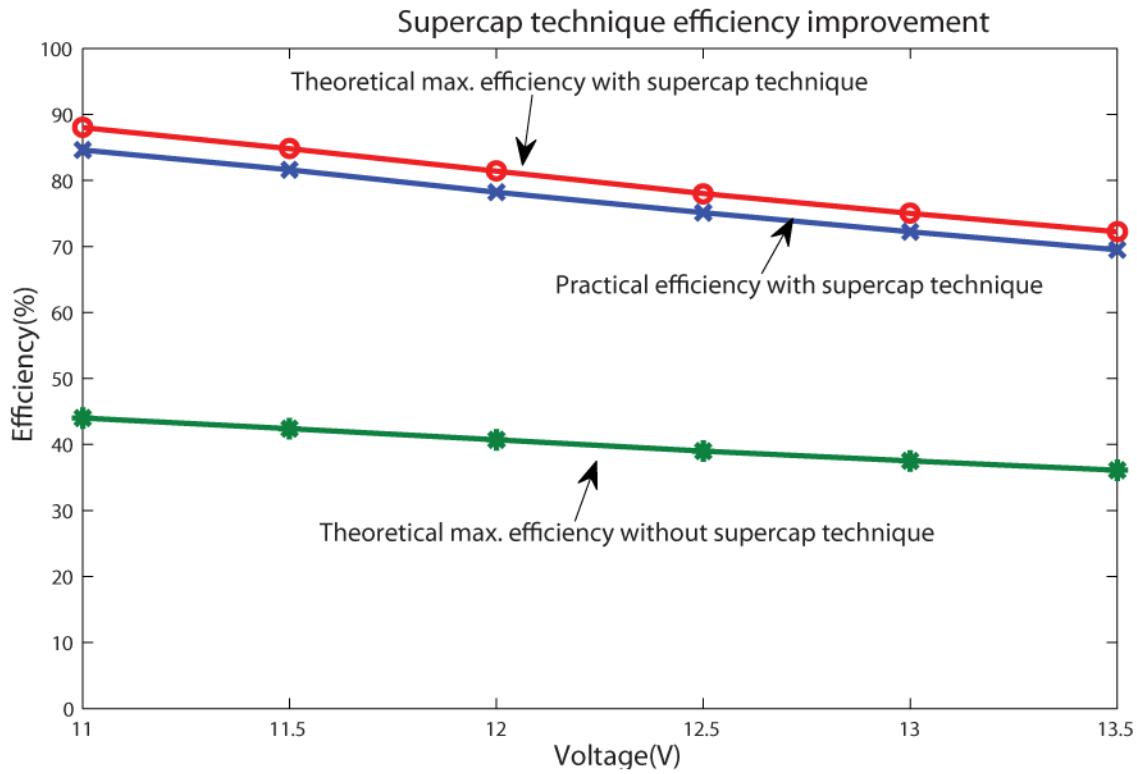


Fig. 2: Efficiency comparison for a 12V to 5V regulator: Theoretical results with supercapacitor technique (upper trace), practical results with supercapacitor technique (middle trace) and basic 12V-5V linear regulator theoretical performance (lower trace)

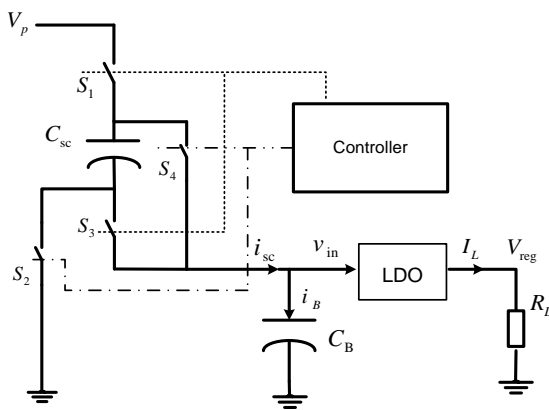


Fig. 3: Simplified circuit arrangement for a 12V to 5V single supercapacitor based linear regulator

Fig. 3 shows an implemented version of the above concept in a 12V-5 V supercapacitor assisted linear regulator. To keep the linear regulator powered during switch transition, a buffer capacitor (C_B) with sufficient capacity is connected between the

linear regulator input and ground. Switches shown by S_1 and S_3 are kept closed at the start, placing the supercapacitor in its charging configuration; S_2 and S_4 are kept open at this time. Load current plus buffer capacitor current flows through the supercapacitor connected in series with the unregulated power supply, charging the capacitor while the voltage level at the LDO input is monitored continuously by a microcontroller. When v_{in} decays to $V_{in(min)}$, S_1 and S_3 are opened and switches S_2 and S_4 are closed. Now the stored energy in the supercapacitor discharges to the regulator's input terminal. When LDO input voltage reaches the minimum input voltage $V_{in(min)}$ of the regulator, S_2 and S_4 open and S_1 and S_3 close. This cycle repeats to keep the overall regulator circuit working continuously. The prototype achieves overall end-to-end efficiencies in the range of 70 to 80%, compared to the maximum theoretical efficiency of 42% for a linear regulator used for the same input-output combination. Fig.2 middle trace shows the improved efficiency in this implementation. Additional implementation details of the circuit are available in [8-14].

3. Circuit theory for capacitor circulation

For a full charge-discharge cycle, the circuit operation moves through four different phases as shown in Fig. 4. We analyze circuit operation using Laplace transform theory. Table 1 lists the parameters and definitions used in time and frequency domains.

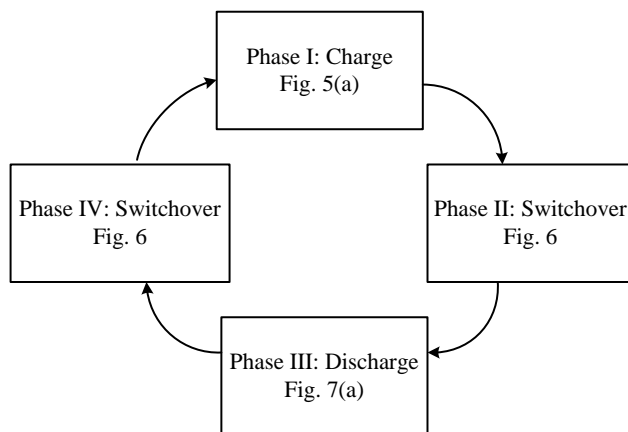


Fig.4 The four phases of circuit operation

In the following analysis, we consider only the steady-state operation of the circuit, when the supercapacitor has achieved its average DC operational voltage. Start-up circuit operation requires a different switching process initially in order to manage the limits of the LDO circuit. A discussion on the start-up process is beyond the scope of this paper.

Table 1: Symbols and definitions used for analysis using Laplace technique

Time domain	Laplace domain	Description
$i_1(t)$	$\tilde{i}_1(s)$	Supercapacitor current
$i_2(t)$	$\tilde{i}_2(s)$	Buffer-capacitor current
I_L	I_L/s	Constant load current
$v_1(t)$	$\tilde{v}_1(s)$	External voltage across supercapacitor
$v_2(t)$	$\tilde{v}_2(s)$	External voltage across buffer-capacitor
$v_{C1}(t)$	$\tilde{v}_{C1}(s)$	Internal voltage across supercapacitor
$v_{C2}(t)$	$\tilde{v}_{C2}(s)$	Internal voltage across buffer-capacitor
V_2^{\min}	V_2^{\min}/s	Threshold voltage for the LDO input
V_1^{IV}	V_1^{IV}/s	External voltage across supercapacitor at the end of phase IV for the assumed initial condition
V_2^{IV}	V_2^{IV}/s	External voltage across buffer- capacitor at the end of a phase IV for the assumed initial condition
$V_{C1}^{\text{I...IV}}$	$V_{C1}^{\text{I...IV}}/s$	Final values of the internal voltages of the supercapacitor at the end of phase I, II, III, IV respectively
$V_{C2}^{\text{I...IV}}$	$V_{C2}^{\text{I...IV}}/s$	Final values of the internal voltages of the buffer-capacitor at the end of phase I, II, III, IV respectively
V_p	V_p/s	Unregulated power supply voltage
C_1	$1/sC_1$	Supercapacitor capacitance
C_2	$1/sC_2$	Buffer-capacitor capacitance
r_1		Equivalent series resistance for C_1
r_2		Equivalent series resistance for C_2
r		On resistance of a solid state relay (SSR) used to perform the switching function
t_{sw}		Transition time between series/parallel due to switch delays

3.1 Phase I: Charging

This is the charging phase of the supercapacitor. The following initial conditions are indicated for this charging phase, assuming that the final conditions of the discharging phase (phase IV) are such that the current flowing through the buffer capacitor is negligibly small and the total load current was drawn from the supercapacitor.

The initial external (i.e., measurable) voltages across buffer and super capacitors at the end of phase IV are given by,

$$V_2^{fIV} = V_2^{\min} \quad (6)$$

$$V_1^{fIV} = V_2^{fIV} + 2rI_L \quad (7)$$

where the factor 2 in Eq.(7) arises from the on-resistance of the two SSR switches S_1 and S_3 (assumed identical).

Eqs.(6, 7) imply the following initial values for the internal (i.e., unobservable) voltages,

$$V_{C1}^{fIV} = V_1^{fIV} + I_L r_1 \quad (8)$$

$$V_{C2}^{fIV} = V_2^{fIV} - \frac{I_L t_{sw}}{C_2} + I_L r_2 \quad (9)$$

where t_{sw} is the transition time in switching from charging to discharging and vice versa , and the buffer and super capacitors have ESR values r_2 and r_1 respectively.

Fig. 5(b) represents the Laplace transformation of the Phase I circuit shown in Fig. 5(a). From the Laplace equivalent circuit, the following relationships can be derived,

$$\tilde{i}_1(s) = \tilde{i}_2(s) + \frac{I_L}{s} \quad (10)$$

$$\frac{V_p}{s} = \frac{V_{C1}^{fIV}}{s} + \left[\frac{1}{sC_1} + r_1 + 2r \right] \tilde{i}_1(s) + \frac{V_{C2}^{fIV}}{s} + \left[\frac{1}{sC_2} + r_2 \right] \tilde{i}_2(s) \quad (11)$$

Here, the tilde (\sim) symbol denotes a Laplace transformed quantity, e.g. $i_1(t) \leftrightarrow \tilde{i}_1(s)$

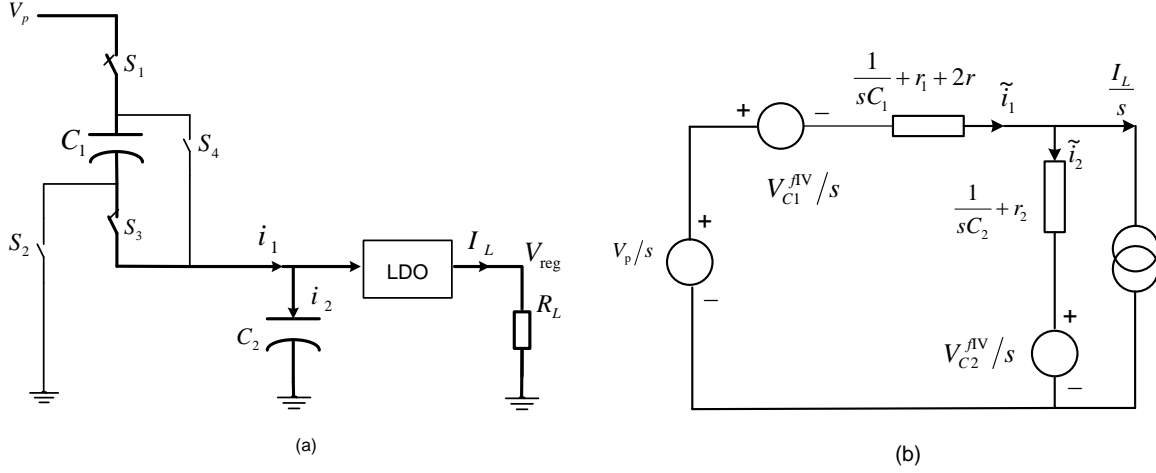


Fig. 5: Supercapacitor charging configuration and its Laplace transformation (a) Switching configuration for the charging phase (b) Laplace transformation of the charging phase where supply voltage and initial capacitor voltages= fixed voltage sources, load= constant current sink, impedances=series combination of capacitive impedance plus ESR (plus switch resistance)

Resolving Eqs. (10) and (11) ,

$$\begin{aligned}
 \tilde{i}_2(s) &= \frac{V_p - V_{C1}^{fV} - V_{C2}^{fV} - [r_{sc} + 2r] I_L - \frac{I_L}{C_1 s}}{\left[\frac{1}{C_1} + \frac{1}{C_2} \right] + [r_1 + r_2 + 2r] s} \\
 &= \frac{a_1}{a_2 + s} - a_3 \left[\frac{1}{s(a_2 + s)} \right]
 \end{aligned} \tag{12}$$

where

$$a_1 = \frac{V_p - V_{C1}^{fV} - V_{C2}^{fV} - [r_1 + 2r] I_L}{[r_1 + r_2 + 2r]}$$

$$a_2 = \left[\frac{C_1 + C_2}{C_1 C_2} \right] \frac{1}{[r_1 + r_2 + 2r]}$$

defines an effective rate constant and,

$$a_3 = \frac{I_L}{C_1 [r_1 + r_2 + 2r]} ,$$

$$a_4 = \frac{a_3}{a_2} = \frac{C_2 I_L}{[C_1 + C_2]}$$

Taking the inverse Laplace transform of Eq. (11), the instantaneous current flowing through the buffer capacitor is,

$$i_2(t) = [a_1 + a_4] e^{-a_2 t} - a_4 \quad (13)$$

so that the instantaneous current through the supercapacitor is,

$$i_1(t) = I_L + i_2(t) \quad (14)$$

Internal voltages across the buffer and super capacitors are given by,

$$v_{C2}(t) = V_{C2}^{fV} + \frac{1}{C_2} \int_0^t i_2(t') dt' \quad (15)$$

and

$$v_{C1}(t) = V_{C1}^{fV} + \frac{1}{C_1} \int_0^t i_1(t') dt' \quad (16)$$

while the external voltages (i.e., the observable voltages including the ESR of r_2 and r_1 are given by),

$$v_2(t) = v_{C2}(t) + i_2 r_2 \quad (17)$$

and

$$v_1(t) = v_{C1}(t) + i_1 r_1 \quad (18)$$

Phase I continues until $v_2(t)$, the LDO input voltage meets the following condition

$$v_2(t) < V_2^{\min}$$

3.2 Phase II: Switchover to discharging

This is the phase when the circuit is getting ready to transfer to the capacitors in parallel operation mode. For a very short duration t_{sw} of the order of few microseconds (as determined by the microprocessor code), the buffer capacitor is expected to discharge into the LDO input. This switchover period is designed to accommodate any transition delays of switches used.

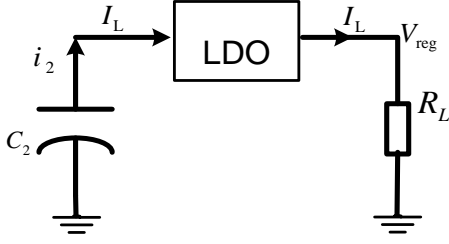


Fig.6: Switching transition from phase I to phase III

Based on Fig. 6, the internal voltage across the buffer capacitor is given by,

$$v_{C_2}(t) = V_{C_2}^{\text{fl}} - \frac{1}{C_2} \int_0^{t_{\text{sw}}} I_L dt' \quad (19)$$

while the internal voltage across the supercapacitor remains fixed at ,

$$v_{C_1}(t) = V_{C_1}^{\text{fl}} \quad (20)$$

since it is effectively disconnected from the circuit during this phase.

The external voltage across the buffer capacitor and supercapacitor are respectively given by

$$v_2(t) = v_{C_2}(t) - I_L r_2 \quad (21)$$

and

$$v_1(t) = v_{C_1}(t) \quad (22)$$

Phase II continues for a period of t_{sw} which is set by the microcontroller. In practice, t_{sw} is very short compared to the times in phase I and III.

3.3 Phase III: Discharging

In this phase, the supercapacitor is placed in parallel with the buffer capacitor so that energy accumulated by the supercapacitor during the phase I charging phase is discharged through the LDO.

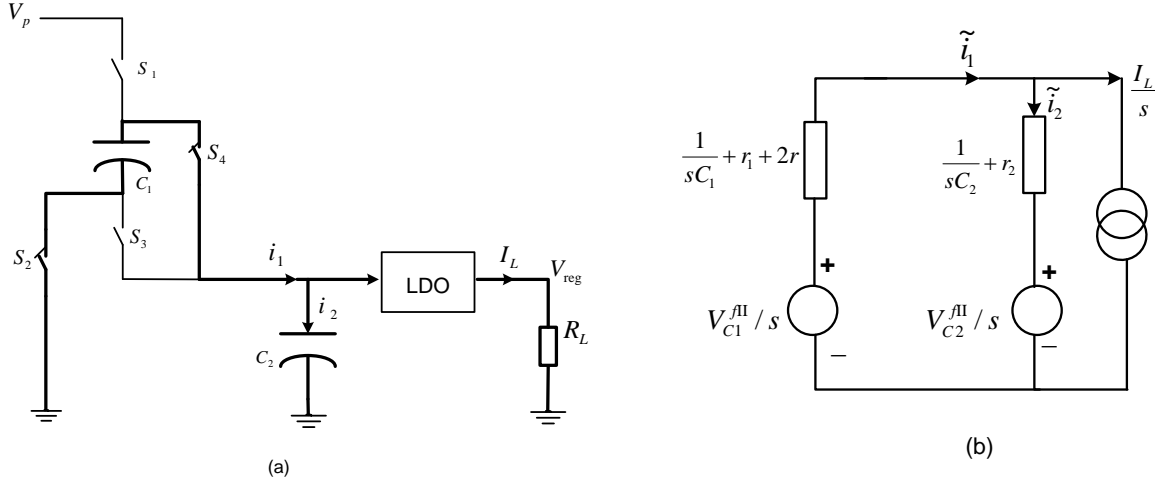


Fig. 7: Discharge phase (a) Supercapacitor discharging (b) Laplace transformation of the discharging configuration

Fig. 7(b) represents the Laplace transformation of the Phase III circuit shown in Fig. 7(a). Based on Laplace transformations, the following relationships can be derived:

$$\tilde{i}_1(s) = \tilde{i}_2(s) + \frac{I_L}{s} \quad (23)$$

$$\frac{V_{C1}^m}{s} - \left[\frac{1}{sC_1} + r_1 + 2r \right] \tilde{i}_1(s) = \frac{V_{C2}^m}{s} + \left[\frac{1}{sC_2} + r_2 \right] \tilde{i}_2(s) \quad (24)$$

Resolving (23) and (24),

$$\begin{aligned} \tilde{i}_2(s) &= \frac{V_{C1}^m - V_{C2}^m - [r_1 + 2r]I_L - \frac{I_L}{sC_1}}{\left[\frac{1}{C_1} + \frac{1}{C_2} \right] + [r_1 + r_2 + 2r]s} \\ &= \frac{a'_1}{a_2 + s} - a_3 \left[\frac{1}{s(a_2 + s)} \right] \end{aligned} \quad (25)$$

where a_2, a_3, a_4 were defined following Eq.(11) and

$$a_1' = \frac{V_{C1}^{III} - V_{C2}^{III} - [r_1 + 2r] I_L}{(r_1 + r_2 + 2r)}$$

Taking inverse Laplace transform of Eq. (24), the instantaneous current flowing through the buffer capacitor is,

$$i_2(t) = (a_1' + a_4)e^{-a_2 t} - a_4 \quad (26)$$

so that the instantaneous current through the supercapacitor is,

$$i_1(t) = I_L + i_2(t) \quad (27)$$

Internal voltages across the buffer and supercapacitors are given by,

$$v_{C2}(t) = V_{C2}^{III} + \frac{1}{C_2} \int_0^t i_2(t') dt' \quad (28)$$

$$\text{and } v_{C1}(t) = V_{C1}^{III} - \frac{1}{C_1} \int_0^t i_1(t') dt' \quad (29)$$

while the external voltages ,

$$v_2(t) = v_{C2}(t) + i_2 r_2 \quad (30)$$

$$\text{and } v_1(t) = v_{C1}(t) - i_1 r_1 \quad (31)$$

Note that apart from the sign change in the $i_1 r_1$ term for v_2 Eqs. (30,31) for the discharging phase have the same form as

Eqs.(17, 18) for the charging phase.

Phase III continues until $v_2(t)$, the LDO input voltage, meets the following condition

$$v_2(t) < V_2^{\min}$$

3.4 Phase IV: Switchover to charging

This is the final phase of the circuit in which the supercapacitor is returned to its initial configuration of being in series with the unregulated supply. During switchover buffer capacitor alone supplies the LDO. Figure 4 depicts the situation here, similar to the Phase II described above.

Based on Fig. 6, the internal voltage across the buffer capacitor is given by,

$$v_{C_2}(t) = V_{C_2}^{III} - \frac{1}{C_2} \int_0^{t_{sw}} I_L dt' \quad (32)$$

while the internal voltage across the supercapacitor remains fixed at,

$$v_{C_1}(t) = V_{C_1}^{III} \quad (33)$$

since it is disconnected from the circuit during this phase.

The external voltage across buffer capacitor and supercapacitor are respectively given by Eqs. (21, 22) listed earlier for phase II. Phase IV continues for a period of t_{sw} set by the microcontroller. Phase I then resumes to continue the cycle.

4. Comparison with experimental results for a 12V-5 V implementation

Using the above theoretical derivations, MATLAB codes were written to evaluate the time-varying capacitor voltages and currents across the four phases of circuit operation. Component values were selected to implement the 12V-5V regulator indicated in [8, 10]:

- (a) A capacitor of value 1.33F based on three series supercapacitors from Maxwell Technologies. ESR of these 2.5 V rated 4F capacitors is 100 mΩ each.
- (b) Switches implemented using solid state relays (SSR), PVN012 from International Rectifier; on resistance $r = 100$ mΩ
- (c) An LDO IC of the type MCP 1827ADJ
- (d) A simple microcontroller from the PIC family PIC16F684

Table 2: Approximate values for MATLAB calculations

V_2^{\min}	V_p	C_1	C_2	r_1	r_2	r	I_L	t_{sw}
5.4 V	12 V	1.33 F	4700 μF	300 mΩ	400 mΩ	100 mΩ	0.2 A	3 ms

Fig. 8(c) represents the external voltages of buffer capacitor and supercapacitor based on the evaluations in MATLAB for the actual practical values of 12V-5V configuration shown in Table 2. This MATLAB evaluations were based on the equation sets

(17, 18) (Phase I); (21, 22) (Phase II); (30, 31) (Phase III) and (21, 22) (Phase IV) shown in the above derivations. In this evaluation and analysis, the supercapacitor model used was the first order approximation with an ESR in series with capacitance value. Hence simulated results have only linear charge-discharge profiles. However as [27] indicates the actual supercapacitor model is more complex. Fig. 8(d) shows the actual scope waveforms of the buffer-capacitor and supercapacitor voltages during the four phases. Comparison between theoretical predictions and practical implementation based on Fig. 8 (c) and (d) is given in Table.3. According to Table 3 MATLAB theoretical predictions are verified in the actual circuit measurements. Furthermore the theoretical model predicts the buffer-capacitor waveform oscillates twice as fast as supercapacitor, and this is verified in the actual circuit measurements.

Table 3: Comparison between theoretical predictions and practical implementation of supercapacitor assisted LDO recirculation model

		Theoretical values			Experimental values		
		Starting voltage(V)	Final voltage (V)	Period (s)	Starting voltage(V)	Final voltage (V)	Period (s)
Supercapacitor $v_1(t)$ signal	During supercap charging	5.57	6.56	6.5	5.58	6.50	5.5
	During supercap discharging	6.42	5.44	6.5	6.26	5.29	5.5
Buffer-capacitor $v_2(t)$ signal	During supercap charging	6.39	5.40	6.5	6.21	5.25	5.5
	During supercap discharging	6.39	5.40	6.5	6.21	5.25	5.5

A more detailed plot of supercapacitor charging to discharging changeover point with transitions from phase I to phase II and then to phase III is shown in Fig. 8 (a). Corresponding MATLAB simulation of this transition is shown in Fig. 8 (b). A more detailed plot of supercapacitor discharging to charging changeover point with transitions from phase III to phase IV and then to phase I is shown in Fig. 8 (e). Corresponding MATLAB simulation is shown in Fig. 8 (f). The simulations and the actual waveforms show nearly similar transitions at the switchover points.

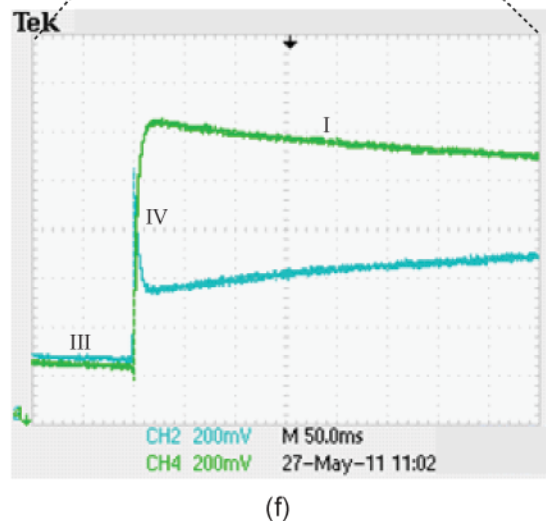
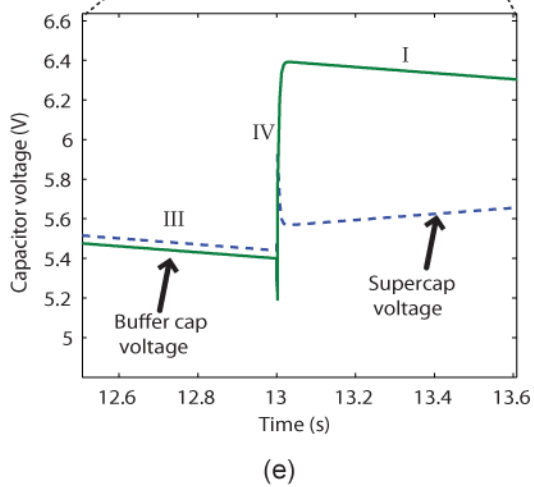
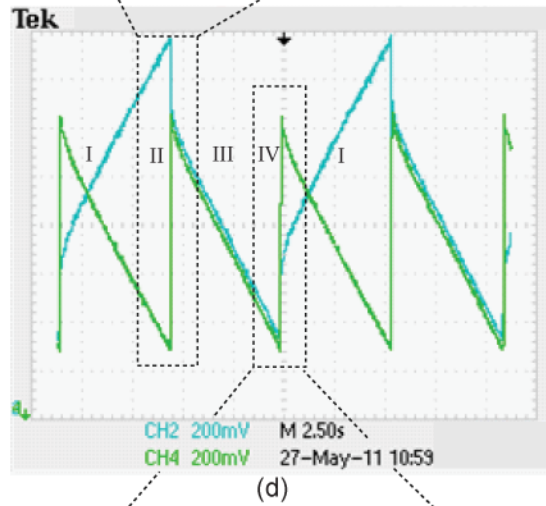
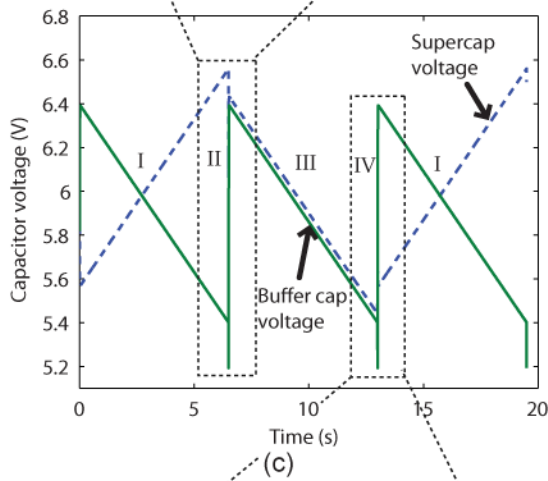
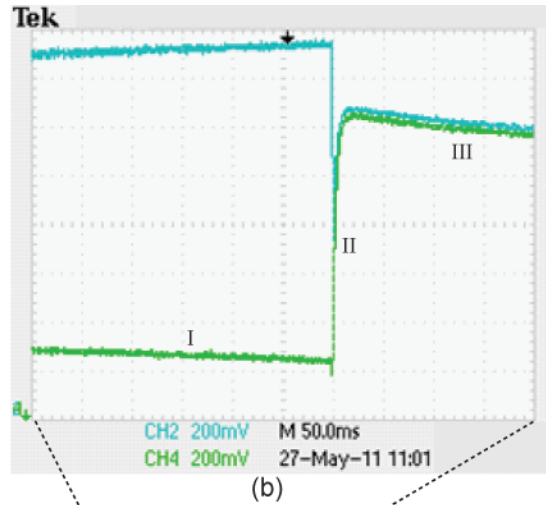
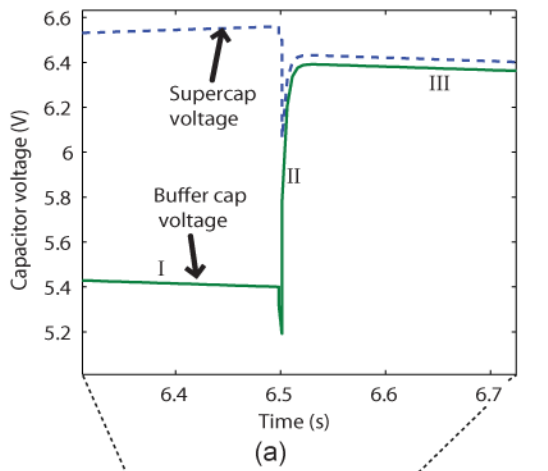


Fig.8: Supercapacitor voltage and buffer-capacitor voltage(LDO input voltage) variations during the circuit operation for 12V-5V supercapacitor assisted LDO model (a) Predicted charging-discharging transition (b) Oscillograph of the charging-discharging transition (c) Predicted waveforms for several cycles of operation (d) Oscillograph during circuit operation (e) Predicted discharging- charging transition (f) Oscillograph of the discharging- charging transition

Conclusion

This paper details a methodology to accurately predict the detailed behavior of a patented new supercapacitor enhanced linear DC-DC converter topology during its four phases and the associated transitions. The work details the behavior of the circuit particularly well during the phase transitions and the analytical results tally well with the practical waveforms observed in a 12V-5V converter, indicating that the technique can be further enhanced to evaluate the secondary losses as well as other configurations. The present work also confirms that several assumptions used in the simplification of the circuit behavior were reasonable and justifiable.

This work also demonstrates that the extracted datasheet parameters with Laplace transform based analytical approaches can accurately predict the detailed behavior of the new low frequency supercapacitor circulation technique for significant efficiency improvements in linear power supplies.

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