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Inkjet-Printed Narrow-Channel Mesoporous Oxide-Based n-Type TFTs and All-Oxide CMOS Electronics

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Oxide semiconductors are becoming the materials of choice for modern-day display industries. The performance of solution-processed oxide thin film transistors (TFTs) has also improved dramatically over the last few years. However, while oxygen deficient n-type semiconductors can demonstrate excellent electronic transport, the performance of p-type materials has remained unsatisfactory. Consequently, only the n-type semiconductor-based pseudo-complementary metal oxide semiconductor (CMOS) technology has attracted tremendous interests recently; yet, the high power dissipation remains a problem. Here, this work demonstrates all-oxide CMOS invertors with high-performance narrow-channel n-type TFTs, which can compensate for the limited carrier mobility of the p-type transistors. These n-type TFTs are fabricated with polymer-templated mesoporous In_2O_3 and with a device geometry that allows near-vertical current transport, thereby rendering the TFT channel lengths to be equal to the semiconductor film thickness (≈50 nm). Unprecedented On-current (1.02 mA μm^{-1}) and transconductance (950 $\mu S\ \mu m^{-1}$) are achieved. The CuO-based p-type TFTs also show a device mobility of no less than 0.5 $cm^2\ V^{-1}\ s^{-1}$. The printed all-oxide CMOS inverters are found to operate at very low supply voltages and demonstrate sharp transfer curves with maximum signal gain of 31 and low power dissipation of only 4 nW, at a supply voltage of 1 V.

1. Introduction

Owing to their superior electronic properties, high transparency, low processing costs, and long-term stability, oxide semiconductors are attracting serious commercial attention in recent times. In the high-end display industry, they have nearly replaced amorphous silicon, especially when it comes to high-definition or high-speed displays.[1–5] Significant developments have also been noted in the printed/flexible electronics domain, where the performance of solution-processed thin film transistors (TFTs) may now easily be compared with their vacuum deposited (e.g. sputtered or pulsed-laser deposited) counterparts.[6] Notably, these solution-processed devices are of high interest for a wide range of portable electronic or Internet of Things (IoT) related devices. However, any digital electronic component essentially requires complementary metal oxide semiconductor (CMOS) technology to ensure high noise immunity and low power consumption.[7] Unfortunately, it is only the oxygen deficient n-type oxide semiconductors, the performance of which nearly matches that of polycrystalline silicon, whereas the performance of the p-type materials is substantially lower in comparison. In fact, the problem associated with the absence of matching/comparable p-type oxide semiconductors range beyond the CMOS electronics to other p–n junction devices, for example, solar cells. Here, the transport properties of p-type oxide semiconductors are primarily limited by their highly localized oxygen *2p* orbitals in the valence band maximum (VBM), deep VBM, rigorous environmental and fabrication conditions and difficulties in high-quality film formation.[8–11]

It should also be noted that the examples of solution-processed p-type oxide semiconductors are essentially limited to NiO, Cu_xO, SnO, and delafossite-type $CuMO_2$ (M = Al and Cr).[8–11] Among these, Cu_xO has been the most promising candidate owing to its high theoretical Hall mobility, non-toxicity, suitable optical properties, and low cost.[12,13] Although it has been a well-known semiconductor even in the pre-silicon era, resurgent interest in Cu_2O has been spurred when Matsuzaki et al. demonstrated a Hall mobility of 90 $cm^2\ V^{-1}\ s^{-1}$ for epitaxial Cu_2O films on MgO in 2008.[14] The subsequent studies have reported about p-type Cu_xO deposition via sputtering,[14] pulsed laser deposition[15,16] and thermal oxidation techniques.[17] Solution-based fabrication techniques involving either spin/spray coating or inkjet printing have also been reported.[15,18–23] However, when it comes to Cu_xO-based TFTs, the typical process temperatures (≥400 °C) or reported operating voltages have always been very high.[24–26]

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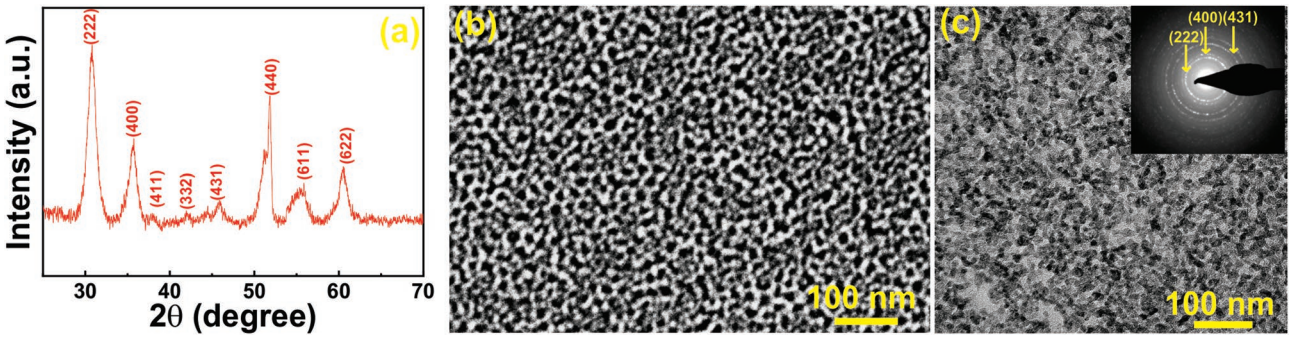

Figure 1. a) Grazing incidence X-ray diffraction pattern of a printed and annealed (350 °C for 1 h) mesoporous In_2O_3 film. b) Scanning electron microscopy image showing a cubic mesoporous structure. c) Transmission electron microscopy image of the printed and annealed In_2O_3 film showing well-connected pores and ligaments in the co-continuous structure. The inset shows selected area electron diffraction (SAED) pattern indicting that the pore walls are made of randomly oriented nanocrystals of In_2O_3.

In the present study, we aim at producing inkjet-printed, all-oxide CMOS electronics by combining high-performance mesoporous In_2O_3-based NMOS and Cu_xO-based PMOS TFTs at polymer substrate compatible process temperatures (350 °C). Initially, the process conditions of Cu_xO have been optimized, including the most suitable temperature, to obtain the best performance and a high device mobility (0.5 $cm^2\ V^{-1}\ s^{-1}$) that can be reproducibly achieved. Next, a suitable polymer structure-directing agent, polyisobutylene-b-poly(ethylene oxide), $(PIB)_{107}$–$(PEO)_{150}$,[27,28] has been used to prepare high surface-to-volume ratio (mesoporous) thin film of In_2O_3 at an identical process temperature of 350 °C to ensure facile single-step fabrication of the CMOS electronics. Mesoporous In_2O_3 has been chosen to create 3D bulk transistors with composite solid polymer electrolyte (CSPE)-based electrolytic gating. The idea was to achieve the highest possible NMOS performance to compensate for the lack of performance in the PMOS TFTs. In line with expectations, unprecedented maximum On-current and transconductance values of 1.02 mA μm^{-1} and 950 $\mu S\ \mu m^{-1}$, respectively, have been observed along with sub-nA Off currents, an On/Off ratio $>10^6$ and a subthreshold slope close to the theoretical Boltzmann limit. The Cu_xO PMOS TFTs are then combined with the mesoporous In_2O_3 NMOS devices to produce inkjet-printed and one-step processed CMOS inverters. The inverters have demonstrated a maximum signal gain of 31 at a low drive voltage of 1.25 V, as well as a very low power dissipation of only 4 nW, at 1 V supply voltage.

2. Results and Discussion

At first, the process parameters were optimized separately for high-performance NMOS and PMOS TFTs. As has previously been mentioned, the NMOS TFTs are designed to provide strong electrical performance in terms of current density, On–Off ratio and sharp subthreshold, which may allow for rapid switching and high signal gain in CMOS inverters. In order to achieve this, electrolyte-gated top-gate TFTs were fabricated with 3D mesoporous indium oxide channel. Similar mesoporous structures have earlier been achieved via inkjet printing of various binary and doped oxides.[29] Here, in order lower the process temperature to 350 °C while maintaining a large (in-plane) pore size and reasonable structural ordering, a polymer based on polyisobutylene (PIB) and poly(ethylene oxide) (PEO) was used. This amphiphilic structure-directing agent has a hydrophilic (PEO) and a hydrophobic (PIB) component. While the former facilitates the self-assembly and controls the ordering of the structure by forming the shell of the micelle, the latter determines the pore size by staying at the core. Note that it is also important to optimize the concentration of the metal oxide precursor and the polymer structure-directing agent in the printable ink to ensure formation of a co-continuous mesoporous structure over a large area. In the end, a small amount of DI water was added to the precursor ink solution to advance the hydrolysis process. The ink formulation was then printed and annealed over a broad temperature range, followed by structural, morphological and electrical characterization.

The structural characterization of the mesoporous In_2O_3 has been carried out using grazing incidence X-ray diffraction (GIXRD). To this end, the sample has been array printed over an area of $1 \times 1\ cm^2$ while maintaining the lateral dimensions of the printed rectangular area comparable to the actual device/TFT channel. The GIXRD result is shown in **Figure 1**a. The diffraction data matched with the Inorganic Crystal Structure Database (ICSD) reference pattern for indium oxide (JCPDS file number of 00-001-0929), thereby confirming the formation of phase-pure In_2O_3. Next, the mesoporous morphology was investigated using scanning electron microscopy (SEM). Figure 1b shows a cubic mesoporous structure, demonstrating the successful co-assembly via inkjet printing. Transmission electron microscopy (TEM) images taken from the mesoporous In_2O_3 layer (directed printed and annealed on 30 nm free-standing silicon nitride (Si_3N_4) grids, see Figure 1c) provide further insight into the nanoscale structure, pore connectivity and crystalline nature of the wall structure. The selected area electron diffraction (SAED) pattern shown in Figure 1c corroborates the formation of polycrystalline In_2O_3.

The structural and morphological characterization confirms the formation of a uniform and large-area co-continuous mesostructure via inkjet printing. In general, it offers a high surface-to-volume ratio and holds promise for applications in surface/interface-dominated functional devices, such as supercapacitors, gas sensors, field-effect transistors, fuel cells, photovoltaics, catalysis etc.[30–38]

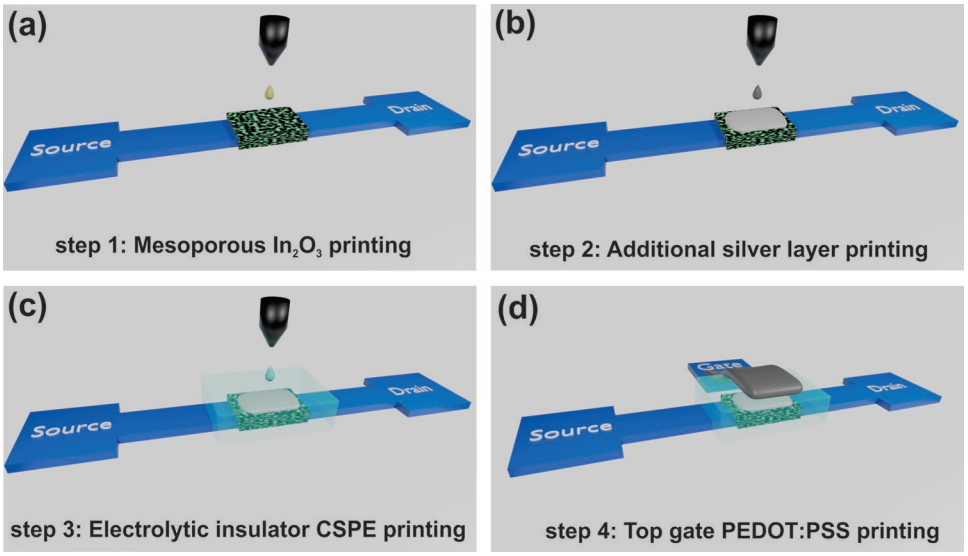

Figure 2. Schematic representation of the step-by-step fabrication procedure of top-gate TFTs with edge-FET device architecture. a) The first step involves printing of the semiconducting mesoporous In_2O_3 channel precursor followed by the chosen annealing routine. b) Next, the metal (silver) layer has been printed on top of the annealed mesoporous film. c) The composite solid polymer electrolyte has been printed then to completely cover the printed channel region. d) Finally, the organic metal poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS) ink has been printed as the top gate electrode.

In the present study, we examined the advantages of such a In_2O_3 mesoporous architecture in fabricating high-performance top-gate TFTs with edge-FET architecture. The non-standard device geometry involves printing of an additional metal layer (e.g., an inkjet-printed silver layer) on top of the mesoporous semiconductor channel.[21,29,39,40] The detailed step-by-step fabrication of the edge-FET NMOS devices is summarized in **Figure 2**a–d. The printed silver layer must maintain a spatial overlap with the source and drain electrodes (as shown in Figure 2b), thus reducing the effective channel lengths to only the thickness of the printed In_2O_3 film. Consequently, the drive current transport through the semiconductor material only takes place at the edges of the printed silver layer, and the TFT devices transform into two common-gate edge-FETs, connected in series. However, in the present case, the semiconductor material possesses a porous structure. Hence, the electrolyte may also penetrate underneath the silver layer, resulting in vertical transport, and a 3D bulk transistor device. Indeed, the capillary forces may ensure penetration of the electrolyte into the porous In_2O_3 mesostructure, however, the gating effects may not be sustainable for a substantial distance from the edge due to Coulombic screening of the identical ions. Note that the latter would oppose strong electric double layer formation.

Following the above-mentioned fabrication protocol of top-gate edge-FETs, mesoporous In_2O_3 channel TFTs were first fabricated with indium tin oxide (ITO) passive structures (drive electrodes) having 20 µm channel widths. Nevertheless, sufficiently large On-current on the order of 4 mA has been recorded for a low supply voltage of 1 V along with a high On–Off ratio of $>10^6$. A set of transfer characteristics of the printed edge-FETs on ITO passives is provided in the Supporting Information, Figure S1, Supporting Information. In fact, an artificial current saturation can be noted in all of these devices, already at $V_{GS} \geq 1.2$ V, which indicates that the channel conductance may actually be limited by the ITO passive structures. Therefore, in order to overcome the passive limited currents, metal (Pt) electrodes were used to fabricate the NMOS TFTs. It was indeed essential to shift to pure metal, as the PMOS TFTs cannot be fabricated onto n-type metallic oxide, ITO, as the passive structure (drive electrodes). The use of platinum as the passive structure (drive electrodes) has been found to resolve the passive limited current problems, which is quite evident from the observed On-current of about 10 mA (fivefold increase when compared to ITO passives) with a channel width of 10 µm and supply voltage of 1 V. The transfer and output characteristics of a representative mesoporous In_2O_3-based NMOS with edge-FET device geometry on platinum passives are shown in **Figure 3**a,b. Besides large current density, the recorded transfer characteristics also demonstrate low hysteresis, thereby confirming a conformal electrolytic insulator-semiconductor interface, free of charge traps. The averaged NMOS TFT performance parameters are summarized for both devices on ITO and Pt passives in Figure 3c–f. The maximum current density, $I_{D,ON}/W$ (1.02 mA µm^{-1}), and transconductance, g_m/W (950 µS µm^{-1}), at 1 V supply voltage are extremely large. However, they are to be treated as geometrical parameters, important for device design. As previously mentioned, there can be partial penetration of the electrolyte underneath the silver layer, thus making it a 3D channel TFT. Consequently, a direct comparison of these values with standard lateral long-channel TFTs, which may easily be an order of magnitude lower, should be avoided. Nonetheless, these edge-FET devices with extraordinary power density may well be suited to deliver large power outputs in applications where it is required, such as high-power switches, amplifiers, optoelectronics devices etc. to drive power from batteries in case of fully printed electronic circuits. Figure 3e,f compares the measured average subthreshold slope, S, and average threshold voltage, V_T, values of the edge-FET devices,

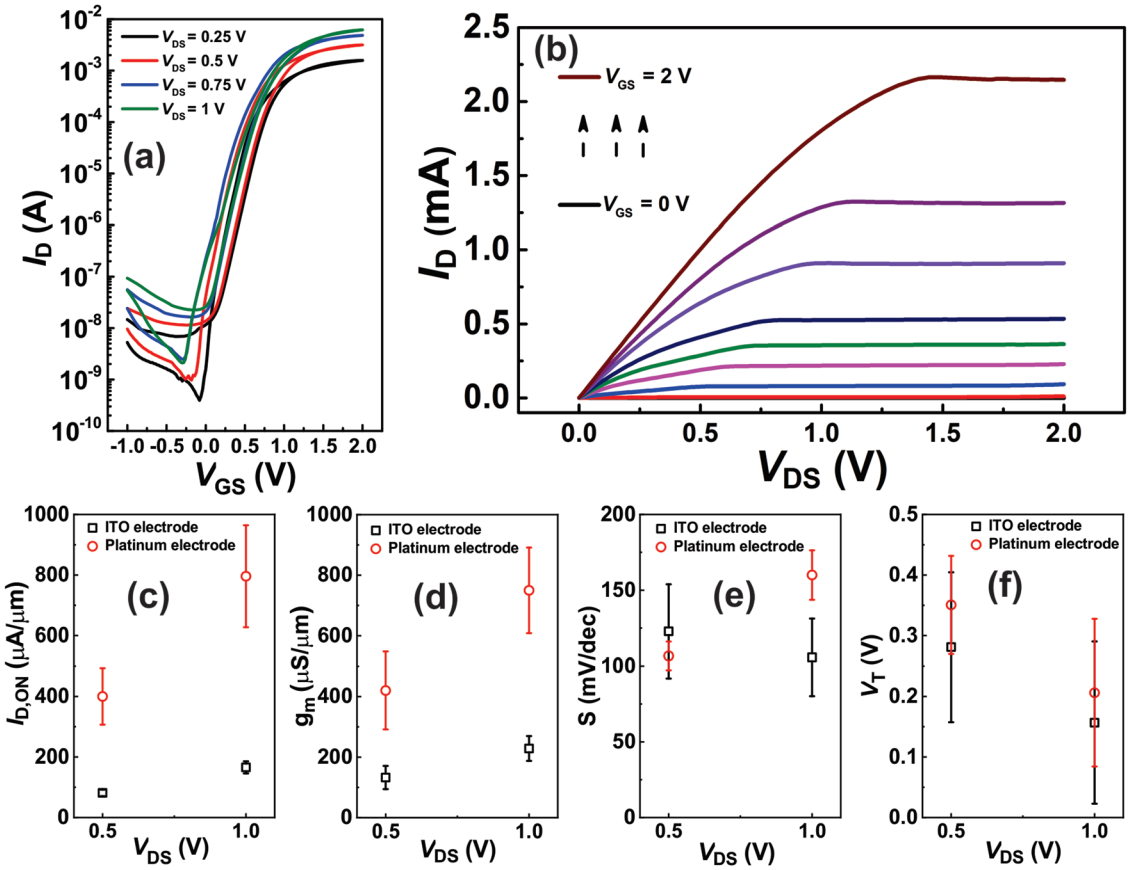

Figure 3. a) Typical transfer characteristics of the mesoporous In_2O_3-based edge-FET TFTs with additional printed silver layer on top of the semiconductor channel, demonstrating a simultaneous low Off current and a very high On-state conductance. The transfer characteristics are obtained by varying the drain voltage (V_{DS}) from 0.25 to 1 V, where the gate voltage is swept from –1 to 2 V. b) Output characteristics of the same device, showing a clear linear and saturation regime. c–f) Comparison of the extracted performance parameters ($I_{D,ON}/W$, g_m/W, S, and V_T) of TFTs fabricated on ITO and Pt electrodes.

fabricated on substrates with ITO and Pt electrodes. The calculated average subthreshold slope of the edge-FET devices (S_{ITO} = 123 mV dec^{-1} and S_{Pt} = 106 mV dec^{-1} at V_{DS} = 0.5 V) are found to be similar for the different passive structure (drive electrode) used. On the other hand, the average threshold voltage (Figure 3f) on ITO passives are estimated to be lower (V_T = 0.28 V) when compared to the edge-FETs on Pt (V_T = 0.35 V). This might be due to the larger channel widths used in case of the TFTs with ITO electrodes (W = 20 μm) as compared to the platinum ones (W = 10 μm). In addition, it may be noted that these TFTs typically show excellent environmental and time stability as has earlier been demonstrated in our previous study, where the In_2O_3 TFTs are found to maintain their strong device performance even after 8 months of air exposure.[18]

The objective of the study was to demonstrate inkjet-printed (high-performance) CMOS inverters, processed with a single annealing step at 350 °C, that is, compatible with polyimide substrates. Consequently, as a logical next step, Cu_xO-based top-gate PMOS TFTs were fabricated. Here, polyethylene glycol (PEG) was added to the Cu_xO precursor ink as viscosity modifier and to ensure uniform and smooth film formation. The structural characterization using GIXRD in **Figure 4**a summarizes the phases that are present when the precursor is annealed at different temperatures. Cu peaks were visible only at low temperatures (275 °C), in agreement with previous findings (existence of a pure copper phase at low temperature) for the synthesis via polyol method (with polyols, such as ethylene glycol, glycerol, etc., acting as reducing agents).[28] Up to 300 °C, the major phase observed was Cu_2O. In contrast, when the precursor was annealed at 350 °C, it was essentially a mixture of Cu_2O and CuO, with CuO being the primary phase. Next, the morphology of the printed and annealed (350 °C) Cu_xO film was studied. The PEG in the semiconducting ink helped to obtain crack-free and smooth Cu_xO films, see SEM image in Figure 4b. In addition, it helped to achieve the optimum viscosity for inkjet printing, while the solvent mixture with dissimilar boiling points reduced the coffee-ring pattern formation.

The transfer and output characteristics of a representative PMOS TFT, processed at 350 °C, are presented in Figure 4c,d. A set of identical TFTs are shown in Figure S2, Supporting Information. Figure S3, Supporting Information displays the performance of the PMOS TFTs processed at 275 and 300 °C, which was found to be weaker in comparison to the Cu_xO TFTs processed at 350 °C. It has been additionally supported by the performance parameters (transconductance and On/Off ratio) extracted from the PMOS TFTs at different temperatures (Figure S4, Supporting

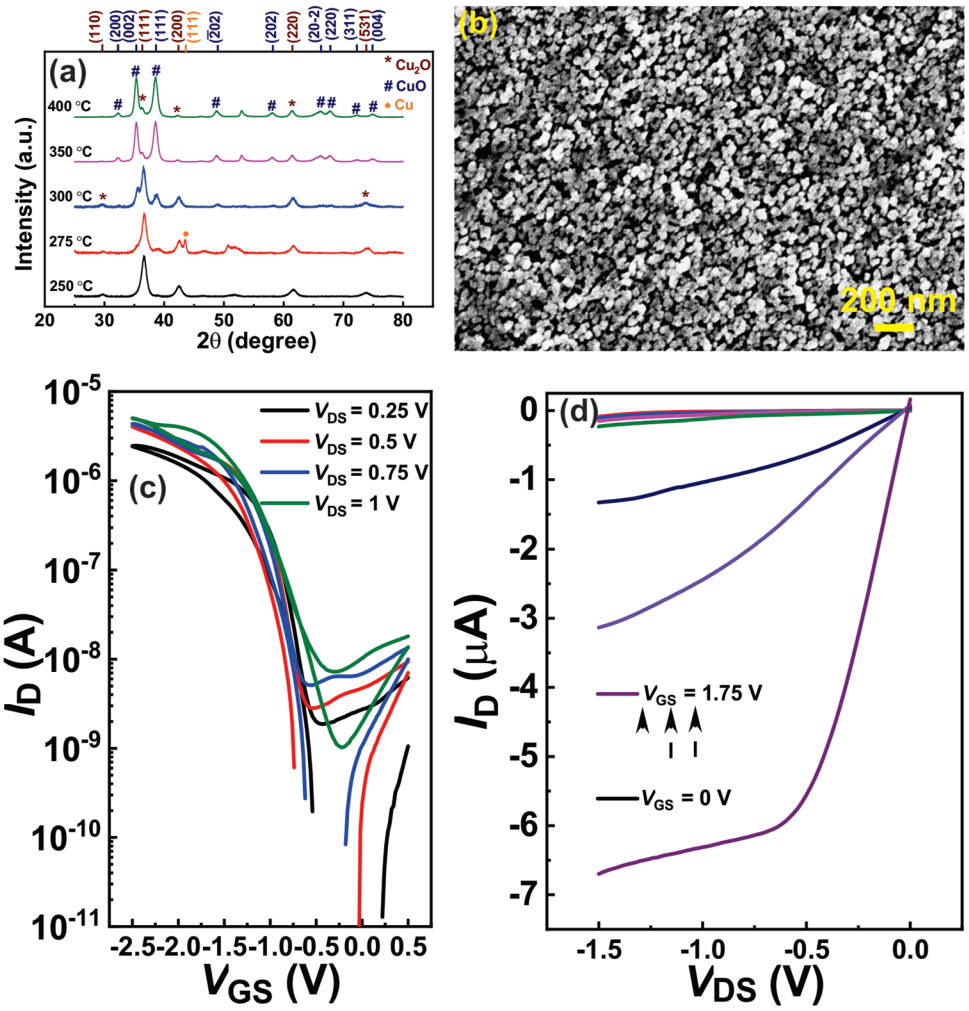

Figure 4. a) Grazing incidence X-ray diffraction patterns of p-type copper oxide semiconductors as a function of annealing temperature. A phase transformation from Cu_2O to CuO is observed with increasing annealing temperature. b) Scanning electron micrograph of the printed and annealed (350 °C, 1 h) Cu_xO film showing a uniform and crack-free morphology. c,d) Transfer and output characteristics of a representative electrolyte-gated Cu_xO-based top-gate PMOS device processed at 350 °C.

Information). Such temperature related improvement in electrical performance in Cu_xO TFTs has already been noted earlier. This may be due to the thermally driven increase in grain size, with a reduction in grain boundary area, associated scattering centers and deep trap states.[41–43] Notably, the output characteristics revealed a clear linear and saturation regime with an estimated hole mobility of 0.5 $cm^2\ V^{-1}\ s^{-1}$. The field-effect mobility was estimated using the following equation:

$$\mu_{sat} = \frac{2L}{WV_{DS}C_{DL}}\left(\frac{\partial\sqrt{I_{DS}}}{\partial V_{GS}}\right)^2 \quad (1)$$

where, I_{DS} is the drain current at saturation, V_T the threshold voltage, V_{DS} the drain voltage, V_{GS} the gate voltage, W the channel width (100 µm), L the channel length (10 µm) and C_{DL} represents the double-layer capacitance of the electrolytic insulator used in this study. A C_{DL} of 3.2 µF cm^{-2} was used for the mobility estimation.[26] The obtained device mobility was compared with available literature data of solution-processed oxide PMOS TFTs (see summary in Figure S5, Supporting Information and **Table 1**). The TFTs also demonstrated an average high On/Off ratio of 6.95×10^3 and an average subthreshold slope of 280 mV dec^{-1}.

Finally, the inkjet-printed CMOS inverters were fabricated by combining the NMOS edge-FETs and PMOS TFTs. Their fabrication procedure is detailed in Figure S6, Supporting Information. The circuit diagram of the CMOS logic inverters is shown in **Figure 5**a. Here, the PMOS and the NMOS TFTs serve as load and drive transistors, respectively. A single-step annealing at 350 °C was carried out after printing the semiconductors for PMOS and NMOS TFTs. The voltage-transfer characteristics (VTC) curves for different supply voltages ranging from 0.75 to 1.25 V are shown in Figure 5b. Notably, the voltage transition did not take place at half of the supply voltage ($V_{DD}/2$), as it is largely determined by the threshold voltage of the NMOS drive transistor, whose switching behavior is much sharper in comparison. Nonetheless, the fabricated CMOS inverters exhibited a clear and sharp signal inversion between the high and low logic states, with a calculated signal gain ($\eta = dV_{OUT}/dV_{IN}$) of 31

Table 1. A comprehensive review of recent publications on Cu_xO-based solution-processed PMOS TFTs alongside the performance of CMOS inverters (whenever reported).

Semiconductor	Fabrication method	Processing temperature [°C]	I_{on}/I_{off}	Device mobility [$cm^2 V^{-1} s^{-1}$]	Inverter gain	Reference
Cu_2O	Spray coating	275	4×10^3	10^{-2}	–	2013[44]
Cu_2O	Spin coating	700	10^2	0.16	–	2013[41]
CuO	Spin coating	500	10^4	10^{-2}	–	2016[42]
CuO	Spin coating	300	10^5	0.26	–	2015[7]
Cu_xO	Inkjet printing	400	10^3	0.22	21 at V_{DD} of 1.5 V	2015[26]
Cu_2O	Spin coating	600	10^4	0.29	–	2015[45]
CuO	Spin coating	250	5×10^4	0.32	–	2017[46]
Cu_xO	Spin coating	220	10^4	0.15	37 at V_{DD} of 60 V	2019[24]
Cu_xO doped with F_4TCNQ	Spin coating	300	10^3	0.25	50 at V_{DD} of 40 V	2020[25]
Cu_xO	Inkjet printing	350	7×10^3	0.5	31 at V_{DD} of 1.25 V	Present work

at a low supply voltage of 1.25 V (Figure 5c). Again, the voltage gain was found to increase linearly with the supply voltage (Figure 5d). Figure 5e shows the drive current, I_{DD}, flowing through the CMOS inverter, which is on the order of a few nA up to the supply voltage of 1 V and then sharply increases to few hundreds of nA for 1.25 V, predominantly due to the increase in the gate current (I_G). On the other hand, the calculated static power dissipation was only 4 nW at the supply voltage of 1 V (Figure 5f). Such low power dissipation along with low voltage operation and polymer substrate compatible processing temperature makes such all-oxide printed electronics technology suitable for battery compatible wearable electronics.

3. Conclusion

In summary, a soft-templating method was successfully adapted for inkjet printing of large-area mesoporous In_2O_3.

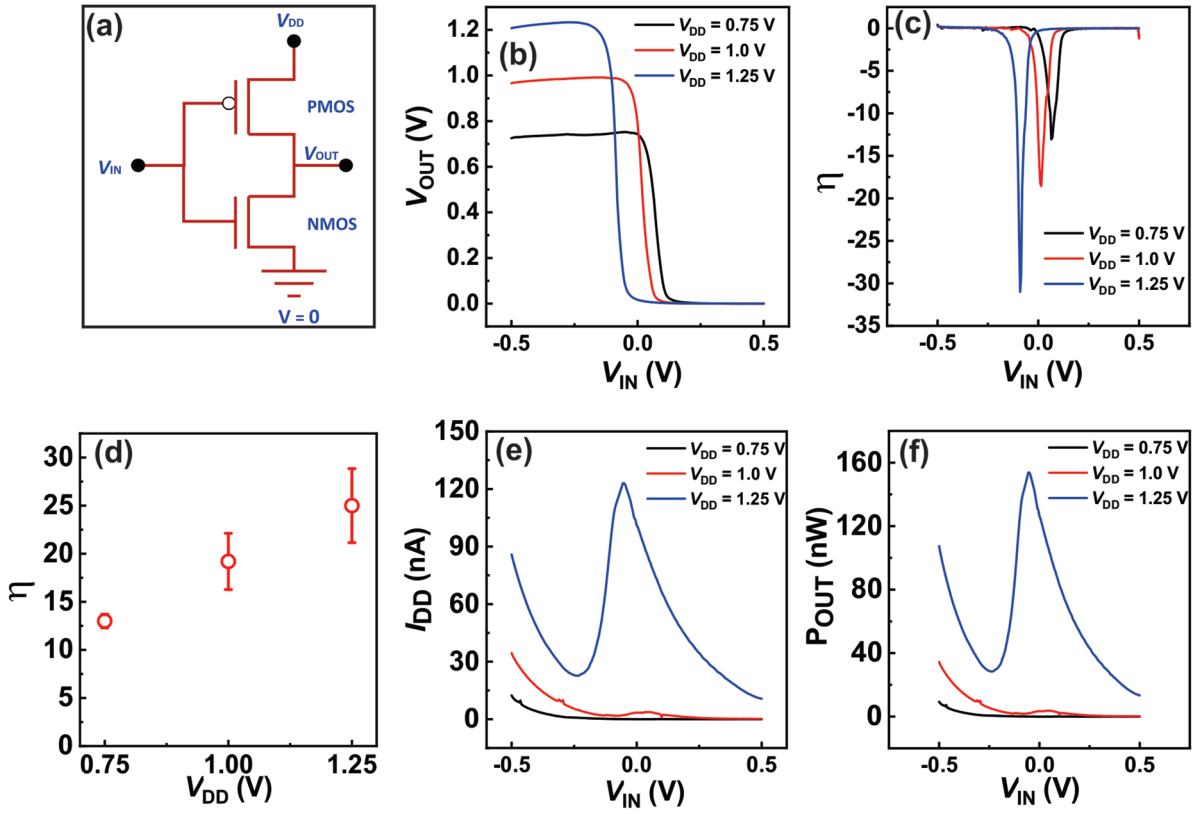

Figure 5. a) Schematic of a CMOS inverter. b) Voltage transfer characteristics (VTC) of an exemplary CMOS invertor for different supply voltages. c) Voltage gain ($\eta = dV_{OUT}/dV_{IN}$) of the CMOS invertor at different supply voltages. d) Voltage gain versus supply voltage from 0.75 to 1.25 V. e,f) Drive current and calculated power dissipation indicating a very low power dissipation of only 4 nW at a supply voltage of 1 V.

The cubic mesoporous layer was used to fabricate high-performance NMOS TFTs having narrow channel (≈50 nm) edge-FET device geometry with near vertical transport of drive currents. The recorded On-state conductance (1.02 mA μm^{-1}) and transconductance (950 $\mu S\ \mu m^{-1}$) values are notable, especially given that a high On/Off ratio $>10^6$ was maintained. On the other hand, an eco-friendly polyol method was used for the fabrication of low-temperature processed Cu_xO-based PMOS TFTs. The PMOS TFTs were tailored regarding annealing temperature and other parameters to obtain the desired copper oxide phase with a decent saturation mobility of 0.5 $cm^2\ V^{-1}\ s^{-1}$ and On/Off ratio of 6.95×10^3. Finally, the respective NMOS and PMOS TFTs were combined to fabricate single-step annealed (350 °C), all-oxide CMOS inverters with a signal gain of 31 and very low power dissipation of only 4 nW at a supply voltage of 1 V.

4. Experimental Section

Preparation of Printable Precursor Ink for n-Type Semiconducting Mesoporous In_2O_3: Indium chloride ($InCl_3$) and ethanol were purchased from Sigma-Aldrich and used as received. Polyisobutylene-b-poly(ethylene oxide), $(PIB)_{107}$–$(PEO)_{150}$, was used as structure-directing agent to produce mesoporous structures at low process temperatures (350 °C).[47] To prepare the indium chloride-based ink, at first 50 mg of $(PIB)_{107}$-$(PEO)_{150}$ was dissolved in 2.25 mL of ethanol and the solution was stirred at room temperature until the polymer was completely dissolved. Subsequently, 0.15 M indium chloride precursor was added and stirred for another 30 min. At the end, in order to facilitate the hydrolysis process, 0.15 mL of deionized water was added under continuous stirring and the resultant solution was stirred for another 30 min, until a clear and transparent ink was obtained.

Preparation of Printable Precursor Ink for p-Type Semiconducting Cu_xO: Copper nitrate hydrate ($Cu(NO_3)_2{\cdot}xH_2O$), poly(ethylene glycol) (PEG) with an average molecular weight of 200 g mol^{-1} and ethanol were purchased from Sigma-Aldrich and used as received without further purification. To prepare the precursor ink, 0.3 M copper nitrate hydrate was dissolved in deionized water, ethanol, and PEG maintaining a volume ratio of 0.6:0.25:0.15. The solution was then stirred at room temperature to obtain a homogeneous and clear solution. The addition of PEG helped in obtaining a crack-free smooth and continuous film of Cu_xO upon annealing. In addition, it also helped in optimizing the ink viscosity to suit the inkjet printing process (the ideal viscosity window for inkjet printing is 12–16 cP). On the other hand, the mixture of solvents with largely different boiling points and room temperature vapor pressures significantly reduced the tendency of coffee ring formation.

Electrolytic Insulator Ink Preparation: The electrolytic insulator, that is, the CSPE, was prepared through a two-step process. The CSPE consisted of four major components: A synthetic polymer, poly(vinyl alcohol) (PVA, 98% hydrolyzed, Sigma-Aldrich) with an average molecular weight of 13–23k g mol^{-1}, the plasticizer, propylene carbonate (PC, 99% anhydrous, Sigma-Aldrich), the solvent, dimethyl sulfoxide (DMSO, 99.99% anhydrous, Sigma-Aldrich), and a salt, lithium perchlorate ($LiClO_4$, 99.99%, Sigma-Aldrich). Initially, 0.3 g of PVA was dissolved in 5 mL of DMSO (solvent for PVA) under continuous stirring at 90 °C for 1 h. Simultaneously, 70 mg of $LiClO_4$ was dissolved in 1 mL of PC and the resultant solution was continuously stirred at room temperature for about 1 h. Finally, both solutions were combined at room temperature and stirred for 12 h.

Device Fabrication: The passive structures (source, drain and gate electrodes) were designed using UV-laser photolithography on a thermally oxidized Si wafer, with sputtered Cr (10 nm)/Pt (40 nm) layers. A positive photoresist S1813 was spin coated onto the wafer. The substrate was then exposed to a 390 nm light using a Heidelberg MPG 501 UV-laser writer. Subsequently, the substrates were developed with MF26A and chemically etched with aqua regia. Top-gate geometry was used for both NMOS edge-FET and PMOS devices. The aspect ratio of the PMOS device, that is, the W/L ratio, was maintained at 100 µm:10 µm in the entire study. In case of NMOS, the devices prepared on Pt electrodes were defined with a device dimension of W/L= 10 µm:50 µm. However, here the channel width was only of importance. With the edge-FET device geometry, the channel length would be reduced to the thickness of the printed mesoporous In_2O_3 layer, which was on the order of 50 nm. In addition, initially the NMOS devices were also fabricated on 180 nm sputtered ITO coated float glass with sheet resistance <10 Ω. The detailed procedure of the passive structure preparation on ITO substrates has been reported in earlier studies.[22,29] In case of ITO passives, a W/L ratio of 20 µm:50 µm was used. In case of CMOS invertors on Si wafer, Cr/Pt electrodes were used for both NMOS and PMOS TFTs. The process temperature of the NMOS and PMOS TFTs was maintained identical (350 °C) in this study. A preheating at 100 °C for 5 min preceded the annealing routine. To get n-type edge-FETs, an additional Ag layer was printed on top of the n-type semiconducting channel, which was subsequently annealed at 100 °C for 30 min. Next, 30 layers of the CSPE ink was array printed (with the interlayer delay of 15 s along with a platen temperature of 35 °C) on top of both the *p*- and *n*- type semiconducting channel layers and allowed to dry at room temperature for about 4–5 h to ensure complete removal of the excess solvent. Finally, a commercially available PEDOT:PSS ink was printed as the gate electrode as shown in Figure 2 and Figure S6, Supporting Information. All the printing steps involved in the device fabrication had been carried out using Dimatix 2831 desktop inkjet printer at room temperature unless otherwise noted.

Characterization of the Semiconducting Active Materials: The grazing incidence X-ray diffraction measurements were carried out using a Rigaku SmartLab diffractometer equipped with a Johansson $K\alpha_1$ monochromator and a Cu source (45 kV, 100 mA); a constant grazing incidence angle of 0.5° was maintained. The surface morphology of the printed and annealed active materials was characterized using a Zeiss Ultra 55 FESEM scanning electron microscope. The transmission electron micrographs were taken using a TITAN Themis microscope operated at 300 kV; the mesoporous In_2O_3 layer was printed and annealed directly onto 30 nm free-standing silicon nitride window TEM grids (Agar Scientific).

Electrical Characterization: The electrical measurements of the inkjet-printed electrolyte-gated TFTs and the invertor devices were performed at room temperature and in ambient conditions using a Keysight B1500A semiconductor device parameter analyzer connected to a MicroXact SPS1000-15 probe station.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

complementary metal oxide semiconductor electronics, inkjet printing, oxide electronics, printed electronics, thin film transistors

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[1] S. K. Garlapati, M. Divya, B. Breitung, R. Kruk, H. Hahn, S. Dasgupta, *Adv. Funct. Mater.* **2018**, *30*, 1707600.
[2] E. Fortunato, P. Barquinha, R. Martins, *Adv. Mater.* **2012**, *24*, 2945.
[3] Q. W. F. Shao, *J. Phys. D: Appl. Phys.* **2021**, *52*, 143002.
[4] S. J. Kim, S. Yoon, H. J. Kim, *Jpn. J. Appl. Phys.* **2014**, *53*, 02BA02.
[5] S. Chung, K. Cho, T. Lee, *Adv. Sci.* **2019**, *6*, 1801445.
[6] R. Martins, A. Nathan, R. Barros, L. Pereira, P. Barquinha, N. Correia, R. Costa, A. Ahnood, I. Ferreira, E. Fortunato, *Adv. Mater.* **2011**, *23*, 4491.
[7] A. Liu, G. Liu, H. Zhu, H. Song, B. Shin, E. Fortunato, R. Martins, F. Shan, *Adv. Funct. Mater.* **2015**, *25*, 7180.
[8] A. Liu, G. Liu, H. Zhu, B. Shin, E. Fortunato, R. Martins, F. Shan, *Appl. Phys. Lett.* **2016**, *108*, 233506.
[9] S. Li, X. Zhang, P. Zhang, X. Sun, H. Zheng, W. Zhang, *Nano Res. Lett.* **2018**, *13*, 259.
[10] A. Liu, Y. Meng, H. Zhu, Y. Y. Noh, G. Liu, F. Shan, *ACS Appl. Mater. Interfaces* **2018**, *10*, 25841.
[11] Z. Wang, P. K. Nayak, J. A. Caraveo-Frescas, H. N. Alshareef, *Adv. Mater.* **2016**, *28*, 3831.
[12] H. A. Al-Jawhari, *Mater. Sci. Semicond. Process.* **2015**, *40*, 241.
[13] S. Nandy, A. Banerjee, E. Fortunato, R. Martins, *Rev. Adv. Sci. Eng.* **2013**, *2*, 273.
[14] K. Matsuzaki, K. Nomura, H. Yanagi, T. Kamiya, M. Hirano, H. Hosono, *Appl. Phys. Lett.* **2008**, *93*, 202107.
[15] S. Y. Sung, S. Y. Kim, K. M. Jo, J. H. Lee, J. J. Kim, S. G. Kim, K. H. Chai, S. J. Pearton, D. P. Norton, Y. W. Heo, *Appl. Phys. Lett.* **2010**, *97*, 2008.
[16] E. Fortunato, V. Figueiredo, P. Barquinha, E. Elamurugu, R. Barros, G. Goṇalves, S. H. K. Park, C. S. Hwang, R. Martins, *Appl. Phys. Lett.* **2010**, *96*, 2008.
[17] V. Figueiredo, J. V. Pinto, J. Deuermeier, R. Barros, E. Alves, R. Martins, E. Fortunato, *IEEE/OSA J. Disp. Technol.* **2013**, *9*, 735.
[18] N. Cherukupally, M. Divya, S. Dasgupta, *Adv. Electron. Mater.* **2020**, *6*, 2000788.
[19] S. Dasgupta, R. Kruk, N. Mechau, H. Hahn, *ACS Nano* **2011**, *5*, 9628.
[20] S. Dasgupta, B. Das, Q. Li, D. Wang, T. T. Baby, S. Indris, M. Knapp, H. Ehrenberg, K. Fink, R. Kruk, H. Hahn, *Adv. Funct. Mater.* **2016**, *26*, 7507.
[21] S. K. Behera, N. Devabharathi, J. R. Pradhan, S. K. Mondal, S. Dasgupta, *Adv. Electron. Mater.* **2019**, *5*, 1900401.
[22] S. K. Mondal, N. Devabharathi, S. Dasgupta, *Nanotechnology* **2019**, *30*, 435201.
[23] S. Y. Kim, C. H. Ahn, J. H. Lee, Y. H. Kwon, S. Hwang, J. Y. Lee, H. K. Cho, *ACS Appl. Mater. Interfaces* **2013**, *5*, 2417.
[24] A. Liu, H. Zhu, Y. Y. Noh, *ACS Appl. Mater. Interfaces* **2019**, *11*, 33157.
[25] A. Liu, H. Zhu, Y. Noh, *Adv. Funct. Mater.* **2020**, *30*, 2002625.
[26] S. K. Garlapati, T. T. Baby, S. Dehm, M. Hammad, V. S. K. Chakravadhanula, R. Kruk, H. Hahn, S. Dasgupta, *Small* **2015**, *11*, 3591.
[27] C. Weidmann, K. Brezesinski, C. Suchomski, K. Tropp, N. Grosser, J. Haetge, B. M. Smarsly, T. Brezesinski, *Chem. Mater.* **2012**, *24*, 486.
[28] E. Celik, P. Cop, R. S. Negi, A. Mazilkin, Y. Ma, P. Klement, J. Schörmann, S. Chatterjee, T. Brezesinski, M. T. Elm, *ACS Nano* **2022**, *16*, 3182.
[29] N. Devabharathi, S. K. Mondal, S. Dasgupta, *Nanoscale* **2019**, *11*, 13731.
[30] Y. Zhai, Y. Dou, D. Zhao, P. F. Fulvio, R. T. Mayes, S. Dai, *Adv. Mater.* **2011**, *23*, 4828.
[31] K. Liu, H. Fu, K. Shi, F. Xiao, L. Jing, B. Xin, *J. Phys. Chem. B* **2005**, *109*, 18719.
[32] N. Devabharathi, R. Parasuraman, A. M. Umarji, S. Dasgupta, *J. Alloys Compd.* **2021**, *865*, 158815.
[33] N. Devabharathi, A. M. Umarji, S. Dasgupta, *ACS Appl. Mater. Interfaces* **2020**, *12*, 57207.
[34] S. H. Joo, S. J. Choi, I. Oh, J. Kwak, *Nature* **2001**, *412*, 169.
[35] W. Chu, S. Chiang, J. Li, S. Kuo, *RSC Adv.* **2014**, *4*, 784.
[36] M. M. Mirhosseini, V. Haddadi-Asl, S. S. Zargarian, *RSC Adv.* **2016**, *6*, 80564.
[37] N. T. Vo, A. K. Patra, D. Kim, *Phys. Chem. Chem. Phys.* **2017**, *19*, 1937.
[38] E. Celik, Y. Ma, T. Brezesinski, M. T. Elm, *Phys. Chem. Chem. Phys.* **2021**, *23*, 10706.
[39] S. K. Mondal, A. Biswas, J. R. Pradhan, S. Dasgupta, *Small Methods* **2021**, *5*, 2100634.
[40] N. Devabharathi, S. K. Mondal, J. R. Pradhan, S. Dasgupta, *IEEE Electron Devices Technol. Manuf.* **2020**, *15*, 3.
[41] S. Y. Kim, C. H. Ahn, J. H. Lee, Y. H. Kwon, S. Hwang, J. Y. Lee, H. K. Cho, *ACS Appl. Mater. Interfaces* **2013**, *5*, 2417.
[42] J. Jang, S. Chung, H. Kang, V. Subramanian, *Thin Solid Films* **2016**, *600*, 157.
[43] J. Yu, G. Liu, A. Liu, Y. Meng, B. Shin, *J. Mater. Chem. C* **2015**, *3*, 9509.
[44] P. Pattanasattayavong, S. Thomas, G. Adamopoulos, M. A. Mclachlan, D. Thomas, M. A. Mclachlan, T. D. Anthopoulos, *Appl. Phys. Lett.* **2013**, *102*, 163505.
[45] J. Yu, G. Liu, A. Liu, Y. Meng, B. Shin, F. Shan, *J. Mater. Chem. C* **2015**, *3*, 9509.
[46] A. Liu, S. Nie, G. Liu, H. Zhu, B. Shin, E. Fortunato, R. Martins, *J. Mater. Chem. C* **2017**, *5*, 2524.
[47] T. von Graberg, P. Hartmann, A. Rein, S. Gross, B. Seelandt, C. Röger, R. Zieba, A. Traut, M. Wark, J. Janek, B. M. Smarsly, *Sci. Technol. Adv. Mater.* **2011**, *12*, 025005.

