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New Control Algorithm for Single-Phase Series Active Power Filter

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This paper presents a single-phase Series Active Power Filter (Series APF) for mitigation of the load voltage harmonic content, while maintaining the voltage on the DC side regulated without the support of a voltage source. The proposed series active power filter control algorithm eliminates the additional voltage source to regulate the DC voltage, and with the adopted topology it is not used a coupling transformer to interface the series active power filter with the electrical power grid. The paper describes the control strategy which encapsulates the grid synchronization scheme, the compensation voltage calculation, the damping algorithm and the dead-time compensation. The topology and control strategy of the series active power filter have been evaluated in simulation software and simulations results are presented. Experimental results, obtained with a developed laboratorial prototype, validate the theoretical assumptions, and are within the harmonic spectrum limits imposed by the international recommendations of the IEEE-519 Standard.

1. Introduction

The dissemination on a large scale of non-linear loads, in recent times, has made trivial their presence and use in industry and domestic households. This, plus the fact that this type of electrical loads cause

distortion on the current waveform, which is harmful for the Power Quality of the electrical power grid, has led to high energy and monetary losses, for all parts involved in the power distribution system and the consumers [1][2].

To deal and overcome these problems, studies of Power Quality problems and development of solutions to mitigate their impact on the electrical power grid have been done over the years. Perhaps, the most well-known solutions regarding the transmission systems are the Flexible AC Transmission System (FACTS) devices, which can actively control some of the transmission system parameters, such as current, voltage, power and impedance [3].

In the same way, the distribution systems have their own solutions, known as Custom Power devices, that act in a similar manner as the FACTS devices, but have a lower rated power, which enables them to compensate Power Quality problems that require for semiconductors with a higher switching frequency rating [4]. These devices enable the providers of electrical power to take a differentiated approach to their clients, regarding the quality and reliability of the delivered power. This allows the customers to choose the Power Quality of the electricity they use, while, hopefully, enhancing the overall Power Quality of the distribution system.

Custom Power devices use power electronics and switching devices (semiconductors) to enhance the quality of the supplied power, when such is required by the customer [2]. Among the Custom Power devices there is a class of conditioners known as Active Power Filters

(APF), where some are connected in series with the power distributing system (e.g., Series Active Power Filter), while others are connected in parallel (e.g., Shunt Active Power Filter), or even in a series-parallel combination, compounding an all new conditioner (e.g., Unified Power Quality Conditioner - UPQC) [1][5].

Although, initially these types of conditioners were developed to deal only with voltage and current harmonic distortion [6][7], the continued research over the years on Active Power Filters has led to new and improved control algorithms and power converter topologies [8][9][10], that made them able to deal with an increasingly larger number of Power Quality problems, as they became optimized in size and cost effectiveness. However there are some issues regarding the hardware and control of the Series APF, like the DC bus voltage regulation, which in some literature requires the usage of an additional power converter [11][12][13], or the requirement of a transformer to connect the Active Power Filter to the electric grid [14][15].

This paper describes the implementation of a Series Active Power Filter without a voltage source on the DC bus of the Voltage Source Inverter (VSI), and also without a coupling transformer to interface the active filter with the electrical power grid. The ultimate goal of this device is to compensate the voltage harmonic distortion, while maintaining the voltage on the DC bus (V_{DC}) regulated, using a single electronic converter to perform the aforementioned tasks.

2. Series Active Power Filter Topology

The Series Active Power Filter is connected in series with the electrical power grid, synthesizing a voltage that is in phase opposition to the harmonic content of the source voltage, to ensure that the waveform of the load voltage is close to a sinusoidal waveform. The adopted topology for the Series Active Power Filter consists in a single-phase H-bridge converter with a capacitor in the DC bus, which is connected in series with the electrical power grid by means of a passive LC output filter, as it is shown in **Figure 1**. A key feature of this topology is the fact that it does not have a coupling transformer to interface the Series Active Power Filter with the electrical power grid. Usually, the coupling transformers have a rated frequency of 50 Hz, which makes the overall system bigger, heavier and more expensive; and also, they have to operate with a high harmonic content, which translates into high energy losses. So, by excluding the coupling transformer, the overall energy losses and size of the Series APF diminishes.

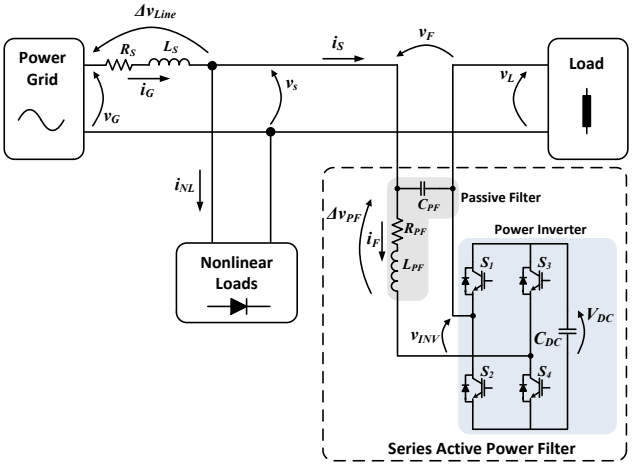

Figure 1. Schematic of the Series Active Power Filter in the electrical power system.

3. Steady State Analysis

The ideal Series Active Power Filter acts as a voltage source, and it does not require drawing active power from the electrical power grid to work properly ($P_F = 0$, where P_F is the active power at the Series APF) [16]. With this in mind, it is possible to construct a simplified schematic for the Series APF, as it is exhibited in the model of **Figure 2**.

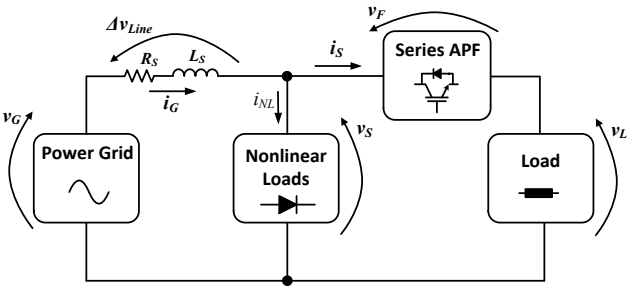

Figure 2. Simplified model of an electrical power system with a Series Active Power filter.

Through the model of **Figure 2**, it is possible to establish equation (1), which relates the electrical power grid voltage, v_G, with the line impedance voltage drop, Δv_{Line}, and the source voltage, v_S.

$$v_S(t) = v_G(t) - \Delta v_{Line}(t) \tag{1}$$

Assuming that v_G is purely sinusoidal and that the current i_G, has a distorted waveform, then v_S also has a distorted waveform, since a distorted current, i_{NL}, flows through the line impedance and causes the distorted voltage drop Δv_{Line}. This point becomes particularly evident in equation (4), when v_G and Δv_{Line} in equation (1) are substituted by equations (2) and (3), respectively.

$$v_G(t) = V_G \sin(\omega_1 t) \tag{2}$$

$$\Delta v_{Line}(t) = L_S \frac{d\, i_G(t)}{dt} + R_S\, i_G(t)$$

$$\Delta v_{Line}(t) = L_S \frac{d\left[\sum_{k=1}^{\infty} I_{G_k} \sin(\omega_k t)\right]}{dt} + R_S \sum_{k=1}^{\infty} I_{G_k} \sin(\omega_k t),\ k \in \mathrm{N} \tag{3}$$

$$\Delta v_{Line}(t) = L_S \sum_{k=1}^{\infty} I_{G_k} \cos(\omega_k t) + R_S \sum_{k=1}^{\infty} I_{G_k} \sin(\omega_k t),\ k \in \mathrm{N}$$

$$v_S(t) = V_G \sin(\omega_1 t) - \left[L_S \sum_{k=1}^{\infty} I_{G_k} \cos(\omega_k t) + R_S \sum_{k=1}^{\infty} I_{G_k} \sin(\omega_k t) \right],\ k \in \mathrm{N} \tag{4}$$

In this case, the Series APF must produce a voltage that should counteract the effects of the distorted voltage drop Δv_{Line}. The voltage produced by the active filter (v_F) can be calculated by removing the fundamental component (v_{S1}) from the voltage v_S, and it must be equal in every aspect to the harmonic content of Δv_{Line} except in its phase which must be opposite. This will make the voltage supplied to the load sinusoidal.

$$v_F(t) = v_S(t) - v_{S1}(t) \tag{5}$$

$$v_L(t) = v_{S1}(t) \tag{6}$$

In a real power system, the Series APF does not behave like an ideal voltage source and has power losses associated with its operation. This means that the Series APF requires a certain amount of active power to work properly ($P_F \neq 0$), and that must be drawn from the electrical power grid. Therefore it is necessary to produce a voltage (v_{REG}) in phase with v_{S1} to maintain the voltage on the DC bus (V_{DC}) regulated. As the Series APF is connected in series with the electrical power grid, the load current flows through the output passive filter causing a voltage drop (Δv_{PF}) as it is discernible from **Figure 1**. This

voltage drop must be compensated, and once this value is calculated through equation (7), it must be added to the compensation voltage, so that it can be synthesized by the Series APF power inverter.

$$\Delta v_{PF}(t) = L_{PF}\frac{di_F(t)}{dt} + R_{PF}\, i_F(t) \tag{7}$$

4. Control Strategy

The control strategy of the proposed Series APF can be divided into four parts, as it is shown in **Figure 3**. The first part refers to the voltage reference synthesis, which is based upon a single-phase digital Phase-Locked Loop algorithm: the Enhanced PLL (EPLL) circuit [17]. This approach features a phase and amplitude lock, being both estimated directly. It also shows immunity to small variations in its internal structure and to noise that might exist in the input signal [17][18][19].

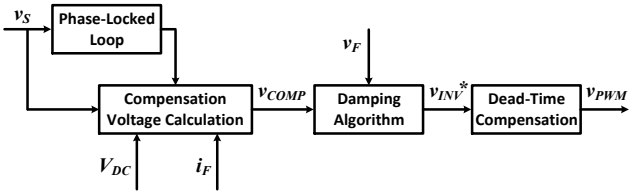

Figure 3. Global control scheme of the Series Active Power Filter.

The second part of the implemented control focuses upon the calculation of the compensation voltages. This approach was first mentioned in [20] and it is composed by a loop that calculates the voltage for harmonic compensation and DC bus regulation. Additionally, it was added to the compensation voltage calculation, a section to compensate the voltage drop on the output passive filter.

The third part of the control strategy consists of a damping algorithm used to minimize the resonance effects caused by the LC output passive filter and the control loop.

Finally, the fourth part refers to a scheme used to minimize the effects of dead-time introduced on the rising edges of the power semiconductors drive signals in order to prevent short-circuits.

4.1. Enhanced Phase-Locked Loop

The adopted Phase-Locked Loop (PLL) algorithm is based upon an Enhanced Phase-Locked Loop (EPLL) strategy [17][18][21], which differs from other phase locking synchronizing schemes as it exhibits a control loop to determine the amplitude of the output signal. This feature allows the EPLL to extract the fundamental component of the input signal, as opposed to other PLL schemes in which the output signal has only the frequency and phase angle of the input signal [21]. **Figure 4** shows the block diagram of the EPLL.

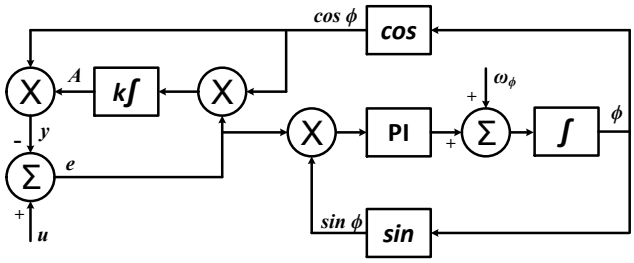

Figure 4. Block diagram of the single-phase Enhanced Phase-Locked Loop (EPLL).

The error signal (e) represents the deviation between the input (u) and output (y) signals, and in steady-state the average value of e must be zero, meaning that the EPLL circuit is stabilized and y is correctly tracking the input signal u. This is achieved by feeding the error signal into a PI controller, and its output is integrated in order to

obtain the phase angle (Φ). This angle also contains the phase difference between the input and output signals, and once this difference is close to zero, the phase angle of fundamental frequency is reached, y is synchronized with u, and the output signal should correspond to the fundamental component of the input signal.

As it was mentioned before, besides phase locking, the EPLL circuit also locks the amplitude (A) of the output signal, which is a result of the external control loop.

4.2. Compensation voltage calculation

The compensation voltage that must be produced by the Series APF power inverter (v_{COMP}) is made of three components (v_H, v_{REG} and v_{PF}), where v_H holds the harmonic voltage to be compensated, v_{REG} has the necessary voltage to regulate the DC bus, and v_{PF} features the required voltage to compensate the voltage drop in the output passive filter. In **Figure 5** is presented the block diagram with the scheme of the compensation voltage calculation.

$$v_{COMP}(t) = v_H(t) + v_{REG}(t) + v_{PF}(t) \tag{8}$$

Taking into account the measured values of the source and DC bus voltages (respectively v_S and V_{DC}), the control strategy proceeds to compare them with their reference values, v_{S1} and V_{DC}^*, which in the case of v_{S1} is the output sinusoidal waveform derived from the PLL circuit, and for V_{DC}^* is defined by a constant value [22][23][24]. The error obtained from the comparison of the DC bus voltage is than inserted in a PI controller and later multiplied by a unitary sine wave

(*pll*) in phase with v_{S1} (provided by the PLL circuit). The final result is the v_{REG} component, according to equation (11).

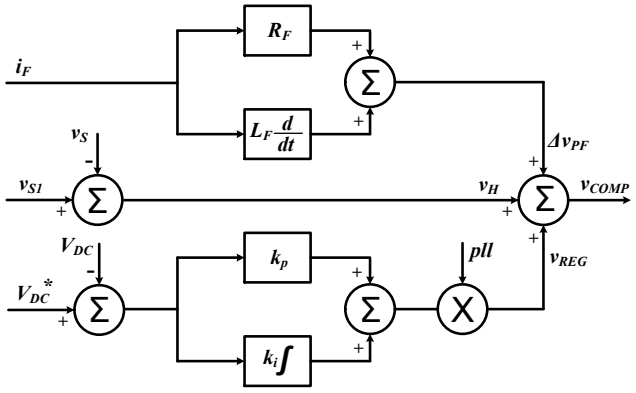

Figure 5. Compensation voltage calculation block diagram.

$$v_H(t) = v_{S1}(t) - v_S(t) \tag{9}$$

$$\Delta V_{DC}(t) = V_{DC}^{*}(t) - V_{DC}(t) \tag{10}$$

$$v_{REG}(t) = pll\left[k_p\ \Delta V_{DC}(t) + k_i \int \Delta V_{DC}(t)\,dt\right] \tag{11}$$

In the case of the passive filter voltage drop ($\Delta v_{PF} = v_{LPF} + v_{RPF}$), the compensation voltage, v_{PF}, is calculated recurring to the measured current that flows through the passive filter (i_F), and in accordance with what is described in equation (12).

$$v_{PF}(t) = v_{LPF}(t) + v_{RPF}(t) = L_{PF}\frac{di_F(t)}{dt} + R_{PF}\ i_F(t) \tag{12}$$

Finally, the total compensation voltage, v_{COMP}, which corresponds to the voltage that must be produced by the series APF power inverter, is obtained by adding (9), (11) and (12), as it is presented in equation (13).

$$v_{COMP}(t) = v_{S1}(t) - v_S(t) + pll\left[k_p\ \Delta V_{DC}(t) + k_i \int \Delta V_{DC}(t)\,dt\right] + L_{PF}\frac{di_F(t)}{dt} + R_{PF}\ i_F(t) \tag{13}$$

4.3. Damping Algorithm

The damping algorithm behavior, based upon [25] [26], is comparable to a virtual resistance that is used to mitigate the high frequency components originated by semiconductor switching and the resonant oscillations that exist in the electrical power grid. The virtual resistance can replace the physical resistance from the coupling filter or, it can work together with a physical resistance, allowing a more subtle control of the damping ratio. **Figure 6** shows in more detail how the last two sections of the control scheme interact with each other.

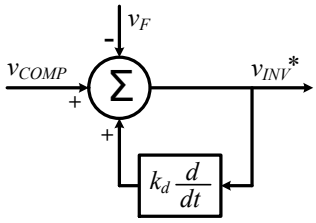

Figure 6. Damping algorithm model.

The input signal of the damping algorithm, v_{COMP}, is added with the derivative of the output signal v_{INV}^*, which is the end result of the compensation voltage calculation.

$$v_{INV}^*(t) = v_{COMP}(t) + \left[k_d \frac{dv_{INV}^*(t)}{dt} \right] - v_F(t) \tag{14}$$

The adopted damping algorithm can ultimately be seen as an evolution of the usual inverter feedback loop that uses the measured output signal of the Series APF as a way to properly follow the reference.

4.4. Dead-time Compensation

It is usual to introduce a delay time, T_d, which delays the rising edges of the drive signals of the power semiconductors in order to

prevent short circuits during the inverter operation [27]. This is one of the elements responsible for errors in the inverter output voltage, such as, during T_d, none of the switching devices is active, and the inverter output voltage becomes impossible to control through the drive signals, being determined by the load conditions, more precisely by the current flow direction. This point is important because, although the load conditions may be altered, the average voltage deviation (Δv) due to the time delay will always oppose the direction of the current flowing to the load [28].

Compensation of the dead-time effect can be accomplished by monitoring the direction of the current flow with a method described in [29]. This method proposes to change the voltage reference whenever the polarity of the current changes, which requires an accurate estimation of Δv, which besides T_d and V_{DC}, is also related to the modulation index, M, the switching frequency, f_S, and the knowledge about the direction of the current. Ultimately, the signals sent to the IGBTs gates are calculated through equations (15) and (16), which are based on the previously stated principles.

$$\Delta v = M\ f_S\ T_d\ V_{DC} \tag{15}$$

$$v_{pwm} = \begin{cases} v_{INV}^{*} + \Delta v, & i_F > 0 \\ v_{INV}^{*} - \Delta v, & i_F \le 0 \end{cases} \tag{16}$$

5. Simulations

In order to verify and validate the theoretical assumptions regarding the operation of the Series APF and of its control strategy,

there were conducted simulations of the entire system using the software PSIM. The simulated system is similar to the model exhibited in **Figure 1**, and the control strategy was implemented with the assistance of a PSIM feature that allows implementation of C/C++ code, thus making the simulated control system very close to the one that was later implemented on a real DSP platform.

The Series APF was conceived to operate in a 230 V single-phase voltage system, with the line impedance being modeled through a RL circuit connected in series with the whole system. Three loads were also added to the simulation model. One of them is a nonlinear load, composed by a full-bridge rectifier with a RC load at the DC side, which is connected before the Series APF and in parallel with the electrical power grid. This load is affected by voltage harmonics, and indeed, it is connected to the system only to intensify this problem due to its harmonic current consumption. The other two loads are a series RL linear load, and a nonlinear load, composed also by a full-bridge rectifier with a RC load at the DC side. These two loads are connected downstream of the Series APF, and thus are not influenced by voltage harmonics [5].

Regarding the simulation model of the Series APF, it is also worth to mention the adopted switching pattern: the Unipolar Carrier-Based PWM (CB-PWM) technique with a switching frequency (f_S) of 20 kHz [30].

Figure 7 shows the results of the conducted simulations when the Series APF is set in operation, where the first screen shows the

source voltage, the second screen shows the load voltage and the third screen shows the compensation voltage produced by the Series APF.

Another key feature of the proposed control scheme is the regulation of the DC bus voltage, which can also be verified through the simulation model, and which has to be conducted simultaneously with the mains voltage harmonic compensation. As it is shown in **Figure 7**, the DC bus voltage, which has a reference value of 200 V, has very small variations on its amplitude and is perfectly regulated around its reference value (the average DC voltage is equal to 200 V).

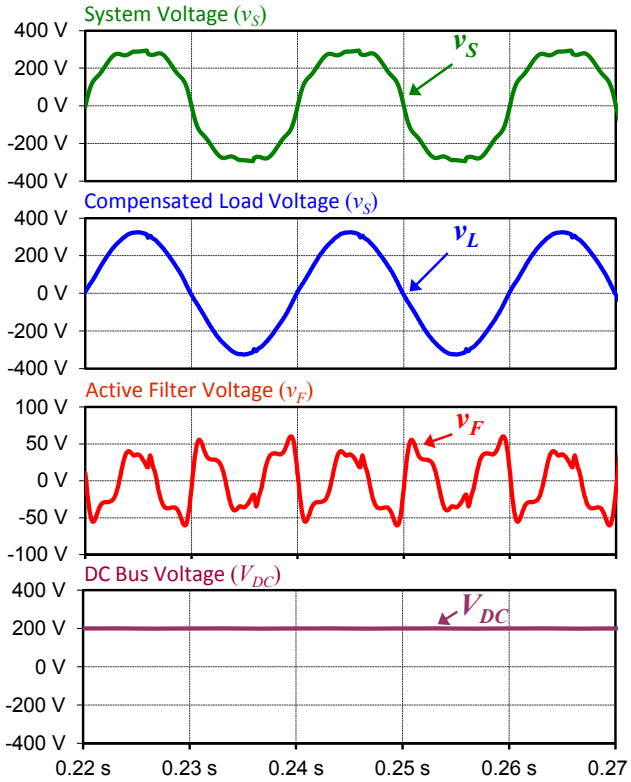

Figure 7. Simulation results of the Series APF.

By comparing the waveforms of the source and load voltages it is noticeable the improvement that the Series APF introduces in the waveform of the load voltage. This fact is corroborated when it is analyzed the harmonic spectrum and the Total Harmonic Distortion

(THD) values of the system voltage and of the load voltage after the Series APF is set into operation, which are presented in **Figure 8**.

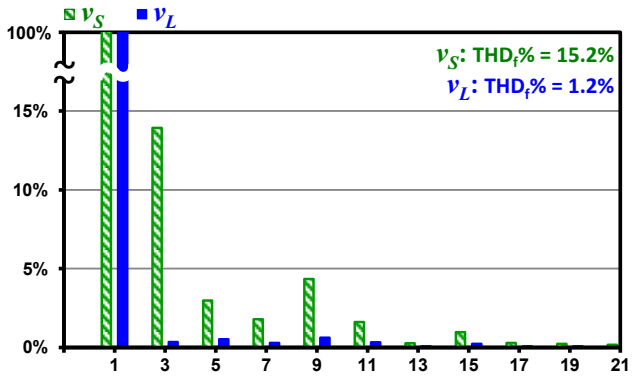

Figure 8. – Harmonic spectrum of the system voltage (v_S) and compensated load voltage (v_L).

6. Experimental Results

Once all steps of the project of the Series APF were concluded, it was possible to proceed with the implementation of a laboratorial prototype of the aforementioned device, which was connected to a single-phase AC 50 V voltage system. By means of two *SEMIKRON SMK145GB066D* dual IGBTs modules, an H-Bridge inverter was developed that served as the power component of the Series APF. The digital control system, which includes all the items described in the Control Strategy section, was implemented in a *TMS320F2812* DSP from *Texas Instruments*. Two boards were designed for conditioning the signals obtained through voltage and current measurements, and for controlling the PWM signals sent to the inverter. It was also designed a passive filter, in order to cut-off the switching high frequency components of the inverter output signal. Except for the system voltage amplitude, all of the prototype and system characteristics were similar to the ones of the simulation model.

The experimental results obtained with the laboratorial prototype are presented in **Figure 9**, where it is shown the distorted system voltage, the compensated load voltage and the voltage produced by the Series APF, in addition with the voltage from the DC bus. Also in **Figure 10** it is possible to compare the indirect improvement occurred in the load current once the Series APF started operating. All of these waveforms were registered with a Yokogawa DL716 digital oscilloscope.

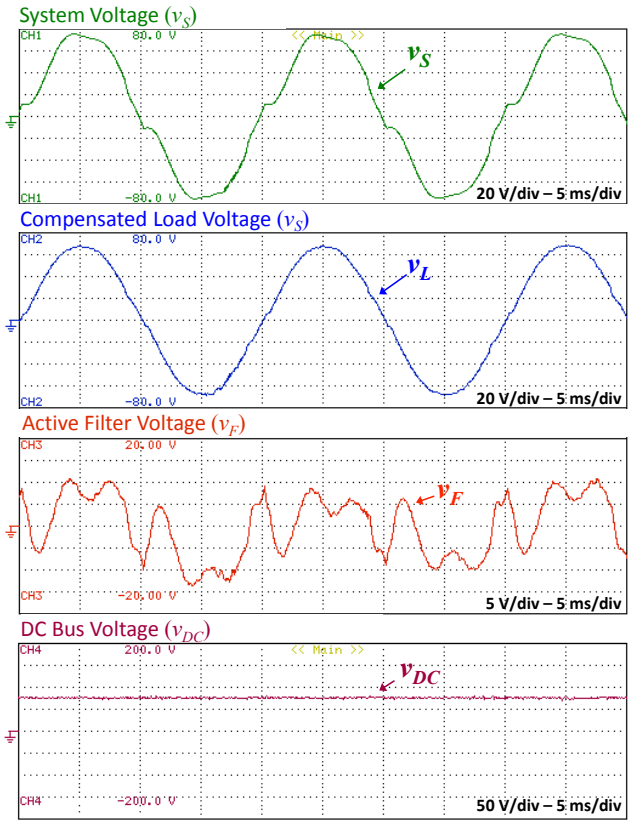

Figure 9. Experimental results obtained with the Series APF.

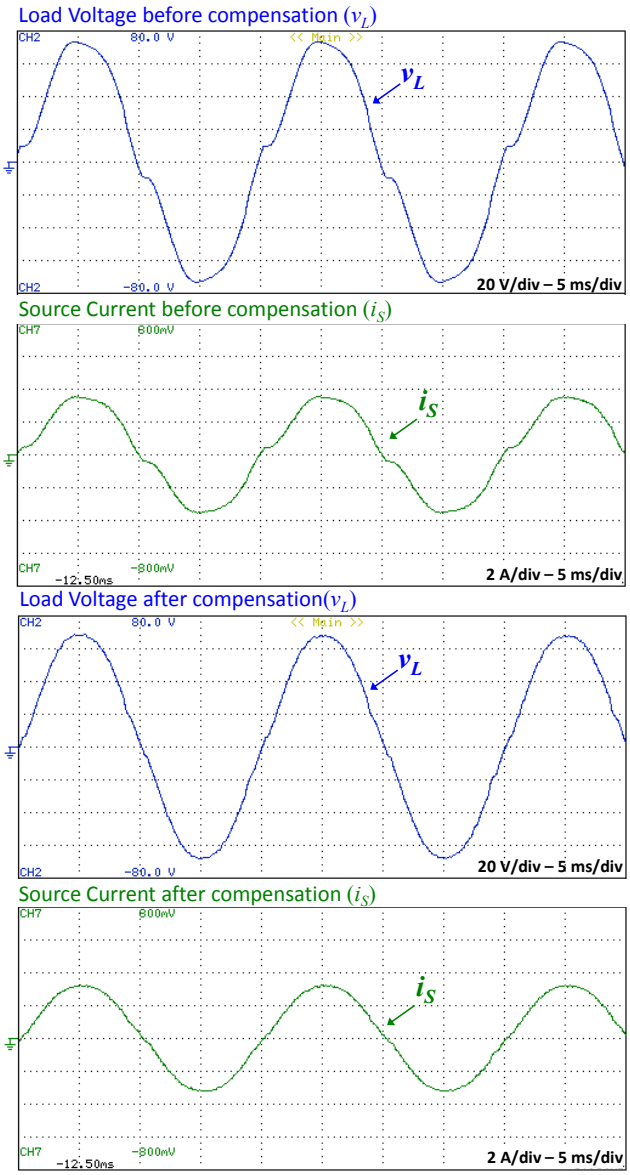

Figure 10. Experimental results obtained with the Series APF.

To quantify the improvements introduced by the Series APF prototype, a *Fluke 434* power quality analyzer was employed to measure and register the harmonic spectrum and the THD values of the system and load voltages. The main characteristics of the equipment used in the experimental measurements are presented in Table I [31][32].

TABLE I
MAIN CHARACTERISTICS OF THE MEASUREMENT EQUIPMENT

Yokogawa DL716 digital oscilloscope	
Number of channels	16
ADC Resolution	12 bit
Maximum sampling rate (per channel)	10 MS/s
PC interface formats	BMP and CSV
Fluke 434 power quality analyzer	
Number of channels	8
ADC Resolution	16 bit
Maximum sampling rate (per channel)	200 kS/s
Harmonics	DC, 1..50
RMS voltage accuracy	± 0.1%
RMS current accuracy (with i400s probes)	± 1%

In **Figure 11** it can be seen that the Series APF mitigates the voltage harmonics, as the THD of the load voltage, which initially was equal to the system voltage, drops from 8.8% to 2.5%.

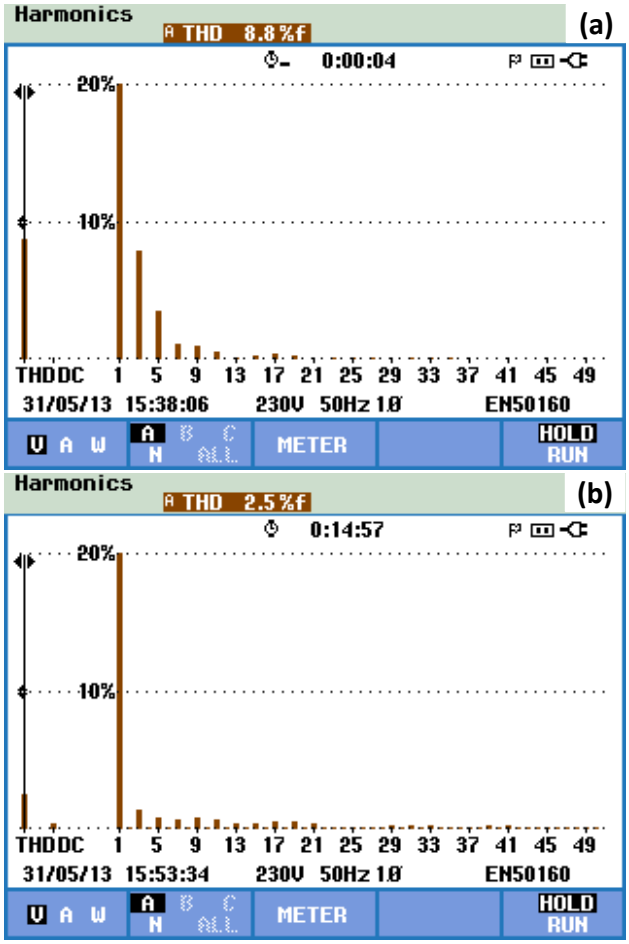

Figure 11. Harmonic spectrum and THD values of the load voltage measured with *Fluke 434*: (a) Before the operation of the Series APF; (b) After the operation of the Series APF.

Table II resumes the values obtained in the experimental tests performed with the series APF prototype.

TABLE II
EXPERIMENTAL RESULTS SUMMARY

Description	Value
RMS value of the source voltage (v_S)	52.3 V
THD$_f$% of the source voltage (v_S)	8.8%
RMS value of the load voltage (v_L)	49.5 V
THD$_f$% of the load voltage (v_L)	2.5%
RMS value of the series APF voltage (v_F)	4.5 V
THD$_f$% of the series APF voltage (v_F)	126%
RMS value of load current with series APF on	3.7 A
DC Bus average voltage (V_{DC})	75 V

7. Conclusions

A single-phase Series Active Power Filter (Series APF) with no power source to regulate the DC voltage, and without coupling transformer, has been proposed, simulated, developed and tested. The control strategy implements an Enhanced Phase-Locked Loop (EPLL) circuit in order to obtain the synchronizing signals which are essential to the calculation of the compensating voltage. It also incorporates a damping algorithm in order to mitigate the resonance inherent to the power system, and a dead-time compensation loop which is responsible for minimizing the dead-time effect. All these elements have been carefully scrutinized, confirming that the control strategy complies with its goals, allowing the Series APF to compensate mains voltage harmonics while maintaining the DC voltage regulated. This last remark is based upon simulation results obtained with the PSIM software and on experimental results as well.

A laboratorial prototype was fully developed in order to test the proposed Series APF. The control system was implemented recurring to a *TMS320F2812* fixed-point DSP. Ultimately, the experimental results validated the theoretical assumptions and the simulation results, as the mains load voltage THD dropped significantly from 8.8% to 2.5%, and the DC bus voltage remained balanced while the Series APF was in operation. The presented experimental results, plus the fact that the proposed Series APF does not require a DC power source or a coupling transformer to be connected to the AC power grid, thus reducing its cost and size, contributes to increase the interest in the Series Active Power Filters.

8. References

[1] Akagi, H., Watanabe, E. H., and Aredes, M., Instantaneous Power Theory and Applications to Power Conditioning, Vol. 31, Hoboken, NJ: John Wiley & Sons, Inc., Chaps. 1, 5, 2008.

[2] Y. Pal, A. Swarup, and B. Singh, "A review of compensating type custom power devices for power quality improvement," *Power System Technology and IEEE Power India Conference, 2008. POWERCON 2008. Joint International Conference on*, pp. 1–8, 2008.

[3] J. V. Milanovic and Y. Zhang, "Modeling of FACTS devices for voltage sag mitigation studies in large power systems," *Power Delivery, IEEE Transactions on*, vol. 25, no. 4, pp. 3044–3052, 2010.

[4] J. J. Paserba, G. F. Reed, M. Takeda, and T. Aritsuka, "FACTS and custom power equipment for the enhancement of power transmission system performance and power quality," *Curitiba, Brazil*, 2000.

[5] Y. Pal, A. Swarup, and B. Singh, "Flexible Control of Single-phase Unified Power Quality Conditioner Using Frequency-domain Approach," *Electric Power Components and Systems*, vol. 41, no. 4, pp. 401–412, 2013.

[6] H. Fujita and H. Akagi, "The unified power quality conditioner: the integration of series and shunt-active filters," *Power Electronics, IEEE Transactions on*, vol. 13, no. 2, pp. 315–322, 1998.

[7] H. Akagi, "New trends in active filters for power conditioning," *Industry Applications, IEEE Transactions on*, vol. 32, no. 6, pp. 1312–1322, 1996.

[8] M. El-Habrouk, M. Darwish, and P. Mehta, "Active power filters: a review," *Electric Power Applications, IEE Proceedings-*, vol. 147, no. 5, pp. 403–413, 2000.

[9] F. Z. Peng, "Harmonic sources and filtering approaches," *Industry Applications Magazine, IEEE*, vol. 7, no. 4, pp. 18–25, 2001.

[10] L. F. Monteiro, J. L. Afonso, J. G. Pinto, E. Watanabe, M. Aredes, and H. Akagi, "Compensation algorithms based on the pq and CPC theories for switching compensators in micro-grids," *Power Electronics Conference, 2009. COBEP'09. Brazilian*, pp.

32–40, 2009.

[11] H. Carneiro, J. Pinto, and J. L. Afonso, “Single-phase series active conditioner for the compensation of voltage harmonics, sags, swell and flicker,” *Industrial Electronics (ISIE), 2011 IEEE International Symposium on*, pp. 384–389, 2011.

[12] R. Strzelecki and P. Mysiak, “Experimental tests results of the diode rectifier with series active power filter,” *Electronics Conference (BEC), 2012 13th Biennial Baltic*, pp. 271–274, 2012.

[13] A. Hamadi, S. Rahmani, and K. Al-Haddad, “A new hybrid series active filter configuration to compensate voltage sag, swell, voltage and current harmonics and reactive power,” *Industrial Electronics, 2009. ISIE 2009. IEEE International Symposium on*, pp. 286–291, 2009.

[14] M. Chaudhari and others, “Three-phase Series Active Power Filter as Power Quality Conditioner,” *Power Electronics, Drives and Energy Systems (PEDES), 2012 IEEE International Conference on*, pp. 1–6, 2012.

[15] A. Ngotakun, K. Areerak, K. Areerak, and A. Srikaew, “Control of series active power filter using fuzzy logic controller,” *Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology (ECTI-CON), 2012 9th International Conference on*, pp. 1–4, 2012.

[16] C. Jacobina, A. Oliveira, N. Rocha, R. Matias, W. Santos, and M. Correa, “Three-Phase Series Active Power Filter Without Isolation Transformer and Active DC Source,” *Applied Power Electronics Conference and Exposition, 2009. APEC 2009. Twenty-Fourth Annual IEEE*, pp. 1596–1601, 2009.

[17] M. Karimi-Ghartemani and M. Iravani, “A new phase-locked loop (PLL) system,” *Circuits and Systems, 2001. MWSCAS 2001. Proceedings of the 44th IEEE 2001 Midwest Symposium on*, vol. 1, pp. 421–424, 2001.

[18] M. Karimi-Ghartemani and M. R. Iravani, “A nonlinear adaptive filter for online signal analysis in power systems: applications,” *Power Delivery, IEEE Transactions on*, vol. 17, no. 2, pp. 617–622, 2002.

[19] A. Chaoui, J. P. Gaubert, F. Krim, and G. Champenois, “PI controlled three-phase shunt active power filter for power quality improvement,” *Electric Power Components and Systems*, vol. 35, no. 12, pp. 1331–1344, 2007.

[20] E. R. Ribeiro and I. Barbi, “Harmonic voltage reduction using a series active filter under different load conditions,” *Power Electronics, IEEE Transactions on*, vol. 21, no. 5, pp. 1394–1402, 2006.

[21] H. Carneiro, L. F. Monteiro, and J. L. Afonso, “Comparisons between synchronizing circuits to control algorithms for single-phase active converters,” *Industrial Electronics, 2009. IECON’09. 35th Annual Conference of IEEE*, pp. 3229–3234, 2009.

[22] A. Nasiri, A. Amac, and A. Emadi, “Series-Parallel Active Filter/Uninterruptible Power Supply System,” *Electric Power Components and Systems*, vol. 32, no. 11, pp. 1151–1163, 2004.

[23] A. Ghamri, M. Benchouia, and A. Golea, “Sliding-mode control based three-phase shunt active power filter: Simulation and experimentation,” *Electric Power Components and Systems*, vol. 40, no. 4, pp. 383–398, 2012.

[24] N. Gupta, S. Singh, and R. Bansal, “A digital signal processor based performance evaluation of three-phase four-wire shunt active filter for harmonic elimination, reactive power compensation, and balancing of non-linear loads under non-ideal mains voltages,” *Electric Power Components and Systems*, vol. 40, no. 10, pp. 1119–1148, 2012.

[25] C. Wessels, J. Dannehl, and F. W. Fuchs, “Active damping of LCL-filter resonance based on virtual resistor for PWM rectifiers—Stability analysis with different filter parameters,” *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, pp. 3532–3538, 2008.

[26] W. Gullvik, L. Norum, and R. Nilsen, “Active damping of resonance oscillations in LCL-filters based on virtual flux and virtual resistor,” *Power Electronics and Applications, 2007 European Conference on*, pp. 1–10, 2007.

[27] A. R. Munoz and T. A. Lipo, “On-line dead-time compensation technique for open-loop PWM-VSI drives,” *Power Electronics, IEEE Transactions on*, vol. 14, no. 4, pp. 683–689, 1999.

[28] S.-G. Jeong and M.-H. Park, “The analysis and compensation of dead-time effects in PWM inverters,” *Industrial Electronics, IEEE Transactions on*, vol. 38, no. 2, pp. 108–114, 1991.

[29] C. H. da Silva, R. R. Pereira, L. E. B. da Silva, G. Lambert-Torres, J. O. P. Pinto, and S. U. Ahn, “Dead-time compensation in Shunt Active Power Filters using fast feedback loop,” *Harmonics and Quality of Power, 2008. ICHQP 2008. 13th*

International Conference on, pp. 1–4, 2008.

[30] J. Holtz, “Pulsewidth modulation-a survey,” *Industrial Electronics, IEEE Transactions on*, vol. 39, no. 5, pp. 410–420, 1992.

[31] Niimi Yoshihis , Takeshita Yukihito, and Yamamoto Chiaki, ”DL716 Digital Scope,” Yokogawa Technical Report-English Edition, pp. 9-14, 2000

[32] Fluke 434/435 Three Phase Power Quality Analyzer Users Manual, 2008