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Reliability of HfO_2-based Ferroelectric FETs: A Critical Review of Current and Future Challenges

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***Abstract*—Ferroelectric transistors (FeFETs) based on doped hafnium oxide (HfO_2) have received much attention due to their technological potential in terms of scalability, high-speed, and low-power operation. Unfortunately, however, HfO_2-FeFETs also suffer from persistent reliability challenges, specifically affecting retention, endurance, and variability. There is a broad consensus that a deep understanding of the reliability physics of HfO_2-FeFETs is an essential prerequisite for the successful commercialization of this promising technology. In this paper, we review the current understanding of the relevant reliability aspects of HfO_2-FeFETs. We initially focus on the reliability physics of ferroelectric capacitors, as a prelude to a comprehensive analysis of FeFET reliability. Then, we interpret key reliability metrics of the FeFET at device-level (i.e., retention, endurance, variability) based on the physical mechanisms previously identified. Our integrative theoretical framework connects apparently unrelated reliability issues and suggests mitigation strategies at either device, circuit, and system level. We conclude the paper by proposing a set of research opportunities to guide future development in this field.**

Index Terms—Ferroelectric FETs, Retention, Endurance, Variability, Reliability

I. Introduction

The accidental discovery of the orthorhombic, ferroelectric phase in hafnium oxide (HfO_2) in 2006 (and first reported in 2011) has revived the interest in ferroelectric transistor (FeFET) technology [1]–[6]. The latest generations of FeFETs are expected to outperform other kinds of emerging memory technologies in terms of energy/speed required for writing operation and help support several disruptive circuit topologies as well as computing architectures [7]. In fact, applications for FeFETs include Non-Volatile Memories (NVMs), Logic-In-Memory (LiM) computing, and synthetic replica of biological elements such as neurons and synapses in artificial neural networks (ANN). Low power consumption, high integration and fast switching speed have encouraged development of ferroelectric HfO_2-based FeFETs (in short, hereafter, HfO_2-FeFETs) [5]. However, results from previous technology generations as well as those in recently published papers demonstrate that these devices suffer from intrinsic reliability issues that limit retention, endurance, and induce variability. Therefore, performance-reliability trade-offs must be quantified and accounted for to ensure that FeFETs can compete successfully against other emerging memory technologies [8], [9].

Historically, the challenge of dimension scaling limited the broad adoption of ferroelectric based devices [10] as ferroelectricity in traditional perovskite oxides is suppressed below a critical thickness (i.e., in the order of tens of nanometers) due to a combination of size/scaling effects, increased depolarization fields, and leakage [11]–[13]. However, this is apparently not the case for HfO_2 ferroelectric oxides, as recently it was shown that polarization switching could still be observed in few-nm-thick doped HfO_2 layers – thanks to the polar phase formation by surface/size effects [11]. This paves the way to the aggressive scaling of FeFETs beyond the 5-nm node [14].

Thus, the remaining challenge to the commercial deployment of scaled HfO_2-FeFETs will be related to their reliability. Therefore, a thorough understanding of the reliability aspects and of the underlying physical mechanisms is crucial to fully exploit HfO_2-FeFETs potential and to select the right device for the desired application. However, given the relatively low maturity level of the technology, reliability physics of these devices is not yet fully understood. Indeed, most reports focus on single reliability issue based on few devices prepared in academic laboratories. The review/perspective articles in the literature mostly focus on performance metrics, and do not systematically discuss the FeFET reliability challenges and corresponding tradeoff between performance and reliability [7], [8], [15]–[20]. Only recently, the authors in [21] offered an integrated theoretical framework to analyze reliability issues of HfO_2-FeFETs (and also negative capacitance FETs, NCFETs).

In this paper, we provide a comprehensive dissertation of the reliability physics of HfO_2-FeFETs, including a critical review of recent literature on the subject. We have three objectives: *i*) to aggregate relevant reliability data available in the literature; *ii*) to identify common points as well as differences in the proposed interpretation of reliability mechanisms; and *iii*) to highlight the most critical reliability aspects depending on the

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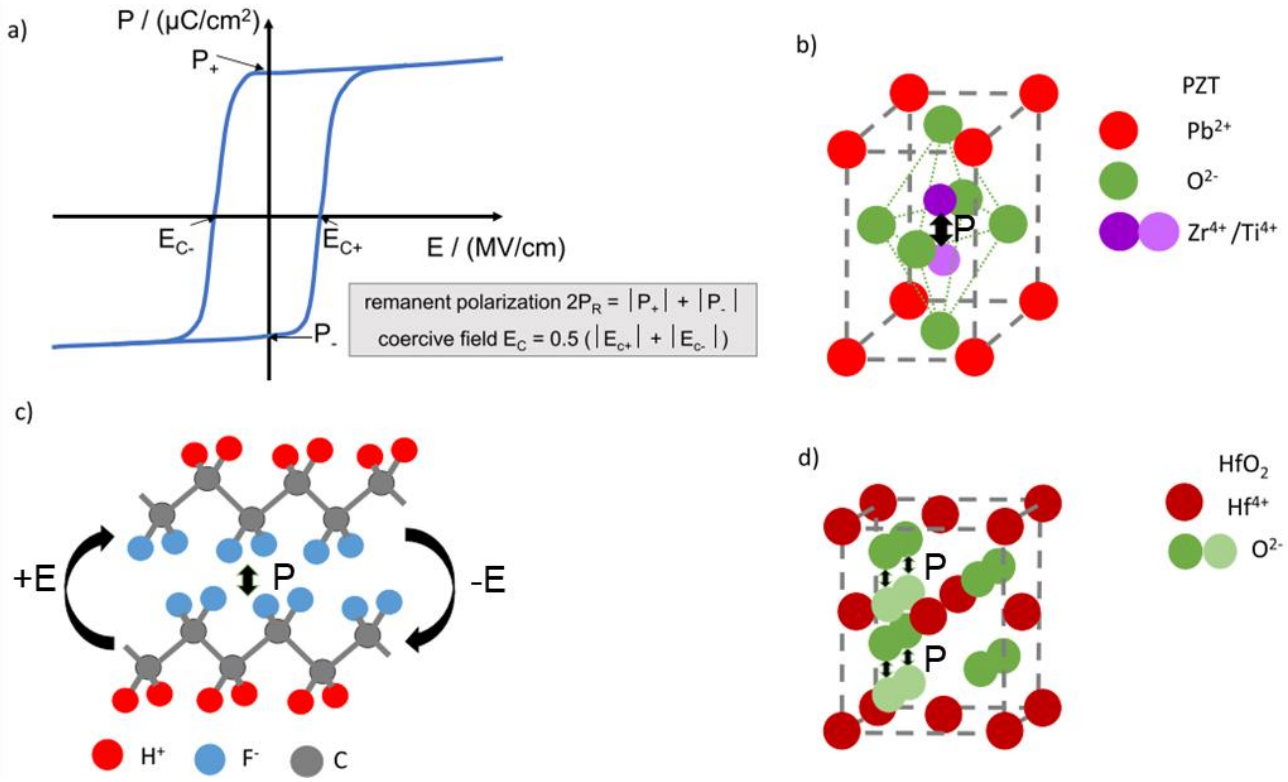

Fig. 1. (a) Illustration of typical hysteresis loop relation between polarization and electric field for a generic ferroelectric material. The most important properties (i.e., remnant/remanent polarization, P_r, and coercive field, E_C) are indicated. (b)-(d) Sketches of crystal structure of different ferroelectric materials: (b) PZT crystal showing the two stable positions of a central Zr^{4+} or Ti^{4+} ion. (c) PVDF polymer chain with the two orientations that can generate the ferroelectric polarization. (d) Orthorhombic HfO_2 crystal indicating the positions of O_2-oxygen ions in the crystal determining polarization switching. Reproduced from [8].

application of interest (e.g., substitute of conventional DRAM-memories, LiM elements, neural networks, etc.). For the first two objectives, we frame the discussion by addressing the physical mechanisms related to reliability of the FeCAP (i.e., ferroelectric capacitor) and FeFET configurations separately. The distinction allows identifying reliability challenges related to the FE-HfO_2 layer itself and how the integration in the MOSFET structure influences reliability [7], [22]. Then, we interpret key reliability metrics of the FeFET at device-level (i.e., retention, endurance, variability) based on the physical mechanisms identified in the previous part. Finally, the third objective is achieved by projecting the device-level reliability metrics at both the circuit and system level. We conclude the paper by providing a perspective on research trends that we envision as most important to move the field forward.

II. Ferroelectric-FETs Memories

A. Basics of Ferroelectric Materials and Memories

Ferroelectricity is a property of any material that has non-zero spontaneous polarization (i.e., without any external electric field) that in addition can switch between two different (or more) polarization values when an external electric field is applied [23]. Fig. 1(a) illustrates the typical hysteresis loop relation between polarization and electric field for a generic ferroelectric material. The hysteresis loop is the essential pre-requisite for the non-volatile memory property of a ferroelectric-based device: the information is written by orienting the polarization in one of the two directions by applying an electric field, and then remnant (or remanent) polarization (Pr) value can be probed/read even when none external electric field is applied, see Fig. 1(a). Generally speaking, ferroelectricity is determined by the polar displacement of atoms in the unit cell of a crystal that originates from the 'symmetry-breaking' (i.e., a small distortion) of a reference, non-polar state [23]. The physical origin of the symmetry breaking as well as the atoms involved in the polar displacement is determined by the specific properties of the material. Fig. 1(b)-(d) show the sketch of pervoskite lead zirconium titanate (PZT), organic polyvinylidene flourid (PVDF), and fluorite HfO_2 crystals indicating (with arrows) the atoms from which polarization switching originates.

Regarding ferroelectricity in HfO_2, several studies were devoted to determine the physical origin of the ferroelectric stable phase at room temperature [24], [25]. Currently there is a general consensus that ferroelectricity in HfO_2 stems from a combination of thermodynamic and kinetic effects [24], [25] which in turn determines the relative fraction of the orthorhombic (ferroelectric) phase vs other non-polar phases (i.e., tethragonal, monoclinic, cubic) [24]. This polymorphism in HfO_2 makes it hard to separate and stabilize the orthorhombic (ferroelectric) phase and as such, optimizing the manufacturing process of FE-HfO_2 layers is of paramount importance to ensure good ferroelectric properties even in ultra-scaled devices [24].

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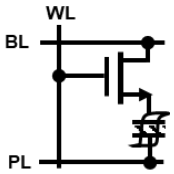
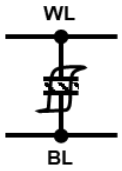
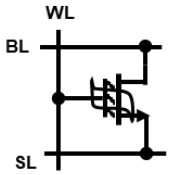
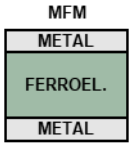
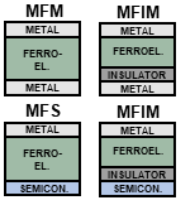
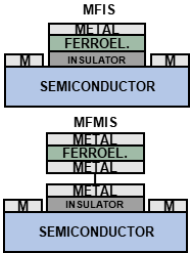
TABLE I
VARIOUS TYPES OF FERROELECTRIC MEMORIES

Type of Memory	FeRAM	FTJ	FeFET
Elementary Cell†			
Ferroelectric Device Structures			
Read-out	Destructive	Non-destructive	Non-destructive
Sensed Quantity	Switching Current	Leakage Current	Drain Current
Retention*	10 y [47], [193]	< 10y [19]	10 y [5], [6], [8], [73], [81]
Endurance**	10^9-10^{12} [22], [38], [73]	10^6-10^7 [194], [195]	10^4-10^6 [5], [6], [8], [73], [81]

†WL = Word Line; BL = Bit Line; PL = Plate Line; SL = Source Line
*Retention is the amount of time that a memory can retain the stored state. Typical (extrapolated) values are indicated.
**Endurance is the number of writing cycles the memory can sustain prior to malfunction. Typical values are indicated.

B. FeRAM, FTJ and FeFET

Depending on how the ferroelectric layer is integrated with other materials/layers, different kind of FE memories can be designed. There are basically three types of memories that incorporate the ferroelectric material in different geometric and operational configurations: ferroelectric random-access-memories (FeRAMs), ferroelectric tunnel junctions (FTJs), and ferroelectric transistors (FeFETs) [8].

FeRAMs are typically composed of a two-terminal ferroelectric capacitor (FeCAP) – usually embedded in the back-end – in series with a select transistor [8]. For this kind of ferroelectric memory, reading requires applying a voltage pulse that, depending on the polarity of the stored polarization state, allows a large or a small current to flow between the two terminals. Because reading can cause polarization reversal, the memorized state is lost and re-writing is required [26]; as such, reading is defined as destructive.

FTJs are two-terminal devices that are either MFM or MFIM capacitors. Other structures are also possible as illustrated in Tab. I. Regardless of the particular structure, FTJs exploit the modulation of the tunneling leakage current by the ferroelectric polarization. Read of the state is carried out by measuring the leakage current of the stack, and as such it does not require refresh after the read operation (i.e., non-destructive readout is achieved) [8].

FeFETs are three-terminal devices that exploit the modulation of the FET channel conductance by the ferroelectric polarization to encode the memory state. As such, reading in FeFETs is a non-destructive process. A comprehensive overview and comparison of HfO2- FeFETs, FeRAMs, FTJs, and of current research trends in the field can be found in [8]. Tab. I summarizes the structures and main characteristics of these three kinds of ferroelectric memories.

C. A Brief History of FeFET

Before getting more into the details of FeFET operation and reliability, we briefly discuss its history. Although ferroelectrity was discovered ~~almost~~ 100 years ago [24], the first demonstration of FeFET in 1963 had to wait the invention of MOSFET in 1960, see Fig. 2 [27]. The device (at the time called solid-state memory resistor) fabricated by Moll and Tarui (Stanford University) was composed of a thin-film semiconductor deposited on a ferroelectric layer realized with triglycine sulfite (TGS). During the 1960s, several thin-film ferroelectric transistors based on different ferroelectric materials were realized [26]. However, it was only in 1974 that the first MFS FeFET employing a perovskite ferroelectric (i.e., bismuth titanate, BTO) stacked on top a transistor structure was realized, effectively enabling miniaturization [26], [28]. However, despite decades-long refinements, the issues related to scaling, retention loss [29], integration into existing manufacturing process (e.g., CMOS) [30], and per-bit cost [8]

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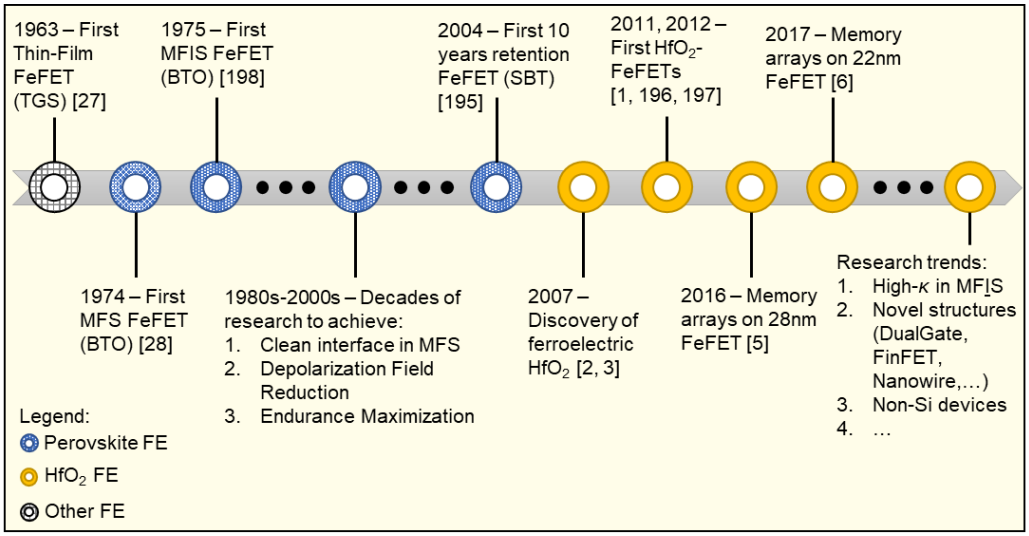

Fig. 2. Ferroelectric FETs time evolution from early demonstrations to current research trends. Major milestones reported here: [1]–[3], [5], [6], [27], [28], [196]–[199]. More about FeFET history and development can be found in: [8], [16], [26].

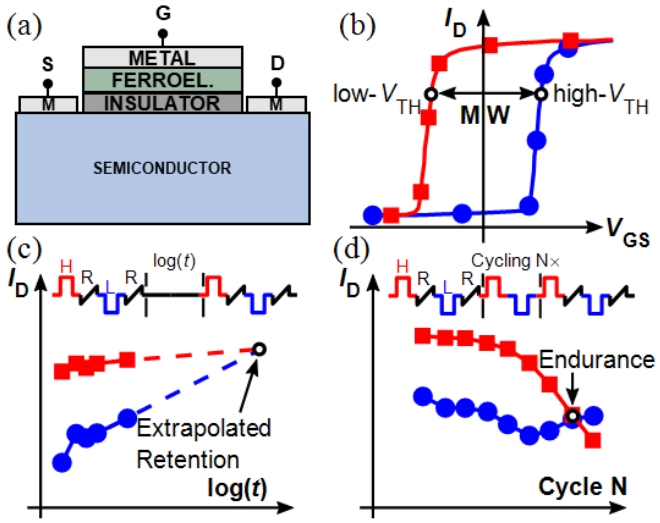

Fig. 3. Definition of key concepts related to the performance and reliability of FeFETs. (a) Sketch of the geometrical structure showing the presence of ferroelectric layer in the gate stack of the transistor. (b) Illustration of I_D–V_{GS} transfer characteristics, having two different branches with either high- or low-threshold voltage (V_{TH}) depending on the stored polarization state. *MW* is defined by the difference of the two V_{TH}'s. (c) Typical retention characteristics of a written cell monitored as the evolution of the drain current I_D over time with no applied voltage. (d) Typical endurance characteristics as a function of number of cycles when applying repeatedly positive/negative voltage pulses. Voltage pulse sequence applied during retention/endurance characterization are also illustrated. Retention/endurance can also be evaluated by monitoring the evolution of V_{TH}'s (or *MW*).

have limited practical use of classical, perovskite ferroelectric (e.g. PZT, SBT, BaTiO, etc.)-based memories only to niche applications [7], [8], [31], [32]. Particularly, the issue of ferroelectric thickness shrinking hindered the down scaling of lateral dimensions (i.e., gate length) beyond the 50-nm node [10]. The prospects of FeFETs changed radically with the discovery of ferroelectric properties in crystalline HfO_2 doped with SiO_2 in 2006 (reported later in 2011) as well as in ZrO_2 and in $Hf_{0.5}Zr_{0.5}O_2$ (HZO) [2], [3]; the latter was thereafter exploited to realize ultra-scaled FeFETs at the 28- and 22-nm nodes [4]–[6]. Technology development efforts so far have proven effective in improving performance metrics of ferroelectric HfO2-based FeFETs (i.e., memory window, power consumption, integration, and process compatibility with complementary metal-oxide-semiconductor technology, CMOS) and NCFETs; however, reliability did not improve as significantly [7], [33]. Thus, despite the relatively low maturity of HfO_2-FeFETs (the first reports date back to only about 10 years ago), it is important to address both performance and reliability improvement to determine their true advantages over other emerging technologies (e.g., resistive RAMs, phase-change memories, magnetic tunnel junctions, etc.).

D. FeFET key concepts

We conclude the introduction by illustrating key concepts related to FeFETs. Fig. 3(a) shows the sketch of the device structure, which resembles that of a conventional MOSFET with a ferroelectric layer inserted in the gate stack in between the gate metal and the insulator layer. Fig. 3(b) shows the I_D–V_{GS} transfer characteristics of the FeFET, exhibiting two different branches with either high- or low-threshold voltage (V_{TH}) depending on the memorized polarization state (the difference between V_{TH}'s defines the memory window, MW). Fig. 3(c), (d) show typical FeFETs retention (endurance) characteristics, monitored as the evolution of the drain current I_D over time with no applied voltage in the case of retention, or with number of cycles when applying repeatedly positive/negative voltage pulses in the case of endurance. Retention/endurance can also be evaluated by monitoring the evolution of V_{TH}'s (or MW) instead of I_D in the same way as described above. The specific reliability considerations (e.g., imprint/retention of opposite state), are discussed in Sections III and IV.

III. HfO_2-FeCAPs Reliability Physics

In general, memory window, retention and endurance depend on the memory design. Although in this paper we focus on FeFETs reliability, in this section we discuss reliability issues connected to the ferroelectric layer in FeCAP configuration. This discussion is helpful to first identify the reliability issues associated with the MFIM structure, which serves as building

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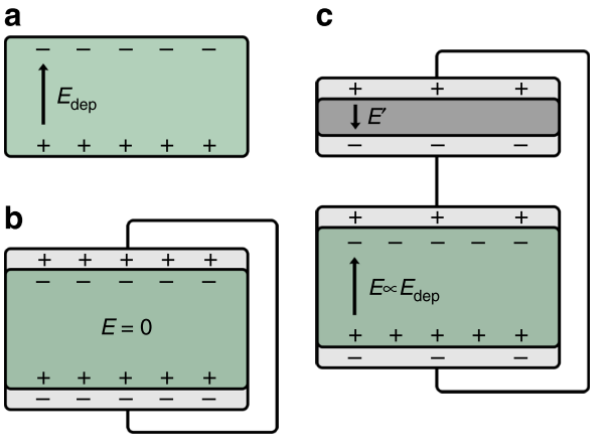

Fig. 4. Schematics showing the compensation of depolarization field in (a) a free-standing ferroelectric material, (b) ferroelectric-only capacitor with (ideal) metal electrodes, and (c) ferroelectric capacitor with a series dielectric capacitor. Reproduced from [43].

block of the MFIS stack employed in FeFETs, which is covered in Sec. IV. The main reliability issues of FE-HfO_2 capacitors in MFIM configuration are depolarization field [29], [34], leakage [29], [35], imprint [36], [37], wake-up [38], fatigue [22], [38], dielectric breakdown [39], [40], and hot atom damage [41], [42]. In the remainder of this section we analyze each of these issues in detail. A list of glossary terms often used in this manuscript is provided in Appendix C.

A. Depolarization Field

The schematics of Fig. 4 shows the depolarization field (E_{dep}) inside a generic ferroelectric layer in three different configurations. In a free-standing ferroelectric, see Fig. 4(a), since there are no free charges the polarization charge is destabilized by $E_{dep} = -P(E)/(\varepsilon_0\varepsilon_{FE})$, where ε_{FE} is the relative dielectric constant of the ferroelectric layer, and ε_0 is the vacuum permittivity. (Note that polarization non-linearly depends on the applied field, and the actual P–E relationship can be described with different models, as discussed in Appendix B). Fig. 4(b) shows that in an ideal MFM structure, the metals can provide the necessary free charge to screen entirely the polarization charge hence $E_{dep} = 0$ [43]. However, non-ideal metals, the presence of dead and/or parasitic layers, or simply the adoption of MFIM structures (see Fig. 4(c)) prevent the full screening of the polarization thus determining a non-zero depolarization field (E_{dep}) that in the latter case can be written as [34]

$$\left|E_{dep}\right| = \left|\frac{PC_{FE}}{\varepsilon_0\varepsilon_{FE}(C_{FE}+C_{DE})}\right| \quad (1)$$

where C_{FE} (C_{DE}) is the ferroelectric (dielectric) capacitance. E_{dep} causes, among other effects [44], polarization to diminish over time when no input bias is applied as a consequence of polarization relaxation (i.e., the orientation of domains and polarization in the opposite direction to the applied field) [45]. Over time, E_{dep} reduces the energy barrier for opposite domain nucleation, causing (partial) polarization back switch and thus causing retention losses in ferroelectric memories [34], [35], [44], [46], [47]. The effect of E_{dep} on retention loss is discussed more in detail in Sec. V.A.

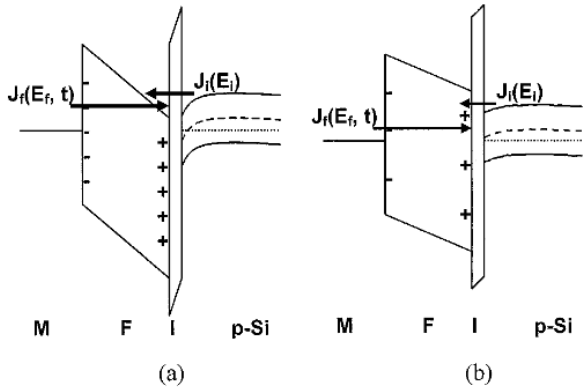

Fig. 5. Illustration of parasitic charge injection causing retention loss in a MFIS stack. (a) Band diagram of the MFIS stack after writing of the polarization state such that it induces an inversion layer in the p-type semiconductor buffer (i.e., low-V_{TH} state, see Fig. 3). The electric field in this case favors electron injection to the ferroelectric/insulator interface from both the gate electrode and the inversion layer. Over time, some of the injected charge traps in the dielectric stack, shifting V_{TH} until (b) the inversion channel is no longer present and hence causing a loss of the stored state. Reproduced from [34].

The presence of traps at the FE/DE interface modifies E_{dep} because in this case part of the polarization charge is screened by trapped charges and not only by the dielectric capacitor. Accordingly, the generalized E_{dep} expression in the case with interface traps reads [48], [49]

$$\left|E_{dep}\right| = \left|\frac{(P+Q_{IT})C_{FE}}{\varepsilon_0\varepsilon_{FE}(C_{FE}+C_{DE})}\right| \quad (2)$$

where Q_{IT} can be either negative or positive, depending on whether electron or hole trapping occurs. Eq. (2) reveals that E_{dep} is effectively tuned by Q_{IT} and that its sign can be reverted conveniently thus improving retention [48].

Reduction of E_{dep} detrimental effect can be achieved in HfO_2 FeCAPs by counteracting the energy barrier reduction for back-switching by either employing electrodes with different work function (giving rise to an internal field that can compensate E_{dep}) [49], by improving interface with electrodes and/or other interfacial layers (if present) [36], or by reducing the monoclinic (non-ferroelectric) phase inside of the FE- HfO_2 layer [12], [50].

B. Parasitic Charge Injection

Besides depolarization field, another mechanism causing retention loss is time-dependent parasitic charge injection (and trapping) [29], [34], [51]. As discussed more in detail in Sec. V.A, retention loss due to E_{dep} over time tends to saturate the polarization to a value proportional to E_C [35], [43], [52]; as such, additional retention loss on long time scales has to be ascribed to other mechanisms such as parasitic charge injection through leakage. Charge injection causes charge accumulation (and possibly trapping) over time at the ferroelectric/insulator junction in MFIM structures which affects the electric field across the structure. This is illustrated schematically in Fig. 5. Depolarization in this case can be understood with Eq. (2), by considering Q_{IT} as being due to trapped injected charge which varies over time depending on the leakage current [51]. Hence, modulation of polarization by injected charge through E_{dep} affects retention.

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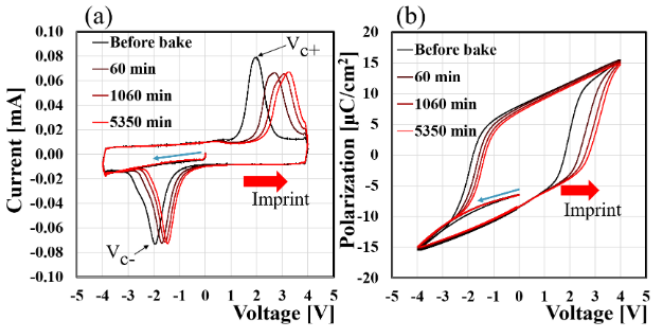

Fig. 6. Illustration of imprint effect on the (a) *I*–*V* curves and (b) corresponding *P*–*V* curves on a MFM capacitor. Curves were obtained by applying a triangular-pulse train with amplitude of ± 4 V. Before baking at 85 °C, the MFM capacitor was set to the polarization state corresponding to writing with negative voltage. Imprint in this case manifests itself as an increase of $+V_c$ (i.e., it shifts to the right). Reproduced from [37].

Possible ways to reduce leakage current and hence charge injection involve employment of high work-function metal layer to increase the barrier for thermionic emission and/or inserting an additional dielectric layer (sufficiently thin not to reduce E_{FE} excessively) between the ferroelectric and the metal electrode [51]. More in general, retention loss due charge injection (and trapping) in MFIM structures can be reduced by improving quality of the deposited FE-HfO_2 and of the interface with the insulator layer, by capping with additional dielectrics, and possibly by inducing internal built-in fields through usage of metal electrodes with different work functions [8], [49], [51].

C. Imprint

Imprint is a unique phenomenon of ferroelectrics that consists in the 'horizontal' shift of the hysteretic *P*–*E* (or *P*–*V*) loop. That is, the ferroelectric bears a preferential polarization state depending on the field that was first applied to it (i.e., when the ferroelectric was initially 'poled') [53]. This 'bias' can be observed as coercive field E_C (or coercive voltage V_C, conventionally defined as the voltage at which peaks in the switching current across the layer occur [37], [54]) shift towards either more positive or more negative values depending on the stored polarization state [37]. That is, if the ferroelectric is in the $-P_s$ ($+P_s$) state, $+E_C$ (or, equivalently, $+V_C$) ($-E_C$/$-V_C$) will increase (decrease). Imprint of $+V_C$ after baking an MFM capacitor in the $-P_s$ state is illustrated in Fig. 6. In general, E_C shifts are asymmetrical [36] as they depend on the stored polarization state as well as field distribution within the structure [37]. As discussed previously, the consequence of imprint is that one polarization state is preferred over the other, and as such it induces retention loss [36]. Basically, the *P*-*V* loop shift induced by the stored polarization state increases over time (and with temperature [36]) and this makes it harder to switch the polarization state (because $+V_C$ or $-V_C$ increase in magnitude), hence causing a significant reduction of the margins between opposite polarization states [36].

In perovskite ferroelectrics, e.g., PZT, imprint was attributed to defect-dipoles originating from oxygen vacancies, that migrate when subject to electric fields leading to shifts in the *P*-*V* loop [55]. In FE-HfO_2, physical causes behind imprint mechanism are still debated in the literature – as discussed in [36]. Nonetheless, a recent contribution by Higashi *et al.* attributed imprint to the electrostatic effect of electron trapping and detrapping at the FE/DE interface [37], [54]. Authors in [37] performed a systematic characterization of the imprint effect showing that during baking (i.e., heating of the device with no applied bias for a long period of time) of FeCAPs in the negative (positive) state, i.e., storing the $-P_s$ ($+P_s$) state, electrons would de-trap (trap) causing a modulation of the depolarization field (in agreement with Eq. (2) as well) in turn causing a positive (negative) shift of the voltage required to cause polarization switching. Therefore, the ferroelectric would switch from the negative to positive (positive to negative) at more positive (more negative) voltage because the variation in trapped charges screens the internal electric field and thus causes domain pinning [37]. Higashi *et al.* also explained imprint recovery with the above model, suggesting that repeated pulses after baking (of opposite polarity to that used to set the initial polarization state) at room temperature would restore the previous amount of trapped charges, shifting back the *P*–*V* loop to its original state. Based on these results, it was also suggested that polarization switching is necessary to achieve imprint recovery, as sub-loop operation would cause only partial recovery from the E_C shifts indicating that imprint happens independently in each domain [37].

Imprint is generally observed when baking the ferroelectric device while applying no input bias, thus it is mixed up with the other sources of polarization loss, namely depolarization field and leakage [37]. One way to assess imprint separately from the other mechanisms is to eliminate the vertical polarization loss in the *P*–*V* loop by applying a same-state set pulse after baking (to re-program the device in the same state as the one prior to the baking process itself), thus allowing to measure only the horizontal shift of the *P*–*V* loop [36], [37].

Being related to trapping, imprint can be effectively mitigated by oxygen vacancies reduction in the FE-HfO_2 layer [50] or possibly by reducing the interface trap density (for instance by using nitrogen-treated oxides [56]).

D. Wake-up

During cycling of the ferroelectric memory for writing, the device undergoes two distinct regimes the first of which is the "wake-up" phase, see Fig. 5. In the first regime, the domains of the pristine ferroelectric partially de-pin and thus increase the remnant polarization. This behavior can be observed up to 10^4–10^5 cycles [22], [36], [38], [57]–[62], see Fig. 7(a), and it is attributed to the redistribution of native defects (i.e., oxygen vacancies) inside of the FE-HfO_2 [38] and to the transition from the tetragonal to the orthorhombic phase [30], [63]. Characteristic of the wake-up phase are the double peaks in the *I*–*V* characteristics of the MFM capacitor around $\pm V_C$ indicating partial domain pinning and non-switching behavior, see Fig. 7(b). When these two peaks merge completely, the pinched hysteresis loop opens up and the wake-up phase ends [38]. Interestingly, wake-up seems to be almost absent in epitaxial HfO_2 films [64], possibly due to either the different structure (i.e., polycrystalline vs epitaxial films) or the different electrodes (i.e., TiN vs $La_{0.67}Sr_{0.33}MnO_3$ (LSMO)) [12], [64].

Pešić *et al.* proposed a detailed modeling approach in [38] revealing the possible cause for wake-up effect, i.e., both domain de-pinning following the redistribution of defects and the gradual transformation of grains from non-poplar

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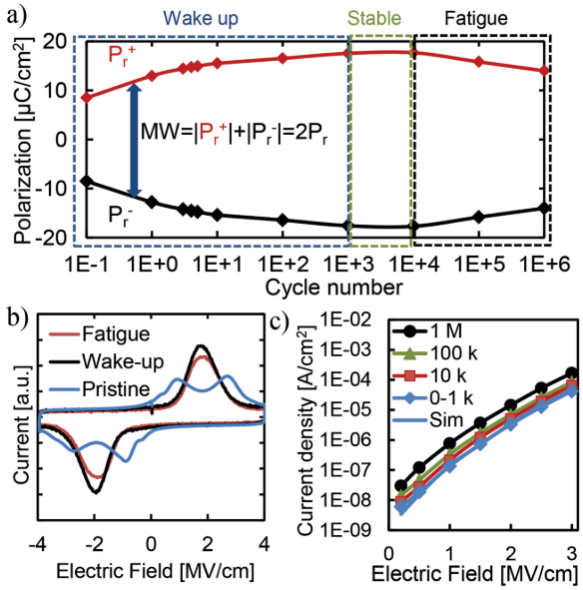

Fig. 7. (a) Measured polarization evolution during bipolar cycling on FE-HfO_2-based ferroelectric capacitors showing both wake-up and fatigue regimes. (b) Measured current–voltage characteristics in the pristine, after wake-up, and after fatigue regimes. (c) Leakage current evolution measured after different numbers of read/write cycles; leakage current starts increasing when the fatigue phase begins. Reproduced from [38].

monoclinic (or tetragonal [30], [63]) to orthorhombic phase during cycling Experimental results obtained by Mehmood *et al.* at different temperatures allowed separating the two causes for wake-up: the initial stage (i.e., up to 10^4 cycles) is dominated by charge redistribution and subsequent depinning of ferroelectric domains; the second stage (i.e., until the fatigue phase starts) is dominated by phase transformation at the interfaces [30]. Recent studies suggest that FE-HfO_2 capacitors with technological solutions such as electrode engineering and epitaxial growth (that reduce oxygen vacancies formation or exhibit more uniform orthorhombic phase) will reduce the wake-up effect (i.e., maximize polarization without preparatory cycles) [38], [64], [65].

E. Fatigue

Further cycling of the device after the end of the wake-up phase causes fatigue. In the fatigue phase, degradation of the ferroelectric layer causes the peaks in the *I-V* loop to spread and reduce thus limiting the memory window (*MW*) of the device [38]. Fatigue is caused by generation of electrical defects (primarily oxygen vacancies, see [38] and refs. therein) within the ferroelectric layer that cause an increase of the leakage current [22], [38]. On the other hand, leakage current stays approximately constant during the wake-up phase, indicating that defect generation occurs mostly during the fatigue phase [38], see Fig. 7(c). Fatigue was attributed in [38] to charge trapping that causes both a partial pinning of the domains (i.e., unable to switch) and a reduction of the electric field in the ferroelectric, in turn reducing the number of switching domains. Both increase of leakage current and temperature acceleration of the degradation confirm that oxygen vacancy generation (and consequent charge trapping increase) is the main limitation to endurance in HfO_2 FeCAPs [38].

Fatigue can be mitigated by reducing charge injection to limit leakage and trapping. For instance, Chen *et al.* showed that NH_3 plasma treatment at either top- or bottom- metal/ferroelectric interface (or both) was effective in reducing leakage and thus fatigue in 12-nm HfO_2 FeCAPs [66].

F. Dielectric Breakdown

One fundamental issue of FE-HfO_2 based devices (with respect to perovskite-ferroelectric based ones) is the high ratio between coercive field of the ferroelectric (≈ 1 MV/cm) and breakdown field of the dielectric itself (≈ 5-6 MV/cm) [20], [67], [68]. Ultimate failure of a ferroelectric memory occurs at (hard) breakdown, hence maximum endurance can be intended as the total number of repeated writing cycles prior to failure. Generally, it is more challenging to achieve high endurance in FE-HfO_2 than perovskite-FEs because the former has much higher coercive field over breakdown field ratio than the latter [20]. Grenouillet *et al.* found excellent endurance up to 10^{12} cycles in Si-doped FE-HfO_2 capacitors at wafer scale, with a clear endurance improvement trend with decreasing device area [39]. This behavior correlates well with the lifetime improvement obtained with area scaling predicted by the Weibull distribution of Time-Dependent Dielectric Breakdown (TDDB), which was also experimentally shown by Florent *et al.* on Al:HfO_2 MFM capacitors [40]. In [40], the time to breakdown (t_{BD}) was found to decrease with increasing temperature and this behavior was attributed to increased trap generation rate. Interestingly, authors in [40] found that despite cycling induces trap generation (and hence reduces *MW*), breakdown is delayed after both the wake-up and fatigue phases due to reduced number of defect clusters (and thus of the possible percolation paths that form preferentially along the grain boundaries [69]) thanks to defect redistribution during cycling.

Chen *et al.* found that TDDB lifetime of MFIS capacitors depends on the annealing technique used to crystallize the Zr:HfO_2 into the orthorhombic, ferroelectric phase [70]. Thus, lifetime was shown to improve with NH_3 plasma treatment during interface layer (IL) ALD deposition combined with micro-wave annealing (MWA) of the 5-nm FE-HfO_2 layer, likely due to reduced leakage current and improved FE/DE interface [70].

G. Hot Atom Damage

A peculiar reliability aspect of ferroelectrics is connected to the so-called "Hot-Atom Damage" (HAD) that is inherent with the transient overshoots occurring when switching between polarization states [41], [71]. During switching in fact, the atoms located between the domain walls (i.e., the regions of a ferroelectric that are undergoing switching and that are not fully stabilized) have to overcome the energy barrier separating the two stable polarization states, see Fig. 8(a). During this process, energy overshoots might occur due to application of large bias with fast sweep rates [41] and switching atoms might therefore cause bond stretching beyond their critical breaking point – similar to hot carriers in MOSFETs [72]. This behavior leads to defect formation that correlates well with increasing leakage

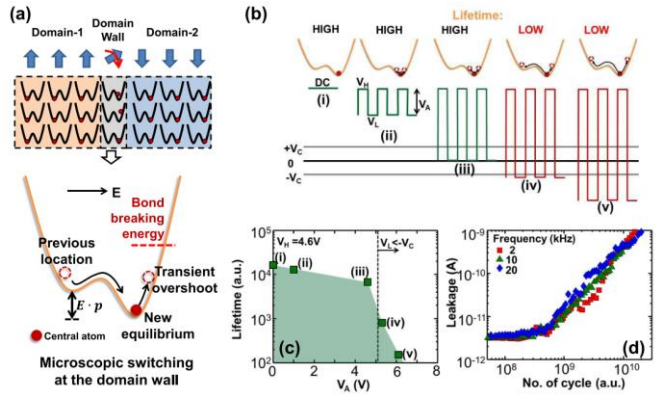

Fig. 8. Illustration of Hot Atom Damage (HAD). (a) Microscopic switching at the domain walls of a ferroelectric material under a given applied electric field (top) and the corresponding double-well energy landscape for each switching (bottom). Switching transients might cause overshoot of the central atom (e.g., Ti/Zr for PZT see also Fig. 2(b)) from the new equilibrium location (hot atom) and eventually cause the breaking of the associated bond. (b) Voltage pulse amplitudes (with respect to $\pm V_C$) modulate the amount of HAD and in turn affect lifetime, shown in (c). (d) Leakage current due to switching pulses with different frequencies shows that damage depends mainly on the number of the switching cycles. Reproduced from [41].

due to either increasing pulse amplitude or frequency, see Fig. 8 [41].

Although this effect was observed for perovskite ferroelectric (e.g., PZT in [41]), a computational study showed that increasing rise/fall times of the writing pulse in FE-HfO_2 leads to improved endurance [42], which is in agreement with the observations about HAD in [41]. Further investigations are required to assess the relevance of HAD in FE-HfO_2 and to identify the possible strategies to suppress the associated defect generation. In [41], several HAD mitigation strategies were devised to reduce the overshoots by employing "soft-switching" bias or circuit schemes by either pulse shaping, series passive elements, temperature control, etc., that effectively showed to improve device lifetime.

IV. HfO_2-FeFETs Reliability Physics

Having covered the reliability issues related to two-terminal ferroelectric capacitors, we now proceed to discuss the physical mechanisms causing reliability issues in HfO_2-FeFETs. Similar to the previous section, we analyze each mechanism individually and discuss also the associated mitigation strategies.

A. Bias Temperature Instability (Trapping)

Bias-Temperature Instability (BTI) is the effect of threshold voltage shift studied in conventional MOSFETs, attributed to trapping. In FeFETs, imprint, charge injection, trapping, can in principle be all considered as sources for BTI. In contrast to two-terminal devices, charge injection is bias-dependent (as the bottom metal electrode is replaced by the semiconductor body), hence characterization is more complex. An effective way to assess BTI impact on the *I–V* characteristics of FeFETs is to perform one spot (or single-pulse) measurements and monitoring the threshold voltage (V_{TH}) evolution during the rising/falling edge of the gate pulses (at fixed drain voltage) [73], [74]. These pulses must be applied after a fixed

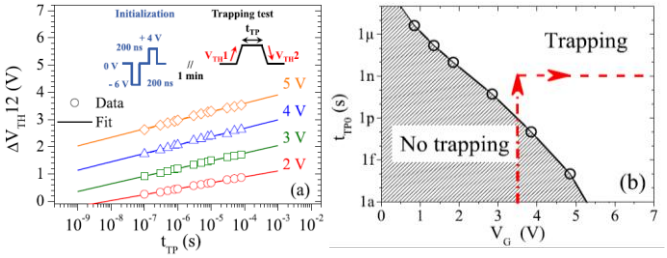

Fig. 9. Trapping characterization of HfO_2-FeFETs after initialization of positive polarization state, i.e., low-V_{TH} state as per definition in Fig. 3. (a) ΔV_{TH} between the rising and falling edges of a trapping pulse (sketched in the figure) as a function of the pulse width (t_{TP}) for varying trapping pulse amplitudes. Symbols represent experimental data and lines indicate fitting curves. (b) Trapping onset time (t_{TP0}) as a function of the gate voltage (i.e., trapping pulse amplitude). t_{TP0} is obtained as the y-intercept of the fitting curves of ΔV_{TH} data in panel (a). For each V_G, t_{TP0} represents the maximum pulse width for 'trapping-free' (i.e., $\Delta V_{TH} = 0$) programming. Reproduced from [74].

polarization state is established in order to assess which mechanism – either charge trapping or polarization switching – dominates the response. Charge trapping causes V_{TH} shifts of the opposite sign with respect to ferroelectric polarization, thus enabling to effectively separate these effects by analyzing the sign of the measured ΔV_{TH} [73], [74].

For instance, Fig. 9(a) shows a positive V_{TH} when measuring on the rising and falling edges of a trapping pulse applied after programming in the positive polarization state (i.e., low-V_{TH} state as per definition in Fig. 3). Extrapolating the fitting curves of ΔV_{TH} data to 0 allows defining a trapping onset time, t_{TP0}, that quantifies the maximum gate pulse width (for a given pulse amplitude) that guarantees trapping-free (i.e., $\Delta V_{TH} = 0$) operation, see Fig. 9(b) [73], [74]. For typical gate pulse amplitude, Fig. 9(b) clearly shows that charge trapping occurs unless pulse widths much shorter than 1 µs are applied. The observed logarithmic dependence of trapping rate with applied gate voltage likely stems from the tunneling rate (τ_{TUN}^{-1}), which, as in the case of MOSFETs, exponentially increases with increasing field on the gate oxide, i.e., $\tau_{TUN}^{-1} \propto exp(\gamma E_{ox})$ [75], [76]. On the other hand, the fact that ΔV_{TH} increases approximately linearly with FE-HfO_2 thickness at short pulse times might indicate that for trap-filling pulses no longer than 1 µs trapping occurs in the IL while at longer time scales trapping occurs in the ferroelectric layer [73].

Interestingly, Yurchuk *et al.* found that the effect of trapping correlates with ferroelectric switching, because the polarization reversal alters the electric field in the gate stack, favoring either electron/hole trapping depending on the stored state [74]. It is likely that this mechanism is the root cause for enhanced degradation during bipolar cycling tests compared to the unipolar case [22]. From the characterization performed in [74] it was found that the small trapping onset time (t_{TP0} < 1 ns) at common writing voltage (3.5 V) can cause ferroelectric polarization to be completely overwhelmed by charge trapping, thus posing constraints on the minimum delay of the read-after-writing operation [73], [74]. On the other hand, trapping could artificially affect endurance if assessed with slow *I-V* characterization [77].

Recently, Xiang *et al.* proposed a model to evaluate the competing roles of charge trapping and polarization in

determining the total V_{TH} shift [78]. In [78], a refined multi-domain *P-E* model was proposed from which the authors deduced that the experimentally observed V_{TH}'s shift in trap-affected FeFETs is determined by the concurrent role of polarization switching and (opposing) trap-induced effects. In addition, the model pointed out the necessity of source-to-drain percolation paths to ensure dominance of polarization switching over trapping. In essence, it was argued that not only the value of polarization determines switching but also its spatial distribution along the channel [78]. Thus, since the chance of S-D FE clustering formation was found to be further enhanced with gate length reduction, a decrease of write voltage (required to trigger polarization switching) with dimension scaling is expected [78].

As already discussed in Sec. III.A, trapping might reduce depolarization field [74], hence improve retention. However, trapping negatively affects endurance, thus trade-offs must be devised to balance retention and endurance (see also Sec. V.E). As discussed in [74], endurance is worsened by trapping as short delays between positive/negative write pulses accelerate *MW* closure due to enhanced degradation by the trapped electrons.

Charge trapping effect on programming can be reduced by introducing delays between read and write operation and/or applying pulses of opposite polarity to the write pulses (without inducing polarization reversal) to accelerate detrapping [74], [79]. Ultimately, reducing trap concentration is the most effective way to mitigate trapping effects. This can be achieved for instance by improving quality of the IL layer and the corresponding interfaces with FE and semiconductor. We will discuss this issue further in Sec. V.B, where endurance improvement strategies are presented.

B. Gate Dielectric Breakdown

Gate dielectric breakdown is a relevant reliability concern for HfO_2-FeFETs due to the high field inside the IL [80]. Typically, breakdown of the gate structure of FeFET occurs after repeated cycling [73], [80], [81], however, *MW* closure generally occurs prior to the failure event due to trap generation and increased trapping [42]. Conversely to HfO_2 FeCAPs, degradation in FETs is more gradual thus soft breakdown events are expected [79]. Interestingly, Chatterjee *et al.* found that their FDSOI HfO_2-FeFET devices exhibited endurance up to 10^7 cycles, after which recoverable failure occurred [80], confirming the assumption of soft breakdown events. While physical mechanisms were not fully investigated, it was hypothesized that breakdown of the SiO_2 IL led to the failure events [80].

More efforts are required to understand the origin of dielectric breakdown and recovery (if present) of HfO_2-FeFETs. In addition, more thorough/systematic studies need to address the possible issue of inverse piezoelectric effect accelerating degradation as also observed in other polar-material systems [82]. A possible strategy to increase lifetime is to employ high-κ interfacial layers (such as AlON [83]) that reduce the field inside the IL.

C. Anode-hole Injection

In FeFETs, it is possible to have anode-hole injection damage due to the field enhancement produced by the ferroelectric polarization [7]. Damage is first initiated by highly energetic electrons injected from the gate terminal to the semiconductor body while applying negative bias [84]. The injected electrons in the semiconductor might lead to generation of electron-hole pairs by impact ionization [7]. The generated holes, attracted by the negative gate bias, then get injected in the gate stack, possibly causing bond breaking and hence damage. This process is illustrated in Fig. 10. Tan *et al.* observed that in ultra-scaled FeFETs with thin FE-HfO_2 (4.5 nm) layer anode-hole injection was the dominant factor to endurance degradation [84]. This was verified by the increased degradation with increasing temperature, which supposedly increased the bond-dissociation rate [72], while the gate leakage current did not vary significantly. As already discussed in fact, increased charge trapping in the bulk of the gate stack is conventionally identified by increased gate leakage [22]; the absence of leakage increase with temperature led Tan *et al.* to associate the observed degradation to the aforementioned effect [84].

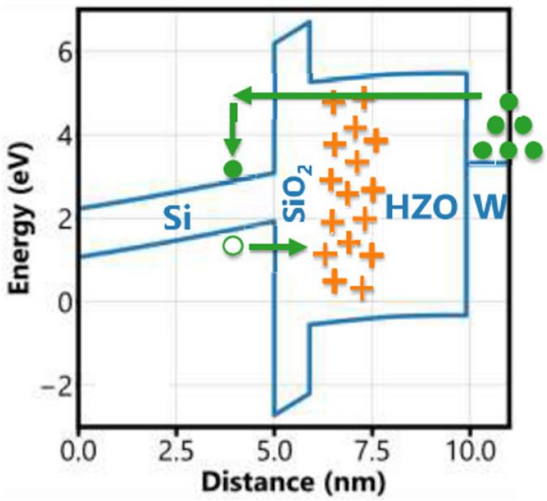

Fig. 10. Simulated energy band diagram after endurance cycling. After applying a negative bias, electrons (green circles) can be injected from the gate electrode (on the right) to the Si body (on the left), generating electron-hole pairs (green-white circles). Generated holes that enter the gate stack might lead to damage (creating positively charged traps, yellow +'s) and negative V_{TH} shifts, reducing MW. Reproduced from [84].

D. Ionizing Radiation

Ionizing radiation is a source of hot carriers (HC), i.e., highly energetic electrons or holes in the long-tail Fermi/Dirac distribution that cause bond breaking and thus generation of traps in the gate stack [72]. Radiation induces electron-hole pairs creation that deteriorate performance of FeFETs through bond breaking (leading to trap generation) [85]. In the case of HfO_2-FeFETs, Chen *et al.* found that total-ionizing-dose (TID) tests with γ-ray caused P_r to decrease with increasing radiation intensity, possibly related to oxygen vacancies generation in the FE-HfO_2 layer [85]. Authors found also that while increasing radiation dose does not affect *MW* or retention considerably, endurance is largely affected due to the reduction of high threshold voltage state due to increased hole trapping in the gate stack [85].

Achieving radiation hardness (i.e., immunity of device against radiation) is crucial for device operating under harsh

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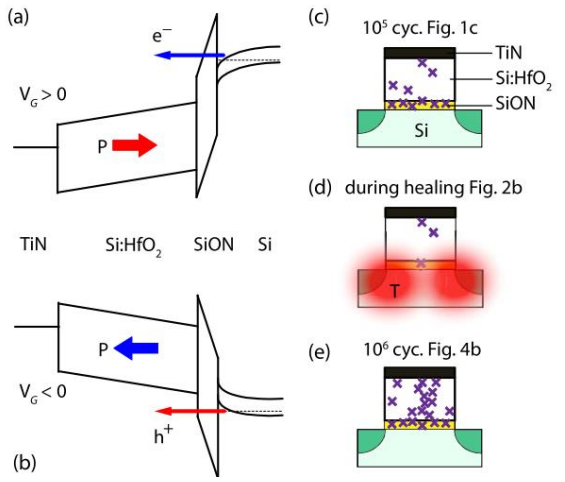

Fig. 11. Sketch of the energy band diagrams of FeFET gate stack during (a) PRG and (b) ERS operation. The predominant carrier fluxes are illustrated. The injected carriers might trap into newly generated defects (due to the high electric field across the stack) and induce degradation. (c) – (e) Illustration of defect generation/healing upon cycling and self-heating, respectively. (d) The magnitude of recoverable damage with self-heating after (c) 10^5 cycles. (e) The healed device still shows permanent breakdown after 10^6 cycles. Reproduced from [87].

conditions such as in space applications. Liu *et al.* showed that using a HfO_2 seed layer between FE-HfO_2 and SiO_2 interfacial layer improved device immunity against γ-ray radiation, hence improving endurance and retention [86]. However, further studies are required in order to identify technological solutions to guarantee radiation hardness.

E. Self-Heating Effects

Device temperature rise above the ambient temperature is referred to 'self-heating' [72]. As previously discussed, temperature rise is undesirable as it increases depolarization, trapping, HC and HAD detrimental effects on FeFET reliability. However, Mulaosmanovic *et al.* found that retention and endurance of HfO_2-FeFETs could be restored to the values prior to undergoing cycling by either inducing self-heating or performing off-chip baking for several hours. In particular, authors showed that applying voltage pulses to induce self-heating in between writing cycles causes a partial redistribution of generated defects from the IL to the FE-HfO_2 [87], which leads to improved endurance, see Fig. 11. In [87] it was also pointed out that this technique cannot be used to arbitrarily extend the operation of FeFETs, as defect generation and, eventually, breakdown would nevertheless limit lifetime even after healing with self-healing pulses.

V. HfO_2-FeFETs Reliability Metrics

Having built a comprehensive picture of the physical mechanism affecting device reliability, we can now move on to discuss the effects that these phenomena have on the behavior of the HfO_2-FeFETs from the memory device standpoint. That is, here we detail how the key reliability metrics of this class of memory (i.e., retention, endurance, variability) are affected by the previously discussed physical mechanisms.

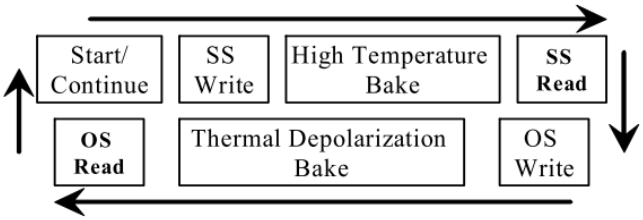

Fig. 12. Illustration of the general characterization scheme for retention measurement. SS is the acronym for "same-state" and OS for "opposite-state". The measurement starts by writing the same-state and baking at a high temperature for a given amount of time. Then reading is performed followed by the writing of the opposite-state. In this state, the device is stressed under thermal depolarization baking typically performed at the maximum operating temperature rating for the application (e.g., 85 °C or 125 °C). Afterwards, the OS data is read and the SS is written again for another cycle to begin with increased baking time. Reproduced from [89].

A. Retention

As already mentioned, retention is the property of a non-volatile memory to retain its state over time, see Tab. I, and it is usually assessed by repeatedly reading the memory state. For FeFETs, either high- and low-V_{TH} or I_{ON}/I_{OFF} state can be assessed [61], [73], [88], see Fig. 3(c). In practice, there are different characterization schemes to evaluate retention of either the same-state (SS) or the opposite-state (OS) during bake of the samples [36], [89] as shown in Fig. 12.

The main causes of retention loss are the depolarization field [29], leakage [51], charge trapping [29], and imprint [36]. Retention loss is in general accelerated by temperature [36], [73], [81], [88], [90] as a consequence of thermal depolarization [91] that reduces the read margin of the memory (i.e., $P_r \sim T^{-1}$). However, *MW* can be restored from thermal depolarization by simply cooling down the device [92].

Interestingly, Gong and Ma [29] pointed out that retention loss due to depolarization field is a minor issue for FE-HfO_2 as E_{dep} over E_C ratio is much lower compared to the perovskite counterparts (such as PZT and SBT). In fact, in the first case, $E_C \approx 1$ MV/cm, while in the second case $E_C \approx 30$–90 kV/cm [29]. Another evidence that depolarization field plays a minor role in HfO_2-FeFETs is the observed asymmetric retention loss of the high- and low-V_{TH} states [10], [73]. However, a recent analysis revealed that traps at the FE/IL interface in HfO_2-FeFETs almost entirely compensate the polarization (~ 90%) and, since this ratio remains constant during retention measurements, authors concluded that the main factor to retention loss is the reduction of polarization due to E_{dep} [93]. Park *et al.* outlined a possible strategy to reduce E_{dep} that involves increasing the total capacitance connected in series with the ferroelectric [20]. This in practice can be achieved by either decreasing t_{IL} or by increasing the doping of the semiconductor substrate [20]. Besides E_{dep}, the other main retention loss mechanisms are imprint [37] and charge trapping induced by leakage, which is also normally reduced in FE-HfO_2 compared to perovskite ferroelectrics [29]. Further studies supported by numerical simulations are required in order to quantitatively assess the role of each of these mechanisms to the total retention loss.

Overall, the improvement of FE-HfO_2 in terms of depolarization field and trapping led to the promising results

published over the years showing extrapolated retention of 10 years at room temperature (RT) [73], [94] or even at 85 °C and more [5], [10], [95].

B. Endurance

In addition to imprint and the associated opposite state retention issue, endurance critically limits the reliability of HfO_2-FeFETs [19]. Best projected endurance of 10^{14} cycles (as per IRDS definition [96]) is still far from being reached, with best demonstrated values in the order of 10^{10}-10^{12} cycles [77], [88]. The origin of the limited endurance in HfO_2-FeFETs is the degradation of the gate stack of the transistor, and particularly of the IL, rather than the degradation of the ferroelectric layer itself [9], [22], [97]. This aspect was first observed by Yurchuk *et al.* in Si:HfO_2-based FeFET [22], who verified that fatigue of the MFM capacitor (with same thickness and composition of the ferroelectric layer employed in the transistor) started degrading after 10^9 cycles, which was much larger than the degradation of the FeFETs, observed at 10^4 cycles. This was explained by increased charge trapping in the IL and also by possible generation of fixed charges that get filled with electrons injected during writing of the high current state [22]. Authors in [22] also observed a correlation between increased interfacial trap density – deduced from the observed increase in charge-pumping current – and increased gate leakage during cycling, further supporting the hypothesis of IL degradation as the fundamental limit to endurance. In [74], it was pointed out that de-trapping of electrons and hole injection during negative writing gate pulses also accelerates degradation (and by the same token, holes de-trapping and electron injection during positive gate pulses) due to increased wear-out of the IL. Several other studies have pointed out the detrimental role of traps in the gate stack either at the interface between semiconductor and IL [79], [97], or near the Si/IL interface, or at the FE/IL interface (also referred to as "border traps") [9], [93]. Ichihara *et al.* argued that endurance could be limited by polarization reduction occurring during cycling and by the increasing trap sites at the FE/IL interface screening the polarization [9], [93].

In general, V_{TH}'s shift (opposite to the V_{TH}'s shift given by polarization switching [74]) and degradation of the sub-threshold swing of the FeFET induce degradation of the *MW* with cycling, as shown in Fig. 11. Drift of both high- and low-V_{TH} are in general non-symmetric [22], [93], [98], and depend on the sign of charged traps (i.e., either positive or negative depending on whether holes or electrons are trapped) [73], [74], [97], [99], on the local field induced by ferroelectric polarization [100], as well as on the doping of the semiconductor substrate [101]. Moreover, the type of stress sequence applied during endurance tests, i.e., either bipolar or unipolar stress, determines different degree of asymmetric degradation [22], [79], [93], also as a consequence of charge injection into traps facilitated by the internal fields induced by the ferroelectric polarization [22]. This behavior was observed also in MFM structures [42], [102].

Mitigation Strategies. Processing/technology strategies to improve endurance and reduce degradation of the gate stack involve: *i*) operation in minor loops instead of the fully saturated *P*–*V* loop [103], *ii*) employment of high-κ oxides as IL or as seed layer [20], [77], [83], [104], [105], *iii*) resorting to

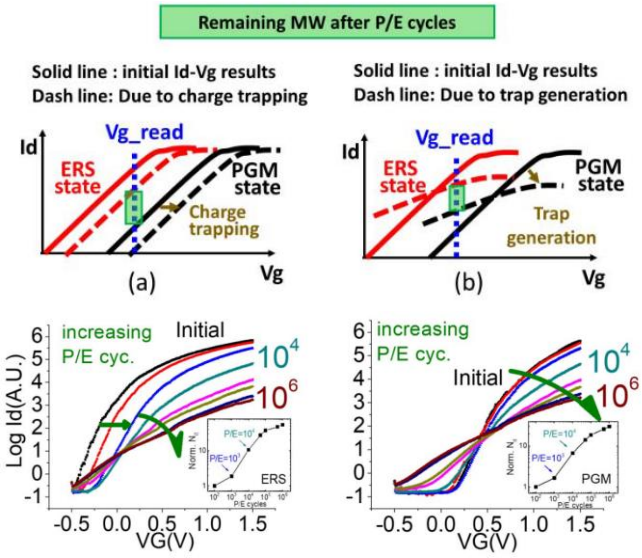

Fig. 13. Top row: illustration of the two main contributions to the drop of FeFET memory window, i.e., (a) charge trapping, and (b) generation of interface/border traps. Bottom row: measured I_D–V_G curves during endurance test for the a) ERS state (after "+" ERS pulse) and (b) PGM state (after "–" PGM pulses). Insets depict normalized N_{IT} vs P/E cycles. Note that here PGM corresponds to high-V_{TH} and ERS to low-V_{TH} (referring to Fig. 3 definitions), which is opposite to the most common nomenclature (see for instance Fig. 11 caption). Reproduced from [9].

MFMIS structures (i.e., HfO_2-FeCAP in the back-end and MOSFET in the front-end) and engineering the ferroelectric/transistor area ratio [33], [34], *iv*) reducing the charge mismatch between the ferroelectric polarization and the semiconductor charge by engineering P_r and/or ε_{FE} [12], [20], *v*) improving the quality of IL layer by high- pressure hydrogen annealing (HPHA) [106] or possibly by NH_3 plasma treatment combined with MWA [70], and *vi*) reducing oxygen vacancies formation by employing ruthenium (or other metals) as the gate electrode [107] *vii*) material-optimization strategies (e.g., nanolaminates, AFE/FE stacks) [108], [109]. On top of these strategies, it is possible to improve endurance by electrical techniques [20] that involve proper de-trapping sequence and delays [74], [79] or performing fast *I*–*V* reads [77] during cycling to reduce V_{TH} shifts due to traps, or to apply self-heating pulses in between writing cycles to partially redistribute the generated defects from the IL to the FE-HfO_2 [87]. Finally, as pointed out in [41], [42] (for PZT and HZO MFM capacitors, respectively) increasing rise/fall edge time is expected to improve endurance because of less transient overshoots that reduce the impact of HAD.

C. Variability

Device-to-device variability causes identically fabricated devices to have different performance, especially at ultra-scaled dimensions [110]. Furthermore, variability in memory devices negatively affects read margins. Variability in FeFETs is related to the non-uniformity of the polycrystalline FE-HfO_2 layer (than can lead up to the full closure of *MW* in ultra-scaled devices [6], [111]) and to the intrinsic stochastic nature of polarization switching [112], [113].

Polycrystalline FE-HfO_2. As discussed in Section II.A, FE-HfO_2 layers present various polymorphs [24], [25]. Therefore,

FE-HfO_2 layers may include both the ferroelectric, orthorhombic phase and the paraelectric, monoclinic and tetragonal phases [114]–[117] giving rise to, among other effects, non-uniform polarization switching. By means of 'atomistic' TCAD simulations, Liu *et al.* found that *MW* is largely affected by the random paraelectric-like grains in the ferroelectric (both in number and size, as well as position) and that the distribution of both high- and low-V_{TH} state widens with gate area scaling and grain size [118]. Particularly, variability is maximized when the random paraelectric grains align along the channel to form a "DE path", making the FeFET behave as a regular high-κ MOSFET (i.e., with no non-volatile property) [118].

Switching stochasticity. On top of the polycrystallinity of FE-HfO_2, the stochastic nature of the orthorhombic grains switching kinetics causes additional variability [113], [119], [120]. Different models have been proposed to describe the mechanism leading to polarization reversal, i.e., phenomenological Merz's law, Kolmogorov–Avrami–Ishibashi (KAI) model, and Nucleation Limited Switching (NLS) model. These will be discussed more in detail in Appendix B. Generally, polarization switching process consists in the nucleation and growth of domains oppositely polarized with respect to the initial state [121]. In the most simplistic, two-bit case, switching from one state to the other happens with higher probability if a larger writing pulse amplitude or width is applied [81], [119], [122].

Mulaosmanovic *et al.* first showed a distribution of discrete (partial) switching events in scaled FeFETs – allowing for the stabilization of multiple V_{TH} states – which were attributed to the switching of multi-domains [119], [122]. This peculiar behavior was also confirmed by Monte Carlo simulations of ferroelectric switching, indicating that variability is intrinsic to the particular E_C (and thus switching time constant) of each domain [113].

Moreover, switching time depends on device area and cycling as shown in [123]. For large area devices, the high number of grains (note that one grain can contain multiple domains [121]) reduces the variability, making switching more uniform [113], [124]. On the other hand, the reduced number of grains in state-of-the-art 28-nm or 22-nm FeFET technology causes considerable device-to-device variability that in turn considerably reduces the mean *MW* (i.e., read margins) [6]. Recent Monte Carlo simulations shows that for devices with relatively few grains, the *MW* could be completely overwhelmed by the device-to-device variability [113], [124]. For these devices, practical application would require optimization strategies such as write pulse engineering.

The presence of defects in the FE-HfO_2 layer can cause an increase in switching time [123] and/or a broadening of the distribution of the switching events [121], [125], further exacerbating variability. Nevertheless, sub-ns polarization switching in highly scaled FeFETs was achieved in [126], [127], proving the excellent potential of FeFETs for high-speed applications. Interestingly, intrinsic variability due to switching can be exploited to create novel computing/security primitives such as random number generators [128]. These novel applications (and associated reliability issues) are discussed more in detail in Sec. VI.

Ni *et al.* proposed variability mitigation strategies that either are dedicated to: *i)* reducing the grain size (i.e., increasing the number of switching elements for a given area) by adopting proper processing techniques (e.g., increasing annealing temperature or duration [129], enhancing electrode surface roughness), or *ii)* improving domain switching uniformity by applying larger writing pulse amplitude and/or width [124].

It is important to recollect that the previously discussed variability issues related to the FE-HfO_2 layer add up to the variability sources of the underlying MOSFET (e.g., random-dopant fluctuations, RDF, line edge roughness, LER, work-function fluctuations, WFF) which in practice might also limit the distinguishability of memory states depending on the transistor dimensions and technology node. So far, only a few studies have been devoted to analyze the impact of traditional variability sources on the performance of FeFETs for both logic [130], [131] and memory [132] applications. A recent study found that while MOSFET-related variability are enhanced by higher P_s (i.e., saturated polarization), P_r, and E_C values, the random distribution of these parameters (due to non-uniform FE-HfO_2) are much more affecting the V_{TH}'s distribution of the analyzed FeFETs [133]. Further investigations are required to better elucidate the relative importance of variability due to FE-HfO_2 and MOSFET-related sources as well as their interplay.

D. Trade-offs Among the Metrics

Designing HfO_2-FeFETs to maximize one specific metric (e.g., *MW*, retention, endurance, etc.) might come at the expense of the others. The so-called "polarization-endurance dilemma" is arguably the most important one, as it clearly indicates that increasing P_r (to increase *MW*) leads to reduced endurance in HfO_2-FeCAPs [12], [15], [62], [64], [134]. This trade-off also affects FeFETs, leading to endurance-*MW* and endurance-retention dilemmas, as shown in Fig. 14 (note that P_r was substituted with *MW* because it is more appropriate for FeFETs).

In general, increasing *MW* (retention) by design comes at the price of reduced endurance, as indicated by the trend lines in Fig. 14. Regarding the endurance-*MW* limits, since endurance is primarily limited by degradation of the IL, which is accelerated by E_{IL} (i.e., electric filed in the IL), to a first approximation we can write

$$MW_{MAX} = (2E_C t_{FE}) \times \eta \quad (3a)$$

$$Endurance \propto E_{IL}^{-1}, \varepsilon_{IL}, E_C^{-1}, \varepsilon_{FE}^{-1}, P_r^{-1}, Q_{comp}^{-1} \quad (3b)$$

MW_{MAX} in Eq. (3a) is the maximum memory window of the pristine device, where $\eta < 1$ is a parameter that depends on E_C, P_s, P_r, ε_0, and ε_{FE} [81], [135]. Eq. (3b) embeds the quantities that determine endurance; particularly, Q_{comp} is the compensation charge of the bound charges (i.e., polarization) accounting for fixed charges, trapped charges, etc. In practice, Q_{comp} accounts for the increase over time of the parasitic charges compensating polarization, and thereby reducing *MW*. Eq. (3) expresses the *MW*-endurance trade-off in terms of parameters related to the FE and IL which stems from the balance of displacement fields in the two layers (i.e., $D_{FE} = D_{IL}$) [136]. This balance implies that in general endurance is expected to worsen for larger *MW*-FeFETs (depending on the ferroelectric/dielectric parameters),

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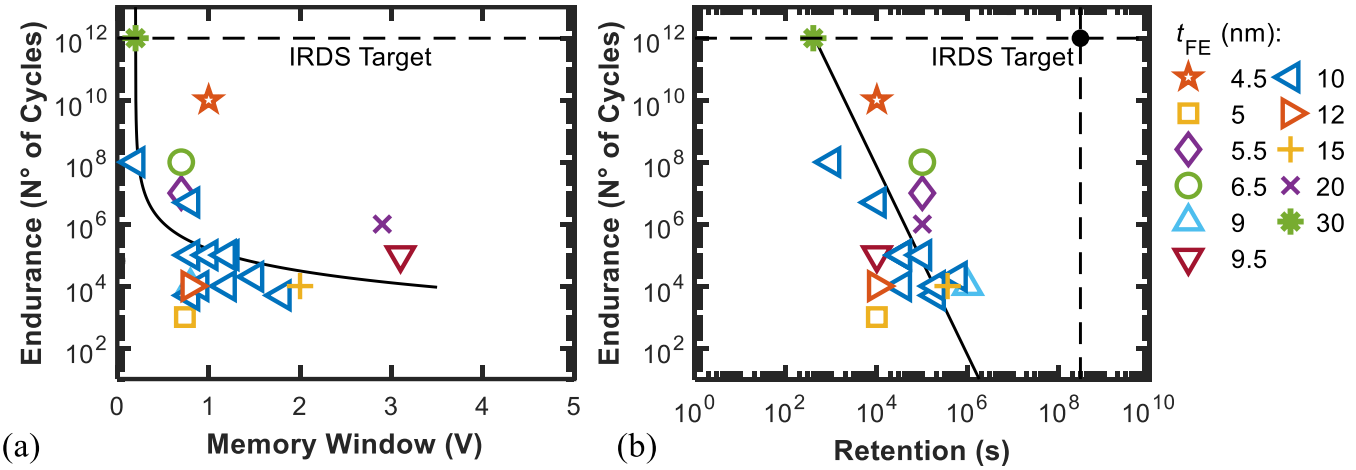

Fig. 14. (a) Endurance-*MW* and (b) endurance-retention dilemmas of HfO_2-FeFETs. Retention refers to maximum measured value (not projected one) at maximum temperature. International Roadmap for Devices and Systems (IRDS) targets for both metrics are indicated. Black solid lines are guides to the eye. Data taken from reports in the literature [5], [6], [10], [57], [60], [61], [73], [77], [80], [81], [83], [87], [90], [94], [97], [105], [122], [197], [200], [201].

see Fig. 14(a). In addition, the evolution over time of *MW* (which influences endurance) is determined by the compensation rate of polarization by the parasitic Q_{comp} [93], [98].

We stress on the fact that the trend lines in Fig. 14 should be intended as mere guides to the eye applicable to the selected set of data and might not be indicative of more general trends, especially in the case of endurance-retention trade-off. In fact, the latter trade-off can assume different forms depending on the device at hand. In this regard, we now describe the different strategies aimed at maximizing FeFETs metrics and the related trade-offs.

- Switching time t_{SW} (defined as the time required to reach domain nucleation [119]) can be reduced by increasing writing pulse amplitude (V_w) for a fixed writing pulse duration (t_w), and viceversa; however, the reduced t_{SW} could accelerate polarization back-switching hence increasing retention loss. In addition, decreasing t_{SW} through either increasing V_w or t_w can also be detrimental for endurance [20], [22], [93], [97].
- Generated traps during writing cycles could also degrade retention [9] because of the consequent increase in gate leakage that accelerates retention loss [29]. Therefore, using high-κ oxides as the IL insulator as a strategy to improve endurance can be also effective to increase retention because of the reduced charge trapping and leakage [104].
- Increasing endurance by operating the device in such a way that the *P*-*V* follows minor/sub-loops instead of the fully-saturated one [103] can be detrimental for retention, as shown for instance in [137].
- Doping FE-HfO_2 with lanthanum (La) impurities reduces formation of oxygen vacancies, thus improving endurance. However at the same time, La-doping induces formation of non-polar tetragonal phase which reduces polarization and increases depolarization field [50], [138].
- Using an anti-ferroelectric (AFE) configuration (i.e., double symmetric hysteresis loops, with $P_r = 0$) leads to a reduction of the switching field that in turn reduces the field stress over the IL compared to the FE counterpart [67]. Nonetheless, the reduction of E_C achieved by employing AFE over FE-HfO_2 would not only decrease the *MW* but also increase E_{dep}/E_C which is detrimental for retention [67].
- Increasing V_w at fixed t_w is expected to increase *MW* [139] and to reduce variability [124] but it worsens endurance due to enhanced field across the gate stack [97]. A rule of thumb in this regard is that endurance decreases with increasing *MW* (endurance-*MW* dilemma), as already shown in Fig. 14(a).

The inverse proportionality between *MW* and endurance holds true while V_w does not exceed the value for *MW* saturation due to full switching of the ferroelectric polarization. In fact, increasing further V_w might lead to increased charge trapping hence reducing *MW* [139] (and also endurance) but possibly improving retention due to reduced E_{dep} [74], see Eq. (2). Unfortunately, there is a considerable scatter of data in the literature, see Fig. 14, due to different measurement conditions, different geometries of FeFETs and also definition of endurance/retention, which complicates the identification of the trade-off trends. Clearly, however, endurance and retention are related to each other as both are influenced by the presence of traps in the stack, by leakage, and – most of all – by the degradation of the IL. In this sense, we argue that the most effective technique to improve both these metrics – without considerably altering device structure and process – is to make use of high-κ insulators (e.g., SiON [104], SiN [77], AlON [83], [101]) to reduce leakage and the field across the thin IL layer.

VI. Application-Specific Reliability

The previously described reliability metrics of HfO_2-FeFETs need to be interpreted according to the specific application for which the device is intended. Because the structure of the FeFET inherently couples the logic capability of a transistor with the nonvolatile memory of the FE layer, it makes this device a very attractive option for a variety of applications, such as: *i*) NVM inside of computational units to enhance logic

TABLE II
RELATIVE RELEVANCE OF APPLICATION-SPECIFIC RELIABILITY ISSUES

	Retention	Endurance	Variability
NVMs	++	+	=
LIMs	+	++	=
Neurons	=/✓	++	=/✓
Synapses (Online Training)	+	++	+
Synapses (Offline Training)	++	–	+
TRNGs	–	++	+/✓
PUFs	++	–	+/✓
Coupled Oscillators	++	=	+

Legend: ++ Most Critical Issue, + Critical Issue, = General Issue, – Not an Issue, ✓ Exploitable

functionality [140], [141], *ii*) LiM elements [142], where computation is performed within memory arrays, *iii*) neuron [143], [144] or synapsis-like [145]–[147] element in neural networks, *iv*) true random number generators (TRNGs) [128] or physically unclonable functions (PUFs) [148], and *v*) novel computing primitives based on oscillatory circuits [149], [150]. For each application, FeFET limits of operation in terms of switching speed, energy consumption, reliability and variability must be carefully weighted in order to identify the most appropriate circuit/system architecture (and vice-versa) [17].

We briefly discuss the most critical reliability aspects for each application, keeping in mind that design and architecture affect the considerations presented in the following.

- **NVMs**. Retention is the most critical concern, as it should be high enough even at relatively high temperatures, especially for specific environments (e.g., automotive applications). Endurance is however the second most important limiting factor, due to the need to store data in FeFETs. However, FeFETs have the opportunity to challenge NAND Flash memory, the endurance of which can already be achieved with state-of-the-art FeFET devices. Variability remains a general concern.
- **LIMs.** Endurance is critical due to the necessity to execute the instructions directly on the FeFET device. This in fact requires repeated writing operation which is ultimately limited by endurance. The endurance constraint can be greatly relaxed by careful design that assigns FeFETs to store the bits that change occasionally during operation [16], [140]. In some cases, decent retention is required to prevent high bit error rate values during readout. Variability remains a general concern.
- **Neurons.** Accumulative switching by applying an appropriate sequence of "sub-threshold" programming pulses (i.e., pulses that are associated with a very small, yet non-zero, switching probability) is exploited to synthesize the biological 'integrate-and-fire' neuron operation [144]. As in LiMs, endurance critically limits writing capability; retention, depending on the required duration of the neuron state might also be important, although typical neurons are refreshed by the network in which they belong at a rate that lies in the ms – s range. However, low retention might be exploited to reset the neuron state in some networks, simplifying the control circuitry [144]. Intrinsic variability due to stochastic switching might be exploited to mimic the probabilistic nature of biological neuron activity [144], with the requirement that process variations are not dominant (see also Sec. VII.D).
- **Synapses.** Depending on the programming scheme, i.e., on- or off-line training, the most detrimental reliability metric varies. On-line training requires FeFETs re-programming during operation, hence endurance is the most limiting factor, especially in large networks where achieving high accuracy requires time-consuming training, associated with a large number of synaptic weight updates. However, since FeFET programming in this case involves multi-level, gradual switching rather than full, binary switching [145], [146] endurance might not be critical [103]. Conversely, in off-line training schemes programming occurs ideally only once, hence (multi-level) retention becomes more crucial, including aspects related to noise immunity and temperature drifts. Variability is also critical, and specific write-and-verify circuitry must be devised to compensate for possible programming errors.
- **TRNGs.** The randomness capability is realized by setting the writing conditions such that switching occurs with ≈50% probability [128]. Stability with temperature and cycling of the $p_{0.5}$ state is crucial to achieve TRNG operation. Hence, endurance is largely more critical than retention. Stochastic switching induced variability must be larger than that introduced by the process, otherwise randomness might be wrongly induced by the latter than by the former.
- **PUFs.** Similar to TRNGs, switching is induced with a pre-defined probability (ideally = 50%) by applying appropriate writing conditions [148]. PUFs need to achieve high output repeatability and uniqueness, for which high retention (also at high temperatures), noise margin and robustness against process variation are required [148].
- **Coupled oscillators.** These circuits are based on coupled FeFETs biased in such a way that bistable oscillatory switching between polarization states is achieved enabling a series of computational capabilities [149]. Retention of the state is most critical, as stable oscillation must be retained over time; variability is also critical as oscillation is established over a specific range of operation [149]. Endurance might not be a critical issue as long as oscillation occurs between states that do not induce excessive trap generation.

Tab. II summarizes the relative relevance of retention, endurance, and variability for each application. As a general remark, it should be pointed out that to avoid the endurance limitations and charge trapping effects, HfO_2-FeFETs should be preferably integrated into circuits that do not require repeated writing of the ferroelectric memory during logic operation nor the immediate read-out after write [17]]. Therefore, FeFETs perform best in applications were their state is set only once and subsequently read-out several times, as it is the case for NVM arrays [17]] and also for neural networks used for prediction or classification tasks (with off-line training). This kind of scenario also ensures that the speed limits are not imposed by polarization switching – which is not less than 100 ps, and more frequently in the order of 10 ns [17]] – but rather by the delay of the logic gates and hence by the clock.

VII. Conclusions and Research Opportunities

In this paper, we have comprehensively covered the reliability issues that affect operation of HfO_2-FeFETs. For each reliability issue, we focused on the physics of these reliability concerns allowing us to clearly identify the mechanisms associated with both the ferroelectric layer and the MOSFET and the strategies to mitigate them. This review allows us to identify a set of research problems that we envision to be critical for driving the field forward.

A. Development of Novel Characterization Methodologies

Novel characterization tools and protocols are instrumental to monitor the evolution of *MW* over time (e.g., on-the-fly characterization) and to estimate the concentration of trapped charge. For instance, spatial position of traps in FE-HfO_2 and their influence on local electric field (and thus on polarization) should be considered instead of assuming uniform trap interfacial layers (e.g., at FE/IL interface). This is further discussed in Appendix A.

B. Comprehensive Assessment of Reliability Issues

So far, reliability investigations of HfO_2-FeFETs focused on the evaluation of retention and endurance mostly. Recent studies however, pointed out the relevance of issues such as self-heating [87], hot-carrier injection [84], hot-atom damage [151], and radiation [85]. These effects need to be more thoroughly assessed to determine the feasibility of HfO_2-FeFETs for new application scenarios such as in harsh environments (e.g., space).

C. Careful Reliability Physics Interpretation of Novel FEOL and BEOL FeFET Transistors

In [84] the observed degradation in endurance with increasing temperature was ascribed to the increased hole injection due to hot electrons. Further, this study showed that bulk traps generation is less of a concern for 4.5-nm thick FE layers [84]. This result indicates that, analogously to classical MOSFET, reliability physics of thick and thin dielectrics is much different. Thus, as HfO_2-FeFETs dimensions scale – with $t_{IL} < \approx 2$ nm, $t_{FE} < \approx 10$ nm, and $L_G < 30$ nm [152] – reliability physics must be carefully interpreted to correctly identify the degradation mechanisms. The need for careful reliability analysis applies to the case of different FeFET structures such as Dual-Gate [153], FinFET/Nanowire [126], [133], [154], Back-gate [94], [155], 3-D vertical structures [156], Non-Si channel FETs [94], [155], [156], etc. In fact, each non-conventional FeFET technology (i.e., that represents an evolution of the one discussed in this work) has unique self-heating and thermal-crosstalk challenges that affect reliability. In particular, the possibility of integrating FeFETs in the backend of the line (BEOL) stack has attracted considerable interest, especially in the context of monolithically integrated 3D circuits [94]. However, as recent literature on BEOL-integrated oxide transistors suggests [157], one may then have to grapple with new degradation pathways not observed in conventional frontend transistors, which calls for specific reliability studies.

D. Thorough Identification of Variability Sources

As mentioned in Sec. V.C, variability sources due to both FE (i.e., P_s, P_r, and E_C), MOSFET (i.e., RDF, LER, WFF, etc.), and process (i.e., geometrical parameters systematic variations) need to be considered simultaneously in order to reveal their possible interplay. Variability can be exploited for different purposes (such as RNGs, PUFs, biological neurons) but it can only be exploited if *desired* variability (due to stochastic polarization switching) is not overcome by the *undesired* variability (coming from other sources).

E. Definition of Reliability-Aware Figures-Of-Merit

Similar to power devices, developing Figures-Of-Merit (FOMs) that simply relate key device parameters (e.g., P_r, E_C) to one another are extremely important to drive forward technology development. Moreover, these FOMs should be reliability-aware, in the sense that they should be capable of capturing performance evolution over time [158]. For instance, in FeFETs, as also pointed out in [136], the optimization of displacement fields $D_{FE} = \varepsilon_0\varepsilon_{FE}E_{FE} + P_r$ and $D_{IL} = \varepsilon_0\varepsilon_{IL}E_{IL} + Q_{comp}$ (Q_{comp} was defined in Sec. V.D, see Eq. (3b)) through parameters tailoring can help to obtaining the optimum design for *MW*, retention, and endurance at the same time.

F. Systematic Reliability Evaluation on Large Data Sets

Current research on reliability and variability of HfO_2-FeFETs is mostly conducted at academic level, partially explaining the large scatter in performance/reliability metrics as shown in Fig. 12. The field would thus greatly benefit from experiments (developed from industrial-university partnerships) carried out systematically on large amounts of good quality samples (e.g., fabricated with an industrial process). One such example is [159]. For instance, this would allow to build more accurate reliability-aware models and to identify performance/reliability trade-offs.

G. Role of Disturbances Associated with Memory Architecture

Proper operation of HfO_2-FeFETs needs to be evaluated in the specific context of the specific memory architecture in which they are employed (e.g., 1T arrays). This is because the reliability of the single devices in general is influenced by the neighboring cells causing the so-called write disturbances [73], [160] that can account for a large fraction of the total degradation [161]. A recent study on HfO_2-FeFETs arranged in AND-array architecture discussed possible strategies for disturb-free operation [162]. More research is required to

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evaluate the suitability of HfO_2-FeFETs for different architectures and to determine whether restrictions on architecture design (like erase at block level in Flash memories) and/or density need to be put forth to ensure reliable operation.

H. Establishment of Reliability-Aware Models

Reliability-aware modeling tools are required to enable variability/reliability assessment at circuit/system level, for instance to assess the hidden impact of indirect write disturbances as discussed previously. More specifically, process development kits (PDKs) at industrial level should be augmented with reliability models (e.g., accounting for trap generation, leakage, etc.) to correctly assess device functionality over time. In general, future reliability-aware modeling efforts should focus on the accurate, quantitative, physics-based modeling (e.g., by means of numerical device simulations combined with experimental characterization) of the degradation mechanisms at the basis of retention loss, endurance, variability, etc. to provide engineers with predictive tools for technology optimization. An overview of modeling frameworks for HfO_2-FeFETs is provided in Appendix B.

Concluding, the promises of HfO_2-FeFET can only be met if performance is boosted taking into consideration the reliability requirements. Careful designs must satisfy both at the same time. This calls to the implementation of trade-offs that can only be best tailored by understanding reliability down from the physical mechanisms up to the application-specific requirements. This article is intended to provide a comprehensive guide to current and perspective experts to achieve this fundamental goal.

APPENDIX A: CHARACTERIZATION TECHNIQUES

Electrical characterization techniques and methods strongly influence the correct interpretation of reliability data and of the underlying physical mechanisms as well as the extraction of key parameters (such as trap concentration). Several different works apply different writing/reading schemes, acceleration tests, etc., that render data comparison and benchmarking often inconsistent and – possibly – misleading. Here we give a brief summary of the tests and characterization strategies often employed to assess FeFETs retention, endurance, variability, and the interplay of the physical mechanisms that limit lifetime of these devices.

Besides electrical characterization techniques, it is important to mention that specific material characterization techniques for FE-HfO_2 are also required to determine the fraction of orthorhombic phase with different dopants, deposition techniques, etc. For instance, Park *et al.* presented an X-ray diffraction based phase analysis to quantify the influence of different dopants on the ferroelectric properties of HfO_2 (e.g., P_r) which in turn influence reliability [163].

A. P-V Loop Measurements

In FeCAPs, *P*–*V* loops are mostly derived indirectly through monitoring of the current through the stack when applying triangular-shaped voltage inputs. Conversely, in FeFETs characterization of the *P*–*V* loop differs from that of MFM stacks (even for the same ferroelectric material and thickness) because of incomplete charge screening and influence of underlying and capping layers on the FE-HfO_2 [164]. In fact,

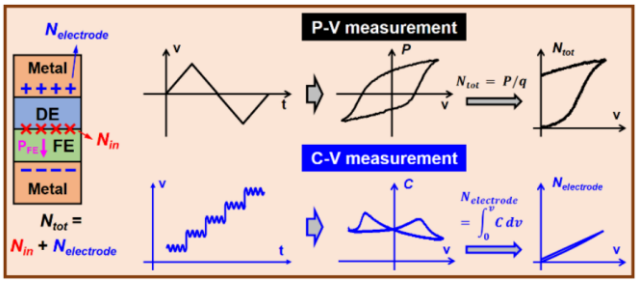

Fig. 15. Illustration of the measurement techniques to probe polarization and screening charge. *P*-*V* curves are obtained from quasi-static, large-signal measurements and as such allow extracting the total charge, N_{tot}, in the gate stack. Conversely, *C*-*V* curves are obtained from high-frequency, small-signal measurements and as such allow extracting only the electrode charge, $N_{electrode}$, corresponding to the charge in the semiconductor (partially) screening the polarization. The remaining charge contributing to polarization screening is attributed to injected charge at the FE/DE interface, N_{in}, and is obtained simply as $N_{in} = N_{tot} - N_{electrode}$. Reproduced from [167].

relatively low doping of the semiconductor body in FeFETs can cause the deep-depletion effect, that impedes the formation of the inversion layer required to screen the polarization charge and thus to correctly characterize the *P*–*V* loop [164]. The prescription in this case is thus to either use low-frequency signals to allow for the thermal generation of the inversion carriers, or more effectively, to short source, drain and body contacts together in order to allow the flow of the required screening charge even under high-frequency operation [164].

B. Careful Estimation of the Screening Charge

As pointed out in [136], a large mismatch between ferroelectric polarization and semiconductor charge (i.e., depletion + inversion or depletion + accumulation) exists which raises the question of where the required screening charge is coming from (this question was also raised for MFIM structures [165]–[167]). Several recent studies [165], [167]–[169] have discussed the origin of this screening charge and associated it with the presence of defects at the FE/IL interface (or at the FE/DE interface in a MFIM structure). To characterize the screening charge, a combination of quasi-static split *C*-*V* (QSCV) and small-signal split *C*-*V* (SSCV) (or Hall characterization) measurements must be carried out to probe the total gate charge (i.e., including the ferroelectric polarization) and the inversion (electrode) charge on MFIS (MFIM) structures [167]–[169] as schematically illustrated in Fig. 15.

First quantitative reports of the trapped charge at the FE/IL or FE/DE interface gave values in the order of ~10^{14} cm^{-2} [167], [168], which is surprising for annealed, atomic-layer deposited films. Deng *et al.* [169] later revealed that the estimation was probably affected by improper characterization of the actual switching charge and extracted more realistic trapped charge density of ~10^{13} cm^{-2}. This latter result was achieved by observing that the actual switching charge is obtained by applying a sequence composed of a switching pulse followed by a non-switching pulse (i.e., analogous to the widely used P-U-N-D scheme). This pulse sequence allows to effectively separate the reversible and irreversible switching components of polarization switching [169]. Nevertheless, defects in the FE-HfO_2 layer are mostly oxygen vacancies/ions that do not act as

fixed traps but rather as mobile species [38]. Therefore, spatial distribution of defects as well as the local influence on electric field (and polarization) of said traps need to be properly modeled to extract plausible volumetric (rather than interfacial) concentrations.

APPENDIX B: MODELING FRAMEWORKS

Here we summarize the modeling frameworks used to describe many aspects related to HfO_2-FeFETs, namely: polarization switching, *P–E*/*P–V* relationship, non-uniformity of ferroelectric layer, retention, endurance, and variability.

A. Polarization Switching

A phenomenological description of polarization switching is given by the simple Merz's law [121] which relates the polarization switching time τ to the applied ferroelectric field (E_{FE}) as follows

$$\tau \sim \exp(E_A/E_{FE}), \tag{4}$$

where E_A is the temperature-dependent activation field (which is a property of the ferroelectric material). This simple empirical description of polarization switching however fails to capture the underlying physical mechanisms, namely domain nucleation and domain walls motion [121] that start occurring when applying fields larger than E_C. A more accurate description is obtained with the NLS model, that describes the evolution of polarization over time as follows

$$\Delta P(t) = 2P_s \int_{-\infty}^{\infty} \{1 - \exp[-(t/\tau)^n]\} F(\log\tau) d(\log\tau) \tag{5}$$

where $F(\log\tau)$ is the distribution function of switching time τ, often described with the Lorentzian distribution [121], [126]. In the NLS model, the ferroelectric is characterized as an ensemble of grains switching independently from one another with a distribution of time constants given by $F(\log\tau)$ [170]. Note that by assuming a delta-function distribution of switching time in Eq. (5), the KAI model is obtained [121]. NLS model assumes that: *i*) domain wall motion stops at the grain boundary and does not propagate to an adjacent grain, *ii*) switching of a grain occurs once corresponding domains with initial opposite polarization are nucleated (i.e., reversed), and *iii*) time of domain wall motion after nucleation is negligible with respect to the first nucleation event [113]. A generalization of the NLS model was proposed in [113] to account for the polycrystalline nature of thin ferroelectrics as well as the variability due to domains having random distribution of activation energies (and thus nucleation rate constants).

Starting from the NLS model, a simple relation between the switching time and writing conditions was derived in [119], which reads

$$t_{SW} = t_0 \exp\left[\frac{c}{k_B T} \cdot \frac{1}{V_{SW}^2}\right] \tag{6}$$

where t_0 is the minimum switching time, k_B is the Boltzmann constant, T is the temperature, c is a material-dependent parameter and $V_{SW} = (V_G – V_0)$ is the switching voltage (V_0 being an offset [171]), i.e., the voltage at which polarization switching occurs during writing. This relationship was experimentally verified for a large number of devices, with different dimensions, with different measurement conditions, temperature etc. [119], [120], [171], [172] indicating that switching behavior is universally determined by Eq. (6). Fig. 16 illustrates Eq. (6) and its capability to reproduce experimental data [171].

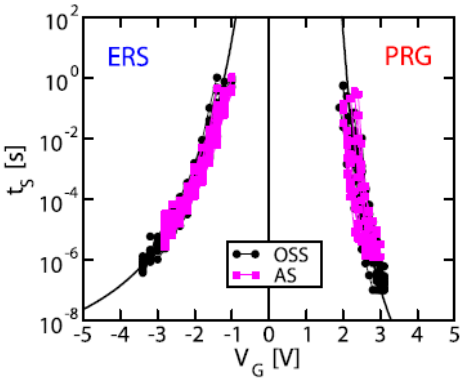

Fig. 16. Typical t_{SW}–V_G data for both erase (ERS) and program (PRG) states. Data was obtained on 15 different devices with different areas, and with two different programming schemes, namely AS = accumulative switching and OSS = one-shot switching. Data is well represented by Eq. (6) (solid lines), indicating a universal time-voltage relationship. Reproduced from [171].

Recently, a compact polycrystalline HfO_2-FeCAP model was employed [173] to describe polarization switching by simplifying the polarization dynamics as described by NLS model to a first-order differential equation finding good agreement well with experimental data from [113], [174]. This model could possibly be extended to efficiently model FeFET switching dynamics.

B. P-E Relationship

Preisach [73], [175]–[177] and Landau-Devonshire (LD) models [99], [178]–[180] are mostly employed to describe the *P–E* relationship in ferroelectrics. The first one defines the *P–E* loop by means of hyperbolic tangent functions, whose branches are shifted depending on the history of the applied field and upon overcoming of E_C. Preisach model for the "saturation loop" reads

$$P(E) = P_s \tanh\left(\frac{E \pm E_C}{2\delta}\right) \tag{7a}$$

$$\delta = E_C \log\left(\frac{P_s - P_r}{P_s + P_r}\right)^{-1} \tag{7b}$$

which can be extended to model sub-loop operation [73]. The advantage of this model is its compact formulation which can be easily employed in circuit simulators [181] and augmented, at least in an empirical form, to account for transient effects and switching.

Landau-Devonshire (LD) model is derived from the physics of phase-transition [182] and describes the energy landscape characteristics of ferroelectrics, with two stable wells (corresponding to the polarization states) separated by an energy barrier. The *P–E* relationship in this case reads

$$E = \alpha P + \beta P^3 + \gamma P^5 - \rho \frac{dP}{dt} \tag{8}$$

where $\alpha, \beta, \gamma, \rho$ are material-dependent parameters [178]. Akin to the Preisach model, the LD model can also be used for circuit simulations [183] at it can also be augmented to include multi-domain effects [113], [184]. This model can be effectively used to derive a simple analytical expression for the *MW* [180] that can be extended to include trapped charge effects to assess the endurance of FE-HfO_2 based FeFETs [99], as also discussed in Appendix B.E.

C. Retention Loss

Despite several modeling efforts to correlate retention loss with E_{dep} have been presented, the physical connection between E_{dep} and polarization relaxation is still not well understood [46], [52], especially in FE-HfO_2. Nevertheless, semi-empirical models are available in the literature that describe $P(t)$ evolution due to depolarization field [35], [46], [47], [52]. For instance, in [52] the time evolution of polarization under the effect of depolarization field was assumed to be described by a first-order approximation differential equation. Assuming that $\Delta P(t)=(P_0-P(t))/P_0 << 1$ on short time scales and that $E_{dep}(t)\rightarrow E_C$, $P(t)\rightarrow P_\infty$ for $t\rightarrow\infty$, the solution can be approximated as follows:

$$\begin{cases} P(t) = P_0 - c_1 \times \ln\left(1+\frac{t}{t_0}\right), & t < \sim 1\ \text{s} \\ P(t) = P_\infty + c_2 \exp\left(-\frac{t}{t_s}\right), & \text{else} \end{cases} \quad (9)$$

where P_0 (P_∞) is the initial (final) polarization value, c_1 is the decay rate, c_2 a proportionality constant, t_0 (t_s) is a characteristic time (that can be extracted from the full equation of $P(t)$). The polarization decay rate due to depolarization field is independent of writing pulse amplitude because, according to Eq. (1), while a higher writing voltage increases the initial polarization it also increases E_{dep}. Hence, retention loss scales proportionally to initial polarization [35] and saturates on a long time range (in absence of leakage [46], [52]) to P_∞ which, in the case of MFIM structure, can be computed from Eq. (1) by setting $E_{dep} = E_C$.

The NLS model was also shown to be effective to capture the polarization loss in MFM capacitors [47]. In the work from Gong *et al.* [47] only the effect of depolarization field was considered, by implementing an iterative procedure that empirically connected the time-varying polarization with E_{dep} .[185] Generalizing this procedure to model retention loss in FE/DE and MFIS stacks requires a more accurate relationship between P_r and E_{dep}, as discussed in works such as [29] and [92] for FE/DE and MFIS stacks, respectively. A more comprehensive model was developed in [186] to account for charge injection and the associated retention loss.

D. Endurance degradation

In [99], Zagni *et al.* presented an analytical expression of the *MW* which included the degradation effects occurring during bipolar cycling/endurance tests due to trap generation and charge trapping in the IL. The model was calibrated against data from [97], in which the evolution of traps over number of cycles was quantified. The analytical formulation therefore relies on the knowledge about the IL degradation mechanisms and can be adapted for different FeFET gate stacks and transistor geometries. Ichihara *et al.* modeled degradation as a concurrent effect of P_s reduction and increase of polarization screening by charged traps with cycling, concluding that reduction of charging/dis-charging of IL traps is key to improve endurance [93], [98].

E. Variability

Kao *et al.* first proposed a TCAD modeling approach to account for the existence of non-ferroelectric grains (i.e., dielectric, DE, grains) inside the FE-HfO_2 (as discussed already in Sec. V.C) to more accurately model the *P–E* loop and applied it to study the negative capacitance effect [187]. Later, this modeling approach was adapted by Liu *et al.* in [118] to study the effect of random FE/DE grains on *MW* of FE-HfO_2 based FeFETs, which allowed them to reveal the detrimental impact of DE "leakage path" along the channel length on the *MW*, as already discussed in Sec. V.C. On top of this, various models to account for the random distribution of E_C as well as the non-uniformity of domains were developed to reproduce features of realistic devices such as switching kinetics [113], device-to-device variations [113], [124], [188], [189] and the gate-bias dependence of V_{TH} shift [78].

Variability due to the stochastic nature of switching can be assessed with the models presented in Appendix B.A, see also [113]. Variability due to MOSFET-related stochastic processes (e.g., RDF, LER, WFF, etc.) or process variations can be analyzed with either sophisticated atomistic [131] or simplified (but substantially faster) TCAD simulations [133].

APPENDIX C: GLOSSARY

Given the heterogeneity of the background of experts in the ferroelectric-devices community (e.g., material scientists, chemists, physicists, device/reliability engineers), we find it useful to include a list of widely used technical terms in this manuscript and in the literature.

- **Defect/Trap**: defects are physical (e.g., dislocations, stacking faults) or chemical (e.g., impurities, vacancies) alterations of a material [190]. When defects alter the electrical response of the material, they are called traps.
- **Degradation:** permanent performance loss as a consequence of prolonged device operation. According to reliability definition (see below), the amount of sustainable degradation sets the threshold for reliability.
- **Ferroelectric Domain**: group of grains with same polarization orientation. Domain boundary (often called domain wall) is the separation between domains with different polarization. Domain-wall motion is considered by KAI model to be the physical mechanism determining polarization switching [191], whereas the NLS model assumes domain nucleation to be the dominating mechanism [47], [113], [191]. Domain-wall pinning is the (local) hindering of their motion due to electric field generated by traps (e.g. oxygen vacancies) in the ferroelectric that reduce the domain switching response to an applied external bias [192]. Similar switching suppression can be caused by domain seed pinning [58].
- **Grain**: units with same polarization orientation or units with no polarization (as for dielectric phases). Grain boundaries arise between adjacent grains.
- **Polarization Relaxation**: is an electric-field driven process that reduces the domain nucleation energy barrier [45], so that opposite domain nucleation occurs, in turn reducing polarization over time. Modeling can be done with the KAI or NLS models considering a region-wise nucleation process [44]–[46].
- **Reliability:** the capability of a device to maintain the desired performance within a specified margin over a prescribed period of operation. In this sense, reliability is the time taken to a given threshold condition, at which the

required minimum margin for the performance metric under consideration is reached.

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