System-level Analysis for Integrated Power Amplifier Design in mmWave Consumer Wireless Communications

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Abstract. System-level specifications for the design of integrated power amplifiers in mmWave wireless communications are derived in the paper. To this aim emerging standards for consumer applications such as wireless ultra-high definition (UHD) multimedia streaming or Gbit wireless LAN are considered (WirelessHD, WiGig, ECMA387, IEEE.802.11.ad, IEEE802.15.3c and upcoming 5G). A power amplifier design in 65 nm CMOS Silicon on Insulator (SOI) technology, targeting a 9 GHz UWB window from 57 to 66 GHz, is also proposed. To increase the power delivered to the antenna up to 18 mW, being still in the limit of maximum 1dB compression point, multiple PA cores have been combined through a Wilkinson power combiner, but other solutions can be also explored for a better power efficiency and linearity.

1 Introduction

Emerging consumer applications in the millimeter-wave (mmWave) wireless domain for short-range multi-Gbps links pose new challenges for the design of the key blocks of the transceivers, particularly the power amplifier (PA).
Traditionally consumer wireless applications have been developed in a spectrum from few hundreds of MHz to 5 GHz. This portion of spectrum includes Bluetooth and Wireless Local Area Networks (WLAN) at 2.4 GHz or 5 GHz, domotic wireless applications or Radio Frequency Identification (RFID) for logistics in the ISM (Industrial Scientific Medical) unlicensed bands (typically sub-GHz bands are considered for this aim), radio and TV broadcasting in VHF/UHF bands, multi-band cellular communications from 800/900 MHz to 2 GHz. Being focused on large volume and low cost markets, these applications witnessed the development of the RF hardware equipment using low cost silicon technologies, BiCMOS and in the last years mainly CMOS. Most of the above systems are narrow band. Therefore, system specifications require that the relevant hardware building blocks should sustain a given performance (e.g. gain, noise figure ...) at high operating frequency, in the order of some GHz, but for a limited bandwidth. Efficiency problems at transmitter side are typically addressed using switching-mode amplifiers or class-C and class-E topologies.
On the other hand higher frequencies in mmWave spectrum (from 10 GHz to hundreds of GHz) have been addressed in the state of art though hetero-junction Bipolar transistors (HBT) and/or high electron mobility FET (HEMT) technologies such as SiGe HBT or GaAs, InP, GaN HEMT [1-3]. Main applications have been

radar transceivers not only for defense but mainly for civil applications, e.g. automotive radar at 24 GHz (short-range) or 77 GHz (long-range), mmWave body scanners for security (e.g., in airports, banks,...), mmWave imaging for medical applications, satellite communications. Heterojunction technologies, being characterized by a niche market, entails high costs for the wireless transceivers that cannot be justified in emerging mmWave consumer applications.
By exploiting the large spectrum available at mmWave, multi-Gbps links can be obtained with conventional modulations schemes and this can enable a lot of new services for consumer users in short-range home or office scenarios such as:
- Wireless Gbps LAN, realizing a convergence with already existing Gbps cabled connections like Gbps Ethernet or 100 Mbps FTTC (Fiber To The Cabinet), or announced Gbps FTTH (Fiber To the Home); convergence of mmWave wireless service and free space optical (FSO) services for last mile connections are also envisaged at the state of art.
- Ultra high definition (UHD) video playing and uncompressed multimedia streaming creating a wireless high speed network among 4K UHD TVs, UHD blue-ray players/recorders, tablets/smart phones, internet access points.
- Multi-view (3D already available) video playing and teleconferencing and digital holography applications.
The development of such applications at mmWave poses new specifications on the wireless transceivers (in terms of cost of the technologies to be used, bandwidth, power, linearity, gain ...) that cannot be addressed by traditional chipset. To this aim in Section 2 we derive from a system-level analysis the main specifications for PA in mmWave multi-Gbps consumer applications. An implementation in CMOS SOI technology is proposed in Section 3. Section 4 presents a comparison with recent state of art and draws some conclusions.

2 System-level Specifications for mmWave PA Design

Several standards and industrial consortia have been already proposed for mmWave consumer wireless applications [4-7]. The WiGig industrial consortium is promoting the development of multi-Gbps wireless connections. Besides classical 2.4 GHz and 5 GHz operating frequencies, also 60 GHz is considered in WiGig as a key operating band for the new generations of multi-band RF transceivers. The WirelessHD consortium is focusing more on UHD video and multimedia streaming, playing and recording and is envisaging the use of a 7 GHz spectrum around 60 GHz. With such a large channel even with simple modulations schemes with a few bits/Hz efficiency is easy to achieve up to 10 Gbps connections. From a standardization point of view these services are covered by standards such as the ECMA-387 or the IEEE 802.15.3c High Speed Interface PHY (HSI PHY) or the 802.11.ad [4-7]. As example, Fig. 1 shows the channelization and worldwide spectrum allocation in the ISM unlicensed band around 60 GHz highlighting multiple-channel bonding options foreseen in ECMA-387. The approach in Fig. 1 allows for scalable data traffic capacity since the wide spectrum from 57 to 66 GHz can be dynamically partitioned in multiple channels (hence allowing to multi services). The above considerations lead to a

specification of a transceiver operating around 60 GHz, with a large bandwidth of 9 GHz, and realized in silicon technologies, CMOS bulk or SOI version, to keep low the cost of the devices in large volume consumer markets. Considering that for analog and RF applications is not required to adopt the last (and more expensive) technology nodes (14nm/28 nm), target CMOS technologies between 90 nm and 45 nm can be addressed [8-10].

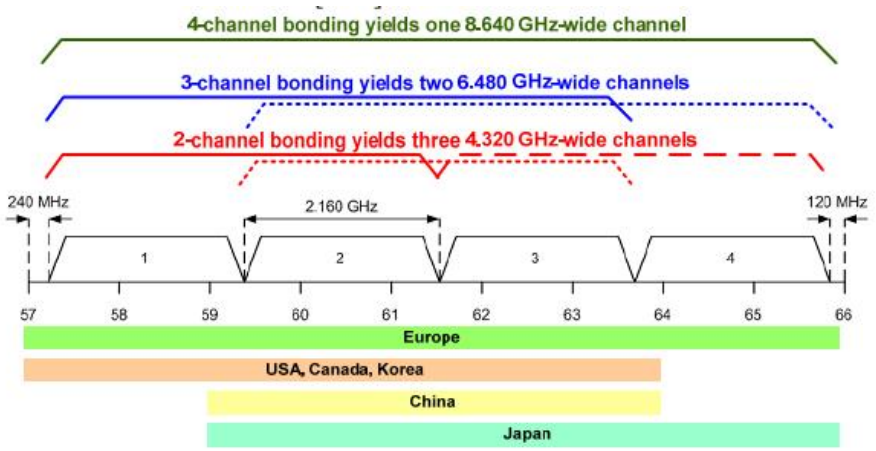

Fig. 1 Worldwide spectrum allocation for multi-Gbps mmWave communications in consumer applications and flexible channelization foreseen in ECMA-387

65 nm CMOS technologies are today mature. They allow for a good trade-off between performance and cost for all the different signal domains of a fully-integrated wireless terminal (analog baseband, digital, RF up to tens of GHz). The voltage supply considering battery duration should be at maximum 1.2 V, this influences at circuit level the design style limiting the number of transistors that can be stacked between supply and ground. On the contrary, ultra low-voltage designs (sub-thresholds circuits with few hundreds of mV supply have been proposed in literature) lead to more complicated circuit-level design limiting too much the output dynamic range, the performance of the transistors, and the transceiver robustness vs. external interference or changing environmental conditions.

Communication services around 60 GHz are also candidate to represent the high-speed connection part of the upcoming 5G wireless networking standard. 5G communication systems, whose deployment and commercialization is expected in 2020, intend to create a synergy among a variety of cellular and wireless LAN systems through the use of the heterogeneous networking (het-net) paradigm. The aim is to maximize the use of RF bandwidth by switching between different systems, based on channel availability at the local level. Among the key technology challenges towards this goal, let recall here the support for high data rates and the need for increased capacity in dense urban environments, both outdoor and indoor. Due to air and water absorption, transmissions in the mmWave band have shorter range than in the “sub-3 GHz” bands used for current cellular systems. This reveals a key advantage in high-density environments, allowing base stations to be situated closer

together. In particular, the portion of spectrum around 60 GHz (with wavelength of few mm) experiences a dramatic attenuation (about 15 dB/km) due to the presence of the absorption peak of molecular oxygen and as such it has been allocated worldwide for unlicensed services as reported in Fig. 1. The link distance to be covered is up to 10 meters in short-range home or office scenario. Considering also what is specified in the standards in terms of Bit Error Rate (BER), modulation and channel coding scheme and expected ratio between the average received energy per bit *Eb* and the one-sided overall receiver noise power spectral density N_0, denoted as Eb/N_0, the transmitted power for the transceiver should be about 10 dBm. As last consideration, we have to consider that standards building up the new 5 G generations massively relies on multi-carrier schemes. Due to large number of sub-channels, OFDM (Orthogonal Frequency Division Multiplexing) [11-13] is characterized by a high PAPR (Peak to Average Power Ratio) i.e. the signal has large envelope fluctuations.
As example in [1] a N-carrier OFDM signal with 4-DPSK modulation has a PAPR of about $10\text{Log}_{10}N$, i.e. roughly 18 dB and 30 dB for a 64-carrier and 1024-carrier OFDM signals respectively. The system degradation due to PA non linearity are [1] the following: additional interference in the receiver, spectral spreading of the transmitted signal which can cause adjacent channel interference, intermodulation effects when several channels are amplified concurrently by the same PA, interference between in-phase and quadrature components of QAM modulated signals due to AM-PM conversion. To avoid distortions a linear PA is needed, thus limiting the use of switch-mode and class C RF PA topologies. Table I summarizes the main specifications derived for the mmWave PA for consumer applications

Table I- Specifications for PA design in mmWave consumer communications

Topology	Peak Power	Center freq.	Band.	Tech.	Max. Supply
Class-A	10 dBm	60 GHz	9 GHz	CMOS bulk/SOI 45-90 nm	1.2 V

3 mmWave PA in 65 nm Silicon Technology

Giving the specifications derived in Section 2, see Table I, a class-A amplifier with a 2-stage Common Source (CS) topology and inter-stage LC matching networks has been designed in 65 nm CMOS SOI. The circuit schematic is reported in Fig. 2. At technology level we considered both a 65 nm bulk CMOS technology and a 65 nm SOI one, but for the final PA design we selected the SOI version. The bulk CMOS version allows for minimal fabrication cost being that used for large volume digital and mixed-signal baseband designs. The SOI version, thanks to its high resistivity substrate (1 kΩcm instead of standard 20 Ωcm), has several advantages vs. bulk technology for 60 GHz design of active and passive devices while avoiding the high extra costs of hetero-junction technologies (SiGe HBT, GaAs or InP HEMT and so on). The CMOS SOI allows for:
- reduction of substrate interference cross-coupling between different circuits integrated in the same chip;

- significantly reduction of junction capacitances so circuits can operate at higher speed or with lower power at the same speed;
- elimination of latch-up and better immunity to short-channel effects;
- reduced amount of energy stored in the supporting substrate leading to higher gains in case of on-chip integrated antennas.

From a circuit topology point of view a cascode topology is normally more efficient for achieving high gains, at low-voltage operation (1.2 V in our case), vs. the CS stage with a single transistor. However stacking the CS and the CG transistors in a cascode approach would determine a limited output voltage-swing that would compromise the output power 1dB compression point (OP1dB) performance of the amplifier. For multi-carrier OFDM systems with high PAPR the linearity and hence the 1dB compression point performance is a key figure of merit. As alternative to CS or cascode stages a folded-cascode topology could be employed cascading several stages, but this way the power consumption is nearly doubled vs. a conventional cascode. This is why we preferred a multi-stage class-A CS topology. To properly size the width of the MOS devices in the proposed class-A PA circuit we exploited the benefit of the invariance of the maximum linearity (and also maximum Ft) bias current density across technology nodes, 0.3 mA/μm as demonstrated in several works at state of art.

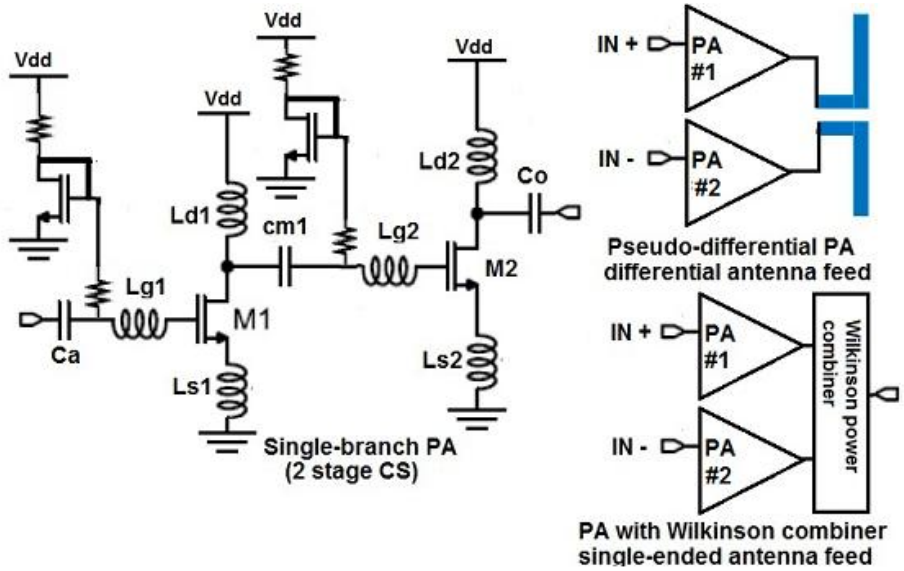

Fig. 2. 2-stage CS PA with pseudo-differential or Wilkinson power combiner

With a 1.2 V power supply, in CMOS SOI technology, the PA circuit shows an insertion gain of 7 dB (the S21 parameter) at 60 GHz varying from roughly 8 dB at 57 GHz to 6 dB at 66 GHz. The 1-dB input compression point IP1dB is 1.76 dBm while the OP1dB is 8.2 dBm (6.6 mW). The DC power is 44 mW. The peak PAE (power-added-efficiency) is 11.5 %. The return loss (S11 parameter) is always below -10 dB, in the target 57-66 GHz spectrum. The stability factor is $K > 4$ for all the frequencies from 57 to 66 GHz, resulting in the unconditional stability of the two-ports active network. To meet the 10 dBm system-level specifications about the transmit power

outlined in Section 2 (Table I) the power of 2 PA blocks of Table II is combined in a pseudo-differential mode if the antenna has differential feed or in case of single-ended feed through Wilkinson Power combiner. The Wilkinson combiner is a 3-port circuit capable of simultaneously achieving port-to-port isolation, impedance matching and ideally not dissipating power in the resistance across ports 2 and 3 when the two ports are balanced. As a result, the OP1dB of the whole amplifier in 65 nm CMOS SOI is 10.7 dBm with Wilkinson combiner (10% loss vs. ideal case) and 11 dBm in the pseudo-differential case. The Wilkinson power combiner can be used also in a cascaded mode to combine the power of 4 PA blocks in a single PA feeding the transmitter antenna: the OP1dB achievable power growths up to 12.51 dBm (roughly 18 mW) with about 25% loss vs. the ideal case of the x4 power level increase. To be noted that maximum output power where the amplifier saturates (Psat) is more than 4 dB above the OP1dB.
Obviously, by increasing by a factor K the number of PA blocks, taking into account also the extra circuit needed to combine their power towards the transmitter antenna, the total area and power consumption increases by a factor higher than K while the maximum transmitter power increases by a factor below K.

Table II- Performance of single PA block in 65 nm CMOS SOI at 1.2 V

IP1dB	OP1dB	S11 in 57-66 GHz spectrum	S21 in 57-66 GHz spectrum	PAE	DC power
1.76 dBm	8.2 dBm	<-10 dB	6 - 8 dB	11%	44 mW

4 Comparison to State of the Art and Conclusions

In our experiments, the power combination mechanism can be useful to meet transmitted power of 11.8 mW and 17.9 mW by combining 2 or 4 basic PA blocks respectively. Comparing these results vs. recent state of art [14, 15] it is worth noting that the above power levels refer to OP1dB and hence are obtained with a very high linearity (less than 1 dB compression vs. the ideal amplifier response). In state of art of mmWave CMOS amplifier for 60 GHz consumer applications such high power levels are typically obtained as maximum saturated power with higher distortions.
An area estimate (excluding pads) of the core for the structure with 2 PAs and a Wilkinson power combiner is about 0.11 mm^2 for each PA plus 0.1 mm^2 for the 2-way Wilkinson combiner for a total area of 0.32 mm^2. The DC power consumption is roughly 90 mW. The single PA channel has an area of 0.11 mm^2 and a DC power of 44 mW.
As future work, we are planning to exploit the whole amplifier curve up to Psat, including also the non linear part above the 1dB compression point, to increase amplifier efficiency by exploiting the low probability that in real OFDM transmissions certain power levels are reached. Also the utilization of an integrated Marchand Balun will be explored in the future to combine the output power of up to 8 transistors [16] so reducing the nonlinearities in the amplitude output characteristic

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