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Invited Paper

Real-time FPGA-based Radar Imaging for Smart Mobility Systems

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ABSTRACT

The paper presents an X-band FMCW (Frequency Modulated Continuous Wave) Radar Imaging system, called X-FRI, for surveillance in smart mobility applications. X-FRI allows for detecting the presence of targets (e.g. obstacles in a railway crossing or urban road crossing, or ships in a small harbor), as well as their speed and their position. With respect to alternative solutions based on LIDAR or camera systems, X-FRI operates in real-time also in bad lighting and weather conditions, night and day. The radio-frequency transceiver is realized through COTS (Commercial Off The Shelf) components on a single-board. An FPGA-based baseband platform allows for real-time Radar image processing.

Keywords: Real-time, RADAR signal processing, X-band FMCW (Frequency Modulated Continuous Wave), FPGA (Field Programmable Gate Array), Surveillance, 2D/3D Fast Fourier Transform (FFT)

1. INTRODUCTION ON IMAGING TECHNOLOGIES FOR SMART MOBILITY

Smart mobility systems for surveillance and/or for ADAS (Advanced Driver Assistance System) require sensing instruments tolerant to bad light and weather conditions. At the state-of-the-art video cameras are the most diffused sensing technology for smart mobility applications due to their availability at low cost. CCD (Charge Coupled Devices) cameras ensure higher image quality than CMOS (Complementary Metal Oxide Semiconductor) ones. The latter allow for single-chip integration of the sensing matrix, plus the read-out and digitalization circuitry, and even of signal processing tasks. The camera-on-chip approach saves space, power consumption and cost, which are key features in the large market of transport systems. However, video-based estimation of position and speed of targets (e.g. pedestrians, bicycle, motorcycle, trucks, railway, cars, ships) in a mobility system, suffer of accuracy and reliability problems in case of bad light/weather conditions.

LIDAR (LIght Detection And Ranging) is another type of sensors for mobility applications allowing for high accurate measurements of distance and, through time-of-flight processing, of speed. As example, the HDL-32E LIDAR from Velodyne [1] has 360° horizontal Field of View (FOV), 20° vertical FOV and allows for obstacle detection with an angular resolution of 0.01° (azimuth) and a distance resolution of 2 cm in the range from 1 m up to 100 m. The size is about 10 cm x 15 cm and the weight is about 1.3 kg. The frame rate is typically 10 Hz (user selectable, 5-20 Hz), and it is constructed to operate in the thermal range -10 °C to +60 °C and to ensure a protection grade IP67. The power cost is 12 W. By further reducing the array size to 16 channels, the VLP-16 LIDAR covers a detection range up to 100 m, with a resolution of 3 cm. It has horizontal and vertical FOV of 30^o and 360^o, respectively. The horizontal and vertical FOV resolutions are 0.1^0 and 2^0 respectively at 5 Hz. VLP-16 operates in the thermal range -10 °C to +60 °C and its package has a protection grade IP67. The power cost is 8 W and the size is about 10 cm x 7 cm for a weight of 0.8 kg. Although the above performances fit well the requirement of an active sensor for vehicle ADAS, the cost is a limit. About 8000 USD are required for VLP-16 and more than 10000 USD for the HDL-32E. Also LIDARs suffer of low robustness in harsh environment situations.

RADAR (RAdio Detection And Ranging) instead has the potentiality to allow for robust detection of targets and their speed, distance and motion direction also during night, or in presence of fog, rain, dust. At the state-of-the-art Radar sensing is typically realized for defense applications or big civil infrastructures [3-7], such as big ports or airports. As example, the pulse compression Radar in [6] operates in Ku-band with a transmitted power of 8 W. It has a detection range from 20 m to 3.7 km with a range resolution of 5 m. The total power consumption is 130 W and the weight 35 kg. The 32 kW peak power for the pulsed Radar in [7] allows for a 45 km covered range with further increased size and weight vs. [6]. The cost of these Radars is in the order of tens of thousands USD. The above characteristics are not suited

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for applications with limited budgets in terms of cost, power consumption, size and weight. Compact Radars operating at mm-waves (e.g. 24 GHz or 77-79 GHz [4, 8]) have been recently proposed, such as the LRR3 (long Range RADAR 3rd generation) sensor technology from Bosch [8]. This Radar sensor allows for target detection up to 200 meters, with a resolution of 10 cm. The FOV is 30^0; no rotating elements are used. The typical power consumption is 4 W, the weight is about 300 g. However, for surveillance applications in small harbour or in parking area 200 m may be not enough.

To overcome the state-of-the-art limit, this paper presents the design of a Radar imaging acquisition and processing platform, called X-FRI, with low power consumption and low complexity, but with performances still suited for smart mobility applications. Hereafter, Section 2 details the transceiver design of the Radar sensor considering both COTS and single-chip approach. Section 3 shows the digital signal processing implementation on FPGA. Section 4 proposes experimental results for some example applications. Conclusions are drawn in Section 5.

2. RADAR IMAGING FRONT-END AT RADIO FREQUENCY

The X-band (9-12 GHz) is a good choice for Radar working frequency, being a tradeoff among different parameters:

- the size of the sensing system and the antenna (proportional to the wavelength, which is roughly 3 cm at 10 GHz);
- the available bandwidth (B) which depends on the required resolution: 400 MHz are needed for a 40 cm resolution;
- the capability of CMOS technology to operate at such frequency, avoiding expensive heterojunction III-V technologies.

A remarkable effect of the X-band choice is that, for short ranges, rainfall, snowfall and fog cause negligible drawbacks on the target detection function of the Radar sensor, because the wavelength is much bigger than the water droplets and ice crystals involved in such weather phenomena. The attenuation of air and vapour in X-band is about 0.007 dB/km while at 77/79 GHz is more than one order of magnitude higher. Therefore, the same covered range at 77/79 GHz can be reached with much higher transmitted power or with a much focused beam than in X-Band, thus reducing the capability to monitor large areas. To keep low the power consumption and the electromagnetic interference (EMI) a FMCW Radar is the most suited choice. Differently from classic pulse Radars, emitting high peak power pulses from hundreds of W to kW, the FMCW Radar emits continuously much lower power levels working with the same Signal to Noise Ratio (SNR). A target distance of 300 m can be covered with an output power limited to 5 mW still ensuring a SNR of 20 dB at receiver side. If the target distance raises to about 1.5 km the same SNR can be reached but with a transmitted power increase at 2 W. The FMCW choice entails a more complex digital processing chain, but that can be implemented in real-time and low power with an FPGA platform. Fig. 1 shows the architecture of the Radar X-Band transceiver, developed in microwave IC technology, in the example case of one transmitting (TX) channel and two receivers (RX). Received echoes are processed by the baseband FPGA by extracting range-Doppler maps. To detect also the exact position of targets, or even to reconstruct their shape, multiple receiving channels have to be used: at least 3 to solve both azimuth and elevation. A linear FMCW approach has been followed: the frequency is periodically swapped, with a linear law and within a time frame T_{SW}, from f_{MIN} to a value $f_{MAX}=f_{MIN}+A\cdot T_{SW}$ (1).

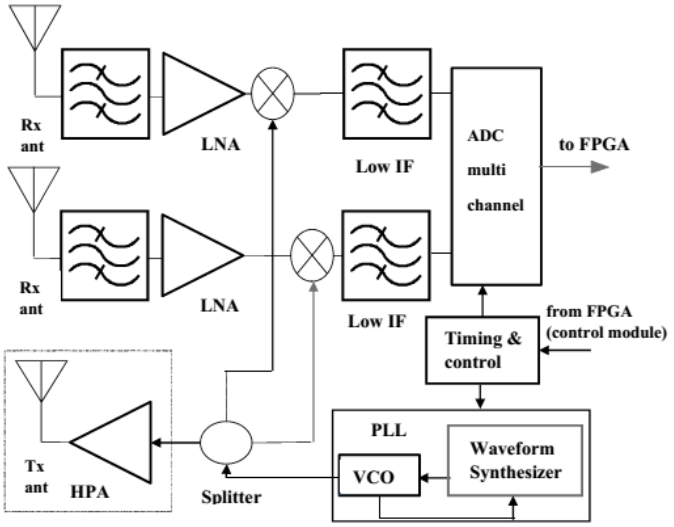

Fig. 1: Transceiver architecture of X-FRI (X- band FMCW Radar Imaging) system, configuration with 1 TX and 2 RX channels

The architecture in Fig. 1 is scalable so that the number of receiving channels can be increased. The instantaneous frequency $f_T(t)$ is generated in the scheme of Fig. 1 by a VCO (Voltage Controlled Oscillator), capable of operating with frequencies from 9.8 GHz up to 11.4 GHz, inserted in a PLL-based (Phase Locked Loop) waveform synthesizer. To this aim, the RFVC1843 VCO by RFMD has been integrated on the same microwave board with a Fractional N delta-sigma PLL capable of generating frequency ramps with sweeps of 400 MHz around a central frequency of 10.65 GHz in 100 µs. The FFT computation time for each frequency ramp of the signal processor, constraints the sweep time T_{SW} at a value of 175 µs. To avoid moving parts in the Radar sensing system, a fixed antenna approach has been followed. For the antenna design, both at receiver and transmitter side, X-band Fabry-Perot resonator technology was adopted to realize compact and efficient antennas characterized by the total absence of side lobes on the azimuth plane. Both the transmitting and receiving antennas are characterized by a half power beamwidth of 60^o in azimuth and 20^o in elevation, and a maximum gain of 13 dBi (G) with an S11 return loss below -10 dB in the bandwidth of interest. The measured performance of these antennas are aligned with results recently published in literature for Fabry-Perot resonating antenna in X-Band [9].

A maximum output power of 2 W (33 dBm) is obtained with the stage marked as HPA (High Power Amplifier) in Fig. 1, realized using the HMC487 device from Hittite plus a 50-Ω matching network with the transmitted antenna. The power amplifier has an input noise figure of 9 dB and a gain higher than 20 dB in the bandwidth of interest. It gives the main contribution to the system power consumption, 9.3 W (1.3 A current from a 7 V voltage supply) having an efficiency of 21.5 %. A low-power Radar configuration has been designed targeting a lower range without the HPA stage. In such case, the output of the VCO can provide up to 5 mW (7 dBm) to the antenna. At the receiver side, in Fig. 1, the noise figure is less than 5 dB. The LNA has a gain of 29 dB. Further 43 dB of gain are obtained in the IF stage. The return loss is lower than -10 dB for a frequency range wider than 500 MHz, centered around 10.65 GHz.

Once fixed the sweep time T_{SW} and the bandwidth B, and the maximum and minimum distance of the target also the bandwidth of the intermediate frequency f_{IF} is defined. Intermediate-frequency signals are from about 15 kHz up to 20 MHz when the target distance moves from 1 m to about 1500 m. The selected ADC circuit, AD9259, sampling the data at intermediate frequency has a pipeline architecture with these characteristics: up to 4 channels, 14 bits, sample rate up to 50 MHz per channel, Spurious Free Dynamic Range of 84 dBc, Signal to Noise and Distortion Ratio (SINAD) of 72.7 dB, differential and integrated non linearity DNL and INL of 0.5 LSB and 1.5 LSB respectively. The power consumption of each channel is 2 mW in power down mode and 98 mW at maximum speed of 50 MSa/s. The power consumption for the X-band transceiver of a 4-channel Radar with one transmitter equipped with the HPA stage is 15.3 W while without the HPA stage is 6 W. Due to the Doppler effect, in case of moving targets, called Vr the relative speed between the Radar sensing node and the target, the frequency f_{IF} at the mixer output is shifted. The information on the speed and on the distance of the target are both contained in the beat signal according to this equation: $f_{IF} = -2 \cdot Vr/\lambda + A \cdot 2d/c$ (2). Since λ around a center frequency of 10.65 GHz is 2.8 cm, while the relative speed of the target is considered at maximum 40 m/s, then the frequency shift on f_{IF} caused by the Doppler effect is within the range ±3 kHz.

The radio-frequency transceiver, realized through COTS (Commercial Off The Shelf) components on a single-board (including also the FPGA-based hardware platform, the whole system can be packaged in a cube of size 10 cm per side), can be also integrated as a single-chip in CMOS SOI (Silicon On Insulator) technology for the large volume vehicle market.

3. RADAR FPGA REAL-TIME IMAGE PROCESSING

The whole data processing chain of the Radar sensing system is implemented on low-cost Xilinx Artix-7 FPGA. This FPGA also manages the low-level interfaces of the system with the external world. The output of the Radar sensor analog section in Section 2 is a baseband signal converted in the digital domain through a 14-bit 4-channel A/D Converter at 40 MSa/s and decimated at 12 bits, providing a data rate of 1.92 Gbit/s (4 channels x 40 MSa/s x 12 bit/Sa).

With reference to Fig. 2, two different approaches can be followed to detect the presence of targets, and estimate their distance, speed and position according to the FMCW radar sensor signal processing.

The first one is applying for each channel a 2D FFT: firstly a 1 D FFT is applied along each linear sweep of the FMCW received signal with a frequency resolution of about 1/Tsw= 5 kHz. Considering the input rate of 40 MSa/s this means an 1D FFT of 8000 samples. A power-of-two value of a 8192-point FFT is selected. The outputs of the first 1D FFT are stored in a transpose RAM by row. The speed information due to doppler shift can be obtained by observing the phase shift due to a target when multiple ramps are applied. As proved in [4], the number N_{ramp} of ramps depends on the maximum speed to be detected and the speed resolution. Considering a 40 m/s maximum speed and a speed resolution of

0.33 m/s the number of sweeps and hence the number of rows is roughly 250. By selecting a power-of-two value of 256 a transpose memory of 256x8192 locations is required. Along the 2048 columns a 256-point FFT has to be applied and as a result a range-doppler 256x8192 map is obtained where peaks along the rows reveal the distance of a target while peaks along the columns reveal the speed of the target. A peak detection algorithm has to be used such as the CA-CFAR (Cell Averaging Constant False Alarm Rate). The phase difference of the radial distance and of the speed results of the 4 different channels can be used to estimate the position of the target in the azimuth direction. To this aim a 3rd 1D FFT is required to be applied for all the 256x8192 4-point vectors of the range-doppler-azimuth cube of data. As a global result a 3D FFT processing is needed. The memory required amounts to 8M words each of at least 24 bits (12 ENOBs each for real and imaginary parts) for about 192 Mbits. The computational cost in term of multiply and add operations is higher than $800*10^6$ multiply and add operations per second. Fig. 3A summarizes the steps of this imaging sensor processing algorithm and the relevant data organization.

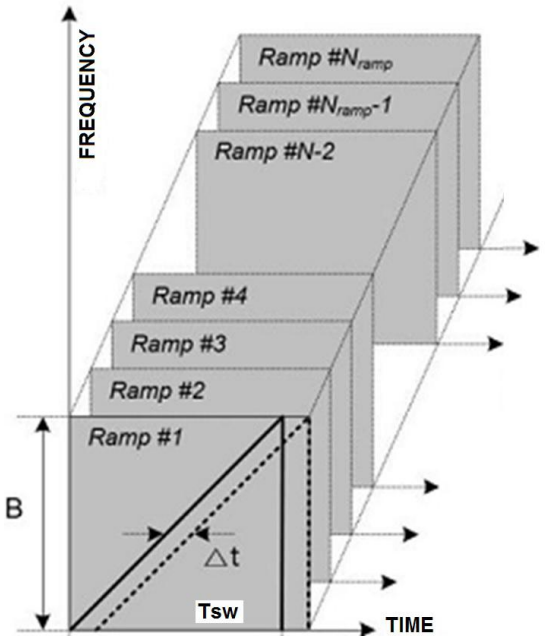

Fig. 2: Linear FMCW ramps transmitted/received by a Radar sensor

As alternative, another possible approach is first solving for each ramp the range-azimuth detection problem with a 4x8192 2D FFT processor. First, a 8192-point FFT has to be calculated for the 4 rows and then a 4-point FFT has to be repeated for the 8192 columns. Once successive frames are obtained, a motion detection algorithm operating in time [10, 11] or frequency domain can be used. The motion estimation in the frequency domain can be also implemented through an FFT. By observing the target for 256 sweeps also in this case a 3rd FFT has to be applied for all the 4x8192 256-point vectors of the 4x8192x256 cube of data. Fig. 3B summarizes the steps of this sensor signal processing algorithm and the relevant data organization. The computational cost is even higher by a 50% vs. the case in Fig. 3A.

In both cases, the bottleneck for real time sensor signal processing is the pipeline processing of the three 1D FFT blocks at 8192, 256 and 4 points, respectively. A preliminary Region Of Interest (ROI) selection task allows removing parts of the observed area that are not of interest thus reducing the computational cost. The signal processing chain includes also the data gain calibration. With respect to traditional DSP architectures for the signal processing algorithm implementation, all the processing chain has been implemented with an FPGA that furthermore manages the low-level hardware interfaces of the system. The processing algorithm has been first prototyped in Matlab environment and then translated in HDL language. The resulting design has been synthesized, placed and routed first on a more complex Xilinx Virtex FPGA and then has been optimised on a lower cost Artix-7 FPGA.

Realized in 28 nm CMOS technology the Artix-7 family is offered at a price comparable to Spartan6 low-cost family but with much higher resources in terms of DSP blocks. Each DSP block has a pre-adder, a 25x18 multiplier and final adder and accumulator. There are 740 DSP blocks in the XC7A200T device. The FPGA has also combinatorial and sequential configurable logic (roughly 135000 LUTs and 270000 FlipFlops), up to 13.14 Mbits of embedded block RAM, up to 16 transceivers capable of 3 Gbit/s data transfer towards external hosts, embedded SDRAM controller. Since 13.14 Mbits of

memory is lower than the 192 Mbits required by a 256x8192x4 memory, then external SDRAMs have to be used. There is also a control module, which implements the interfaces of the FPGA with the 14-bit ADC and starts the waveform generation. The control module also implements a unit to write and read from an on-board FLASH memory. This allows for the storage of relevant processing intermediate outputs in a non-volatile memory, used to reload such data when needed (for example when restoring from blackouts). Specific FPGA blocks implement the operations described in Fig. 3. A pipeline cascade of the 3 1D FFT blocks is implemented. To avoid dependencies among range and doppler and azimuth data proper ping-pong buffers are used, mapped in external SDRAMs. Each of the 1D FFT algorithm was designed exploiting the IP we developed in [12, 13, 16] with Radix-4 stages for the 256-point FFT (4 stages) and for the 4-point FFT (1-stage). A mixed Radix-2/Radix-4 architecture (6 Radix-4 stages plus 1 final Radix-2 stage) has been implemented for the 8192-point FFT.

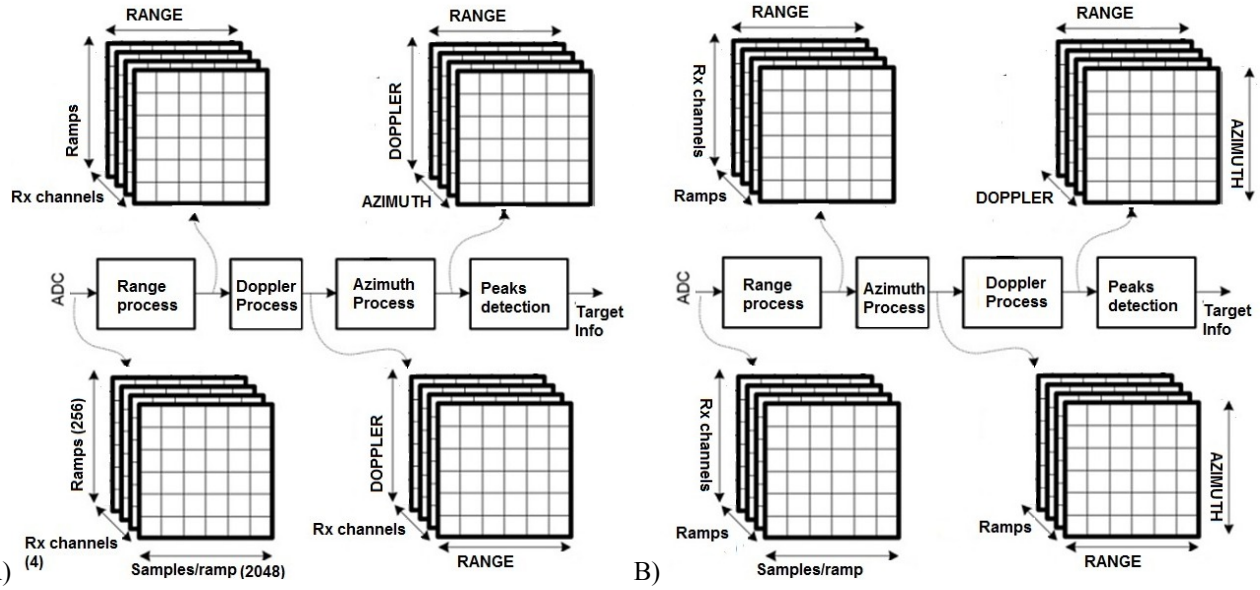

Fig. 3: A) Range-doppler 2D FFT signal processing plus a 3rd FFT along the channels for azimuth estimation and peak estimation; B) Range-azimuth 2D FFT signal processing plus a 3rd FFT for motion estimation in the frequency domain and peak estimation

By running the FPGA clocks at 200 MHz with an Artix-7 XC7A200T device the required computation can be implemented in a 200 ms observation time. The power budget for the FPGA based signal processing is about 1 W.

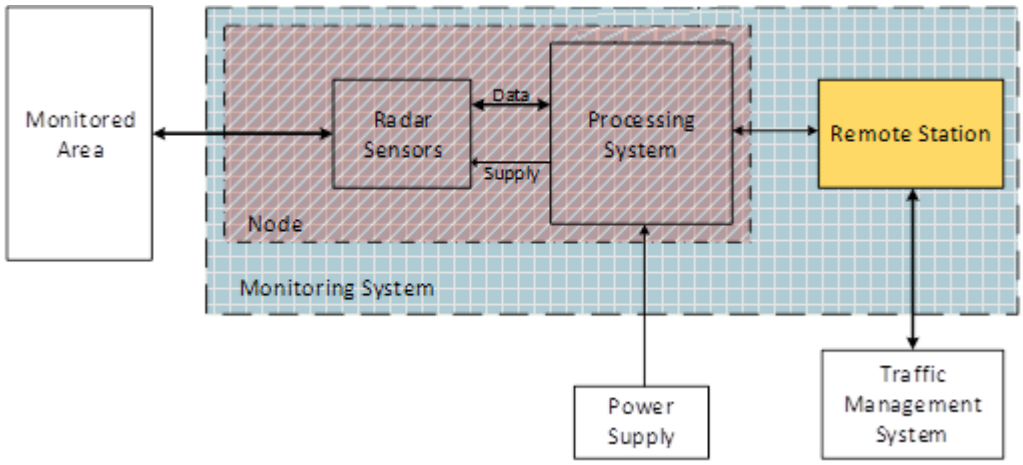

Fig. 4: Radar imaging system including sensors nodes plus a remote server for traffic management

To be noted that a complete imaging system may be organized as a network of multiple Radar sensor nodes. As example, to monitor an urban road crossing or a railroad crossing, achieving high SIL (Safety Integrity Level) values (thus being suitable for real-time and automatic traffic control) up to 4 Radar sensing nodes (clients) can be placed at the 4 corners of the crossing. A central server node, which can be placed also far away the monitored area, communicates with the central traffic management system. The server node can be based on programmable processors [14] since it has less constraints in terms of computational power, size and cost. The same scheme, summarized in Fig. 4, can apply to arrays of networked Radars larger than 4 nodes, to monitor large parking areas, or an harbour, or even the borders

4. EXAMPLE APPLICATIONS

Using the implemented sensing acquisition and processing platform, different FMCW Radar imaging systems have been implemented, operating in the X-band for surveillance in mobility systems:

- X-FRI1 with a detected range up to 300 m by transmitting an output power up to 7 dBm (5 mW).
- X-FRI2 with a detected range up to 1500 m by transmitting an output power up to 33 dBm (2 W).

To increase the safety of railroad crossing or road urban crossing, the proposed Radar sensor has been configured to use multiple receiving channels. For the processing first range-azimuth data have been extracted through the 2D FFT. During some tests obstacles such as a car have been detected while moving on a railway crossing in an area 20 m x 25 m. X-FRI1 configuration is enough for monitoring a road or a railway crossing. In such case, the speed information was not needed since the main objective is detecting the presence of an obstacle moving in the railway area. If also speed information has to be extracted, this can be done in the frequency domain by applying the third 1D FFT processor as already showed in Fig. 3.

The X-FRI2 configuration, with the 2 W power amplifier, has been tested on real scenarios for the surveillance of harbours, such has the ingress/egress of ships of different materials (wood and iron, fiberglass and iron, just wood) on the harbour of the naval academy in Livorno, Italy in a NATO contest in collaboration with the CNIT RASS laboratory [15]. Fig. 5 shows the range-speed map obtained during a test with multiple targets entering, or leaving, or moving around the small harbour within a distance of 1500 m and a speed in the range ± 7 m/s. The colors from blue to red represent the detected power spectral density with a variation of about 80 dBm from blue (minimum) to red (maximum)

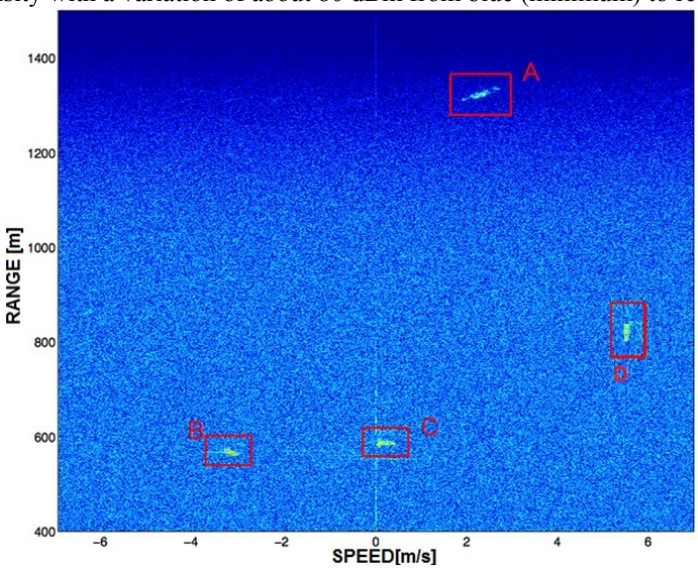

Fig. 5: Multi target detection in a small harbour, X-FRI2 Radar

5. CONCLUSIONS AND LESSON LEARNT

The paper has presented a compact and low-power design, and experimental measurement results, for an acquisition and FPGA-based processing platform of a multi-channel Radar imaging system. A transceiver operating in a bandwidth of 400 MHz around 10 GHz emits FCMW signals with a power configurable from few mW to 2 W depending on the target distance to to be covered if around 300 m or 1.5 Km. The distance resolution is better than 40 cm. The received signals from the different acquisition channels are processed to extract range, azimuth and doppler information, i.e. position and

speed of the target. With respect to the Velodyne LIDARs the proposed Radar achieves a worst distance accuracy (tens of cm instead of few cm) but a much larger detection range, up to 1.5 Km, instead of 100 m only. The size and power consumption of the proposed Radar is comparable to that of the VLP-16 LIDAR but the target cost is one order of magnitude lower than 8000 USD. When compared to state-of-the-art Radars in Table 1, the proposed solution stands for its extended detection range vs. the mm-wave LRR in [8], and for much lower power consumption vs. the pulsed Radars in [6, 7]. Future work in this direction will be related to the characterization of the proposed Radar sensing system in the harsh operating conditions of aerial and land vehicles [17, 18].

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	Max Distance	Resolution	Size	Power	Cost
HDL-32 [1]	100 m	2 cm	10 cm x 15	12 W	10000 USD
VLP-16 [2]	100 m	3 cm	10 cm x 7 cm	8 W	<8000 USD
This work, X-RFI2	1.5 Km	37.5 cm	10 cm x 10 cm	15 W	< 1000 USD
This work, X-RFI1	300 m	37.5 cm	10 cm x 10 cm	6 W	<500 USD
LRR3 [8]	200 m	10 cm	7 cm x 5 cm	4 W	< 1000 USD
[6]	3.7 Km	5 m	N/A	130 W	N/A

Table 1: Comparison of the proposed work to state-of-the-art LIDAR and RADAR imaging sensors for smart mobility

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