Design Exploration of mm-Wave Integrated Transceivers for Short-range Mobile Communications towards 5G

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This paper presents a design exploration, at both system and circuit levels, of integrated transceivers for the upcoming fifth generation (5G) of wireless communications. First, a system level model for 5G communications is carried out to derive transceiver design specifications. Being 5G still in pre-standardization phase, a few currently used standards (ECMA-387, IEEE 802.15.3c, and LTE-A) are taken into account as the reference for the signal format. Following a top-down flow, this work presents the design in 65 nm CMOS SOI and bulk technologies of the key blocks of a fully integrated transceiver: low noise amplifier (LNA), power amplifier (PA) and on-chip antenna. Different circuit topologies are presented and compared allowing for different trade-offs between gain, power consumption, noise figure, output power, linearity, integration cost and link performance. The best configuration of antenna and LNA co-design results in a peak gain higher than 27 dB, a noise figure below 5 dB and a power consumption of 35 mW. A linear PA design is presented to face the high Peak to Average Power Ratio (PAPR) of multi-carrier transmissions envisaged for 5G, featuring a 1dB compression point output power (OP1dB) of 8.2 dBm. The delivered output power in the linear region can be increased up to 13.2 dBm by combining four basic PA blocks through a Wilkinson power combiner/divider circuit. The proposed circuits are shown to enable future 5G connections, operating in a mm-wave spectrum range (spanning 9 GHz, from 57 GHz to 66 GHz), with a data-rate of several Gb/s in a short-range scenario, spanning from few centimeters to tens of meters.

Keywords: 5G Communications; System-level 5G model; 60 GHz; Low Noise Amplifier (LNA); Power Amplifier (PA); On-chip antenna; Design space exploration

1. Introduction: towards 5G

1.1. *Challenges of 5G*

Fifth generation (5G) communication systems, whose deployment and commercialization is expected in 2020, intend to create a synergy among a variety of cellular and wireless local-area network (LAN) systems through the use of the heterogeneous networking (het-net) paradigm.[1]

The aim is to maximize the use of RF bandwidth by switching between different systems, based on channel availability at the local level. Among the key technology challenges towards this goal, let recall here the support for high data rates (e.g., to enable mobile ultra-high definition video and virtual reality applications) and the need for increased capacity in dense urban environments, both outdoor and indoor.

1.2. *The mm-wave band as a key enabler of 5G*

A viable option for fostering the capacity of 5G communications is to exploit the mm-wave band (30–300 GHz), which is currently underused and offers opportunities for GHz-wide channels.[2-7] Furthermore, due to air and water absorption, transmissions in the mm-wave band have shorter range than in the "sub-3 GHz" bands used for current cellular systems and this reveals a key advantage in high-density environments, allowing base stations to be situated closer together.[6] In particular, the portion of mm-wave spectrum around 60 GHz (with wavelength of about 5 mm) experiences a dramatic attenuation (about 15 dB/km) due to the presence of the absorption peak of molecular oxygen,[7] and as such it has been allocated worldwide for unlicensed services.

1.3. *Standards for WPANs in the 60 GHz band*

The availability of a wide unlicensed spectrum around 60 GHz has stimulated the development of several standards for wireless personal area networks (WPANs), specifically designed for that frequency band. These are ECMA-387, WirelessHD, IEEE 802.15.3c, and IEEE 802.11ad, also known as WiGig (see Ref. 8, Sect. XI). All of the standards above include both single- and multi-carrier modes. It is very likely that these standards, already available, will act as members of the collection of protocols that 5G will be built upon.[3, 9]

1.4. *Evolution of LTE-A as a support for MTC in 5G*

Machine Type Communications (MTC) is considered one of the key enablers for advanced services such as smart cities/factories/hospitals and automated vehicles.[10, 11] The peculiar features of MTC have however raised new technical challenges that shall be addressed by 5G wireless communications systems.[12] Towards this goal, the Third Generation Partnership Project (3GPP) is working at providing support for MTC in the future releases of LTE, namely LTE Rel-12, -13 and -14, globally referred to as LTE-Advanced (LTE-A)[13-15]. Therefore, a significant research and standardization effort has been recently carried out in the context of LTE-A evolution towards 5G for MTC.[10-16] Recent advancements of the technology enabled the utilization of the spectrum up to the mm-wave band, by 5G systems. Further decisions about the utilization of this new spectrum are expected at WRC-2019 (World Radio Conference).

The considerations outlined above entail severe requirements to be met by the RF hardware in the perspective of 5G wireless devices. To this aim, several mm-wave amplifier designs in silicon or III-V technologies have been proposed at state-of-art.[17-26] Most of them miss a system-level analysis of 5G specifications, and therefore do not allow exploiting all the capabilities envisaged for this new standard, such as:

i) operating frequencies around the 60 GHz band for very dense cell deployment and transceivers with a wideband front-end (9 GHz-wide, see Fig. 1), to enable several channelization strategies and flexible reception of multi-format multi-Gb/s signals;
ii) integration at such high frequencies of all active and passive devices, including even the antenna for short-range links, covering distances up to tens of meters, using CMOS silicon technologies for low-cost and compact 5G terminals;

iii) LNA and highly linear PA ensuring specific target performance over the whole 9 GHz spectrum for low-distortion handling of wideband multi-carrier signals.

To address the above issues, in Sect. 2 we present a system-level analysis of 5G communications deriving transceiver specifications taking into account constraints on bandwidth, link budget and Quality of Service (QoS). In Sects. 3, 4 and 5 we present integrated designs in CMOS SOI and bulk technologies of PAs, LNAs, and integrated antennas, respectively. Performance of complete transceiver configurations for 5G connections is derived in Sect. 6. Some conclusions are drawn in Sect. 7.

2. System-level Analysis for 5 G in the mm-Wave Band

2.1. *Constraints on RF bandwidth and link budget*

The receiver's front-end shall be able to handle the whole spectrum depicted in Fig. 1, which spans over a whole 8.640 GHz band, ranging from 57.24 up to 65.88 GHz, with channelization $B_c = 2.16\,\text{GHz}$. Actually, such a wideband front-end guarantees the full compatibility with transmission modes featuring multiple-channel bonding for scalable capacity, like, for instance, those envisaged in ECMA-387 standard.[27]

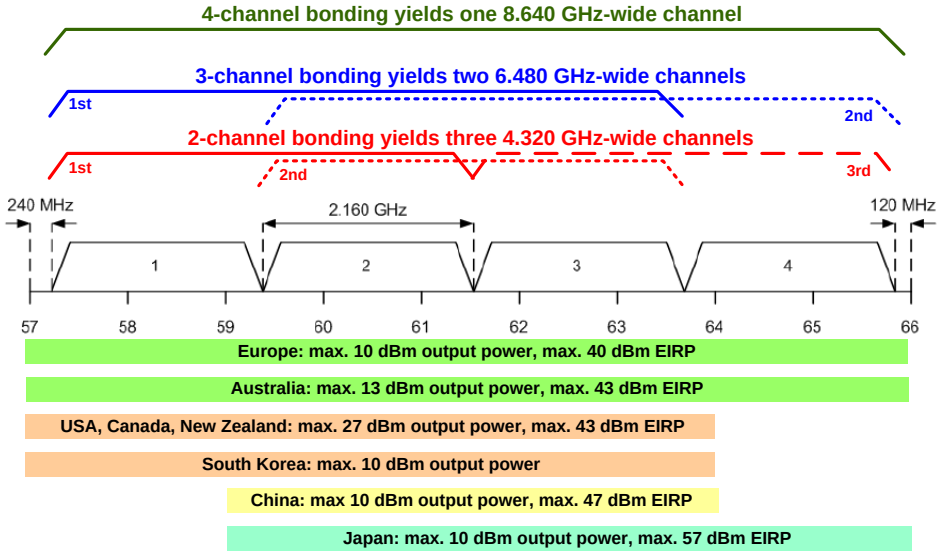

Fig. 1. Worldwide channelization, spectrum allocation and maximum transmitted power levels in the ISM unlicensed band around 60 GHz, for indoor services; highlighting multiple-channel bonding options of ECMA-387 yielding scalable data traffic capacity

Figure 1 also highlights the maximum output power and the maximum EIRP (Emitted Isotropic Radiated Power) permitted worldwide in different countries for indoor services. The maximum output power from the RF amplifier to be handled to the transmit antenna is limited to 10 dBm in Europe, China, Japan and South Korea, while it is set to 13 dBm in Australia and it grows up to 27 dBm in US, Canada and New Zealand. The spectrum

utilization ranges from a minimum of 5 GHz in China, up to 7 GHz in US, Canada, Japan, South Korea and New Zealand, and to the whole 9 GHz in Europe and Australia.
For a radio link over a distance d, using any of the single- or multiple-bonding channels depicted in Fig. 1, the received power P_{RX} is given by

$$P_{RX}\big|_{\mathrm{dBm}} = P_{TX}\big|_{\mathrm{dBm}} + 2G_A\big|_{\mathrm{dBi}} - PL(d)\big|_{\mathrm{dB}} \quad (1)$$

where P_{TX} is the transmit power, $PL(d)$ is the propagation path loss (PL) and G_A is the gain of transmit and receive antennas (assumed identical). In this work, differently from other mm-wave transceiver architectures implementing two antennas,[28, 29] we suggest the use of the same antenna for both the receiver (RX) and the transmitter (TX). To this purpose, the considered transceiver architecture, shown in Fig. 2, adopts a time-division duplexing scheme and a voltage-controlled antenna switch. The antenna switch can be realized following the approach patented in Ref. 30, and in Refs. 31, 32. For the TX chain, a direct conversion scheme is adopted where the key block is the wideband and linear PA. For the RX chain, the key block is the wideband and low noise amplifier, whereas the demodulator exploits an I/Q homodyne demodulation scheme reusing the mixer circuitry already proposed in Ref. 33. The on-chip design of the circuits within the green block in Fig. 2 (LNA, antenna and PA) will be detailed in Sects. 3, 4 and 5, respectively.

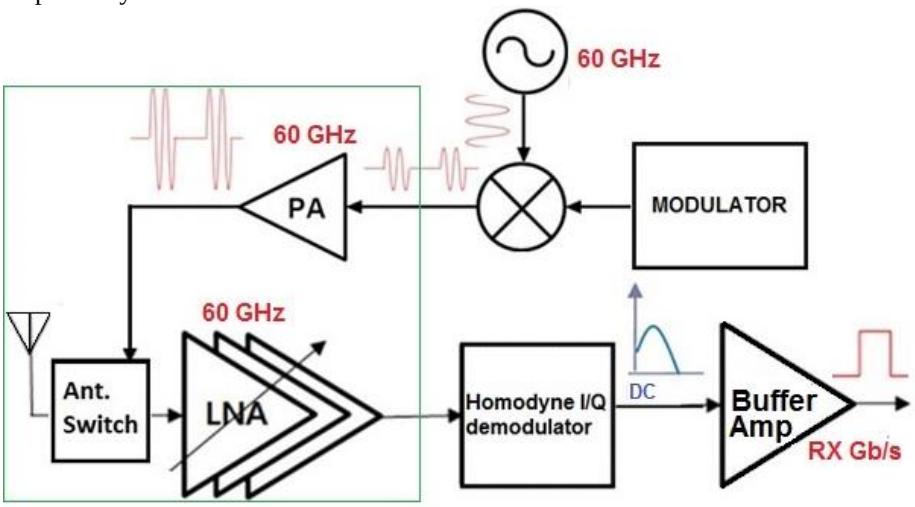

Fig. 2. Transceiver architecture

In case of a short-range (i.e. d < 10 m) 60 GHz link for home/office scenarios, free-space line-of-sight (LOS) propagation can be assumed, as proved in Ref. 7. So, the relevant PL and received carrier-to-noise ratio (C/N) can be evaluated as in (2) and (3) being $\eta_0\big|_{\mathrm{dBm/Hz}} = -174\ \mathrm{dBm/Hz}$ the one-sided power spectral density (p.s.d.) of the ambient noise at temperature $T_0 = 290\,\mathrm{K}$, B_N the noise bandwidth of the selected RF channel (as in Fig. 1) and F the receiver's overall noise figure.

$$PL(d)\big|_{\mathrm{dB}} = 20\log_{10}(d) + 68\,\mathrm{dB}, \quad (2)$$

$$C/N\big|_{\mathrm{dB}} = P_{RX}\big|_{\mathrm{dBm}} - \eta_0\big|_{\mathrm{dBm/Hz}} - B_N\big|_{\mathrm{dBHz}} - F\big|_{\mathrm{dB}}, \quad (3)$$

If the receiver front-end is made of a LNA stage with gain G_{LNA} and noise figure F_{LNA}, followed by a stage with noise figure* F_{RX}, the overall noise figure is given by the Friis' formula

$$F = F_{LNA} + (F_{RX} - 1)/G_{LNA} \quad (4)$$

2.2. *Constraints on RF elements due to QoS specifications*

The QoS can be expressed as the maximum tolerable value of the bit error rate (*BER*) or of the packet error rate (*PER*). The *BER* is a more meaningful performance metric for streaming services such as digital video broadcasting (DVB),[34] while the *PER* is used for packet-oriented communications, such in the case of IP-based services. In any case, given a modulation and coding scheme (MCS) with constellation size *Q* and rate *r*, both *BER* and *PER* requirements can be translated, either analytically or by simulations, into a required value of the ratio, denoted as $(E_b/N_0)_{req}$, between the average received energy per bit E_b and the one-sided overall receiver noise p.s.d. $N_0 = F\,\eta_0$. To this respect, Table 1 lists some MCSs and the relevant values of $(E_b/N_0)_{req}$ over White Gaussian Noise (WGN) channel for the wireless digital video transmission systems outlined hereafter (for each system the most robust MCS was selected among those envisaged by the standard).

LTE-A. It is expected that the evolution of LTE-Advanced will be integrated into 5G, while ensuring backward compatibility.[15] Thus, according to Ref. 35, a LTE-A waveform, featuring BPSK modulation and rate 1/3 turbo code, achieves a *BER*=10^{-5} at $(E_b/N_0)_{req} = 3.93\,\mathrm{dB}$ for a frame size *K*=40 and at $(E_b/N_0)_{req} = 0.42\,\mathrm{dB}$ for a frame size *K*=5114. Performance improves with increasing *K*, due to an increase in interleaver gain, but this also entails a larger number of iterations in the decoder and therefore also a longer latency.

ECMA-387. The simplest and strongest mode (without the use of time domain spreading sequences) is Mode A1, featuring BPSK scheme plus concatenated Reed-Solomon (RS) and convolutional encoding with rate 1/2. The relevant $(E_b/N_0)_{req}$ value can be obtained by re-working some data from Ref. 36. In detail, Fig. 5 of Ref. 36 shows that, when using A1, the required $PER = 8\%$ (as from Ch. 13 of Ref. 27) is obtained with $(E_s/N_0)_{req} = 0.59\,\mathrm{dB}$, where $E_s = E_b\, r \log_2 Q$ is the average received energy per symbol interval, so that we get $(E_b/N_0)_{req} = 3.9\,\mathrm{dB}$. For an L-bit long packet, we have $PER = 1-(1-BER)^L$, which, assuming $L = 1\,\mathrm{kB} = 8192\,\mathrm{bit}$ as in Ref. 36, yields $BER = 10^{-5}$.

IEEE 802.15.3c. The simplest and strongest physical layer mode for High Speed Interface (HSI PHY) is made of QPSK and Low-Density Parity-Check (LDPC) encoding with rate 1/2. The relevant $(E_b/N_0)_{req}$ value is obtained from Fig. 5 of Ref. 37, by letting $BER < 10^{-7}$ according to Ref. 37.

* Typically, this stage includes a mixer, whose noise figure F_{Mixer} is the dominant one.

DVB-T2. Though not operating at 60 GHz, neither being considered in the building of 5G, Second Generation Terrestrial DVB (DVB-T2) standard is nevertheless taken into consideration here as a representative case of a high-definition digital video streaming service. Thus, DVB-T2 is taken into account as a performance benchmark only. According to the numerical results presented in Ref. 34, DVB-T2 employing 16-QAM (Quadrature Amplitude Modulation) and concatenated BCH (Bose-Chaudhuri-Hocquenghem) and LDPC codes with rate 1/2 and 5/6 achieve a *BER*=10^{-5} at $(E_b / N_0)_{req} = 3.3\,\text{dB}$ and $(E_b / N_0)_{req} = 6.2\,\text{dB}$, respectively. Let's now assume that the transmitted signals, over any channel of Fig. 1, use the customary root-raised cosine (RRC) spectral shape with roll-off factor α. The symbol rate R_s (in Baud) over a B_c-wide channel results then $R_s = B_c / (1+\alpha)$ and the achievable bit rate is given by $R_b = R_s \; r \log_2 Q$, whose values are reported in the last line of Table 1, for $\alpha = 0.25$, as in ECMA-387. The required receiver's C/N can be obtained by taking the values of $(E_b / N_0)_{req}$ from Table 1, neglecting pilots and other signalling overhead

$$(C/N)_{req} = (E_b / N_0)_{req} \; M \; r \log_2 Q \tag{5}$$

where *M* is a custom margin for implementation losses, with typical value of 5 dB.[38] By letting $C/N \geq (C/N)_{req}$, from (1), (3) and (5) we get the following constraint on the receiver features

$$\begin{aligned} 2G_A\big|_{\text{dBi}} - F\big|_{\text{dB}} \geq (E_b / N_0)_{req}\big|_{\text{dB}} + 10\log_{10}(r \log_2 Q) + M\big|_{\text{dB}} - \\ - P_{TX}\big|_{\text{dBm}} + PL(d)\big|_{\text{dB}} + \eta_0\big|_{\text{dBm/Hz}} + B_N\big|_{\text{dBHz}} \end{aligned} \tag{6}$$

2.3. *Numerical evaluation of link design constraints*

The receiver's noise bandwidth, B_N in (6), can be evaluated by considering an RF filter matched to the transmit RRC pulses, i.e., $B_N = R_s = B_c / (1+\alpha)$. Considering a single channel with bandwidth $B_c = 2.16\,\text{GHz}$, the noise bandwidth turns out $B_N = 1.728\,\text{GHz}$. Moreover, in case of ν-channel bonding ($\nu = 2, 3, 4$) for increased capacity, B_N scales proportionally to the number ν of used channels. If P_{TX} is scaled accordingly (i.e., keeping constant the per-channel transmitted power), then all the previous analysis is still valid.

Table 1. MCS and $(E_b / N_0)_{req}$ for some wireless digital transmission systems

System [Ref.]	LTE-A [12]	ECMA-387 Mode A1 [27] (reworked data from [36])	IEEE 802.15.3c HSI PHY [37]	DVB-T2 [34]
Modulation size Q	2 (BPSK)	2 (BPSK)	4 (QPSK)	16 (16-QAM)
Code type	Turbo	Concatenated: RS & Convolutional	LDPC	Concatenated: BCH & LDPC
Code rate r	1/3	$224/240 \cdot 1/2$	1/2	1/2 , 5/6
Maximum *BER*	10^{-5}	10^{-5} PER = 8% packet = 1 kB	10^{-8}	10^{-5}
$(E_b / N_0)_{req}$	3.93 dB @ *K*= 40 0.42 dB @ *K*=5114	3.9 dB	4 dB	3.3 dB @ 1/2 6.2 dB @ 5/6
Allowed bit rate R_b	0.576 Gb/s	0.807 Gb/s	1.728 Gb/s	3.456 Gb/s,

on a 2.16 GHz channel, using RRC pulse shape with roll-off 25%				5.760 Gb/s

By plugging the numerical values assessed in Sects. 2.1 and 2.2, and also the PL model in (2), into the design constraint of (6), we get the lower bound of $2G_A|_{\mathrm{dBi}} - F|_{\mathrm{dB}}$ in (7). This figure of merit is numerically evaluated and plotted in Fig. 3 versus the link distance d, for the four systems described in Table 1: LTE-A, ECMA-387, IEEE 802.15.3c, DVB-T2. In Fig. 3 the maximum transmitted power is considered 10 dBm, which is the maximum P_{TX} allowed in some countries, such as Japan or South Korea. From Fig. 3 it is clear that to reach a link distance of about 10 m with the LTE-A and ECMA-387 schemes, the receiver specifications should ensure that $(2G_A|_{\mathrm{dBi}} - F|_{\mathrm{dB}}) > 1\,\mathrm{dB}$. Consequently, the antenna gain G_A should be at least 3 dBi while the noise figure F of the receiver should not exceed 5 dB over the whole 57-66 GHz band. Currently, 60 GHz mixers in 65 nm CMOS SOI are already available in literature with a noise figure F_{Mixer} below 12 dB.[33] According to the Friis' formula in (4) and letting $F_{RX} \cong F_{Mixer}$, if we are able to design a LNA with a gain of at least 15 dB, then its noise figure F_{LNA} determines the noise figure F of the whole receiving chain, i.e., $F \cong F_{LNA}$.

$$2G_A|_{\mathrm{dBi}} - F|_{\mathrm{dB}} \geq (E_b / N_0)_{req}|_{\mathrm{dB}} + 10\log_{10}(r\log_2 Q) - 18.63 + 20\log_{10}(d) \qquad (7)$$

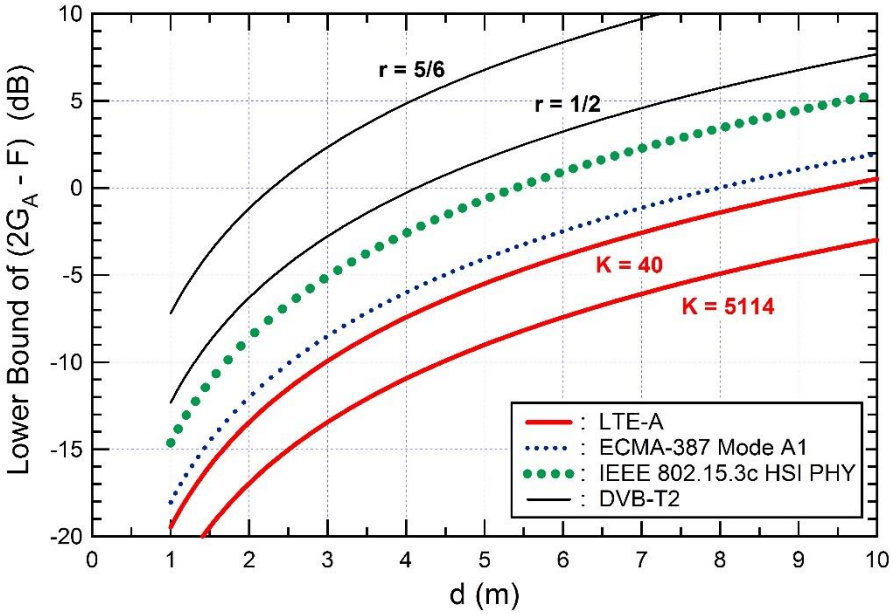

Fig. 3. Receiver design constraints vs. link distance

Summarizing, the specifications for LNA and antenna are a gain of at least 15 dB and 3 dBi, respectively, over a 9 GHz-wide bandwidth, spanning from 57 to 66 GHz, with a noise figure for the LNA below 5 dB. With these specifications, a link distance of about 10 m is reached for the LTE-A and ECMA-387 schemes; for IEEE 802.15.3c scheme the link distance reduces to 6 m. As specified in Sect. 2.1, in some countries such as US,

Canada and in Europe the maximum allowed transmitted power P_{TX} is higher than 10 dBm. In such cases, according to (6), by increasing the performance of the transmitter with a value of P_{TX} beyond 10 dBm, the specifications on antenna gain and receiver noise figure in Fig. 3 can be relaxed. For example, with $P_{TX} = 14$ dBm the lower bound on $2G_A\big|_{\text{dBi}} - F\big|_{\text{dB}}$ enabling a link distance of 10 m with IEEE 802.15.3c is reduced from 5 dB to 1 dB. Moreover, with $P_{TX} = 14$ dBm, G_A > 3 dBi and $F \sim F_{LNA}$ < 5 dB the maximum link distance with the ECMA-387 scheme increases to roughly 15 m, whereas with the LTE-A scheme is from 17 m to 25 m depending on the frame size *K*.
Table 2 summarizes the specifications derived for the key blocks of the transceiver and adopted for the circuit design phase in Sects. 3, 4 and 5. The distance values in the second row of Table 2 are obtained with an output-transmitted power (P_{TX}) of 10 dBm, whereas the distance values in the third row of Table 2 refer to a P_{TX} of 14 dBm. It is worth noting that in Fig. 3 and in Table 2, LTE-A and DVB-T2 are considered under the hypothesis of migrating their RF spectrum around 60 GHz. For the PA, a linear circuit able to reach the target output power of 10 dBm or 14 dBm with a compression point lower than 1 dB should be designed. The linearity of the PA is important in non–constant envelope schemes, such as the ASK (Amplitude Shift Keying) or the OFDM (Orthogonal Frequency Division Multiplexing); in particular, the latter is considered in 5G short-range high-bandwidth communication systems and is characterized by high peak to average power ratio (PAPR). Simulations in Ref. 39 with an OFDM communication system proved that an increase in 0.5 dB of the PA non-linearity could lead to a decrease of one order of magnitude of the *BER* link performance. Therefore, the specifications on output power (P_{TX} in Table 2) refer to the PA metric known in literature as OP1dB (1 dB output power compression point) and not to the metric P_{sat} (the maximum transmitted power at which the amplifier saturates).

Table 2. Transceiver specifications derived from system modelling

P_{TX}	ECMA-387 range	LTE-A range, K=40 to K=5114	IEEE 802.15.3c range	Antenna gain	LNA gain	F_{LNA}	F_{Mixer}	Band
10 dBm	9 m	10.5 to 15.5 m	6 m	> 3 dBi	> 15 dB	< 5 dB	< 12 dB	57-66 GHz
14 dBm	15 m	17 to 25 m	10 m					

3. Wideband LNA with Integrated Antenna for 5G

3.1. *Technology selection and LNA design flow*

Given the specifications from the system-level model in Sect. 2, we have performed a layout-level design of CMOS hard macrocells for the key blocks of a 60 GHz transceiver: LNA, PA and on-chip antenna. For the mixer the already available solution from Ref. 33 can be reused since it meets the requirements in Table 2. Such macrocells can be integrated at layout level in a complete 5G SoC terminal. 3D electromagnetic characterizations of active/passive circuits and layout-level silicon design have been carried out in HFSS and Cadence CAD environments, respectively. Being the 5G standard not defined yet, we propose several configurations for the above blocks to

explore different trade-offs between implementation cost and mm-wave circuit performance.

At technology level this paper adopts a 65 nm CMOS technology from STM in two different versions, bulk and SOI (Silicon on Insulator); voltage supply is at 1.2 V. Six thick copper staked layers (M_1-M_{6Z}) and an aluminium capping layer are available for on-chip interconnections. The bulk CMOS technology allows for minimal fabrication cost being the one used for large volume digital and mixed-signal baseband designs. The SOI version, thanks to its high resistivity substrate (1 kΩ cm instead of standard 20 Ω cm), has several advantages vs. bulk technology for 60 GHz design of active and passive devices while avoiding the high extra costs of hetero-junction technologies traditionally used for mm-waves such as SiGe HBT, GaAs or InP HEMT. The 65 nm CMOS technologies are also low cost solutions when compared to cutting-edge silicon technologies, such as the 14-nm Fin-FET used for multi-processor systems-on-chip.

The CMOS SOI allows for the following advantages vs. bulk technology:

i) reduction of substrate interference cross-coupling between different circuits integrated in the same chip; ii) significant reduction of junction capacitances so that circuits can operate at higher speed, or with lower power at the same speed; iii) elimination of latch-up and better immunity to short-channel effects; iv) reduced amount of energy stored in the supporting substrate leading to higher gains in case of on-chip integrated antennas.

Targeting the LNA specifications in Table 2 of G_{LNA} > 15 dB, F_{LNA} < 5 dB for the whole 9 GHz band, we designed six different LNA circuits to explore different trade-off in terms of performance, implementation cost and power consumption. In detail, 1-stage, 2-stage and 3-stage LNA topologies with inter-stage LC-matching have been designed at layout-level in 65 nm bulk and 65 nm SOI CMOS technologies. Differently from state-of-art LNA designs with pre-defined 50 Ω input matching constraint, in this work, co-designing on-chip also the antenna, the impedance matching is a new degree of freedom to be tuned during the design phase to optimize circuit performance.

For 60 GHz applications, Ref. 17 suggests the design metrics in (8) to define the transistor width W in μm of the first LNA stage to minimize the noise figure, being J_{opt} the optimal I_{DS} value per μm, and W_{opt} the optimal W value for a given source resistance R_S.

$$J_{opt} = 0.15\ \text{mA}/\mu\text{m},\ W_{opt}=1200/R_S\ \mu\text{m}/\Omega \tag{8}$$

If the final LNA source impedance is constrained to a predefined value of 50 Ω, to match off-chip antenna impedance, the above rules lead to a fixed transistor width of 24 μm and to a fixed current value of 3.6 mA. However, other works in recent literature[40] proved that, the value of W_{opt} obtained from (8) to minimize the noise figure with R_S=50 Ω, does not allow to obtain the best result in terms of linearity and gain performance of the amplifier. To take into account these targets (gain and linearity), the transistor width should be larger than W_{opt}. Therefore, in our LNA design, to optimize not only the noise figure but also the amplifier gain and linearity, we fixed the MOSFET current density close to 0.15 mA/μm, and we explored the performances of the amplifier in terms of gain

and linearity for different values of R_S, by changing, consequently, the value of W according with (8). To limit the design space to be explored, the source impedance should be in a range from 20 Ω to 100 Ω, i.e. a range for which an on-chip antenna with impedance equal to R_S can be easily designed and realized (see Sect. 4). This way, different configurations of the LNA parameters were simulated allowing also for different LNA input impedance values and different gain G_{LNA} and nosie figure F_{LNA} trade-offs. The gain and noise figure should be $G_{LNA} > 15$ dB and $F_{LNA} < 5$ dB, respectively, over the whole 57- 66 GHz band.

3.2. *Wideband LNA circuit design*

Following the design flow in Sect. 3.1, three LNA topologies (1-, 2- and 3-stage) have been designed in bulk and SOI 65 nm CMOS technology. Fig. 4 shows the circuit details.

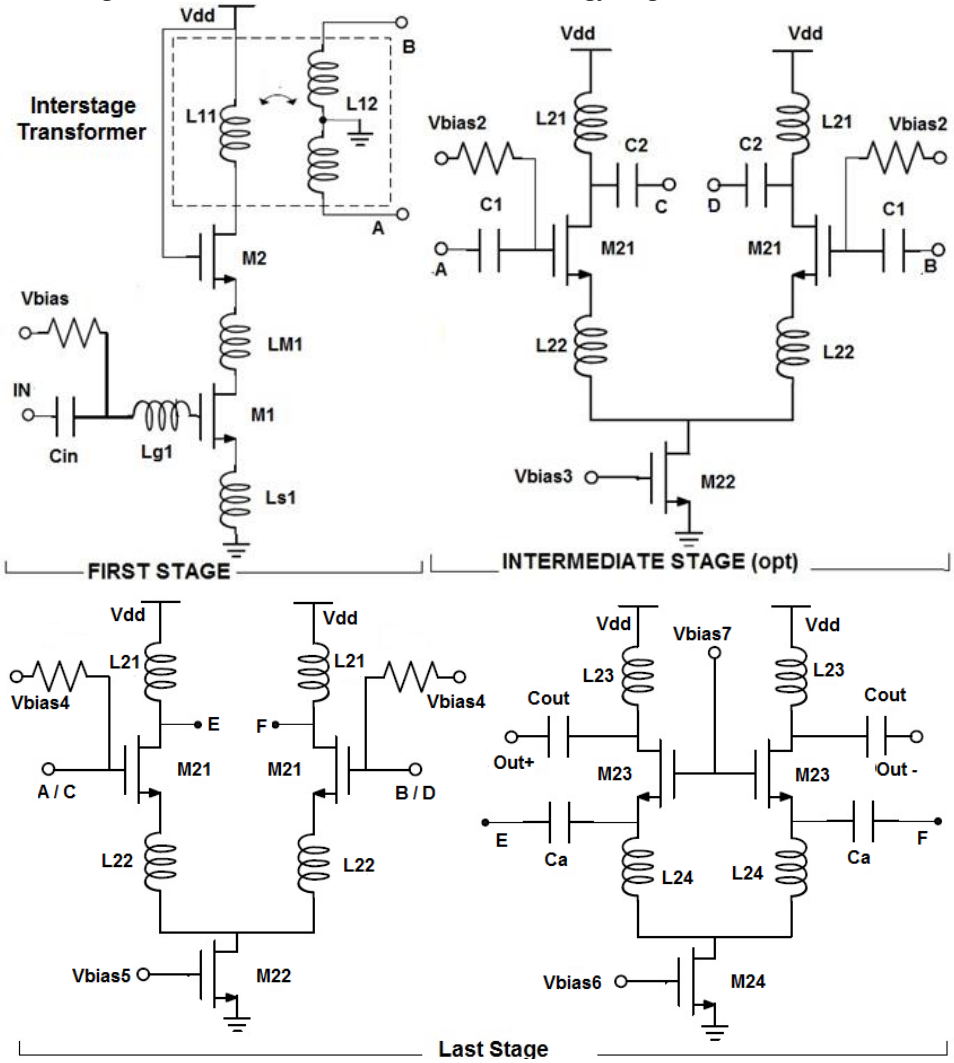

Fig. 4. Building circuitry of 1-, 2- and 3-stage LNAs

The 1-stage LNA consists of a single-ended cascode stage, First Stage in Fig. 4, which provides a proper differential output signal. Within a multi-stage amplifier configuration, the output of the First Stage in Fig. 4 can be delivered to a fully differential second stage of amplification through an integrated inter-stage transformer that provides, in addition, the maximum power delivery from the first to the following stages of the amplifier. The results of our exploration design activity prove that the single stage configuration never reaches, neither in bulk nor in SOI CMOS technologies, the target gain of at least 15 dB with a noise figure below 5 dB. The 1-stage LNA alone, in 65 nm CMOS SOI technology, allows for a peak gain of only 10 dB. Its power consumption is 7 mW. In CMOS bulk technology the same 1-stage amplifier has a 9 dB gain.

To increase the amplifier gain a 2-stage LNA topology has been designed. Its layout in 65 nm CMOS SOI technology is showed in Fig. 8 in Sect. 5. The 2-stage LNA is realized as the cascade of the first stage described above (First Stage in Fig. 4) and a second stage consisting of a fully differential cascode amplifier (Last Stage in Fig. 4). The proposed fully differential cascode amplifier is modified vs. conventional solutions to remove the staked transistor, common-source (CS) and common-gate (CG), and thus reducing the problems due to low-supply voltage. The inter-stage transformer of Fig. 4 has been realized through two octagonal and symmetrical coupled planar inductors, both with 24 μm of diameter, one turns each, 3 μm spaced and 6 μm wide. The structure has been designed by using all the metal layers available in the technology: thick copper-staked layers (M_1-M_{6Z}) and aluminium capping layer (AP). Near to the intersection the first spiral has been designed in M_{6Z} and AP, whereas the secondary spiral in M_1-M_5. This structure does not need under-pass, so eliminating the parasitic effects due to vertical vias. In the CMOS SOI implemented versions the primary spiral exhibits a self-inductance (L_{TP}) of 183 pH with an associated quality factor (Q_{TP}) equal to 15.5, whereas the secondary spiral exhibits the same self-inductance ($L_{TS} = 143\,\text{pH}$) with a Q_{TS} equal approximately to 30, at 60 GHz. In the CMOS bulk design implementations the transformer has been sized to achieve similar values for L_{TP} and L_{TS}. In bulk CMOS quality factors Q are decreased by 12%.

The W (width) parameter of the M1 and M2 MOS of the First Stage has been set to 40 μm, with transistors polarized at weak inversion (V_{GS} of roughly 0.8 V). According to (8) this leads to a current value of 6 mA and source impedance of 30 Ω. The size of the transistors in other stages is from 30 μm to 60 μm, while the value of L (channel length) has been taken at its minimum, 0.06 μm. The Last Stage in Fig. 4 is a fully differential cascode, which allows the increase of the power gain and the benefits of the common mode rejection ratio (CMRR). The cascode configuration is implemented by using a common-source and an AC coupled common-gate stage (i.e., it is a pseudo-cascode) instead of the standard cascode configuration like that realized for the First Stage. This in order to have only two staked transistors between $V_{DD} = 1.2\,\text{V}$ and GND.

To further increase the LNA gain a 3-stage LNA configuration has been also designed: the first and third stages are de-facto similar to the already discussed First and Last

Stages of Fig. 4, while a new Intermediate Stage (see Fig. 4) is added consisting of a differential common source amplifier AC coupled with the preceding and following stages.

Fig. 5 details the gain and noise figure performances achieved for the 2-stage and 3-stage LNAs in CMOS SOI technology. The 2-stage LNA circuit in CMOS SOI technology has a power gain $G_{LNA} > 15\,\text{dB}$ (peak value 23.3 dB at 59 GHz) and $F_{LNA} < 5\,\text{dB}$ over the 57-66 GHz spectrum. The minimum F_{LNA} for the 2-stage LNA in the considered spectrum is 4.7 dB. Such values refer to a 30 Ω source impedance that during the design tuning has been found as a value ensuring a good trade-off between noise, gain and bandwidth and that can be easily achieved when designing the integrated antenna. For the 3-stage LNA configuration and for the implementation in bulk CMOS technology the optimal impedance matching has been found heuristically at different values, but always in the range 30-35 Ω.

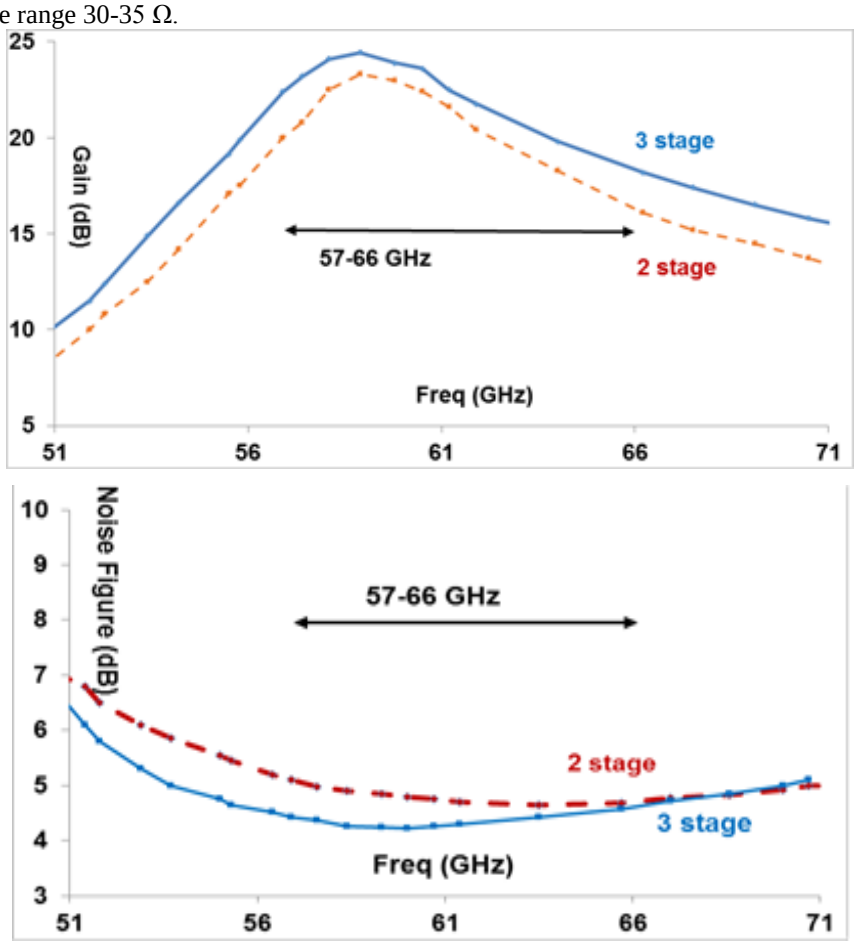

Fig. 5. Gain and noise figure in dB for 2- and 3-stage LNAs, 65nm CMOS SOI

The power consumption of the 2-stage LNA circuit at 1.2 V supply is about 26 mW. The 3-stage LNA in CMOS SOI technology gets the target performance $F_{LNA} < 5\,\text{dB}$ over

the 57-66 GHz spectrum with a power gain increased vs. the 2-stage version in the same technology: peak gain of 24.4 dB at 58.9 GHz and at least 18 dB from 57 to 66 GHz. The minimum F_{LNA} for the 3-stage LNA in the considered spectrum is 4.3 dB. However, the 3-stage LNA has a power consumption of 35 mW, increased by 30% vs. the 2-stage LNA. The input return loss (S_{11} parameter) for 2- and 3-stage LNAs is below -10 dB for the 57-66 GHz band. The same circuits have been re-designed in the 65 nm CMOS bulk technology to evaluate if the system-level specifications from Sect. 2.3 can be met with a low cost technology. As far the LNA gain is concerned the performance in bulk CMOS are at least 0.5 dB lower than the CMOS SOI counterpart. Moreover, the 2- and 3-stage LNAs when realized in bulk CMOS have a noise figure that, in the 57-66 GHz spectrum of interest, increases to 6 dB thus missing the target value of being lower than 5 dB.

The stability factor of both 2- and 3-stage LNAs in bulk or SOI CMOS are always greater than 4, demonstrating that the LNAs are unconditionally stable for 60 GHz applications. BIBO (Bounded Input Bounded Output) stability of 2- and 3-stage LNAs has been also checked by analysing in time-domain the transient response to impulse inputs. The number of LNA stages has not been further increased since it resulted difficult for a 4-stage amplifier to guarantee the stability over the whole 9 GHz spectrum.

Summarizing the 1-stage, 2-stage and 3-stage LNAs in CMOS bulk and SOI technologies have been designed keeping as targets a $F_{LNA} < 5\,\mathrm{dB}$ and a minimum gain of 15 dB through the whole 57 to 66 GHz spectrum. The 1-stage LNA circuit misses the target gain requirement being limited 10 dB. In the low-cost bulk CMOS technology even the 2-stage and 3-stage LNA circuits fail the specifications of Table 2 since their noise figure is higher than the 5 dB target. In CMOS SOI technology both 2-stage and 3-stage LNAs meet the required specifications: the best solution in terms of low-power is the 2–stage LNA (saving 9 mW), while the best solution in terms of performance is the 3-stage LNA (1 dB peak gain and -0.5 dB noise figure). As discussed in Sect. 6, the power consumption of the whole transceiver is dominated by the contribution of the PA and not by the LNA. Therefore, we selected as best option for the LNA the 3-stage circuit in CMOS SOI technology.

Table 3. LNA results in 65 nm CMOS and comparison with state-of-art

Ref	Topology	Min G_{LNA}, dB	Max G_{LNA}, dB	Min F_{LNA}, dB	Power, mW
Our	3-stage: cascode + CS + pseudo-cascode	18	24.4	4.3	35
[29]	2 stage cascode	N/A	11.46	4.7	N/A
[41]	3 stage cascode	N/A	20.5	6.5	20
[42]	1 CS +3 cascode	10.5	19	4.5	30
[43]	1 CS +2 cascode	N/A	22.3	6.1	35

Table 3 compares the achieved performance vs. recent LNA designs in 65 nm CMOS technology node.[29, 41-43] To be noted that our design has been optimized to cover a wide bandwidth range of 9 GHz from 57 GHz to 66 GHz (and hence we report in Table 3 minimum and maximum gain) while other state-of-art designs are often optimized in terms of gain and noise figure around a smaller band, typically 2 – 3 GHz around 60

GHz. By comparing the proposed solution with Ref. 43, having the same power consumption and a similar 3-stage topology but different input matching specifications this work allows for improved gain and noise performance by roughly 2 dB. The input impedance is constrained to 50 Ω in Ref. 43, while in this work has been considered a new degree of freedom with a final input impedance value of 30 Ω after circuit tuning and optimization. Due to the on-chip antenna co-design, the specification for the antenna impedance matching of 30 Ω instead of classic 50 Ω is not a major issue to be solved.

4. Wideband On-Chip Antenna Design

For the antenna design, we explored in 65 nm CMOS technology 5 different topologies allowing for different trade-offs between gain, bandwidth and area: a folded dipole, an inverted-F and a bow-tie antenna plus, as reference for performance comparison, an half-wave dipole from Refs. 28, 29 and a double-slot from Ref. 44. The shape of the above 5 antenna topologies are already known in the state of the art. What is specific to the proposed design is the antenna sizing, reported in this paragraph, and the performance achieved reported in Table 4. Hereafter, Fig. 6 shows for the final selected antenna the 3D radiation pattern and its projection on the YZ plane, compared to the case of an omnidirectional antenna. Although this work shares the same antenna in time-division mode between RX and TX chains, through an antenna switch (see Sect. 2.1 and Fig. 2), the antenna has been designed to match the input impedance of the LNA optimizing gain and noise performance of the receiver. An antenna impedance constraint of about 30 Ω has been derived as a specification from Sect. 3. Then the value of the output impedance of the PA in Sect. 5 has been adapted through proper matching network to this constraint. According to this approach (first on-chip antenna co-designed with the LNA, then PA matched to the impedance found as optimal for the LNA) the LNA design has a higher priority than the PA design. Alternative design strategies could be followed, e.g. first on-chip antenna co-designed with the PA, then LNA matched to the impedance found as optimal for the PA. The rationale of our choice is that, given the system specification from the system model in Sect. 2, the LNA performance was much hard to reach than the PA one. Moreover, the 30 Ω impedance value found as optimal for the LNA-antenna matching is not difficult to match also for the PA.

Firstly, taking as reference the topology in Refs. 28, 29 we designed a dipole antenna in CMOS SOI technology using the M_{6Z} metal layer. It has a length of 760 μm with a 23 μm of width for the two-dipole arms and a gap between them of about 1 μm. The integrated dipole can be connected to the active circuitry with a coplanar strip-line of 334 μm length. Such values have been sized to meet the impedance matching of the LNA designed in Sect. 3 and to maximize the gain around 60 GHz. Table 4 shows the area, radiation efficiency, gain performance of the antennas and if their return loss S_{11} is lower than -10 dBm or not, over the target spectrum range 57 to 66 GHz. The same dipole antenna designed in CMOS bulk technology has similar area (the length and width sizing depends mainly on the operating wavelength) while the losses due to the low resistivity substrate lead to a negative gain in bulk CMOS. To improve gain performance of the

dipole antenna we modified it in this work in a folded dipole, which allows a gain in SOI technology of 3.3 dBi with similar area occupation of the simple dipole antenna.

Table 4 shows the area occupied when placing a rectangular macrocell including the different antennas in the chip layout. The real area occupation of all the antennas should consider that other active or passive circuits should not be placed in the near reactive-field region of the radiating structure. This imposes a distance from each antenna structure of at least $\lambda/2\pi$, about 400 μm in our case. Therefore, during chip layout an area of about 1.7 mm^2 is reserved to the dipole antenna and 1.8 mm^2 to the folded dipole one.

Trying to reduce the antenna area occupation, we investigated also a folded PIFA (planar inverted-F antenna) topology that is a folded quarter-wave monopole with a ground plane. The PIFA can be realized with lower area occupation than dipole and the other topologies in a 450 × 250 μm^2 box (0.1125 mm^2). A 1250 × 1050 μm^2 (1.3 mm^2) space has to be left without integrated active or passive devices. The achieved antenna gain with the PIFA in CMOS SOI technology is 6 dB lower than the half-wave dipole. The radiation efficiency of the PIFA is poor (only 15%) and the return loss bandwidth is limited to 5 GHz. Hence, the PIFA area saving of roughly 25% vs. the dipole antenna topology does not justify its adoption due to the reduction in bandwidth and gain. Being the PIFA performance in CMOS SOI technology already well below the target specifications in Table 2 the PIFA has not been realized in bulk CMOS technology.

A planar bow-tie dipole has been also considered since it is a topology known to provide ultra wide band radiation performance. The bandwidth and the lower frequency of this kind of antenna mainly depend on the length of the arms, the center angle, and the length of the smaller base of the trapezium that defines the radiating structure. In this work the bow-tie antenna has been designed with 337 μm length for the arm, 18 degrees for the center angle and 75.5 μm for the length of the smaller base of the trapezium. The bow-tie antenna can be connected to the LNA through a stripline of length 648 μm. The bow-tie allows for the best bandwidth performance since the S_{11} is below -10 dB for more than 20 GHz starting from a 50 GHz lower limit. However, its gain is far from the system-level requirements.

Finally as an alternative to the above antennas, we evaluated also the double slot topology already proposed in Ref. 44 with a coplanar wave-guide feeding line of length 560 μm and width 22 μm. The double slot has a length of 910 μm and a width of 22.76 μm. The gap between antenna and ground plane is 40 μm. This antenna exhibits good radiation efficiency, 67%, and maximum gain result, 4.44 dBi, among the antenna topologies considered in this work. The peak return loss (S_{11}) has also a good value, -23 dB. However, the useful bandwidth of the double slot antenna, where the S_{11} is below -10 dB, is only from 59 to 60 GHz. The result of 1 GHz useful bandwidth is too narrow with respect to the target spectrum of interest from 57 to 66 GHz. An area of about 2.3 mm^2 (including the 0.51 mm^2 of the effective layout antenna occupation) should be left without integrating other active or passive devices.

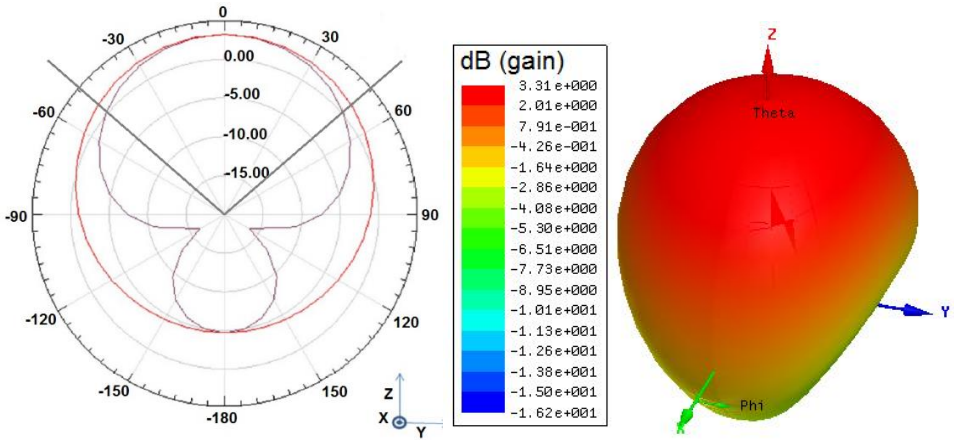

Fig. 6. Radiation pattern of the selected antenna

As conclusion, considering the trade-off among multiple design parameters (gain, efficiency, useful bandwidth, area occupation) a folded dipole topology in 65 nm SOI technology has been selected (second row of Table 4). This on-chip antenna meets the target specification in Sect. 2 with a 3.3 dBi gain, return loss below -10 dB for the entire 9 GHz spectrum, LNA impedance matching at 30 Ω. Fig. 6 shows the 3D radiation pattern for the selected folded dipole antenna and its projection along the YZ axis. The 3dB beamwidth is about 100 degrees (see gray lines in Fig. 6 from about -50 to + 50 degrees).

If we compare the results of on-chip antenna to other works in literature proposing a 60 GHz transceiver with an off-chip antenna, e.g. Yagi-Uda[45] or Patch-array[46] printed on the electronic board, the following considerations can be done. The off-chip antenna can allow at 60 GHz for much higher gain, from 3 dBi to 14 dBi in Ref. 46 with a patch array occupying an area of tens of mm^2. However, the proposed on-chip antenna approach offers the potentiality of a very compact design: the antenna is already included in the integrated transceiver with an area cost below 2 mm^2, one order of magnitude lower than the area occupied by off-chip antenna printed on the electronic board. The achieved gain of the on-chip antenna is still enough to exploit the full capability of 60 GHz links since short-range communications up to 20 m (see results in Sect. 6) can be achieved.

Table 4. On-chip antenna results in 65 nm CMOS technology

Topology	Tech.	Gain, dBi	Effic. %	$S_{11} < -10$ dB, 57-66 GHz	Area, mm^2
Half-wave Dipole [29]	SOI	3.05	65	Y	0.25
	Bulk	-2.27	34		
Folded-dipole	SOI	3.31	66	Y	0.26
Double slot [44]	SOI	4.44	67	N	0.51
PIFA	SOI	-3.35	15	N	0.11
Bow-Tie	SOI	-3.2	37	Y	0.49

	Bulk	-7.3	20		

5. mm-Wave Linear PA for 5G Communications

The multicarrier modulations that will be massively exploited in 5G communication with high PAPR require a linear PA. Avoiding more efficient but non-linear topologies such as class-C or class-E PA, a class-A amplifier with a 2-stage Common Source (CS) topology and inter-stage LC matching networks has been designed in 65 nm CMOS SOI technology. As already discussed for the LNA and antenna designs the low-cost bulk CMOS technology version leads to remarkable performance drop vs. the CMOS SOI one at mm-wave and hence is not further discussed. Even though a cascode topology is normally more efficient for a PA to achieve high gains, at low-voltage operation (1.2 V) stacking the CS and the CG determines a limited output voltage-swing that would compromise the OP1dB of all the cascaded system. The problem could be solved employing a folded-cascode topology and cascading several stages but the power consumption would be nearly doubled vs. conventional cascode. The proposed class-A PA circuit in Fig. 7, whose layout is in Fig. 8 (on the right), exploits the benefit of the invariance of the maximum linearity bias current density (0.3 mA/μm) across technology nodes.

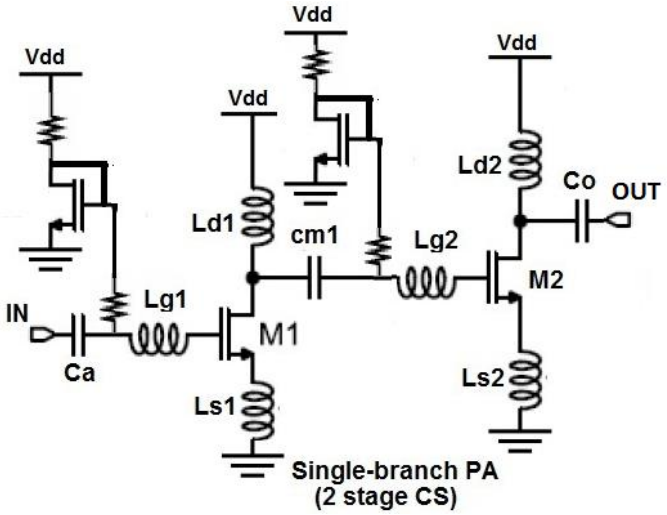

Fig. 7. Single branch 2-stage CS power amplifier circuit

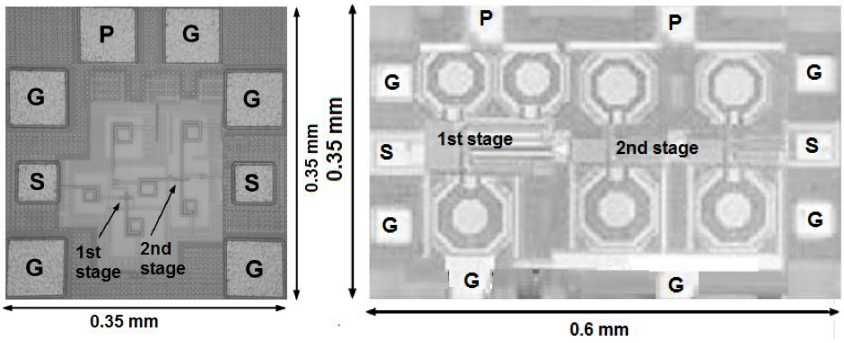

Fig. 8. Layout of a single-branch 2-stage PA (right) and of the 2-stage LNA (left), labels for the pads are G (Ground), S (Signal) and P (Power)

The value of J_{opt} for the PA at TX side, doubled vs. the same parameter considered in Eq. (8) for the LNA at RX side, was experimentally found in Ref. 47. The J_{opt} value for the PA remains constant for different finger widths and technology nodes, even in a cascode topology.[17] With a 1.2 V power supply the PA circuit proposed in Fig. 7 has a gain of 7 dB at 60 GHz (varying from roughly 8 dB at 57 GHz to 6 dB at 66 GHz), a 1-dB output compression point OP1dB of 8.2 dBm and a 1-dB input compression point IP1dB of 1.76 dBm. The DC power is 44 mW. The peak PAE (power-added-efficiency) is 11.5%. The return loss (S_{11} parameter) is always below -10 dB, in the target 57-66 GHz spectrum. The stability factor is higher than 4 for all the frequencies from 57 to 66 GHz, resulting in the unconditional stability of the two-port network. The die area has a size of 0.12 mm^2.

To reach the 10 dBm and 14 dBm system-level specifications about the transmit power outlined in Sect. 2 (see Table 2) the power of multiple PA blocks should be combined. To this aim, we propose the scheme in Fig. 9 where the use of 4-way Wilkinson power divider and combiner allows adding up the output power of 4 PA basic blocks reaching an output power of 13.2 dBm OP1dB. In this case, the DC power consumption of the 4-way PA raises to roughly 180 mW and its area, including the 4 single-branch PAs plus the Wilkinson power divider and combiner, is roughly 0.6 mm^2. An *N*-way Wilkinson power divider is a *N*-port circuit[48, 49] capable of simultaneously achieving port-to-port isolation, impedance matching and ideally not dissipating power if the ports are balanced. Since it is a reciprocal and passive circuit, the use of input and output ports can be reversed and the power divider can be used as a power combiner. For the design of the Wilkinson power combiner and divider circuits we refer to the topology proposed in Ref. 48, re-adapting the circuit schematics from the 130 nm technology to the target 65 nm SOI technology. With respect to the ideal divider/combiner circuits, our realization has an insertion loss of about 0.5 dB for each 4-way Wilkinson stage, i.e. about 1 dB insertion loss for the circuit in Fig. 9. The Ports imbalance is below 0.1 dB and the port isolation is 30 dB for all the ports. Due to these non-idealities the maximum output power, 13.2 dBm is lower than the maximum theoretical value of 14.2 dBm if the combiner/divider circuits would be lossless.

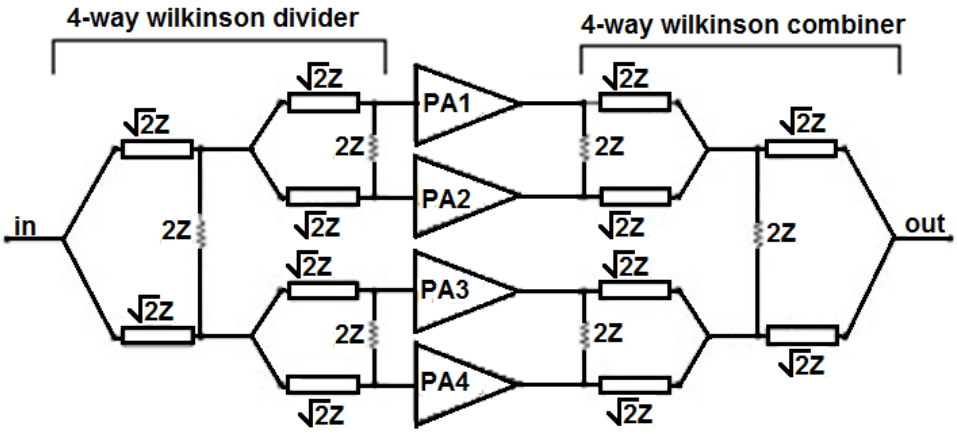

Fig. 9. 4-way PA with Wilkinson power divider and combiner

Table 5. 1dB compression point output power vs. state-of-art

Ref.	Techn. / V_{DD}	OP1dB	Center freq., GHz
This work, 4-way PA	65 nm / 1.2V	13.2	61
[42]	65 nm / 1.8V	8	60
[22]	45 nm / 2V	11.2	60
[23]	65 nm / 1.2V	9.7	52
[24]	45 nm / 1.1V	11	60
[25]	28 nm / 1V	12	53
[26]	90 nm / 1.2V	12.1	N/A
[50]	90 nm / 1.2V	2	60
[46]	90 nm / 1.5V	7.6	60

Table 5 compares the 4-way PA to recent state-of-art[22-26, 42, 46, 50] in terms of OP1dB, i.e. in terms of the delivered output power in the linear region where distortions vs. an ideal linear amplifier are less than 1 dB. Our circuit solution of Fig. 9 allows for best performance in terms of OP1dB, 13.2 dBm, higher even than Ref. 22 but using a lower supply voltage, 1.2 V instead of 2 V in Ref. 22. Using in our case for the PA the same supply voltage of all the other blocks, including also the baseband and digital circuitry, reduces the overall system complexity avoiding extra DC-DC converter in the power management unit.

6. mm-Wave Transceivers Performance for 5G Communications

Taking into account the results of the system analysis in Sect. 2 and the results of key blocks (LNA, on-chip antenna and PA) designed in Sects. 3, 4 and 5, hereafter we estimate the performance of single-chip mm-wave transceivers implemented in 65 nm 1.2 V CMOS SOI technology. For the missing circuitry (e.g. mixers, VCO, etc.) we considered the results achieved in recent literature.[33] By using the folded dipole antenna with the 3-stage LNA, at receiver side a peak gain up 27.7 dB can be reached, with a minimum gain higher than 21 dB over the whole 9 GHz spectrum. With the high LNA

gain performance the noise figure of the receiver is de-facto equivalent to the noise performance of the LNA (minimum 4.3 dB, maximum 5 dB for the whole 9 GHz spectrum) thanks to the Friis formula in (4). Considering also the 13.2 dBm of OP1dB of the 4-way PA, using (6) the maximum connection distance is about 10 m and 15 m for the IEEE 802.15.3c and ECMA-387 standards, respectively. This configuration of the mm-wave transceiver has an area occupation (layout die area excluding pads) of about 2.8 mm^2. The area is dominated by the contribution (1.8 mm^2, see Sect. 4) of the on-chip folded dipole antenna including the area free of passive or active devices around it to avoid interference. The power consumption is 255 mW, dominated by the contribution of the 4-way PA (180 mW). The 3-stage LNA requires 35 mW while the other blocks (mixer, VCO, etc.) require 40 mW.

A second transceiver configuration with a lower power consumption can be obtained by using at receiver side the 2-stage LNA topology and at transmitter side the single branch PA (whose layout is in Fig. 8) while keeping the other blocks (mixer, VCO, etc.) unchanged. This configuration reduces the power consumption to about 110 mW and the area occupation would be roughly 2.2 mm^2. However, the reduced transmitted power of 8.2 dBm OP1dB, and the slightly reduced LNA gain (-1 dB) and increased noise figure (+0.4 dB) lead to a reduction of the maximum achieved distance, halved vs. the first transceiver configuration: 5 m for the IEEE 802.15.3c standard and 8 m for the ECMA-387.

In Table 6 we summarize the main performance estimated for the 2 above transceiver configurations comparing them with published results of state-of-art 60 GHz transceivers in CMOS technology.[28, 45, 46, 50, 51] A direct and fair comparison is difficult to achieve since most of state-of-art tranceiver adopts a simple OOK or incoherent ASK modulation scheme, while in this work we refer to more complex ECMA-387 or IEEE 802.15.3c schemes. Moreover, lots of them target very low connection distances, below 1 m, while in this work we demonstrated that connections up to 20 m are possible. From Table 6 it is clear that using CMOS technologies also advanced links, building up the emerging 5G communication standard, can be realized with connection distances of tens of meters and power and area costs for the transceiver of few hundreds of mW and few mm^2 respectively.

It is worth noting that in the recent literature some works[55-60] present the design in CMOS technology of 60 GHz transceivers employing more complex modulation schemes, such as 16- and 64-QAM. These modulations, compared with the above considered OOK, ASK or BPSK, exhibit higher spectral efficiency, but also lower energy efficiency and higher complexity. For example, 64-QAM was shown to allow a bit-rate of 10.56 Gb/s for each 2.16 GHz channel,[57] and up to 42 Gb/s for the whole 57 GHz to 66 GHz spectrum.[60] Let remark that the all of these 64-QAM modulators used a transmitted output power that was comparable with the values considered in this work and listed in Table 6: for instance, the power setting used in Ref. 60 are P_{sat} = 10.4 dBm and OP1dB = 6.1 dBm.

However, the data rate increase provided by such complex modulation schemes is paid in terms of:
- greater hardware complexity (e.g., in Ref. 60 the core area of the transceiver in 65 nm CMOS technology is 7.18 mm^2, and the sum of the transmitter and receiver power is 976 mW; these values are then much higher than those relevant to the transceivers in Table 6);
- greater *BER* (e.g., between 10^{-2} and 10^{-3} in Refs. 55-60 with respect to 10^{-5}, which is the worst case *BER* of this work, see Table 1) and shorter link ranges (e.g., few cm in Refs. 55-60 with 16- and 64-QAM, while the same transceivers can reach a distance of some meters by adopting a simpler QPSK modulation).
Therefore, for applications aimed at providing data links at a rate of few Gb/s over link distances of several meters, the transceivers analyzed in Table 4 still represent the best suited solution. More complex modulation schemes, instead, can be used for providing higher data rates (up to tens of Gb/s) over distances lower than 1 m, provided that the associated degradation of signal quality (in terms of *BER*) is tolerable.

Table 6. Transceiver comparison vs. state-of-art

Ref.	Antenna Technology and Gain	Data-Rate, Gb/s and Modulation	Distance, m	TX OP1dB, dBm	Area, mm^2	Power mW
Our	On-chip folded dipole, 3.3 dBi gain	3.2 (BPSK ECMA-387)	8	8.2	2 (with antenna)	110
Our			20	13.2	2.5 (with antenna)	255
[45]	Off-chip, Yagi-Uda, 7 dBi gain	10.7 (OOK)	0.1	5	0.5	67
[46]	Off-chip patch array, 14 dBi gain	1 (OOK)	0.6	7.6	1.1	286
[28]	On-chip half-wave dipole, 3.03 dBi gain	2 (OOK)	10	11	3.5 (with antenna)	150
[50]	Off-chip	3.5 (OOK)	N/A	2	4.14	264
[51]	On-Chip, magnetic conductor coupled with wide-slot squared antenna, -2 dBi gain	1.2 (OOK)	0.1	1.2	3.8 (with antenna)	51

7. Conclusions

This paper presented a design exploration at system and circuit levels of mm-wave integrated transceivers for the upcoming 5G wireless communications. A system level model for 5G communications allowed the derivation of transceiver design specifications taking into account multi-Gb/s communication schemes such as LTE-A, ECMA-387 and IEEE 802.15.3c. Several circuit topologies have been designed and compared for the key transceiver blocks in 65 nm CMOS technology considering bulk and SOI technology versions: 3 different LNAs, 2 PAs and 5 on-chip antenna topologies. The proposed circuits allow for different trade-offs in a multi-dimension design space (area, power consumption, gain, noise figure, output power). Differently from classic state-of-the-art

solutions, in this work the antenna is integrated on-chip and is co-designed with the LNA since the fixed 50 Ω impedance matching constraint is removed and the input impedance is considered as a new degree of freedom that can be tuned during the design phase. The results achieved give several hints for the development of upcoming 5G communication technology. CMOS bulk technology offers poor performances, particularly for passive devices (i.e. negative gain of the antenna), and hence is not suited for fully integrated 5G transceiver design. Using a 65 nm CMOS SOI technology at mm-wave (from 57 to 66 GHz), the antenna can be integrated on-chip with positive gain of 3.3 dBi (folded dipole). Multi-stage LNA can be designed with a noise figure below 5 dB and a peak gain up to 24 dB (minimum gain 18 dB in the 9 GHz spectrum). Thanks to the use of mm-wave power combiner/divider a linear 4-way PA with an OP1dB up to 13.2 dBm can be designed. By using these blocks for a mm-wave transceiver design a configuration able to sustain multiple-standards can be derived, with a link distance of 15 m for the ECMA-387 standard and 10 m for the IEEE 802.15.3c one. The power consumption is about 255 mW. Combining other LNA and PA blocks (2-stage LNA and single-branch PA) a low power transceiver configuration, with less than 110 mW, can be obtained but with halved connection link distance. In both transceiver configurations the size of the design is less than 3 mm^2 (excluding pads) and is dominated by the size of the on-chip antenna and of the free space needed around it, about 1.8 mm^2. It is worth noting that the circuit performance reported in the paper refer to typical conditions (1.2 V power supply, 27 ^{0}C). The effect of PVT (process-voltage-temperature) variation for our design is in line with the data reported in literature.[52-54] For example, considering the variation of the noise figure (a key parameter of the transceiver) a 0.2 V degradation in the supply voltage from nominal 1.2 V to 1 V is shown to cause a noise figure increase of about 0.5 dB. A temperature increase of 40 ^{0}C causes a noise figure increase within 0.4 dB. By combining PVT variations (with Monte Carlo process variations) in worst case vs. the typical condition, the noise figure degradation is within 1.5 dB. To attenuate the PVT dependence some techniques have been proposed at the state-of-art[52-54] (e.g. on-chip temperature or power detection circuits to implement a dynamic control of the bias current to compensate the PVT variation effects), which are outside the scope of this paper.

The sustained communication distance and the multi-Gb/s data rate is suitable for high-speed networking in home and office scenarios, or on-board vehicles (cars, trains, satellites, ships, airplanes, airplanes) or body area sensor networks (for healthcare and wellness).

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