# A Back to Back Multilevel Converter for Driving Low Inductance Brushless AC Machines

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## Keywords

«Multilevel converter», «Variable speed drive», «Vector control», «Brushless drive», «AC/AC converter».

## Abstract

Traditionally, multilevel converters are utilised in medium voltage applications, allowing the dc-link voltage to exceed the switch maximum blocking voltage. Here, their application to control high-efficiency brushless permanent magnet synchronous machines exhibiting low phase inductance is explored, the relative advantages being shown to include reduced current ripple and improved harmonic spectrum. A cost benefit analysis is included along with experimental results from a prototype 5-level back-to-back converter.

## Introduction

Six-switch, two level converters have traditionally been used to excite Permanent Magnet Synchronous Machine (PMSM) drive systems. However, as the phase inductance of the machines has reduced, to facilitate the production of high power-dense units with high fundamental electrical frequency, the switching frequency of the converter has had to increase to keep the ripple current within bounds. Since the switching frequency is ultimately limited by losses and device speed limits, multilevel converters are considered an attractive alternative due to their ability to reduce the ripple current without an increase in the switching frequency. Here then, the paper considers a comparison of back-to-back multilevel converters, with a classical two level counterpart, for the control of a relatively low voltage, low inductance PMSM.

## Back-to-Back System Configuration

2×5-level diode clamped converters, connected back to back, have been developed to demonstrate the suitability of multilevel converters for driving low inductance Brushless AC (BLAC) machines in AC-DC-AC applications, Fig.1. The back-to-back connection is utilised to allow balancing of the DC link capacitor voltages under a full range of operating conditions [1] whereas, only a limited operating range is possible if a passive rectifier (diode bridge) is employed [2]. Additional advantages brought by the back-to-back connection have been shown to include: the ability to draw almost sinusoidal currents from the supply, the input power factor can be controlled and the back-to-back topology automatically regenerates power back to the supply when the operating conditions dictate [3]. Alternatively, a passive rectifier draws a pulsed current from the supply and does not allow a regenerative current to return to the supply. The pulsed current can cause Electromagnetic Interference (EMI) and may require the addition of a power filter to the system, whilst an energy dumping circuit would be required if the drive was to operate in the generating region. Furthermore, the back-to-back topology allows the DC link voltage to be varied, within limits, which allows further current ripple reductions and reduced losses during low speed machine operation.

Whilst the matrix converter topology allows 4-quadrant AC/AC conversion, it does not provide the benefits of reduced current ripple and associated reduced machine eddy current losses that the multilevel topology offers.

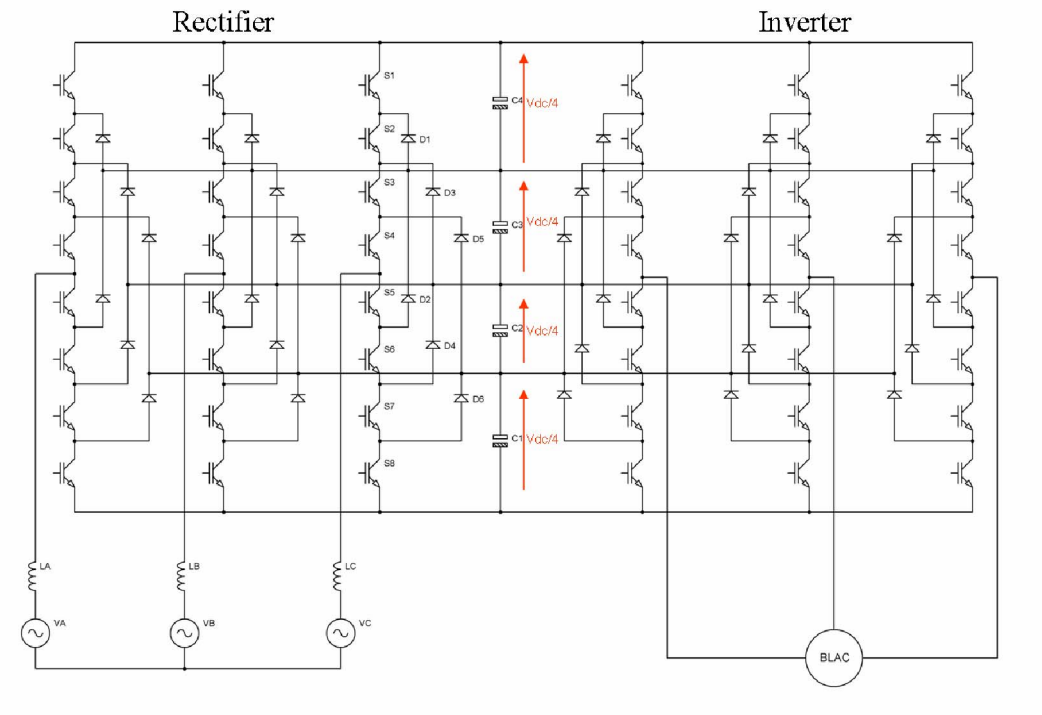


Fig. 1: 5-Level Diode Clamped Back-to-Back Converter

Referring to Fig.1, the two converters are connected by the multilevel DC link created by the series connection of 4 capacitors (C1 - C4). Each phase is constructed from 8 switches (S1 - S8) and 6 clamping diodes (D1 - D6). The output voltage is formed by operating switches S1, S2, S3 and S4 complementary to switches S5, S6, S7 and S8 respectively. For example, to produce a voltage of $3V_{DC}/4$, at the C phase rectifier input, switches S2 - S5 are closed and switches S1, S6 - S8 are open. Diode D1 then clamps the phase C rectifier input to $3V_{DC}/4$ for current flowing from the rectifier to the supply and diode D2 does the same for current flowing from the supply into the rectifier.

Providing correct balancing of the DC link voltage across the 4 DC link capacitors, each switch experiences a voltage of $V_{DC}/4$ across its terminals and the clamping diodes experience up to $3V_{DC}/4$ depending upon their position in the circuit. The inductors in series with the 3 phase voltage supplies fulfil 3 purposes: i) to provide energy storage to allow for voltage boost operation of the rectifier, ii) to provide a reactive voltage drop permitting input power factor control and iii) to filter converter switching frequency harmonics in the 3 phase supply currents.

## Control of Back-to-Back Converter

Fig. 2 illustrates the Field Orientated Control (FOC) scheme employed to control the inverter and rectifier. The machine currents are converted into the rotating dq axis such that simple proportional + integral (PI) controllers can be used. The d axis current is controlled to be zero and the q axis current is used to control the torque with the addition of an outer speed control loop. In order to balance the voltages across the series connected DC link capacitors a switching scheme detailed in [1, 4] is employed. This scheme uses a minimum energy principle to choose the best redundant switching vectors in each modulation period such that the DC link capacitor voltage imbalance is minimised. Rotor position is obtained with a resolver.

The rectifier control is similar to that of the inverter with the exception of the outer control loop managing the total DC link voltage and position information being obtained from a phase locked loop locked to the 3 phase supply voltage.

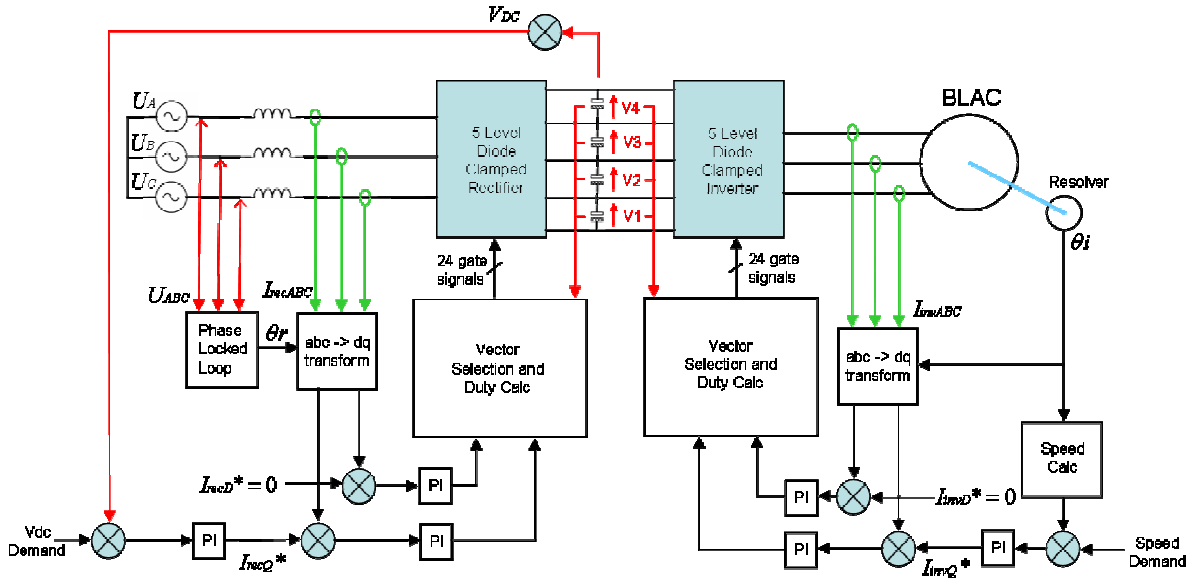


Fig. 2: Control Scheme

The control scheme is implemented on a Texas Instruments TMS320C6713DSK development board with peripheral support such as analogue to digital conversion and resolver to digital conversion on a custom made daughterboard. The required gate drive signals are generated using a Xilinx Spartan 3 FPGA development board. The experimental rig is shown in Fig. 3.

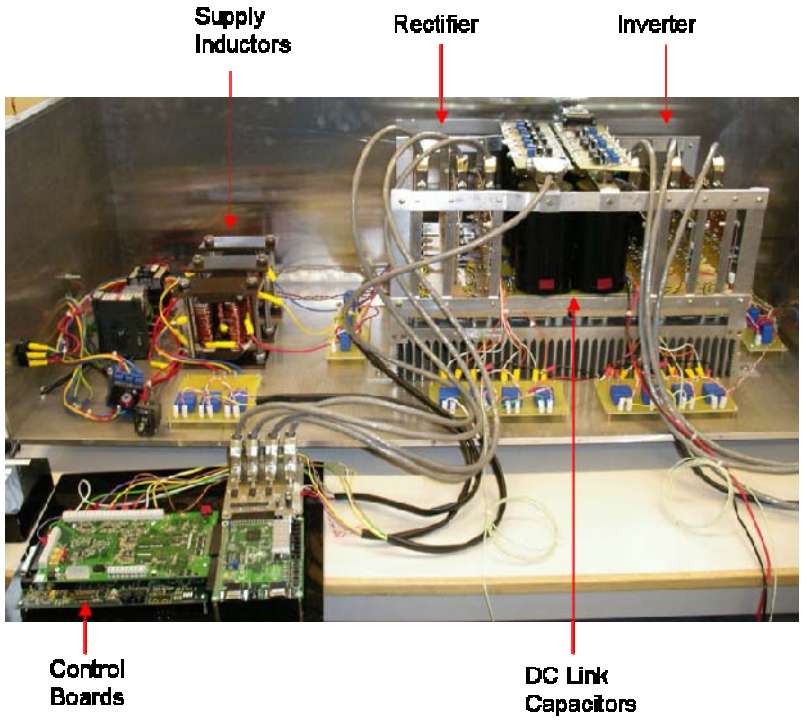


Fig. 3: Experimental Rig

## Current Ripple Analysis

In BLAC drive systems, current ripple is caused due to the non-perfect estimation of the required sinusoidal voltage drive waveforms from PWM approximations. As the inductance of the machine is reduced, to facilitate high speed, high power dense machines, this current ripple will increase which is undesirable due to the creation of a ripple torque and increased losses in the machine due to eddy currents [5].

Considering the electrical equation of the BLAC machine for a single phase:

$$V = IR + L\frac{dI}{dt} + E \tag{1}$$

where $V$, $I$, $R$, $L$ and $E$ are the terminal phase voltage, machine phase current, phase resistance, phase inductance and back-emf respectively, it is possible to derive an equation for the peak-to-peak current ripple when driven by a classical 2-level converter. Considering further that the converter is modulated with a PWM signal of duty cycle $\partial$ and switching frequency $F$ operating from a DC link voltage of $V_{DC}$, the peak-to-peak current ripple is given by:

$$I_{pp} = \frac{V_{DC}}{FL}\left(\partial - \partial^2\right) \tag{2}$$

This derivation makes the assumptions that the average current remains constant during a single PWM period and that all the ripple voltage due to the ripple current appears across the inductance. The maximum value of (2) occurs at $\partial = 0.5$. A similar analysis can be performed for the multilevel case with $n$ levels, giving:

$$I_{pp} = \frac{V_{DC}}{LF}\left(\partial - (n-1)\partial^2\right) \tag{3}$$

For example, a 3 level converter has maximum peak-to-peak current ripple values at $\partial = 0.25$ and $\partial = 0.75$ with the maximum value being half that of the 2-level case since the incremental voltage applied to the machine is $V_{DC}/2$.

Fig. 4 shows the results of this analysis for 2, 3, 4 and 5-level converters. The currents data have been normalised to that of the maximum peak-to-peak current ripple for 2-levels. It can be seen, from Fig. 4 that 3, 4, and 5-level variants reduce the current ripple by 50%, 33% and 25%, respectively, compared to classical 2-level variants. A similar analysis has been performed in [6] for a 5-level converter.

Fig. 5 shows simulated current ripple under a q axis step current demand of 100A for a machine with $100\mu H$ phase inductance operating from a 600V DC link. With the d axis current controlled to be zero, a steady q axis current demand results in a constant torque produced by the machine, which further results in a steady acceleration of the machine when zero load torque is applied. The voltage demand (or peak duty cycle) therefore sweeps from zero to a maximum of 1. The normalised peak current ripples can therefore be compared between the theoretical values in Fig. 4 and the simulated values in Fig. 5. It can be seen that the simulated maximum peak-to-peak ripple current for 3, 4 and 5-levels is reduced by 51%, 37% and 27%, respectively, over the 2-level converter which corresponds well with the theoretical results in Fig. 4.

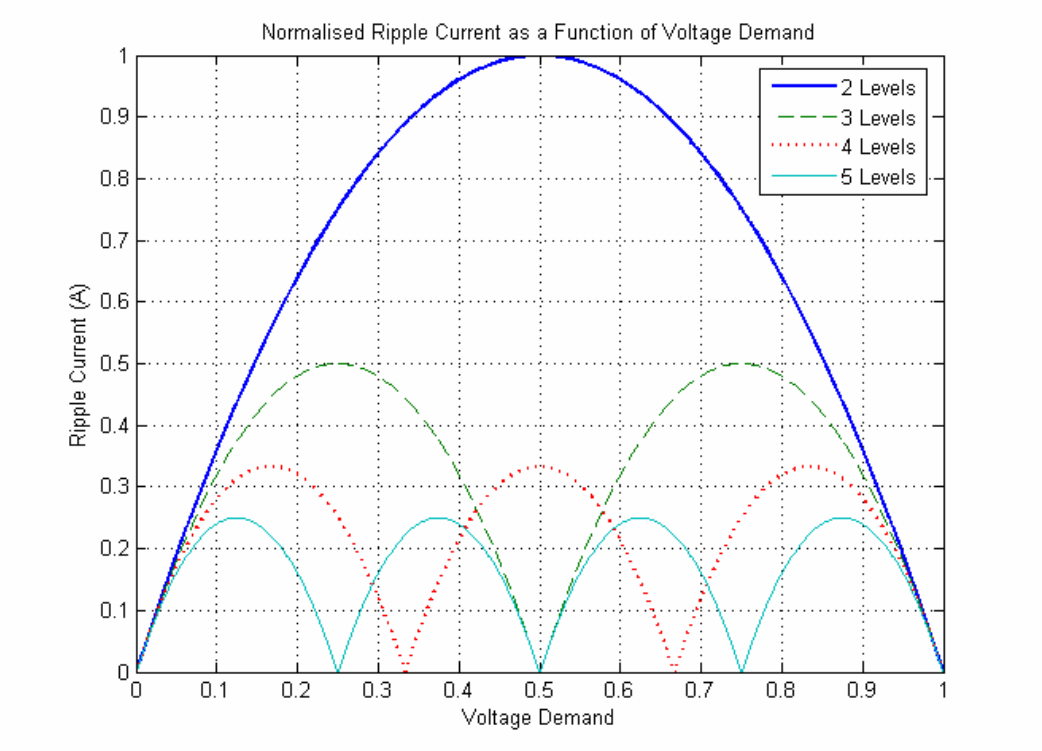


Fig. 4: Peak to Peak Ripple Current Vs Converter Voltage Demand

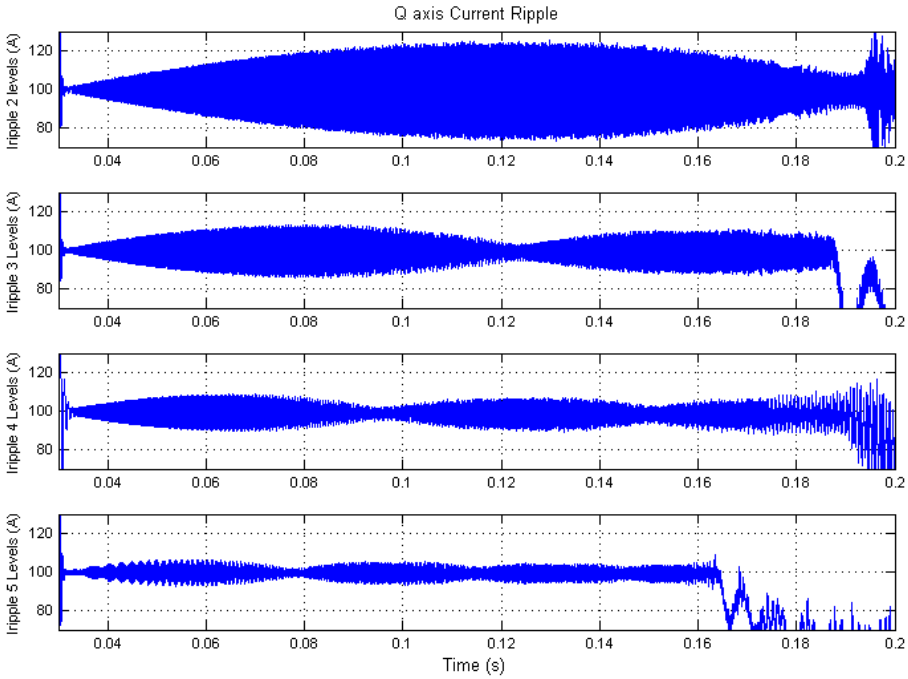


Fig. 5: Simulated Current Ripple

## Harmonic Performance

The multilevel back-to-back system is also used to investigate the expected reduction in Total Harmonic Distortion (THD) of the currents flowing in the BLAC machine. The inverter is controlled such that the machine operates at a constant speed under a fixed load torque in order that the machine currents are of constant frequency and amplitude at steady state. A section of machine current data is extracted from the simulation results and a Fast Fourier Transform (FFT) is applied to estimate the

harmonic content of the currents and calculate a THD value. For each converter a speed demand is chosen to provide maximum ripple current allowing a proper comparison between the different levels.

Table I shows the percentage THD and the THD normalised to the 2-level value. Fig. 6 shows a plot of the normalised THD values versus converter levels. It can be seen that the THD improves as the number of levels increases and also that it follows in the similar pattern of roughly 50%, 33% and 25% reduction over 2-levels as in the case of the current ripple.

| Levels | THD (%) | Normalised THD |
|---|---|---|
| 2 | 15.3 | 1 |
| 3 | 7.8 | 0.51 |
| 4 | 5.8 | 0.38 |
| 5 | 4.1 | 0.27 |

**Table I: Total harmonic distortion of machine currents**

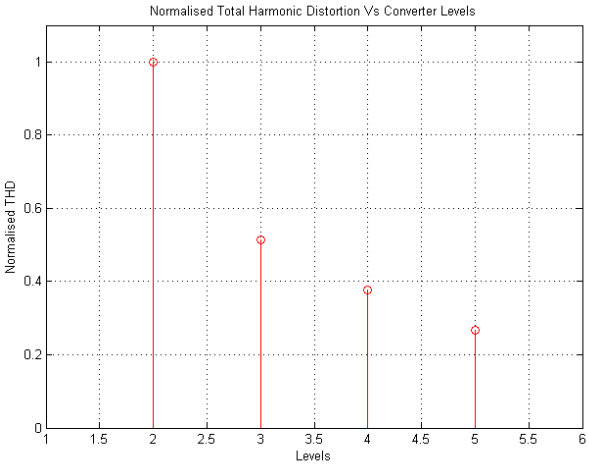


Fig.6: Normalised THD versus Converter Levels

## Cost of Multilevel Converters

The main disadvantage of employing multilevel converters is the increased number of components required and hence the increase in cost. This section aims to estimate the cost of diode clamped converters and compare it against the benefits of reduced current ripple produced by the multilevel action.

Table II shows the number of the main components in 2, 3, 4 and 5-level converters, along with an estimated cost for a single converter. Table III shows the same data for back-to-back connected converters. In both cases the estimated cost has been normalized to the cost of a single classical 2-level converter. To derive this data the following points are noted:

- The price data was collated from the Farnell 2006 catalogue, where devices were chosen from the same family where possible, to fit with a 5kW drive rating.
- It is assumed that the capacitor balancing scheme operates correctly and so the voltage rating of devices such as IGBTs and DC link capacitors are reduced for an increasing number of converter levels.
- IGBTs were chosen with integral freewheel diodes and so these diodes do not appear in Tables II and III.
- The number of current and voltage transducers was set to measure each variable required in the control algorithm, even when one value could be inferred from others, e.g. 3 current transducers are specified for measuring the 3 phase machine currents.
- The cost of the required control was not considered but it should be noted that the complexity of the capacitor balancing algorithm rises sharply with an increasing number of converter levels.

**Table II: Number of main components and estimated cost for a single converter**

| Converter Levels | IGBTs | Clamping Diodes | DC Link Capacitors | Gate Drive Circuits | Voltage Transducers | Current Transducers | Normalized Cost |
|---|---|---|---|---|---|---|---|
| 2 | 6 | 0 | 1 | 6 | 0 | 3 | 1 |
| 3 | 12 | 6 | 2 | 12 | 1 | 3 | 1.23 |
| 4 | 18 | 12 | 3 | 18 | 2 | 3 | 1.65 |
| 5 | 24 | 18 | 4 | 24 | 3 | 3 | 2.21 |

**Table III: Number of main components and estimated cost for a back-to-back converter**

| Converter Levels | IGBTs | Clamping Diodes | DC Link Capacitors | Gate Drive Circuits | Voltage Transducers | Current Transducers | Normalized Cost |
|---|---|---|---|---|---|---|---|
| 2 | 12 | 0 | 1 | 12 | 4 | 6 | 1.98 |
| 3 | 24 | 12 | 2 | 24 | 5 | 6 | 2.50 |
| 4 | 36 | 24 | 3 | 36 | 6 | 6 | 3.31 |
| 5 | 48 | 36 | 4 | 48 | 7 | 6 | 4.24 |

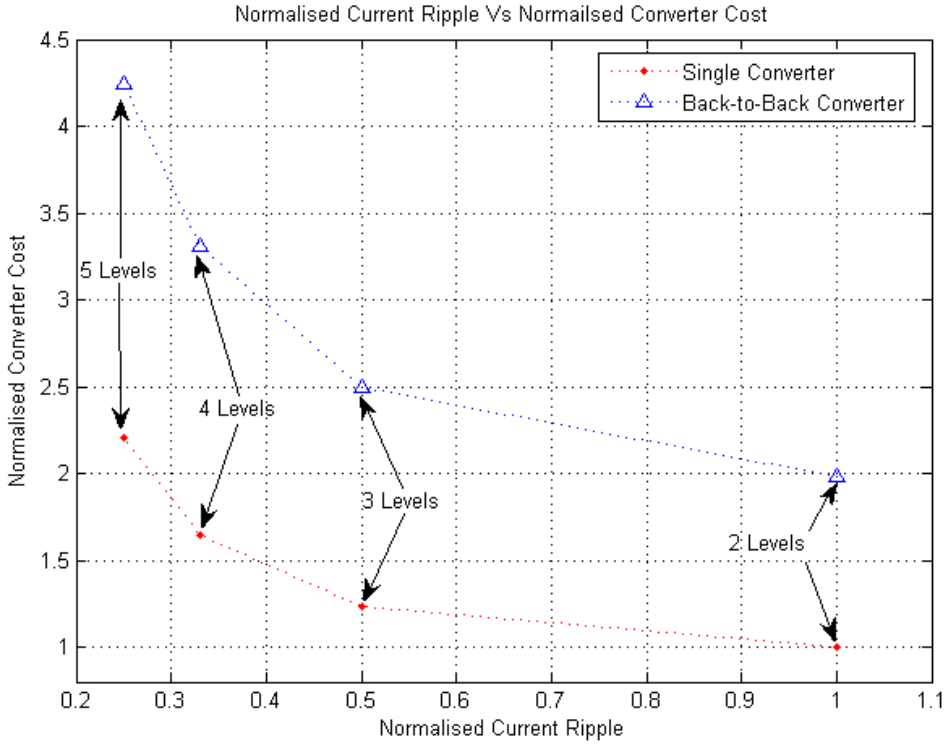


Fig. 7: Comparison of number of levels, converter cost and theoretical current ripple

Fig. 7 compares the normalised converter cost against the theoretical maximum current ripple for 2, 3, 4 and 5-level converters for both single converters and the back-to-back case. It shows that for just over 2x the cost, a reduction of 4x the maximum current ripple can be achieved in specifying a 5-level converter over a classical 2-level converter.

Fig. 7 also shows that the back-to-back converters are approximately 2x the cost of a single converter due to having almost 2x the number of components. The additional advantages of having almost sinusoidal input currents, unity power factor and allowing for regeneration, offset this cost for AC-DC-AC applications.

## Experimental Results

This section includes experimental results obtained from the prototype back-to-back converter which was controlled to produce both 5-level and 2-level outputs to allow comparisons between the different levels to be drawn.

Fig. 8 shows a measured phase current in a relatively high inductance (20mH) BLAC machine for both 2 and 5-level converters. The rectifier operated from a 25Vrms, 400Hz supply to generate a 120V dc link while the inverter operated at modulation index of 0.9 and a switching frequency of 24kHz. A mechanical load for the BLAC machine was provided by a brushed DC machine. Fig. 8 illustrates the reduction in current ripple between 2 and 5-levels. In this case the maximum current ripples were found to be 122mA pk-pk and 34 mA pk-pk for the 2 and 5-levels respectively. This corresponds to a reduction to 28% of the 2-level maximum current ripple for the 5-level converter which corresponds well with the theoretical reductions shown in Fig. 4.

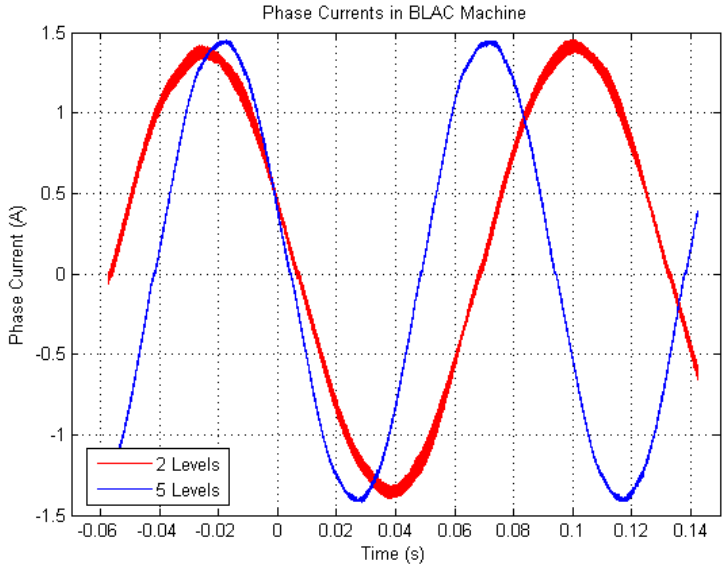


Fig 8: Machine phase currents for high inductance machine.

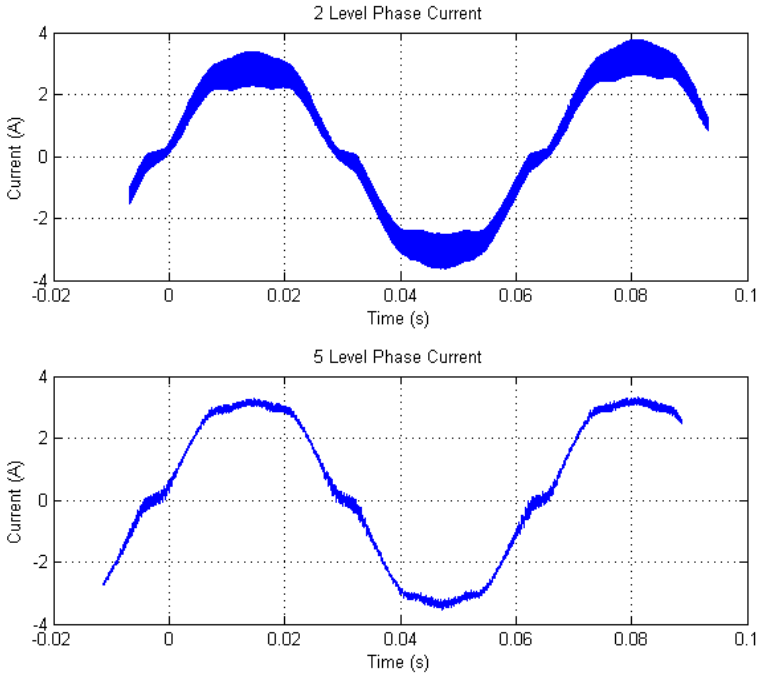


Fig. 9: Phase Currents in 3 phase 500µH inductors

In order to test the performance at low inductances three, star-connected, 500μH inductors were driven by the back-to-back converter operating from a 50Vdc link. A single inductor current is shown in Fig. 9 for both 2 and 5-levels. Again the reduction in maximum current ripple can be seen from Fig. 9 where the maximum current ripple is 1.12A pk-pk and 0.31A pk-pk for the 2 and 5-levels respectively.

The currents data in Fig.9 was used to calculate a THD figure giving 13.5% and 8.0% for the 2 and 5-levels respectively. This shows a reduction to 59% of the 2-level THD for the 5-level converter.

## Conclusion

For an increased cost, diode clamped multilevel converters are an attractive alternative to classical 2-level, six switch converters for AC-DC-AC motor drives employing low inductance brushless ac machines. Benefits shown are reduced current ripple and improved harmonic content of motor currents. The increase is cost can be justified for applications where the current ripple would be prohibitively large, resulting in a large torque ripple and high machine eddy current losses, when driven with a classical 2-level converter. Experimental results from a prototype 5-level back-to-back converter have been included to verify the theoretical and simulated claims.

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