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Gbps Wireless Transceivers for High Bandwidth Interconnections in Distributed Cyber Physical Systems

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ABSTRACT

In Cyber Physical Systems there is a growing use of high speed sensors like photo and video camera, radio and light detection and ranging (Radar/Lidar) sensors. Hence Cyber Physical Systems can benefit from the high communication data rate, several Gbps, that can be provided by mm-wave wireless transceivers. At such high frequency the wavelength is few mm and hence the whole transciever including the antenna can be integrated in a single chip. To this aim this paper presents the design of 60 GHz transciever architecture to ensure connection distances up to 10 m and data rate up to 4 Gbps. At 60 GHz there are more than 7 GHz of unlicensed bandwidth (available for free for development of new services). By using a CMOS SOI technology RF, analog and digital baseband circuitry can be integrated in the same chip minimizing noise coupling. Even the antenna is integrated on chip reducing cost and size vs. classic off-chip antenna solutions. Therefore the proposed transciever can enable at physical layer the implementation of low cost nodes for a Cyber Physical System with data rates of several Gbps and with a communication distance suitable for home/office scenarios, or on-board vehicles such as cars, trains, ships, airplanes.

Keywords: Distributed systems, Cyber Physical Systems, Wireless sensing nodes, Gbps connections,

1. Needs of High Speed Wireless Connections in Cyber Physical Systems

Cyber Physical Systems are feedback systems where sensing, actuation, and processing is usually distributed among several nodes (Electronic Control Units, Actuator Control units and smart sensors) connected through digital networks, both cabled or wireless [1, 2]. Indeed most of today control systems are realized according to a distributed paradigm to improve the scalability and flexibility of the solution, to increase the interoperability of subsystems from different providers/vendors, to reduce the "single point of failure" risk of a centralized approach.

A key issue in emerging Cyber Physical Systems is the networking at high speed of all the nodes belonging to the network. In this scenario there is a growing use of high speed sensors like photo and video camera, radio and light detection and ranging (Radar/Lidar) sensors, photo detectors and so on, to increase the knowledge of the environment where the system is operating, and to increase the amount of data acquired and used by the "cyber" part of the system to make a decision/actuation.

This increases the need for high speed communications, with wireless connections to avoid wiring harness, beyond 1 Gbps [3-5]. Hence at the physical level of a Cyber Physical System there is the need of high speed wireless solutions reaching data rates well beyond the tens of Mbps offered today by Wireless LAN or Bluetooth devices. To this aim some standardization initiatives such as the Wi-Gig alliance have been already started and a new IEEE 802.11ad standard is emerging [6-8].

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Gbps wireless data transfer is also the target of the upcoming 5G generation of mobile communications. Since Fiber to the Cabinet (FTTC) solutions are already available for high speed cabled connections, the next challenge to win is the development of Gbps wireless connections [9]; the convergence of high speed fiber and wireless networks should be also realized [9-11]. This trend characterizes several application fields of which transports, surveillance, domotics, health at home, aerospace, defence, smart cities and smart offices are just some examples.

From the hardware perspective the wireless transceivers have to be integrated in the Cyber Physical System nodes to keep low their cost, power consumption and size. Lowering the power consumption allows for increasing the battery life or even allows for supplying the nodes with energy harvesting sources avoiding the extra cost, size and weight of power supply wires/cables.

To address the above issue the paper proposes the design of integrated transceivers, implemented using the same CMOS technology of the digital part, able to reach a transfer data rate above 1 Gbps at a distance of at least 10 meters. This can enable the diffusion of local area network of high speed sensing and processing nodes in home and office scenarios, or on-board vehicles such as cars, trains, satellites, ships, airplanes.

Indeed is the RF part the most challenging to be designed while the state of art is rich of solutions for the A/D converters or for the baseband signal processing chain [12].

Hereafter Section 2 presents the 60 GHz transciever architecture, while Section 3 discusses achievable link performance of ten nodes placed at distances from 1 cm to 10 m. Finally, conclusions are drawn in Section 4.

2 60 GHz Transceiver Architecture

To design the wireless transceiver the selected target frequency is 60 GHz. Indeed around such frequency band there is a worldwide available free spectrum of several GHz, e.g. 7 GHz bandwidth from 59 to 66 GHz in Europe [13-18]. Moreover, at such high frequency the wavelength amounts to few millimeter and hence also the antenna can be integrated on chip further reducing area and complexity.

Even adopting a simple modulation scheme like the OOK (On-Off Keying) or in-coherent ASK (Amplitude Shift Keying) with a spectrum efficiency of 1 bit/s/Hz, a data rate of several Gbps can be achieved while the complexity and cost of the transciever is kept small. Indeed as reported in Fig. 1 for an in-coherent ASK receiver just an envelope detector is needed at receiver side.

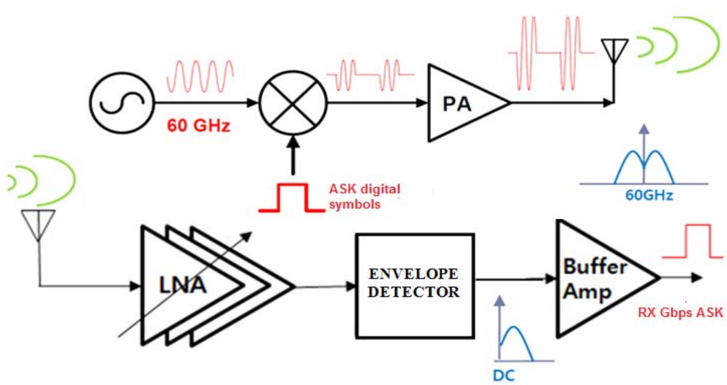

Fig. 1: Architecture of the transciever

Avoiding complex PLL (Phased Locked Loop) for local oscillators and synchronizations and avoiding high-Q LC filter the whole transciever can be integrated single-chip with a small area and with very low power consumption in wireless smart sensor or actuation nodes. Using more complex modulation schemes like multi-carrier technology with Quadrature-amplitude constellation a higher spectrum efficiency and hence a higher bit-rate can be achieved. However this spectrum efficiency will be paid in terms of reduced robustness of the system and increased cost and complexity of the nodes belonging to the network. Since Cyber Physical subsystems are feedback systems, often operating in harsh environments, the most suited trade-off among cost, complexity, robustness, spectrum efficiency and bit-rate is achieved with OOK/ASK schemes.

We designed the ASK incoherent transceiver whose architecture is reported in Fig. 1 in a 65 nm CMOS Silicon On Insulator (SOI) technology. The voltage supply for all the circuits, including Low Noise Amplifier (LNA) and Power Amplifier (PA), is 1.2 V. Cadence and HFSS tools have been used. The SOI version of the CMOS technology allows for much better performance of the RF circuitry vs. classic bulk technology minimizing parasitic passive components and avoiding RF power irradiation losses in the substrate. Thanks to the insulator substrate the signal coupling between the digital, RF, and baseband analog parts of the circuit is reduced. Hence a CMOS SOI technology provides the right trade-off balance between performance and cost for the mixed-signal electronics required in the sensing/actuation nodes of a Cyber Physical System.

The receiver we designed is characterized by a noise figure (NF) of about 4 dB with a gain for the LNA higher than 20 dB. Thanks to the Friis formula and the gain of the LNA stage, the NF of the receiver is due to the NF of the LNA itself. The LNA has a 2 stage cascode circuit solution with inter-stage transmission line coupling. The power consumption of the LNA amounts to 10 mW.

Since the antenna is integrated on chip, tightly coupled with the LNA, the classic 50 Ohm impedance matching constraint can be removed. Therefore the impedance value at which the antenna and the LNA are matched is a new degree of freedom in the design space, to be exploited to optimize receiver performance such as noise, gain and power consumption. In this design an optimal trade-off between the different receiver cost of figures has been found with a 75 Ohm impedance value.

The designed transmitter, see Fig. 2, has a maximum transmitted power of 12 mW before saturation. It has been realized as the cascade of a differential 60 GHz local oscillator, an OOK modulator controlled by the D_IN digital input, and a pseudo-differential power amplifier. Each branch of the power amplifier (PA#1 and PA#2 in Fig. 2) has a multi-stage class A common source (CS) topology with LC inter-stage matching, as reported in the schematic of Fig. 3. The power efficiency is in the order of 10% which can be considered a quite good result at these frequencies if compared to the state of art results [17-20].

The power consumption of the whole transciever is around 160 mW: 150 mW supply for the transmitter and the rest for the receiver.

A double slot antenna has been integrated on-chip with a total area occupation less than 1 mm^2. The on-chip antenna features a S11 bandwidth of 8 GHz and a gain of roughly 3 dBi. Other antenna topologies have been investigated such as bow-tie antenna and inverted-F antenna. The inverted-F antenna reduces area while the gain is much lower than the double slot. The Bow-tie is an end fire antenna while in Cyber physical Systems with nodes distributed in the environment a more "omni-directional" antenna, such as the double slot can be preferred.

Therefore the 8 GHz bandwidth of the antenna make it suitable for 60 GHz applications where 7 GHz of unlicensed bandwidth are available. The gain of 3dBi is not so high but, as discussed in the next section, is enough to ensure a communication distance range up to 10 m.

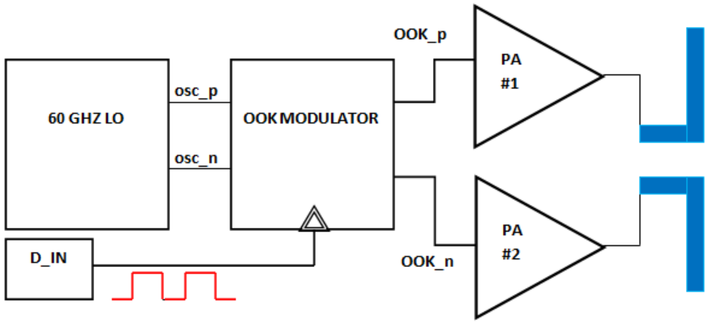

Fig. 2: Block diagram of the transmitter with pseudo differential PA and On-chip dipole antenna

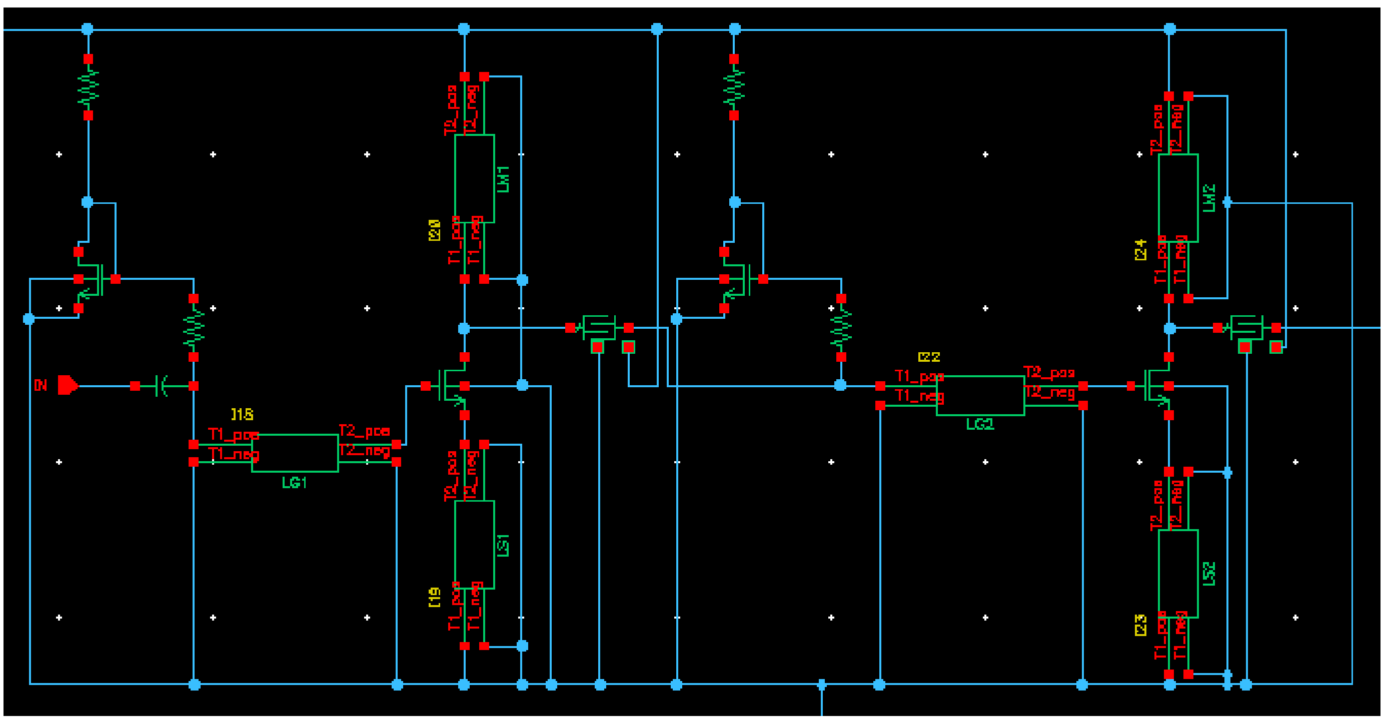

Fig. 3: Power amplifier circuit (2 stage class-A with LC inter-stage matching)

3 Data Link Performance

Using the transceiver designed in Section 2 the achieved data rate from 59 to 66 GHz is smaller than the theoretical 7 Gbps (7 GHz x 1 bit/s/Hz). Indeed to improve the bit error rate and packet error rate performance of the link a channel coding scheme is used at baseband. Adopting a Reed-Solomon channel coding approach in the baseband signal processing chain a coding gain of 8 dB is achieved with a redundancy of 40%. Therefore the maximum effective achievable data rate is roughly 4 Gbps.

With reference to the designed integrated transceiver we have set up a simulation environment for a network of ten nodes placed at distances from 1 cm to 10 m. Fig. 4 reports the simulated Signal to Noise Ratio (SNR) as a function of the connection distance. Fig. 5 reports the simulated Bit Error Rate (BER).

As result the integration of our transciever can enable at physical layer the implementation of very low cost, single chip, integrated antenna, nodes with data rates of several Gbps while ensuring a distance communication range up to 10 m. The proposed technology can enable the realization of a point-multipoint link in which each node of the network can communicate with each other without wiring in a dynamic configuration. This is a key enabling technology for the success of Cyber Physical Systems where high speed sensor nodes are used such as radars, cameras, array of detectors and so on.

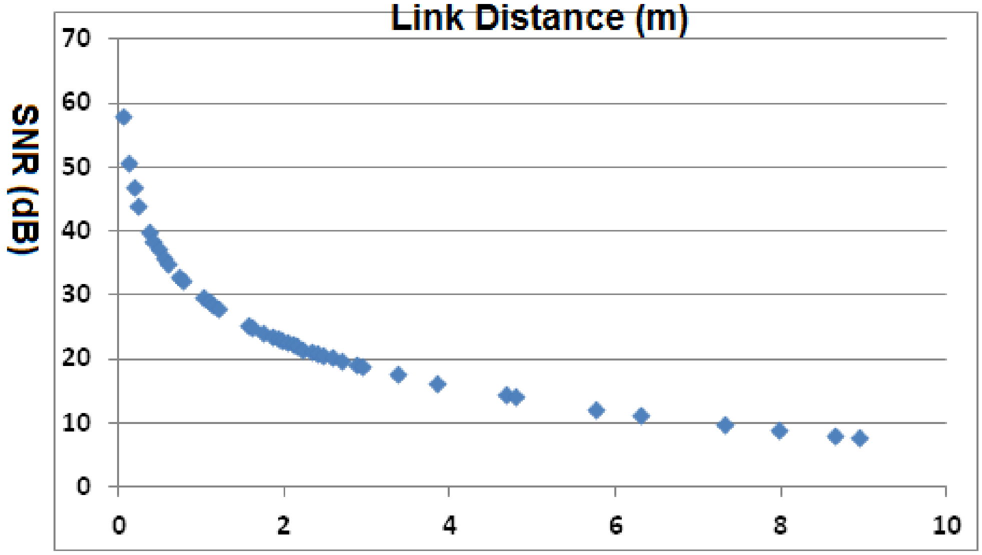

Fig. 4: Simulated SNR (dB) vs. connection distance (m)

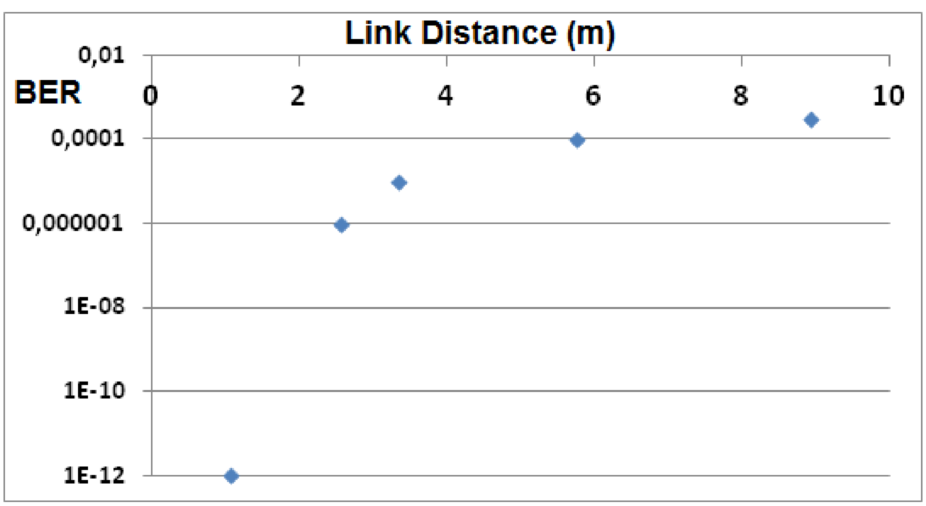

Fig. 5: Simulated BER vs. connection distance (m)

At higher layers of the networking protocol stack our solution can be made compliant with upcoming IEEE 802.11ad wireless networking standard [6, 7] (WiFi/WiGig Alliance) that foresees 3 physical layer frequencies at 2.4 GHz, 5 GHz and 60 GHz. This standard will make easy also the interoperability of the new emerging 60 GHz communication link with pre-existent Bluetooth or WLAN links at 2.4 GHz and 5 GHz.

4 Conclusion

Cyber Physical Systems where high bandwidth sensors are used can benefit of the high communication data rate, several Gbps, that can be provided by 60 GHz wireless transceivers. At such high frequency the wavelength is few mm and hence the whole transciever including the antenna can be integrated in a single chip of few squared mm^2. With a power consumption of about 160 mW the transceiver has a maximum transmitted power of 12 mW that ensures connection distance up to 10 m. By using a CMOS SOI technology RF, analog and digital baseband circuitry can be integrated in the same chip minimizing noise coupling. Therefore the proposed transciever can enable at physical layer the implementation of low cost nodes for the Cyber Physical System with data rates of several Gbps and with a communication distance suitable for home and office scenarios, or on-board vehicles such as cars, trains, satellites, ships, airplanes.

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