A three-phase to single-phase matrix converter for high-frequency induction heating

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Abstract

The paper describes a new three-phase to single-phase matrix converter featuring unity input power factor, very low input total harmonic distortion, and soft-switching over the full power range, for high frequency induction heating applications. A variable output pulse density modulation scheme has been proposed for stable operation of the converter, with the notable feature of requiring no on-line calculations for the synthesis of three-phase input current system. Practical issues in realising the converter, viz. line frequency synchronisation and output current circulation, are described. Good agreement between simulation and experimental results confirm the benefits of the proposed converter.

Introduction

Radio frequency (R.F.) induction heating requires a high frequency AC power supply, typically 100-200 kHz. However, the conventional AC-DC-AC converter topology makes use of large energy storage components, and requires complicated control algorithms to provide a unity power factor sinusoidal input current [1], [2]. Other systems [3]-[6] usually assume that a DC power supply is available, requiring power quality improvements for interfacing to the utility supply, as reviewed in [7], [8]. Recently, matrix converters offering direct AC-AC conversion whilst requiring near-zero energy storage components, have attracted a great deal of attention. Although matrix converters are well-known for synthesizing relatively low frequency outputs from the utility supply [9]-[13], there remains limited material concerning the use of matrix converters for high frequency applications, viz. induction heating. Generally, since fast switching devices are used in matrix converters, it is possible to make a high-frequency matrix converter—as now reported.

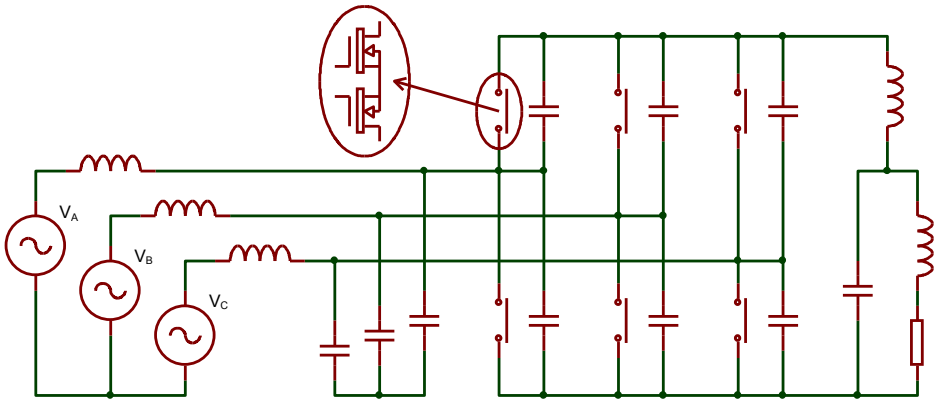

Fig. 1: Simplified high-frequency three-phase to single-phase matrix converter

The proposed three-phase to single-phase matrix converter (TPMC), shown in Fig. 1, uses a new pulse density modulation (PDM) scheme to synthesise three-phase input current system, whilst controlling power level by varying pulse width of the output waveform.

Proposed matrix converter and principle of operation

With the help of the more detailed circuit diagram, Fig. 2, the operation of the proposed three-phase to single-phase matrix converter can be examined. The bidirectional switches connected to the output terminal X and their associated commutating capacitors (also snubbers) belong to the load-commutated (LC) row, and bidirectional switches connected to the output terminal Y and their associated snubbers form the pulse-width-modulation (PWM) row.

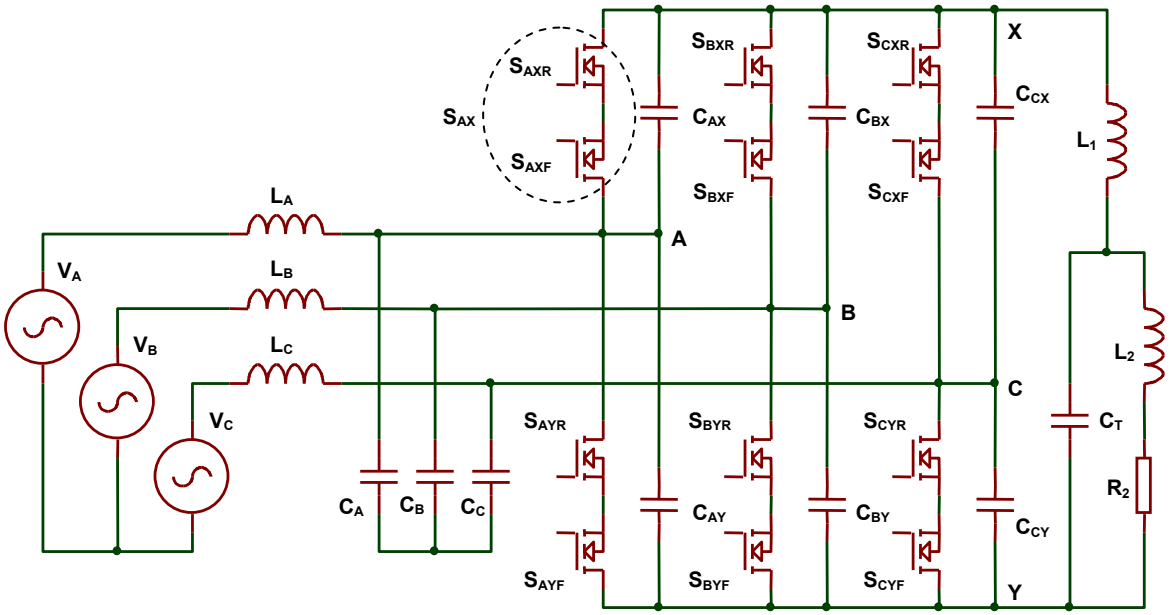

Fig. 2: Proposed high-frequency three-phase to single-phase matrix converter

During a single switching cycle, only two (active) input phase legs are used to supply high frequency current to the load circuit, and these input phase legs play the role of the two phase legs in the single-phase matrix converter proposed recently [14]. The same switching pattern and single-step voltage commutation strategy are applicable to the two active input phase legs of the TPMC, implying the power control method of PWM and soft switching conditions remain realisable.

The modulation task now centers on distributing the time that each output terminal spends connected to an input phase in such a way that a sinusoidal three-phase current is drawn from the power supply, at a high power factor.

Considering a balanced three-phase system, the sum of three input current must always be zero, implying either one input phase current will flow into two other input phases or two input phase currents will flow into the remaining input phase. By closely examining the ideal input current waveforms of a balanced three-phase system, Fig. 3, a current shaping algorithm utilising pulse density modulation can be proposed, as follows. In Fig. 3, the input voltage sectors have been numbered in such a way that they are convenient for the implementation of the switching algorithm.

Consider, for example sector I of the input current waveforms in Fig. 3. When phase C current is positive, the instantaneous current flowing into phase B equals to the total instantaneous current coming out of phases A and C. Similarly, the instantaneous current coming out of phase A equals to the total instantaneous current flowing into phases B and C, in the second half sector, when phase C current is negative. The same situation holds for all other input sectors, where one phase current is

most positive, the other phase current is most negative, and the remaining phase current passes zero at the middle of the input sector.

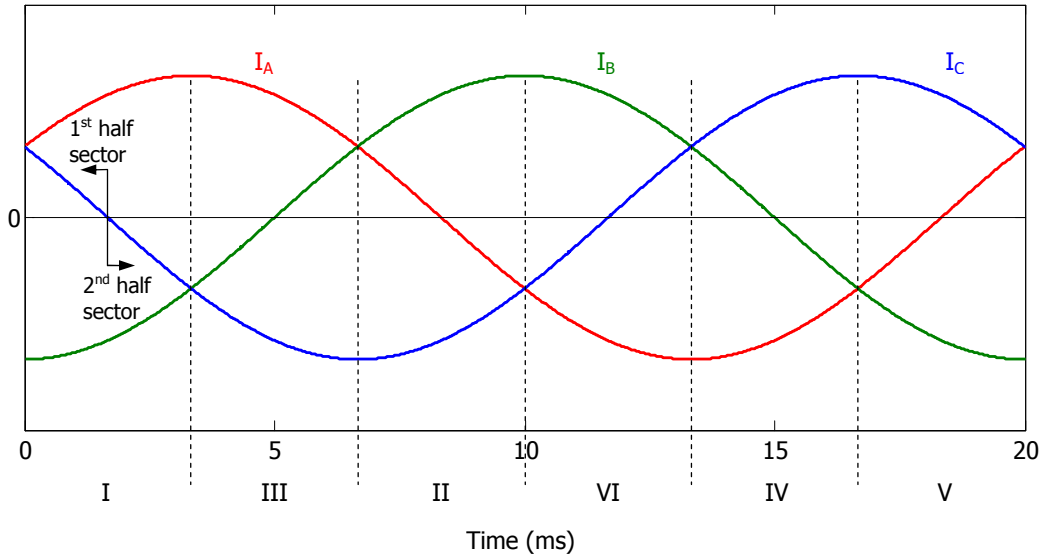

Fig. 3: Ideal input current waveforms of a balanced three-phase system

In the first half of input sector I, there are two positive voltage sources viz. V_{AB} and V_{CB}, available to supply power to the load, corresponding to two single-phase matrix converters formed by phases A and B, and phases C and B. For the positive half-cycle of output current, either S_{AX} or S_{CX} is used to connect either terminal A or C, to terminal X, whilst S_{BY} is used to connect terminal B to terminal Y. Similarly, S_{BX} is used to connect terminal B to terminal X, whilst either S_{AY} or S_{CY} is used to connect either terminal A or C, to terminal Y, in the negative half-cycle of output current. In the second half sector, similar situation exists with two available positive voltage sources are V_{AB} and V_{AC}. Table I summarises all valid switching states for the proposed input current shaping algorithm in all six input sectors (only absolute values are considered in current equations).

Using similar underlying principles for synthesising a localised average value of input currents as normally used in conventional matrix converters, a block of switching cycles can be distributed among input phases such that their time-average (or equivalently pulse density) values follow the required functions of a three-phase current system, preferably in phase with the input three-phase voltage system. From the analysis of one input sector in the previous paragraph, the combination of two pulse patterns for two input phases with smaller average absolute value must be the exact pulse pattern for the remaining input phase with the highest average absolute value, in order to maintain the current equation for every block of switching cycles (PDM block). Specifically, only PDM patterns for the most positive and the most negative input phases are allowed to be taken from a preset PDM pattern set, whilst the third PDM pattern for the remaining input phase has to be determined from the logical combination of the first two PDM patterns, in order to fulfill the requirement that $I_A + I_B + I_C = 0$ in a 3-wire system.

The PDM block length (number of switching cycles in a PDM block) should be large in order to have good magnitude resolution—however, this reduces the time resolution. Furthermore, a large number of PDM blocks (corresponding to a small PDM block length) is required to ensure an effective line frequency synchronisation algorithm. A trade-off is therefore normally made for the PDM block length, and a length of 16 (switching cycles) has been chosen for use with the proposed converter.

Table I: Available switching states of three-phase to single-phase matrix converter

Input sector		Current equation	Available sources	Positive I_{out}		Negative I_{out}	
				X	Y	X	Y
I	1st half	$I_B = I_A + I_C$	V_{AB}, V_{CB}	S_{AX}/S_{CX}	S_{BY}	S_{BX}	S_{AY}/S_{CY}
	2nd half	$I_A = I_B + I_C$	V_{AB}, V_{AC}	S_{AX}	S_{BY}/S_{CY}	S_{BX}/S_{CX}	S_{AY}
II	1st half	$I_C = I_A + I_B$	V_{AC}, V_{BC}	S_{AX}/S_{BX}	S_{CY}	S_{CX}	S_{AY}/S_{BY}
	2nd half	$I_B = I_A + I_C$	V_{BA}, V_{BC}	S_{BX}	S_{AY}/S_{CY}	S_{AX}/S_{CX}	S_{BY}
III	1st half	$I_A = I_B + I_C$	V_{AB}, V_{AC}	S_{AX}	S_{BY}/S_{CY}	S_{BX}/S_{CX}	S_{AY}
	2nd half	$I_C = I_A + I_B$	V_{AC}, V_{BC}	S_{AX}/S_{BX}	S_{CY}	S_{CX}	S_{AY}/S_{BY}
IV	1st half	$I_A = I_B + I_C$	V_{BA}, V_{CA}	S_{BX}/S_{CX}	S_{AY}	S_{AX}	S_{BY}/S_{CY}
	2nd half	$I_C = I_A + I_B$	V_{CA}, V_{CB}	S_{CX}	S_{AY}/S_{BY}	S_{AX}/S_{BX}	S_{CY}
V	1st half	$I_C = I_A + I_B$	V_{CA}, V_{CB}	S_{CX}	S_{AY}/S_{BY}	S_{AX}/S_{BX}	S_{CY}
	2nd half	$I_B = I_A + I_C$	V_{AB}, V_{CB}	S_{AX}/S_{CX}	S_{BY}	S_{BX}	S_{AY}/S_{CY}
VI	1st half	$I_B = I_A + I_C$	V_{BA}, V_{BC}	S_{BX}	S_{AY}/S_{CY}	S_{AX}/S_{CX}	S_{BY}
	2nd half	$I_A = I_B + I_C$	V_{BA}, V_{CA}	S_{BX}/S_{CX}	S_{AY}	S_{AX}	S_{BY}/S_{CY}

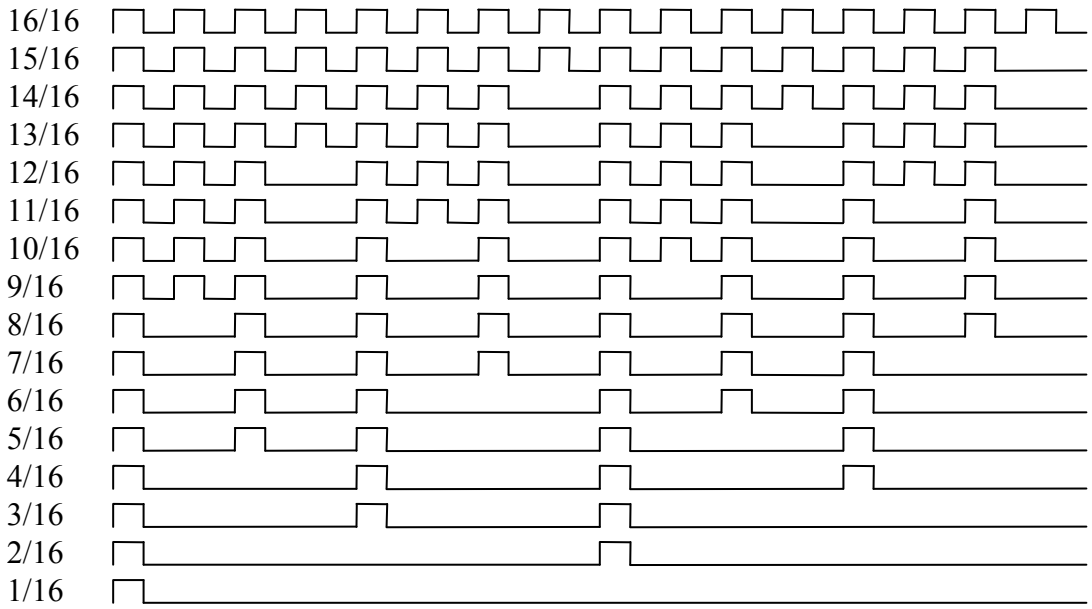

Fig. 4: Generic pulse density modulation patterns with a block length of 16 (switching cycles)

With the primary goal of reducing input current total harmonic distortion, the PDM patterns should be symmetric and have as many number of spatial sequences as possible, to lower the magnitude of subharmonics introduced [15]. More importantly, the PDM pattern set should be constructed such that any pattern will be a part of patterns with higher densities. One possible PDM pattern set is shown in Fig. 4.

In a balanced three-phase system, the phase currents are sinusoidal with constant power being transferred from the supply to the load. It is therefore proposed to use a variable pulse density modulation scheme such that a quasi-constant power condition is regularly maintained, creating opportunities to synthesise sinusoidal input currents.

Although the maximum line-to-line voltage contains an underlying 50 Hz, six-step rectification ripple, during any given PDM block (which is 92 μs in duration for an output frequency of 174 kHz), it is reasonable to assume that the available line-to-line voltage is essentially constant. Hence, during one PDM block, the output power can be considered to be proportional to the pulse density in the following analysis. Also, one input sector will be considered as long as 36 PDM blocks (174 kHz output frequency), and the mismatch in frequency between input and output will be considered later. Due to the symmetry of the waveform in one input sector, only one half sector needs to be analysed. Considering the first half of input sector I, which consists of 18 PDM blocks, the available line-to-line voltage can be expressed by,

$$v_{LL} = \sqrt{3}\hat{v}_i \cos(\omega_i t - \pi/6) \propto \cos(\omega_i t - \pi/6), \quad 0 \le \omega_i t \le \pi/6 \tag{1}$$

where $\hat{v}_i$ is the amplitude of the line-to-neutral input voltage. As the load power is quadratically proportional to the input voltage for a given pulse density, the output power should remain 'constant' if the output pulse density $\delta_{PDM}(t)$ is modulated by,

$$\delta_{PDM}(t) = \frac{\cos^2(\pi/6)}{\cos^2(\omega_i t - \pi/6)}, \quad 0 \le \omega_i t \le \pi/6 \tag{2}$$

In Fig. 5, the output pulse density δ_{PDM} for this variable pulse density modulation (VPDM) algorithm is presented as a function of PDM block number, along with the quantised output pulse density.

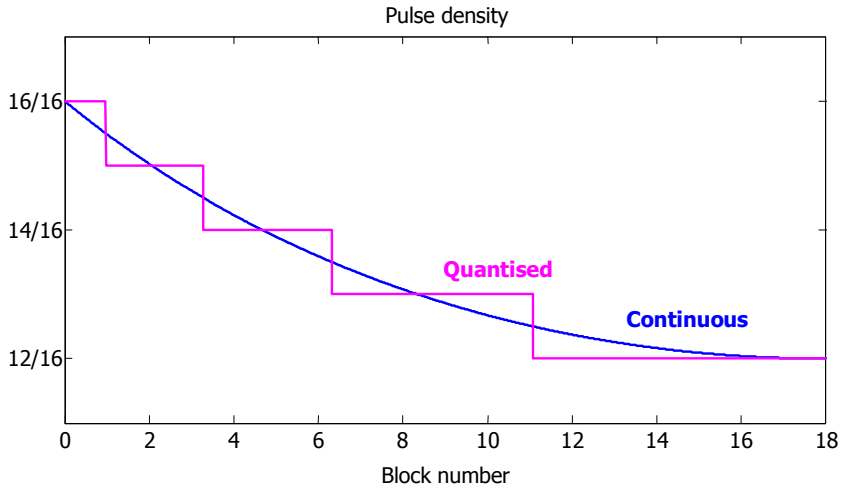

Fig. 5: Continuous and quantised output pulse densities

By utilising the output pulse density δ_{PDM} for the input phase with the highest pulse density, implementing linear pulse density for the input phase with the lowest time-average value and modifying PDM values for the third input phase according to the current equation, PDM values for all input phases in any input sector can be calculated. Starting with quantised pulse density (Fig. 5) and taking into account the monotonic nature of input currents in any input sector, the VPDM algorithm for input sector I can be developed, as shown in Fig. 6. PDM values for other input sector can easily be obtained, making use the symmetry of any two adjacent input sectors. For this particular VPDM scheme, the generic PDM patterns can be customised to have a better symmetry, because the realisation constraints have reduced to just a few special cases for some specific PDM patterns. The PDM patterns used for this VPDM algorithm are shown in Fig. 7.

From the description of operating principle of the TPMC, it is notable that the converter does not require any on-line calculations for synthesising three-phase input currents.

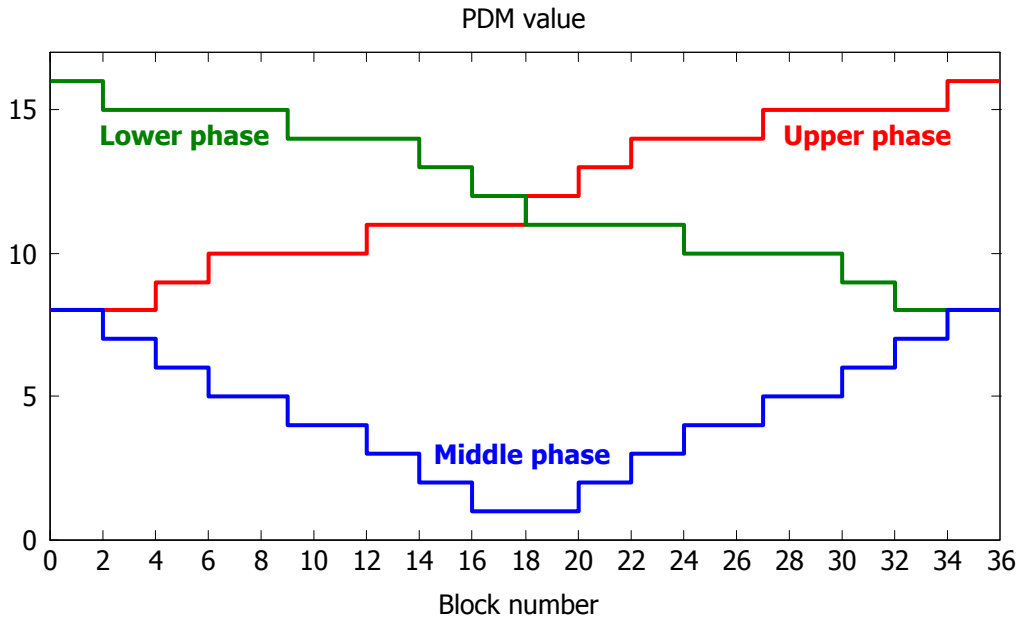

Fig. 6: PDM values for input sector I

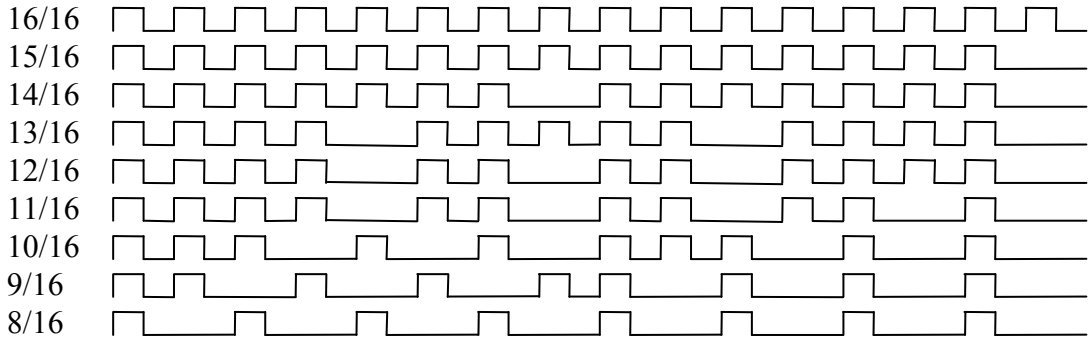

Fig. 7: Alternative PDM pattern set

Implementation considerations

In this section, the considerations of line frequency synchronisation and output current circulation methods are presented.

Since the line frequency is allowed to vary within a standardized tolerance band, it is unlikely that the line period is an integer multiple of the PDM block period (sixteen switching cycles). This poses a fundamental problem, line frequency synchronisation, for realising a practical solution. A basic synchronising algorithm is therefore proposed.

When approaching the end of an input sector, the detection of new input sector is activated. The last PDM block will be repeated if reached and the detection of new input sector is performed continuously. Once a new input sector is detected, the PDM values for that input sector will be used at the end of the current PDM block. The input current waveform is therefore synchronised with the input voltage waveform six times during each line period.

Using the proposed VPDM strategy, there are switching cycles in which no power will be transferred from the supply to the load, and the load current needs to circulate through an intentionally established path to prevent overvoltage spikes. To avoid short-circuited input phases, only bidirectional switches belonging to a particular input phase are allowed to be turned-on simultaneously for output current

free-wheeling. Considering an input phase leg with its associated switches, Fig. 8, two possible current circulation strategies are: turn-on all the devices in both bidirectional switches, and turn on only forward devices for forward current, and only reverse devices for reverse current. Here, the forward load current flows through the load circuit from terminal X to terminal Y, and the reverse load current goes from terminal Y to terminal X through the load.

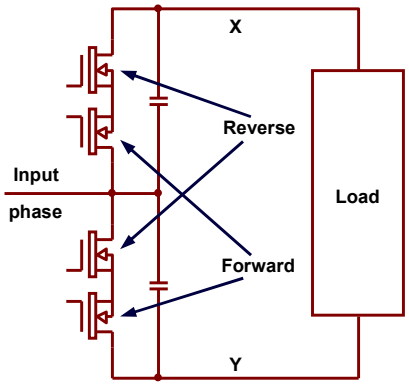

Fig. 8: Bidirectional switches of one input phase leg for output current circulation

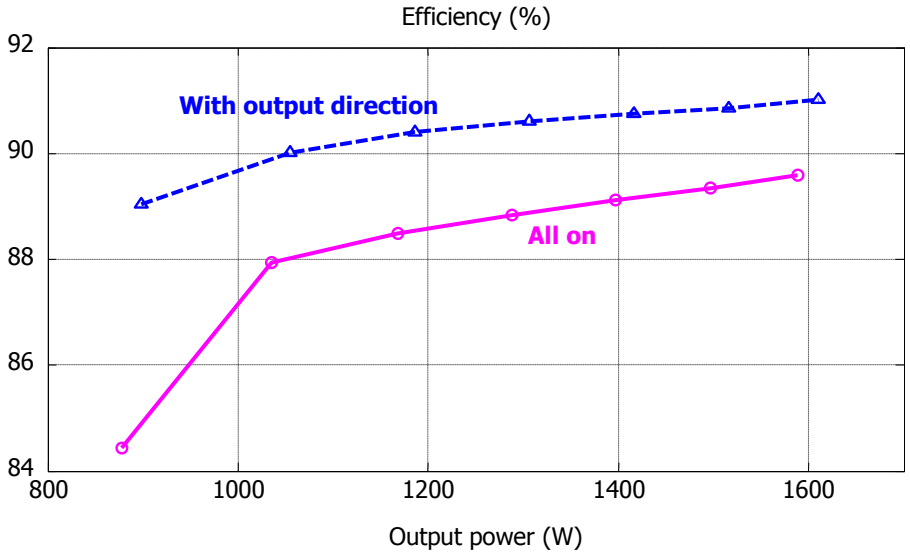

Fig. 9: Effect of output current circulation methods on efficiency

When starting an output circulating switching cycle, both the bidirectional switches in the least active phase leg will be turned on to create a current path and short-circuit the load circuit, leading to an energy discharge from the charged snubbers in all phase legs. If all the switching devices in the least active phase leg were turned-on for output circulation, an AC current path exists, allowing high frequency oscillations to occur in different current loops formed by phase legs' snubbers and stray inductances. This can lead to excessive conduction losses on the conducting switching devices. The output circulation method making use of the output current direction can help ameliorate such conduction losses, as verified by simulation results, Fig. 9. In the previous development of the VPDM strategy, the second output circulation method (with output current direction) was used exclusively. This method of output circulation is therefore proposed for VPDM strategies.

Performance evaluation

Referring to Fig. 2, the following component values have been used in simulations: $L_A = L_B = L_C = 1$ mH, $C_A = C_B = C_C = 1.5$ µF, $C_{AX} = C_{BX} = C_{CX} = 4.7$ nF, $C_{AY} = C_{BY} = C_{CY} = 10$ nF, $L_1 = 18.824$ µH, C_T

= 257.75 nF, L_2 = 4.424 mH, R_2 = 1.1405 Ω at output frequency of 174 kHz. The power device is IXYS-IXFK64N50P.

Imput power quality

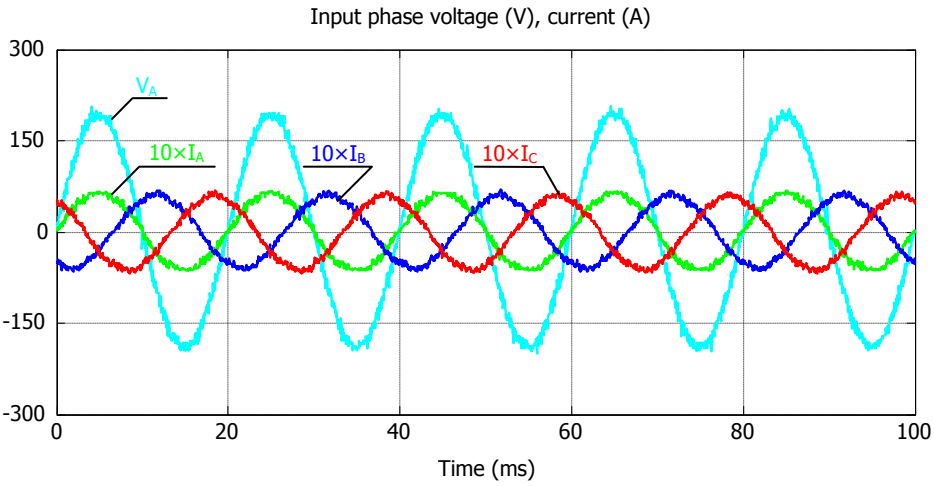

Fig. 10: Experimental input waveforms of TPMC at PWM pulse width = 1.5 µs (maximum value)

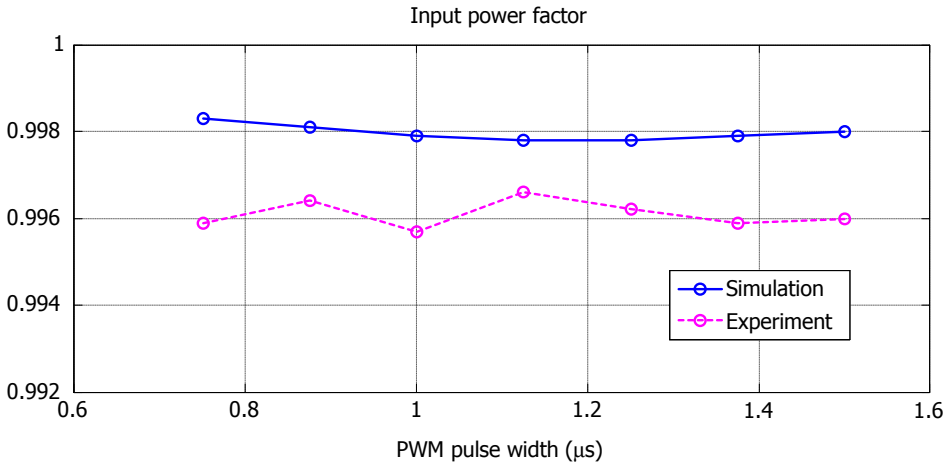

Fig. 11: Input power factor of TPMC

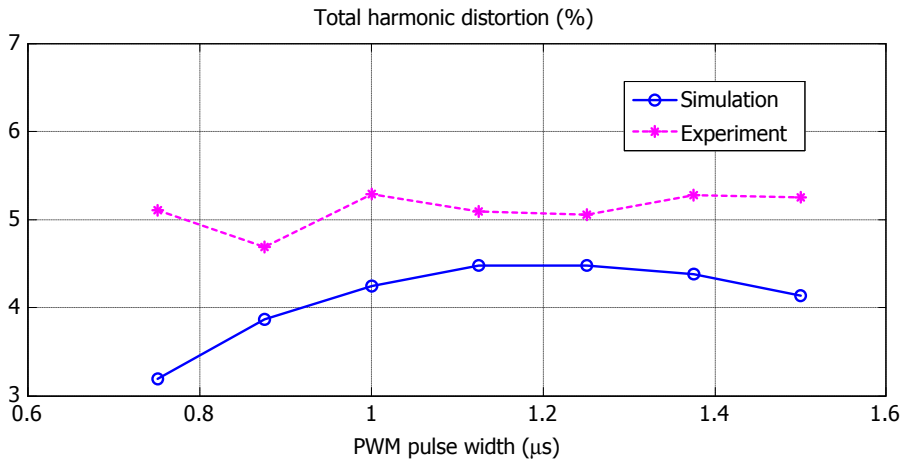

Fig. 12: Input current total harmonic distortion of TPMC

Typical experimental input waveforms can be seen in Fig. 10, for a 2 kW input power, at an output frequency of 174 kHz. It is evident that the input current is of very high quality, with unity

displacement power factor, and very low harmonic content. A power supply unit has been used to provide an exact 50 Hz input to the TPMC, showing the effectiveness of the line frequency synchronisation method and demonstrating that the converter can operate under out of line frequency synchronisation conditions.

Among input quantities, power factor and total harmonic distortion (THD) are normally used to evaluate the input power quality. Over the full power control range, input power factor is very high and essentially constant, with very good agreement between simulation and experimental results, as can be seen in Fig. 11.

Also, the input current THD is very low (≤ 5.3%) and practically constant over the full power range, as shown in Fig. 12. It is notable that this performance has been achieved without the need for on-line calculations on a powerful 32-bit DSP controller, as often required in a related systems [16].

Power controllability

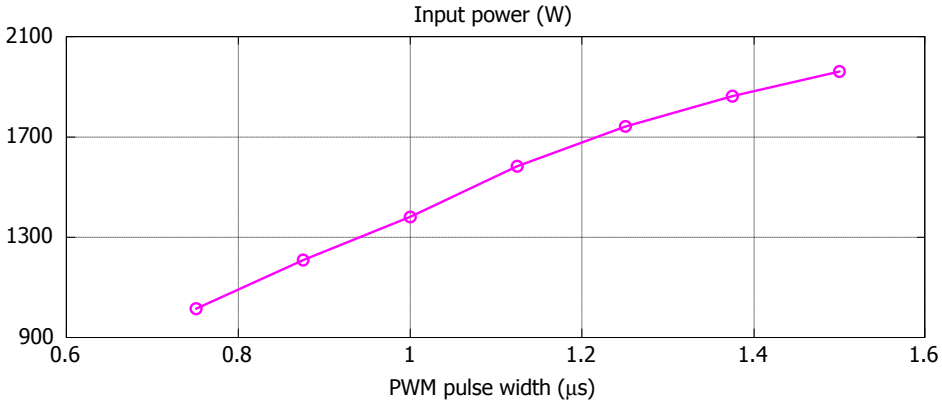

Fig. 13: Experimental power control capability of TPMC

Controllability complexity of the system can be attractive to control system designers, and is now considered. It can be seen, from Fig. 13, that the input power is almost proportional to PWM duty, making the system's model computationally effective in model-based control techniques, such as predictive or observer-based control.

Efficiency

The TPMC also features high efficiency values (≥ 91.3%) over the full power range, as shown in Fig. 14, with efficiency of about 92.6% at full power.

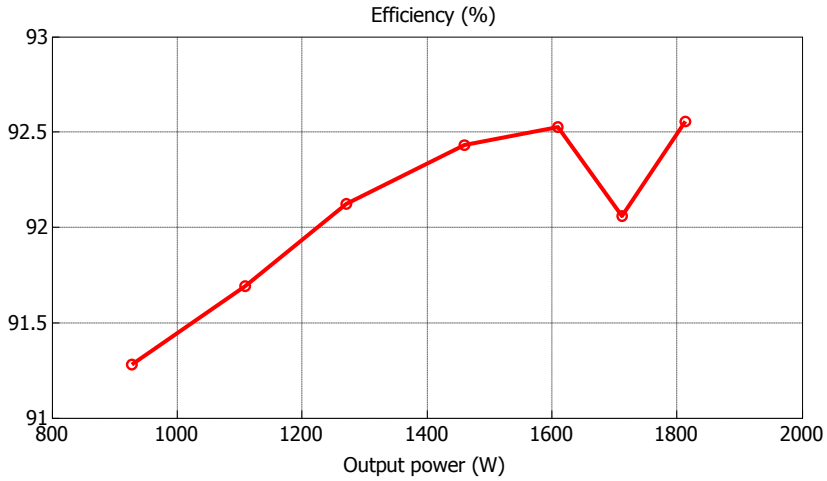

Fig. 14: Experimental efficiency of TPMC

Conclusion

The paper has described a newly developed, high performance three-phase to single-phase matrix converter, with very good input quality, for high frequency induction heating applications. For synthesising three-phase input current system, a variable output pulse density modulation scheme has been proposed, notably without any on-line calculations being required. This aids in reducing development time and cost, and initial and operational cost, leading to more competitive products and faster time to market. Unity power factor and very low input current THD (≤ 5.3%) have been achieved over the full power range, not only at rated power level, as is normally reported in published literature, and shows the effectiveness of the proposed VPDM strategy. Realisation considerations, viz. line frequency synchronisation and output current circulation, are also described, making the implementation of the converter more commercially realistic. The converter exhibits a high efficiency (≥ 91.3% over the full power range) owing to soft switching conditions being maintained over a wide control range. Excellent performance of the proposed converter has been confirmed by good correlations between simulation and experimental results.

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