This paper reports a 15 GHz quadrature voltage controlled oscillator (QVCO) designed in a 130 nm CMOS technology. The phase noise performance of the QVCO and of a phase locked loop (PLL) where the QVCO was inserted were compared with the literature and with telecom standards and commercial products for broadcast satellite applications.

Keywords: DVBS, CMOS, QVCO, PLL, design, phase noise

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designed wider than the n-channel ones: the gate width of the p-channel transistors was fixed equal to 56 μm and the gate width of the n-channel transistors was fixed equal to 10 μm. For sake of good locking capability and of flicker noise minimization, the coupling n-channel transistors width was fixed equal to 16 μm.

The tank was designed using a single octagonal coil differential inductor resonating with the parasitic capacitances. A compact model as that described in [8] was extracted from electromagnetic simulations carried out both with the 2D 1/2 electromagnetic simulator Momentum by Agilent Technologies and with the 3D electromagnetic simulator by CST. The inductor exhibits an inductance of about 290 pH and a maximum quality factor in the range of 27. It is worth pointing out that these values of inductance and quality factor are very close to those recently claimed in [9] for a 65 nm CMOS LC VCO working in the Ku-band.

To obtain tuning capability, two 20-finger accumulation MOS varactors with a minimum gate length of 350 nm were introduced [10].

III. EXPERIMENTAL RESULTS

Figure 2 shows the microphotograph of the fabricated prototype. In the middle of the chip are visible the two inductors of the VCO core. In the microphotograph are also visible the two buffers to drive the load of the instruments. Under an experimental point of view, the use of the buffers is mandatory, in order to perform reliable measurements. Without buffers, the losses of the external load connected to the circuit during the characterization can degrade the VCO performance or, on the other hand, high-Q lines connected to the pads via the coplanar probes and coaxial cables can improve the VCO performance.

The GSGSG pads for the differential in-phase (I+, I−) and in quadrature (Q+, Q−) RF output signals are visible on the top and on the bottom of the chip, respectively. At the left side the pad GSG pad for the tuning voltage (Vtune) is visible. Eventually, three pads for the supply (VDD) are distributed along the pad ring. The chip size is 900 × 1100 μm², pads enclosed.

The differential output signals were made available to the single-ended input of the Agilent E4408B spectrum analyzer using a wideband Anaren 30070 hybrid.

Figure 3 reports the output frequency variation with the tuning voltage. A difference less than 1.3% between simulations and measurements was obtained on the whole tuning range. The carrier frequency (f0) goes from 14.6 to 15.8 GHz for Vtune ranging between 0 and 1.2 V corresponding to a tuning range of 7.4%. The QVCO delivers about −20 dBm on a 50 Ω load and it sinks 9.4 mA from a 1.2 V supply.

Phase noise measurements were carried out for Vtune ranging between 0 V and 0.6 V using an Agilent E5500 phase noise meter. Figure 4 shows the measured phase noise for f0 = 14.6 GHz. The VQCO exhibits a phase noise of −106 dBc/Hz at the offset frequency (Δf) of 1 MHz. This value is very close to the −107 dBc/Hz (at 1 MHz from a 10.7 GHz carrier) recently claimed for the VCO used in the PLL of a monolithic Ku-band receiver [2]. For other values of applied Vtune the phase noise did not change in agreement with simulations.
IV. DISCUSSION

Since the VCO has to be employed in a PLL, the measured phase noise depicted in Fig. 4 has been therefore inserted in a PLL simulation carried out with Matlab. The noise contributions of the pre-scaler, of the phase and frequency detector, and of the reference have been set to typical values. The loop filter was designed so that to obtain a PLL bandwidth of 400 kHz and a phase margin of 60°. Figure 5 shows the simulated phase noise (black curve). The white lines are the contributions of the single building blocks.

The PLL phase noise is very close to the DVBS phase noise specifications (open circles) at the offset frequencies of 100 kHz and 1 MHz [11]. The simulated phase noise is a higher than standard limit in the offset frequency range 100 kHz–1 MHz. The simulated phase noise is also comparable with the phase noise exhibited by the TFF1004HN commercial product [4] and it is better for offset frequencies lower than 100 kHz. As further discussion about Fig. 5, it is worth pointing out that the phase noise and, in particular, the tuning range specifications have to be addressed by introducing a switched capacitor bank in the VCO topology during the design of the final PLL.

Eventually, the performance of the fabricated QVCO has been compared with other 130 nm CMOS VCOs reported in the literature through the following figure-of-merit (FOM) that allows for a comparison normalized with respect to the power and the frequency [12]:

\[
FOM = L(\Delta f) - 20 \log \left( \frac{f_0}{\Delta f} \right) + 10 \log \left( \frac{P_{DC}}{1 \text{ mW}} \right)
\]  

where \(L(\Delta f)\) is the phase noise at \(\Delta f\), and \(P_{DC}\) is the dissipated DC power (Table 1).

Figure 6 plots the FOM versus the oscillation frequency. The QVCO reported in the present work is well aligned with the other VCO’s trend extracted from the literature.

A comparison with Ku-band cross-coupled VCO designed in 90 nm, see for instance [20], or 65 nm, see for instance [21], CMOS technologies does not point out a remarkable improvement in the phase noise even if these technologies are more expensive than the 130 nm CMOS adopted in the present work. The adoption of a 90 nm/65 nm CMOS technology may help with reducing the dissipated power and therefore with improving the FOM but not the phase noise itself.

V. CONCLUSIONS

A 130 nm CMOS QVCO exhibiting a central frequency of 15 GHz has been demonstrated. The phase-noise-related FOM is well aligned with other 130 nm CMOS VCOs reported in the literature. In particular, the comparison with other CMOS VCOs claimed in the literature for Ku-band satellite receiver, with the DVB-S standard, and with commercial products implemented in SiGe BiCMOS technologies suggests that the 130 nm CMOS technology can be evaluated with interest for the design of a DVB-S satellite receiver front-end.

It is authors opinion that the main contribution of the present paper is not in the circuit topology in itself, that was already used in the past for a plant of applications, but rather in having provided demonstration that a bulk standard (e.g. not SOI) 130 nm CMOS technology can be employed to
design a PLL for the realization of silicon monolithic DVBS satellite receivers, that nowadays were demonstrated only using bipolar or SiGe technologies.

In particular, the fact that the demonstrated VCO is an I/Q VCO allows for the conclusion that a DVBS receiver could be fabricated with a direct-conversion architecture implemented in a bulk 130 nm CMOS technology, which would be a product completely new with respect to a traditional superheterodyne one (e.g. a SiGe BiCMOS LNB cascaded with the low-voltage CMOS IF tuner).

Eventually, it has to be pointed out that in the final design of the PLL a VQCO topology exhibiting a switched capacitor bank will help with addressing the tuning range specifications.

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