

RPC front-end electronics for the ATLAS LVL1 trigger detector

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Abstract

A front-end circuit for RPC detectors realized with an eight-channel full custom chip in GaAs technology is described. This chip exhibits a 150 μV minimum threshold, 3 dB noise figure, 160 MHz bandwidth and 50 mW/channel power consumption. © 1998 Published by Elsevier Science B.V. All rights reserved.

Front-end circuits for particle detectors are usually projected assuming that the pick-up system can be described as a capacitor. This approximation is correct if the charge collection time is large with respect to the propagation time in the pick-up strips. In this case, a charge amplifier is needed. An RPC operating in avalanche mode produces typically a single signal of 5 ns FWHM and 1.5 ns time jitter [1]; in the muon spectrometer of an experiment at the LHC the pick-up propagation time can be as long as 10–15 ns. In this case, the pick-up strips must be described not as point-like capacitors but as signal transmission lines [2,3]. Consequently, the signal source is a resistor equivalent to the line impedance and the noise is dominated by this resistor, so that a voltage amplifier is needed.

The good time performance of RPC detectors, crucial for bunch-crossing identification, requires

a large bandwidth because the large amplitude fluctuations of the detector signal impose a rise time of the order of the RPC time jitter. Here we describe a front-end circuit based on a three-stage voltage amplifier (Fig. 1) connected to a comparator. It is implemented in a full custom VLSI chip in GaAs technology. The amplifier frequency response is optimized for the typical time structure of the avalanche signal according to the following conditions:

- same rise time for the amplifier and input signals;
- minimum return-to-zero time for the output signal.

The resulting frequency response has a maximum at 100 MHz and a 3 dB bandwidth of 160 MHz. The amplifier output is bipolar giving zero integrated charge thus avoiding a possible dependence of the steady output voltage on the counting rate. The comparator has a variable threshold which can be set at a minimum value of 50 mV giving adequate immunity with respect to the noise. The

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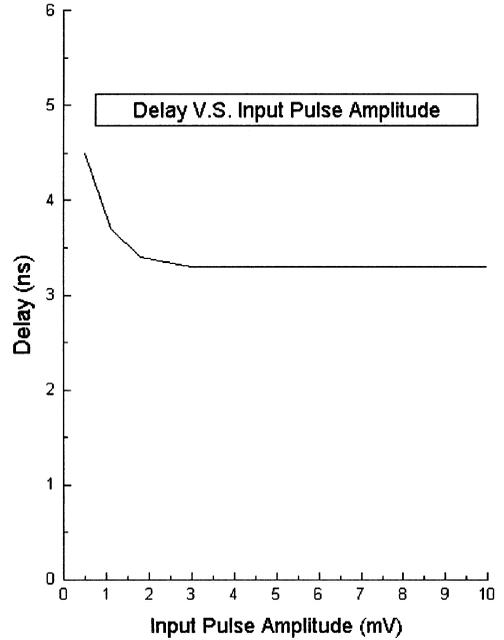
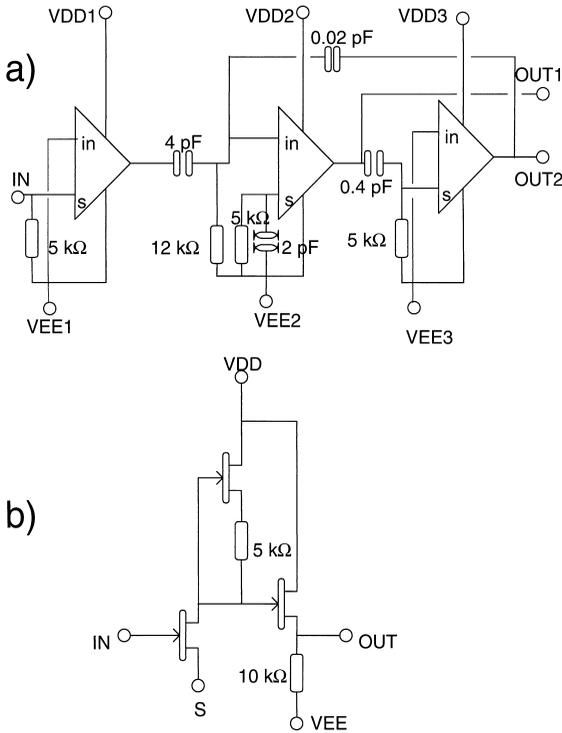


Fig. 2. Output signal delay versus the input signal amplitude.

Fig. 1. Block diagram of the three-stage amplifier: (a) interconnection of the three stages; (b) sketch of a single stage.

ECL output is capable of driving a few metre long 100Ω flat cable connecting the front end to the local trigger logic. The minimum comparator threshold combined with the amplifier gain fixes the minimum detectable signal amplitude at 150 μV. A two-channel full custom prototype chip of the front-end circuit has been already realized in GaAs technology. This chip, which is a preliminary step before the eight-channel final version, has been already tested on board and mounted on the detector for the H8 test beam. The output signal delay versus the input signal amplitude is shown in Fig. 2. The equivalent discrimination threshold versus the input pulse width is shown in Fig. 3. In Fig. 4 the efficiency of the RPC detectors versus the applied HV for fixed threshold (0.5 mV) is shown.

The measured power consumption of the prototype chip is 10 mW for the amplifier and 40 mW for the comparator.

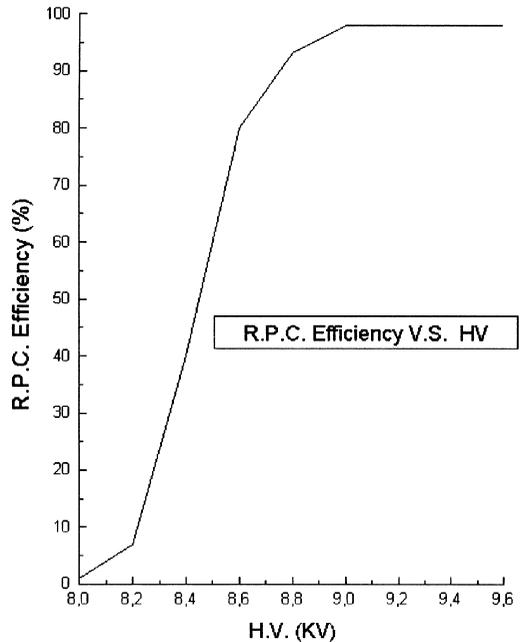


Fig. 3. Equivalent threshold versus the input pulse width.

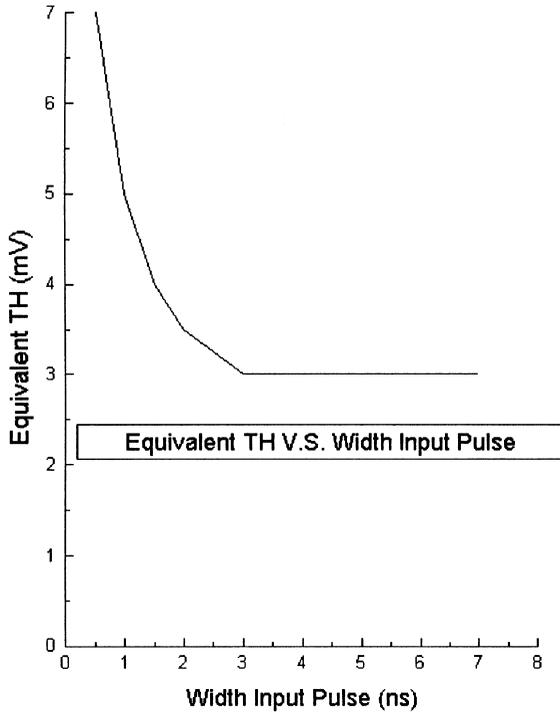


Fig. 4. Chamber efficiency as a function of the applied voltage.

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