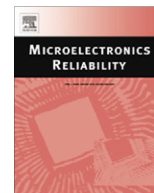
Microelectronics Reliability xxx (2011) xxx–xxx

Contents lists available at SciVerse ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel



Temperature dependence of neutron-induced soft errors in SRAMs

M. Bagatin [a,*], S. Gerardin [a], A. Paccagnella [a], C. Andreani [b], G. Gorini [c], C.D. Frost [d]

[a] Dipartimento di Ingegneria dell'Informazione, Università di Padova, Padova, Italy
[b] Università di Roma–Tor Vergata, Roma, Italy
[c] Università di Milano–Bicocca, Milano, Italy
[d] Rutherford Appleton Laboratories, Didcot, UK

ARTICLE INFO

Article history:
Received 8 March 2011
Received in revised form 14 July 2011
Accepted 19 August 2011
Available online xxxx

ABSTRACT

We irradiated commercial SRAMs with wide-spectrum neutrons at different temperatures. We observed that, depending on the vendor, the soft error rate either increases or slightly decreases with temperature, even in devices belonging to the same technology node. SPICE simulations were used to investigate the temperature dependence of the cell feedback time and restoring current. The shape and magnitude of the particle-induced transient current is discussed as a function of temperature. The variability in the response is attributed to the balance of contrasting factors, such as cell speed reduction and increased diffusion with increasing temperature.

© 2011 Elsevier Ltd. All rights reserved.

1. Introduction

Soft errors are a serious concern not only in space but also at sea level, due to neutrons originating from the interactions of cosmic rays with the atmosphere, and alpha particles, coming from radioactive contaminants in the chip package and solder materials [1].

A large amount of work has been carried out in the field of soft errors (also known as Single Event Upsets, SEU). Experimental, simulation, and modeling efforts have led to a deep understanding of these phenomena, especially in SRAM cells, which, nowadays, are the most radiation-sensitive type of solid-state storage [1]. Funneling phenomena have been discovered and modeled [2]. The role of the struck junction load on the induced transient has been elucidated [3]. Neutron nuclear reactions leading to charged byproducts have been analyzed in the context of terrestrial soft error rate (SER) [4]. Yet, despite the huge amount of work, some areas have received relatively little attention from the research community. It is well known that electronic chips must operate at temperatures significantly higher than room temperature, especially for high-performance, space, or automotive applications. Contrary to Single Event Latchup (SEL) tests that are performed at the highest operating temperature [5], SEU measurements are usually carried out at room temperature [6], and little is known about the SEU temperature dependence.

Only few works in the literature analyzed temperature effects on SER [7–9]. Some conclude that temperature plays a marginal role in determining the critical charge in SRAMs and, in general, the SER [7]. Sexton et al. observed an increased SEU sensitivity at high temperature in hardened memories and attributed this behavior to variations in the conductivity of the feedback and load resistors [8]. Truyen et al. performed TCAD simulations of heavy-ion strikes in 180-nm 6-T cells as a function of temperature [9]. Experimental work has been performed on pn diodes with heavy-ion microbeam, showing that the shape of the particle-induced current pulse changes with temperature [10] due to carrier mobility and lifetime variations. Laird et al. analyzed the temperature dependence of transients in inverters through laser testing [11].

To the best of our knowledge, few experimental SER data as a function of temperature are available in the literature for commercial memories in the terrestrial radiation environment. This work aims at providing more experimental data and analyzing the impact of high temperature on the SER of commercial SRAMs. We performed neutron irradiations and then we used SPICE simulations and analytical modeling to assess the critical charge and collection efficiency as a function of temperature.

2. Studied devices and experimental procedure

Throughout this work we used commercially-available SRAMs manufactured by different vendors (Table 1). We evaluated the likely CMOS technology node of our samples from the die size. Devices with the same capacity and die area have been associated to the same CMOS technology node.

The neutron irradiation was performed at the ISIS facility of the Rutherford Appleton Laboratory, Didcot, using the VESUVIO and ROTAX instruments. ISIS is a spallation neutron source, which uses 800-MeV protons to produce neutrons. The VESUVIO beam matches the terrestrial neutron flux with an acceleration factor between 10^7 and 10^8, containing both high-energy and thermal neutrons. The VESUVIO beam can be correlated with the LANSCE

* Corresponding author.
E-mail address: marta.bagatin@dei.unipd.it (M. Bagatin).

0026-2714/$ - see front matter © 2011 Elsevier Ltd. All rights reserved.
doi:10.1016/j.microrel.2011.08.011

Please cite this article in press as: Bagatin M et al. Temperature dependence of neutron-induced soft errors in SRAMs. Microelectron Reliab (2011), doi:10.1016/j.microrel.2011.08.011

ARTICLE IN PRESS

Table 1
Irradiated SRAM chips.

Device	Vendor	Size (Mbit)	Supply voltage (V)	Temp. range (°C)	CMOS node[a] (nm)
A	STM	4	3	0–70	180
B	Renesas	4	3	−40 to 85	180
C	ISSI	4	3	0–70	130
D	Cypress	4	3	−40 to 85	90
E	BSI	4	2.4–5.5	0–70	250

[a] CMOS technology node has been estimated by the die size. Devices with the same die area have been associated to the same CMOS technology node.

facility flux (the *de facto* standard for SER measurements [12]) using the LANSCE-equivalent flux [13], which accounts for the effectiveness of a beam in producing single event effects with respect to LANSCE. The ROTAX beam features only the thermal and epi-thermal neutrons.

We used a flux of $\sim 5 \times 10^5$ n/cm^2/s. The irradiation procedure was the standard one for SRAM SER testing: the memory under test is written with a checkerboard pattern and it is periodically read during exposure to detect bit errors at different operating voltages and temperatures. Data and address of the memory locations where errors are detected are logged for analysis. Heating elements placed around the devices were used to raise and constantly monitor the chip temperature during the exposure. The drawn current was measured under exposure to detect possible SEL. Thousands of errors were collected for each condition, to minimize statistical errors. Finally, SPICE simulations have been performed to evaluate both the behavior of a single transistor and that of an entire SRAM cell at different temperatures, using freely available models [14].

3. Results

Some of the parts (Devices D and E) exhibited frequent SEL with wide-spectrum neutrons even at room temperature (RT) and at the lowest possible supply voltage, and were therefore discarded from the analysis. We remark that SEL can lead to more severe consequences than soft errors, possibly to the destruction of the component, and commercially available parts may still suffer from this problem in relation to neutrons. One of the tested memories (Device C) was sensitive to thermal neutrons, due to the likely presence of BPSG inside the chip, and was separately studied to analyze the temperature dependence of the errors induced by thermal neutrons.

No dependence of SER on the supply voltage was observed for Devices A and B with high-energy neutrons, whereas C exhibited increased sensitivity at lower supply voltage with thermal neutrons (Fig. 1). We do not have detailed architectural information on these samples, but, given the results, we can speculate that Devices A and B are equipped with internal voltage regulators that maintain the supply voltage of the cells always at the same level, irrespective of the external bias; on the contrary, in Device C the cell voltage varies with the external supply voltage.

Let us now analyze the temperature dependence of SER. Fig. 2 displays the normalized SER as a function of temperature for Devices A and B. Thousands of events were collected for each experimental point in order to achieve good statistical accuracy and observe even small variations (>2%). Besides, irradiation runs at different temperatures were carried out in different orders to detect possible temperature hysteresis effects, which were not observed. The two memories feature a different behavior. In Device A, the cross section slightly decreases (<7%) in the temperature range 25–85 °C, whereas in Device B, it increases by 15% in the same range. It is worth to remark that Devices A and B are manufactured in the same technology node by different foundries.

Fig. 3 displays the normalized error rate at 20 °C and 60 °C for Device C irradiated with thermal neutrons at two different supply voltages. The temperature dependence is greatly enhanced at higher supply voltage (even though the overall error rate is lower at high V_{dd}, Fig. 1). At 2.5 V the increase in sensitivity is about 6%, while at 3 V the error rate at high temperature is more than 30% larger than that at RT for the same voltage.

4. Discussion

As just seen, different devices exhibit different SER trends versus temperature. According to the information we gathered from the datasheets, all the SRAMs feature 6-T cells, so the observed changes are not related to increasing resistance of the pull-up resistors as in Ref. [8].

A full cell 3D or mixed-mode simulations would be needed to accurately reproduce the temperature dependence. This would require knowledge of the memory cell structure and doping profiles, which is obviously not available for commercial memories. The purpose of this discussion is therefore to pinpoint the main parameters governing the SER temperature dependence. To this end we will use a simplified approach that combines SPICE simulations and analytical modeling. The conclusions we will draw are mostly qualitative, but, nevertheless, can provide good insight.

We may relate the SER temperature dependence on either differences in the MOSFET characteristics, leading to a change in the circuit response, or to alterations in the particle-induced pulses. Despite the difficulties in defining the concept of critical charge

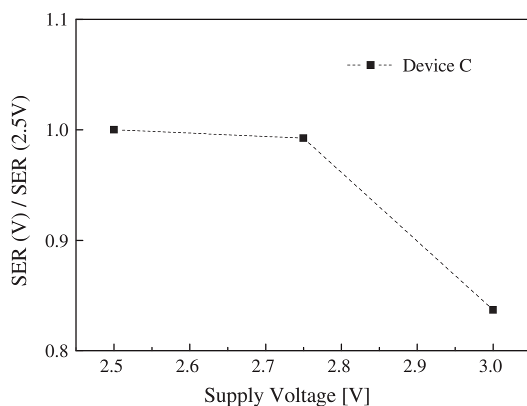


Fig. 1. Experimental error rate as a function of supply voltage normalized to V_{dd} = 2.5 V for Device C irradiated with thermal neutrons at room temperature.

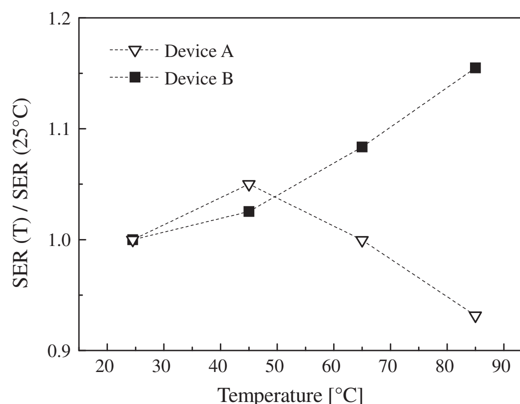


Fig. 2. Experimental error rate as a function of temperature during high-energy neutrons exposure (Devices A and B).

Please cite this article in press as: Bagatin M et al. Temperature dependence of neutron-induced soft errors in SRAMs. Microelectron Reliab (2011), doi:10.1016/j.microrel.2011.08.011

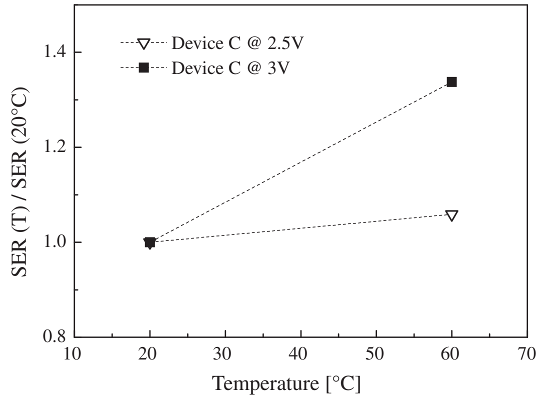


Fig. 3. Experimental error rate normalized to $T = 20$ °C as a function of temperature during thermal neutrons exposure (Device C).

[3], the SER of a memory (even in scaled devices [15]) can still be fitted by the well-known empirical expression [16], where we have made explicit the temperature (T) dependence:

$$SER(T) = \kappa A_{diff,n} \exp\left(-\frac{Q_{crit,e}(T)}{\eta(T)}\right) \quad (1)$$

κ is an overall (technology-dependent) scaling factor, $A_{diff,n}$ is the diffusion area, $Q_{crit,e}$ is the critical charge, and η is the charge collection efficiency. The last two parameters may vary with T, as indicated in (1). $Q_{crit,e}$ will be calculated through SPICE simulations by injecting a current pulse in the cell. The collection efficiency η represents a measure of the charge collected by the circuit node after an ion strike and will be discussed in Section 4.2. For simplicity, we will focus on strikes occurring in (or near) the drain of the off NMOSFET, which still accounts for most of the SEUs, even in scaled devices [17].

4.1. Circuit response

MOSFETs have a positive temperature coefficient, meaning that the drive current decreases as T increases. This reduction is mostly due to a lower mobility at high T, because of the increased phonon scattering. For instance, the hole mobility temperature dependence (as a function of doping) in bulk Silicon can be expressed by the following empirical formula [18]:

$$\mu_p = 88 \cdot T_n^{-0.57} + \frac{1.36 \times 10^8 \cdot T^{-2.33}}{1 + \frac{N}{1.26 \times 10^{17} \cdot T_n^{2.4}} \cdot 0.88 \cdot T_n^{-0.146}} \quad (2)$$

where T is the temperature (in K), T_n is the temperature divided by 300 K, and N is the doping concentration. A similar expression exists for the electrons mobility [22,18]. Other scattering mechanisms come into play (surface roughness, carrier–carrier scattering, quantum effects) to determine the mobility in the channel, which can be lumped together in the following simplified equation, used also by BSIM3 and BSIM4 models:

$$\mu = \mu(T_0) \cdot \left(\frac{T}{T_0}\right)^{\mu_{Te}} \quad (3)$$

where T_0 is a reference temperature and μ_{Te} a fitting parameter. The threshold voltage depends on T as well, although in a less pronounced way, causing the MOSFET temperature response to be dominated by mobility changes. Temperature also impacts the junction capacitance, although in a minor way.

Some of the most interesting experimental data we collected (Fig. 2) are onto the 0.18 μm CMOS node, so this feature size has been used in our simulations. Data on 90 nm will also be shown to illustrate scaling trends.

Fig. 4 shows the simulated I_{ds}–V_{gs} characteristics of a 180-nm PMOS transistor in the linear region ($V_{ds} = 25$ mV). The electrical characteristic at high V_g shows a decrease in I_{ds} at high T compared to RT. This means that the PMOS at higher temperature is less strong than at RT: this has a detrimental effect on the cell SER.

We can also simulate the behavior of an entire 6-transistor SRAM cell. Fig. 5 reports the cell speed at different temperatures, i.e. the T dependence of the minimum pulse width duration (t_{PW}) required at the word line to write the cell. t_{PW} monotonically increases with T, for both 90-nm and 180-nm cells: the cell is slower at high T.

If we consider the two effects we described so far, their contributions to the SER sensitivity go towards opposite directions. On one hand, the ability of the PMOS to restore the state of the struck cell is reduced at high T, due to the lower drive current, which has a detrimental effect on the cell radiation sensitivity. On the other hand, the cell speed is reduced at high T, which is beneficial for the SER, since pulses injected by ionizing particles propagate more slowly and the ion-induced spike is less likely to be latched. These effects can be accounted for in the following formula [24]:

$$Q_{crit} = C_n \cdot V_{dd} + t_{FLIP} \cdot I_{RESTORE} \quad (4)$$

where C_n is the total capacitance of the struck node, t_{FLIP} the flipping time, and $I_{RESTORE}$ the restore current. Also C_n depends on T, since, for instance, the size of the depletion regions varies, as we shall see later.

Fig. 6 displays the simulated Q_{crit} of a memory cell as a function of temperature and pulse duration. The current pulse injected into the sensitive node is modeled through an exponential multiplied with a power law [7]:

$$I_{pulse}(t, \tau_{pulse}, Q) = \frac{2}{\sqrt{\pi}} \cdot \frac{Q}{\tau_{pulse}} \cdot \sqrt{\frac{t}{\tau_{pulse}}} \cdot \exp\left(\frac{t}{\tau_{pulse}}\right) \quad (5)$$

where τ_{pulse} is the width of the current pulse and Q is the total amount of injected charge. τ_{pulse} has been varied to simulate the effect of current pulses with different durations, corresponding to strikes in different locations, at different angles, etc. [4]. As observed in Fig. 6, our simulations show a net decrease of the Q_{crit} for long pulses, meaning that at high T the detrimental reduction in the PMOS restore current overcomes the beneficial (from the SER standpoint) reduction in the cell speed. The effect is less pronounced for short pulses. From a circuit-only perspective (i.e., neglecting the temperature impact of on the pulse amplitude, shape, and duration), we expect that the SER due to particles going through the

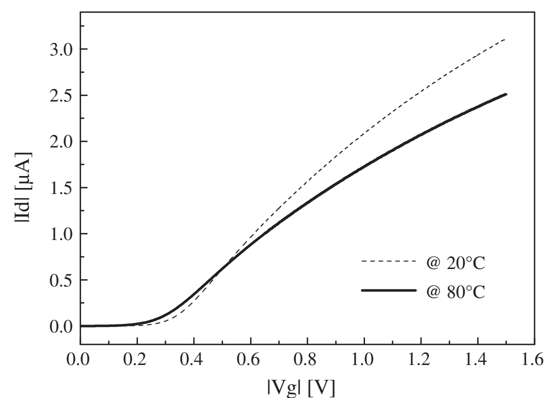


Fig. 4. Simulated I_{ds}–V_{gs} characteristic for a PMOSFET (180 nm) ($V_{ds} = 25$ mV), performed at 20 °C and at 80 °C.

Please cite this article in press as: Bagatin M et al. Temperature dependence of neutron-induced soft errors in SRAMs. Microelectron Reliab (2011), doi:10.1016/j.microrel.2011.08.011

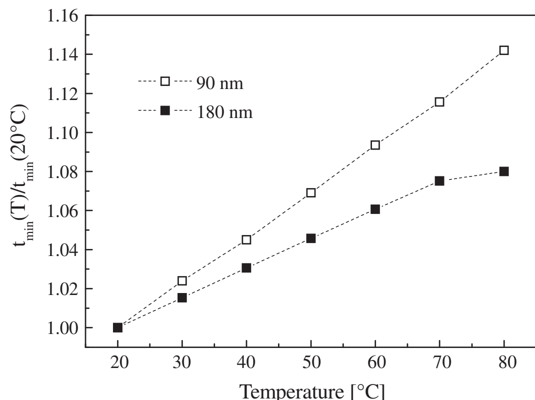


Fig. 5. Simulated minimum write pulse needed at the word line for a 6-T SRAM cell as a function of temperature.

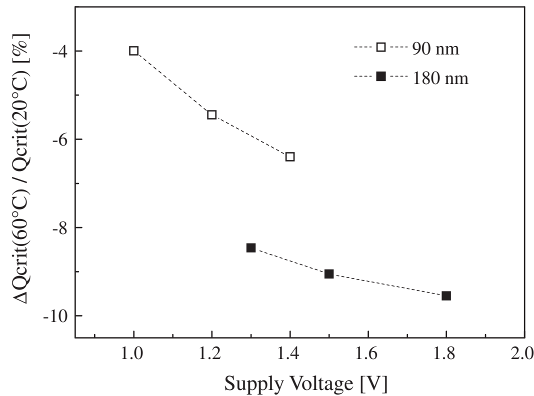


Fig. 7. Simulated percentage variation in the critical charge at 60 °C as a function of supply voltage normalized to ΔQ_{crit} at 20 °C, for a 6-T SRAM cell.

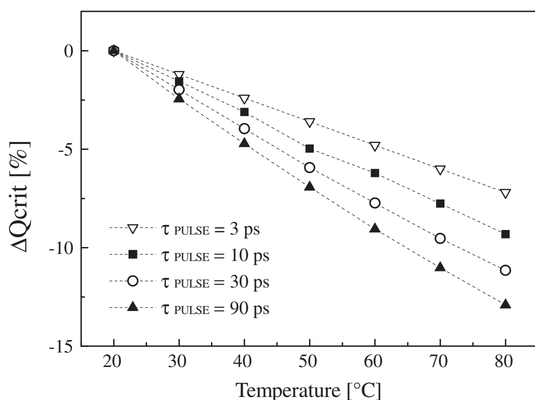


Fig. 6. Simulated percentage variation in the critical charge as a function of temperature, normalized to 20 °C for different pulse widths (180-nm SPICE models, V_{dd} = 1.5 V).

drain is less affected by T than that due to particles passing close to the drain.

Fig. 7 shows the simulated dependence of the critical charge at 60 °C on the supply voltage. The impact of T is enhanced at high voltage. This may explain our data (Fig. 3), where we observe an enhanced temperature dependence at high supply voltage.

Our results are not restricted to these models. Indeed, we performed the same simulations with parameter sets from other vendors and belonging to different technology nodes and found qualitatively the same dependences.

Besides MOSFET drive current, temperature also affects the resistivity of the interconnects, further reducing the cell speed (this is not considered in our simulations).

4.2. Radiation-induced current pulse

Temperature may affect the current pulse induced by the striking particle as well. Charge collection depends on several factors related to the impinging particle (LET, energy, angle, secondary particles), device structure (size, doping, etc.), and external circuit (node impedance). To add more complexity, several charge transport mechanisms are involved in determining an upset, from simple drift to ambipolar diffusion. It is almost impossible to analytically account for all the different terms that determine the charge collection in a struck cell, but we can capture the main parameters which show a dependence on temperature.

For strikes passing through the drain, charge is collected at a sensitive node in two stages: drift and diffusion [19]. Roche et al. [24] demonstrated that the peak of the drift current is expressed by the equation:

$$I_0 = \langle \mu E_{field} \rangle LET \tag{6}$$

Since mobility decreases with T and the electric field E_{field} weakly depends on temperature, the peak of the drift current decreases at high T. This has been both verified with 3-D simulation tools [9] and experimentally observed in diode structures and in inverters [10,11]. Also the LET varies with T, as the bandgap increases with it, but the variation is modest.

The size of the depletion region is weakly affected by temperature. Indeed x_d depends on the square root of the applied reverse bias plus the built-in potential V_i, the last term determining the temperature dependence to a first order. Calculating the depletion width for a large range of conditions, we found that the DR only marginally (<1%) shrinks at high T. Unless otherwise stated, in the following the reported maximum percentage changes refer to the 20–80 °C temperature range.

Funneling (which may not necessarily impact the SER [3]) depends on the ratio between the mobility of holes and electrons, μ_e/μ_h [18,19] according to the equation proposed by Edmonds:

$$Q_{tot} = Q_{drift}\left(1 + \frac{\mu_e}{\mu_h}\right) + Q_{diff} \tag{7}$$

We studied the term μ_e/μ_h as a function of temperature, using Eq. (2) and its counterpart for electrons. For doping levels higher than 10^{18} cm^{-3}, the ratio grows, whereas for lower levels, it either decreases or is non-monotonic in the considered range. In all cases the variation is lower than 5%.

After the first prompt collection, charge can be collected by diffusion in the vicinity of the depletion (and funnel) regions. Actually, diffusion may be the main driver for those strikes that do not intercept the drain, which are the majority with secondary byproducts of neutrons [4]. The width of the regions which can provide electrons depends on the diffusion length, $L = \sqrt{D^* \cdot \tau}$ where D^* is the ambipolar diffusion constant, and τ is the minority carrier lifetime in the bulk p substrate.

D^* increases or decreases with T depending on the doping level (11% with $N = 10^{18}$ cm^{-3}, −9% with $N = 10^{17}$ cm^{-3}), according to the following expression:

$$D^* = 2kT/q \cdot \frac{\mu_e(T) \cdot \mu_h(T)}{\mu_e(T) + \mu_h(T)} \tag{8}$$

The minority carrier lifetime τ is determined by Shockley–Read-Hall and Auger recombination, which both increase with T. The

Please cite this article in press as: Bagatin M et al. Temperature dependence of neutron-induced soft errors in SRAMs. Microelectron Reliab (2011), doi:10.1016/j.microrel.2011.08.011

Table 2
Factors impacting the SER temperature dependence.

Parameter	T dependence	Impact on SER	Variation range[a]	Reference	Main driver	Description
LET	≈	≈	<1.5%		E_g	Linear energy transfer
I_{DS}	↓↓	↑↑	<20%		$\mu_{channel}$	MOSFET drain current
t_{write}	↑↑	↓↓	<8%		$\mu_{channel}$	Cell write time
I_0	↓↓	↓↓	10–20%		μ_{track}	Peak drift current
x_d	↑	↑	<2%			Depletion region width
$l_{funneling}$	↑↓	≈	−3% to 3%		μ_e/μ_h	Funneling length
L_{diff}	↑↓	↑↓	n.a.	[23]	D^*, τ	Diffusion length
D^*	↑↓	↑↓	−7% to 11%		$(\mu_e\mu_h)/\mu_e + \mu_h$	Ambipolar diffusivity
τ	↑	↑	n.a.	[10][20-23]	SRH(T), Auger(T)	Minority carrier lifetime

[a] Estimated variation for 180-nm technology, for substrate doping from 10^{16} to 10^{18} cm^{-3}, in the temperature range 20–80 °C.

net result is an increase in the diffusion length, but since there is no consensus on the lifetime T dependence [20–22], no quantitative estimate is possible.

In more scaled technologies, the temperature dependence of the parasitic bipolar amplification should be considered as well.

4.3. SER versus temperature

As we have shown, temperature may impact the SER in many different ways, by altering:

(a) the characteristics of the memory cells (in terms of write speed and strength of the restoring device);
(b) the current pulse generated by the impinging particles (affecting the transport properties of the charge generated by radiation).

The most important parameters are summarized in Table 2. Our analysis shows that there is no clear dominant factor. Some of the terms we analyzed go in the direction of raising the sensitivity at high temperature (transistor drain current); others have the opposite effects (drift collection); and some others (ambipolar diffusion) may increase or decrease the SER depending on substrate doping and well engineering. This is confirmed by our experimental data, which show either a SER increase or a slight decrease (Fig. 2).

5. Conclusions

We irradiated commercial SRAMs with thermal and wide-spectrum neutron beams, studying the impact of temperature on the soft error rate. The experimental data, simulations, and analytical modeling show that, depending on the device, temperature may or may not increase the soft error sensitivity by a modest amount. Circuit analysis and discussion of charge collection mechanisms have shown that no dominant parameter exists, and that the temperature dependence results from a complex mix of factors. Contrary to latch-up, it is not possible to identify a worst-case condition with respect to temperature. Our data suggest that testing at room temperature may result in underestimation of the terrestrial SER of less than 20% in the common operating temperature range of commercial devices.

Acknowledgements

This work was supported within the CNR-CCLRC Agreement No. 01/9001 concerning collaboration in scientific research at the spallation neutron source ISIS. The financial support of the Consiglio Nazionale delle Ricerche in this research is hereby acknowledged.

References

[1] Baumann RC. Radiation-induced soft errors in advanced semiconductor technologies. IEEE Trans Device Matter Rel 2005;5(3):305–16.
[2] Hsieh CM, Murley PC, O'Brien RR. A field-funneling effect on the collection of alpha-particle-generated carriers in silicon devices. IEEE Electr Device Lett 1981;2:103–5.
[3] Dodd PE, Sexton FW. Critical charge concepts for CMOS SRAMs. IEEE Trans Nucl Sci 1995;42:1764–71.
[4] Palau JM, Hubert G, Coulie K, Sagnes B, Calvet MC, Fourtine S. Device simulation study of the SEU sensitivity of SRAMs to internal ion tracks generated by nuclear reactions. IEEE Trans Nucl Sci 2001;48:225–31.
[5] Kolasinski WA, Koga R, Schnauss E, Duffey J. The effect of elevated temperatures on latchup and bit errors in CMOS devices. IEEE Trans Nucl Sci 1986;33.
[6] Grandlund T, Olsson N. SEUs induced by thermal to high-energy neutrons in SRAMs. IEEE Trans Nucl Sci 2006;53:3798–802.
[7] Heijmen T. Factors that impact the critical charge of memory elements.In: IOLTS 2006 proceedings. p. 57–62.
[8] Sexton FW, Fu JS, Kohler RA, Koga R. SEU characterization of a hardened CMOS 64K and 256K SRAM. IEEE Trans Nucl Sci 1989;36:2311–7.
[9] Truyen D, Boch J, Sagnes B, Renaud N, Leduc E, Arnal S, et al. Temperature effect on heavy-ion induced parasitic current on SRAM by device simulation: effect on SEU sensitivity. IEEE Trans Nucl Sci 2007;54:1025–9.
[10] Guo G, Hirao T, Laird JS, Onoda S, Wasaka T, Yamakawa T, et al. Temperature dependence of single-event transient current Induced by heavy-ion microbeam on $p^+/n/n^+$ epilayer junctions. IEEE Trans Nucl Sci 2004;51:2834–9.
[11] Laird JS, Chen Y, Edmonds L, Vo T. Temperature dependence of spatially resolved picosecond laser induced transients in a deep submicron CMOS inverter. IEEE Trans Nucl Sci 2009;56:220–8.
[12] <http://lansce.lanl.gov/>, retrieved online on March 2011.
[13] Platt SP, Török Z, Frost CD, Ansell S. Charge-collection and single-event upset measurements at the ISIS neutron source. IEEE Trans Nucl Sci 2008;55:2126–32.
[14] <www.mosis.com> retrieved online on 03.03.11.
[15] Heijmen T. Analytical semi-empirical model for SER sensitivity estimation of deep-submicron CMOS circuits. In: IOLTS 2005 proceeding. p. 3–6.
[16] Hazucha P, Svensson C. Impact of CMOS technology scaling on the atmospheric neutron soft error rate. IEEE Trans. Nucl. Sci. 2000;47:2586–94.
[17] Correas V et al. Innovative simulations of heavy ion cross sections in 130 nm CMOS SRAM. IEEE Trans Nucl Sci 2007;54:2413–8.
[18] Arora ND, Hauser JR, Roulston DJ. Electron and hole mobilities in silicon as a function of concentration and temperature. IEEE Trans Electr Device 1982;29:292–5.
[19] Edmonds LD. A simple estimate of funneling-assisted charge collection. IEEE Trans Nucl Sci 1991;38:828–33.
[20] Huldt L, Nilsson NG, Svantesson KG. The temperature dependence of band-to-band Auger recombination in silicon. Appl Phys Lett 1979;35:776.
[21] Lochmann W, Haug A. Phonon-assisted Auger recombination in Si with direct calculation of theoverlap integrals. Solid-State Commun 1980;35:553–6.
[22] Tyagi MS, van Overstraeten R. Minority carrier recombination in heavily-doped Silicon. Solid-State Electron 1983;26:577–97.
[23] Goebel H, Hoffmann K. Full dynamic power diode model including temperature behavior for use in circuit simulators. In: Proc. of 1992 international symposium on power semiconductor devices & ICs.; 1992. p. 130–35.
[24] Roche P, Palau J-M, Tavernier C, Bruguier G, Ecoffet R, Gasiot J. Determination on key parameters for SEU using full cell 3-D SRAM simulations. IEEE Trans Nucl Sci 1999;46:1354–62.

Please cite this article in press as: Bagatin M et al. Temperature dependence of neutron-induced soft errors in SRAMs. Microelectron Reliab (2011), doi:10.1016/j.microrel.2011.08.011