High Efficiency and High Linearity Power Amplifier Design

Paolo Colantonio,[1] José Angel García,[2] Franco Giannini,[1] Carmen Gómez,[2] Nuno Borges Carvalho,[3] Ernesto Limiti,[1] José Carlos Pedro[3]

[1] University of Roma Tor Vergata, Electronic Engineering Department, Italy
[2] Department of Communication Engineering, E.T.S.I. de TELECOMUNICACION, University of Cantabria, Spain
[3] Instituto de Telecomunicações, University of Aveiro, Portugal

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ABSTRACT: The optimum high-frequency Class-F loading conditions are inferred, accounting for the effects of actual output device behavior, and deriving useful charts for an effective design. The important role of the biasing point selection is stressed, demonstrating that it must be different from the Class-B theoretical one to get the expected improvement. The IMD behavior of the Class-F amplifier is presented and the large-signal sweet-spot origin in the IMD output characteristics is discussed, together with possible strategies to improve intermodulation distortion performances. The control of the sweet spot position is demonstrated via proper terminating impedances, both at fundamental and harmonic frequencies and low frequencies. © 2005 Wiley Periodicals, Inc. Int J RF and Microwave CAE 15: 453–468, 2005.

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I. INTRODUCTION

Power amplifiers (PAs) are core elements in many microwave subsystems. High-output-power levels are typically joined with high-efficiency operating conditions, especially in mobile- or satellite-communication systems, and with low-intermodulation levels. In modern apparatuses, therefore, high efficiency and high linearity performances, while maintaining a high level of output power and gain, really become the major challenge of the design.

While continuous improvements in device technology and in material development are assuring major progress in power devices' performances, design approaches have been proposed to identify suitable device bias and loading conditions. In particular, Class-F design strategy is a popular solution improving efficiency (and output power) for PAs operating at relatively high frequency (up to the X-band), becoming an interesting methodology for PAs realized with high-performance devices [1]. The popularity of the Class-F technique is due to its design simplicity, being based on output-harmonic termination control only. In the last years, starting from Snider's work [2] for a Class-B bias condition, more realistic design approaches have been proposed in open literature [3, 4] or in text books [5, 6]. Accounting for some practical aspects related to the finite number of harmonics that can be effectively controlled and to the actual device's physical behavior, the relevance of a suitable voltage harmonic components ratio has been stressed, both in terms of amplitude and phase [7–12]. A comprehensive theory of multiharmonic manipulation design strategy has been presented in [13]: moving from a weighting procedure for the 2nd- and 3rd-order harmonic output-voltage components, a methodology is outlined, assuring the proper phase and amplitude

Correspondence to: Ernesto Limiti; e-mail: limiti@ing.uniroma2.it
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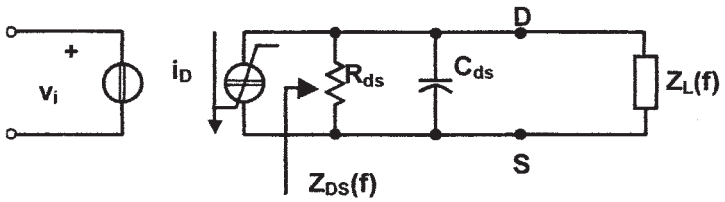

Figure 1. Simplified active-device output model.

ratios. This is accomplished by a careful selection of both the input and output terminations of the active device.

While the general bases of the harmonic manipulation procedure have been clarified and translated in design guidelines, very few hints are available in order to face the practical problems of an actual high-frequency (HF) Class-F design. As an example, the effect of bias conditions on the drain-current conduction angle, resulting in different phase relationships between generated harmonic current components in the HF Class-F scheme, has to be better explained, due to its crucial role in establishing amplifier performances. Moreover, since the output-device behavior is generally simplified, assuming a controlled current source with a shunt capacitive impedance only, the effect of the finite values of the output drain resistance R_{ds} must be evidenced, since it determines the 3rd-harmonic drain-voltage component, thus heavily influencing the amplifier performances. These two aspects are addressed in the following and translated in the design charts in order to help designers effectively trade-off among often conflicting design goals.

Nevertheless, the harmonic-tuning approach is often referred as an highly nonlinear design approach that degrades linearity performances. After presenting the measured data on an HF Class-F amplifier, linearity will be thusly considered. The linearity of PAs is an issue of primary concern in telecommunication applications where the signal format involves nonconstant envelopes. That is the case for modern pulse-shaped QPSK digital transmission, or in multicarrier systems in general, where spectral efficiency is achieved at the expense of amplitude-varying envelopes. PA nonlinearities, from which AM-AM and AM-PM conversion are two typical symptoms, generate new spectral components, or intermodulation distortion noise (IMD), known as spectral regrowth, which may again jeopardize the sought spectral mask. To prevent this, IMD must be combatted by the use of "linear" PA operation modes, typically, unsaturated class A or AB, to the detriment of the highly efficient Class B or C or, mostly, the saturated Class E, D, or F. Unfortunately, the highly quiescent power consumption associated with reasonably large values of output power back-off has such a high cost in the PA's power-added efficiency that it is usually understood that the basic target of PA design is to obtain Class-B efficiency with Class-A distortion. And, although this may be, in general, not possible, there are some particular PA features that provide a way to escape from this apparent dead end.

One such PA characteristic, which has recently seen an increased interest, is the so-called large-signal IMD sweet spot [21, 22]. Sweet spots are particular points of the IMD versus input power characteristic where only a few dBs of output-power back-off (and thus a few percent of efficiency degradation) can lead to astonishing high levels of the power-to-IMD ratio (IMR).

In the following, the origin of large-signal sweet spots is clarified, together with a clear indication of the parameters affecting them and the subsequent possibility of optimization of the sweet spots' position and level.

II. TUNED LOAD REFERENCE AMPLIFIER

Simplified device models are usually considered by assuming the device operating in its active region, as a voltage (MESFET) or current (HBT) controlled current source i_d [14, 15]. Linear output-device impedance is assumed, represented by the parallel connection of a drain-source resistance R_{ds} and capacitance C_{ds}, whose values are estimated from device S-parameter measurements (Fig. 1).

The results estimated through this model are clearly valid in a limited frequency range, since device parasitics are neglected. Moreover, hard output nonlinear phenomena only (such as pinch-off, resistive behaviour, and drain-current saturation phenomena) have been represented by this model, while input nonlinearities and local (small-signal) output nonlinear phenomena have been neglected.

Nevertheless, useful design considerations and a proper estimation of the −1-dB compression point (1 dBcp) starting from a few available device parameters, such as the drain bias voltage (V_{DD}) and current (I_{DC}), the maximum drain current (I_{max}), and the knee voltage (V_k) can be carried out [16]. From Figure 1, the drain voltage v_{ds} can be properly shaped by choosing suitable external loading impedances $Z_L(f)$. Drain current $i_d(t)$ and voltage $v_{ds}(t)$ are expressed in terms of their Fourier series expansion:

$$i_D(t) = I_0 + \sum_{n=1}^{\infty} I_n \cdot \cos(n\omega t), \tag{1}$$

$$v_{DS}(t) = V_{DD} - \sum_{n=1}^{\infty} V_n \cdot \cos(n\omega t + \psi_n), \tag{2}$$

where

$$V_n = Z_{DS}(nf) \cdot I_n = Z_{DS,nf} \cdot e^{f\psi_n} \cdot I_n. \tag{3}$$

Closed-form expressions for I_n, as a function of the drain current conduction angle α [9], can be obtained utilizing two different simplifying assumptions for the device transconductance g_m. In particular, the cases of a constant g_m, referred to as a truncated sinusoidal model (TSM), and a more realistic linearly v_i-dependent g_m, hereinafter described as quadratic model (QM), are presented. Device physical limitations impose constraints to the drain-voltage waveform:

$$V_k \le v_{DS}(t) \le V_{BR}, \tag{4}$$

with V_{BR} being the drain-source breakdown voltage and V_k its "knee voltage."

The Class-F performances are usually compared to those of the reference tuned load (TL) amplifier in order to evaluate the achieved level of improvement [14, 15, 17]. The TL approach implies that load impedances are

$$Z_{DS,TL}(nf) = \begin{cases} R_{TL}(\alpha) & n = 1 \\ 0 & n > 1, \end{cases} \tag{5}$$

where

$$R_{TL}(\alpha) = \begin{cases} R_A \cdot \pi \cdot \dfrac{1 - \cos\left(\dfrac{\alpha}{2}\right)}{\alpha - \sin(\alpha)} & \text{TSM} \\ R_A \cdot \dfrac{\pi \cdot \alpha^4}{128} \cdot \dfrac{1}{(12 - \alpha^2) \cdot \sin\left(\dfrac{\alpha}{2}\right) - 6\alpha \cdot \cos\left(\dfrac{\alpha}{2}\right)} & \text{QM} \end{cases} \tag{6}$$

and

$$R_A = 2 \cdot \frac{V_{DD}}{I_{\max}} \cdot (1 - \kappa) \quad \kappa = \frac{V_k}{V_{DD}}. \tag{7}$$

Similarly, closed-form expressions are derived for the PA main parameters, such as dc power consumption, output power, and drain efficiency [9].

A difference between the ideal TSM and the more realistic QM results is that the fundamental-frequency output load moves toward an open-circuit termination for lower drain-conduction angles, that is, for Class-C bias conditions. Moreover, moving from Class-A ($\alpha = 2\pi$) towards Class-B ($\alpha = \pi$), while drain efficiency increases from 50% to 78.5% (for the TSM) or from 46.2% to 83.5% (for the QM), power gain decreases by 6 dB.

III. HF CLASS-F APPROACH

In the approach by Snider [2], from a Class-B bias condition ($\alpha = \pi$) with a TSM for the drain current, mathematical analysis has been carried out assuming ideal drain-current (half sinusoid) and voltage (squared) waveforms; this prevents waveform overlapping, hence nulling the power dissipated on the active device. The resulting impedances $Z_{DS}(f)$ are derived as the ratio between the voltage and current Fourier harmonic components:

$$Z_{DS,F,ideal}(nf) = \begin{cases} \frac{4}{\pi} \cdot R_{TL}(\alpha)\Big|_{\alpha=\pi} & n = 1 \\ 0 & n\ even \\ \infty & n\ odd \end{cases}. \quad (8)$$

Assuming a "current-source" model, the drain-voltage waveform is generated from the corresponding drain-current waveform by loading each harmonic through suitable impedance values, as stated by eq. (3). As a consequence, if a pure Class-B bias condition is considered, drain-current odd-harmonic components are not generated at all, therefore avoiding the synthesis of voltage odd-harmonic components by finite and real impedances.

Although such ideal results are mathematical achievements only, Class-F designs have been successfully applied for years, with the capacity of selecting a bias point near the Class-B condition, that is, with a low but nonzero current I_{DC}, and assuming the same harmonic impedances carried out in the ideal case [2]. Such a "rule of thumb" of deep AB bias actually hides a critical issue, which is related to the generation of properly-phased voltage harmonic components, starting from properly-phased drain-current harmonic ones [9]. In high-frequency applications (that is, dealing with an HF Class-F amplifier) only a finite and small number of drain-voltage harmonic components are effectively controlled, due to several practical aspects: firstly, the shunting effects of the device output capacitive behaviour C_{ds} (Fig. 1), which limits the effectiveness of high-frequency harmonic terminations; secondly, the availability of reliable models (linear and nonlinear) at harmonic frequencies; finally, the increasing of circuit complexity, as required for the synthesis of a large number of harmonic terminations not balanced by a corresponding performance improvement [18, 19].

As a consequence, more realistic approaches have been developed [7–12], leading to design conditions quite different from the ideal ones [9].

Moreover, the active device output resistance R_{ds} (see Fig. 1), whose value represents an upper limit for the harmonic impedance values Z_{DS} that can be practically synthesised, has been almost systematically neglected. If its effects are accounted for, the optimum Class-F operating conditions, both in terms of bias and impedance values, have to be substantially revisited. To this goal, in the following the control of harmonic impedances up to $3f_o$ only, with f_o the fundamental operating frequency, will be assumed. A short-circuit termination will be considered at $2f_o$ while purely resistive terminations at the fundamental (f_o) and 3rd ($3f_o$) harmonic components are assumed. Such design choices are dictated by two major considerations: first of all, in this case simplified and closed-form expressions can be relatively easily obtained; moreover, it can be shown that optimum results are obtainable with purely real terminations, while complex loads lead to suboptimum results only [9, 10].

Under the above hypothesis, the drain-voltage waveform for a real HF Class-F amplifier is expressed as a function of drain current harmonic components as follows:

$$v_{DS,F}(t) = V_{DD} - R_1 \cdot I_1 \cdot [\cos(\omega t) + k_3 \cdot \cos(3\omega t)], \quad (9)$$

where

$$k_3 = \frac{V_{3,F}}{V_{1,F}} = \frac{R_3 \cdot I_3}{R_1 \cdot I_1}. \quad (10)$$

The drain-current harmonics I_n are therefore unaffected by output terminations, according to the adopted model.

The search for an optimum HF Class-F load conditions is therefore equivalent to the determination of the optimum R_1 and R_3 values (taking into account the R_{ds} constraint), which assures maximization of the fundamental voltage components $V_{1,F}$, that is, to obtain a $V_{1,F}$ value higher than $V_{1,TL} = V_{DD} - V_k$, while fulfilling the physical-constraint condition (4). It is therefore possible to define a voltage-amplitude gain function $\delta(k_3)$ [9] as the ratio between the maximum fundamental voltage-amplitude achievable through an HF Class-F approach ($V_{1,F}$) and this value ($V_{1,TL}$):

$$\delta(k_3) = \frac{V_{1,F}}{V_{1,TL}} = \frac{R_1}{R_{TL}} = \begin{cases} \frac{3 \cdot \sqrt{3 \cdot k_3}}{(3 \cdot k_3 - 1) \cdot \sqrt{3 \cdot k_3 - 1}} & if\ k_3 \le -\frac{1}{9} \\ \frac{1}{1 + k_3} & otherwise \end{cases}, \quad (11)$$

as graphically represented in Figure 2.

As a consequence, eq. (9) is rewritten as

$$v_{DS,F}(t) = V_{DD} - \delta(k_3) R_{TL} \cdot I_1 \cdot [\cos(\omega t) + k_3 \cdot \cos(3\omega t)], \quad (12)$$

where the load terminations are expressed as

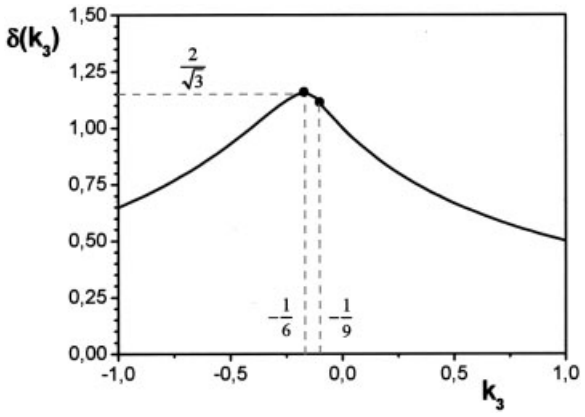

Figure 2. Voltage-gain function δ .

$$R_1 = \delta(k_3) \cdot R_{TL} \quad R_3 = \delta(k_3) \cdot R_{TL} \cdot k_3 \frac{I_1}{I_3}. \quad (13)$$

Under the above hypothesis, the achievable improvements with a HF Class-F approach in terms of power gain, output power, and drain efficiency with respect to the corresponding TL design figures are easily computed if $\delta(k_3)$ is introduced as follows:

$$\eta_F(\alpha) = \delta(k_3) \cdot \eta_{TL}(\alpha), \quad (14)$$

$$P_{out,F}(\alpha) = \delta(k_3) \cdot P_{out,TL}(\alpha). \quad (15)$$

From Figure 2, an optimum k_3 value ($-1/6$) results, corresponding to a maximum fundamental-drain voltage-amplitude increase, given by $2/\sqrt{3} \approx 1.155$. Obviously, the same level of improvements are achieved on drain efficiency, output power, and power-gain levels [9, 10], according to eqs. (14) and (15). The crucial role of the drain harmonic components (I_1/I_3) phase relationships is evidenced by eq. (13). In particular, a negative k_3 value can be synthesised only if I_1 and I_3 are opposite in sign, thus allowing an improvement of the amplifier performances, that is, obtaining $\delta(k_3) > 1$; otherwise, detrimental effects are expected since $\delta(k_3) < 1$, according to eq. (11) and Figure 2.

In order to identify drain-conduction angle α, allowing HF Class-F approaches (that is, improvements with respect to a TL approach), the product $I_1 \cdot I_3$ is reported in Figure 3 for TSM and QM. The sign of the above product directly indicates the phase relationship between the fundamental and 3rd-harmonic current components, and therefore the phase of the corresponding voltage harmonic components, hence giving information on the sign of the k_3 parameter.

From Figure 3, assuming a more realistic quadratic model for the drain-current waveform supplied by the active device, a Class-B bias condition ($\alpha = \pi$) implies a positive value for k_3, resulting in $\delta(k_3) < 1$, worsening amplifier performances with respect to a TL solution. The same consideration holds for both models under Class-C bias conditions, therefore justifying the lack of successful realizations of Class-F amplifiers in such biasing conditions.

HF Class-F load impedances R_1 and R_3, computed using eq. (13), are plotted in Figure 4, with k_3 at its optimum value ($-1/6$). As a first consequence, since positive values only are physically realizable for the two loads R_1 and R_3, the corresponding performance improvements ($\delta = 1.15$) will be achieved only for a finite range of drain conduction angles α, which in turns appears to be largely different if a TSM or a QM is assumed.

To stress the relevance of the proper phase relationship between the drain-current harmonic components (f_o and $3f_o$), the ideal drain efficiency and output power achievable through eqs. (14) and (15) are reported in Figure 5, assuming the optimum value for k_3 (that is, $-1/6$) but a physically acceptable 3rd-harmonic impedance is given by

$$R_3 = \delta(k_3) \cdot R_{TL} \cdot \left| k_3 \frac{I_1}{I_3} \right|. \quad (16)$$

From the above plots, drain-current conduction angles $\alpha > \pi$ only assure improvements over the TL solution. Moreover, such improvements are attainable only if the 3rd-harmonic load value R_3 is properly synthesized according to eq. (16), with $k_3 = -1/6$, as plotted in Figure 6, as a function of the drain-conduction angle α. Otherwise, the level of the achievable improvements results in being much lower, as dis-

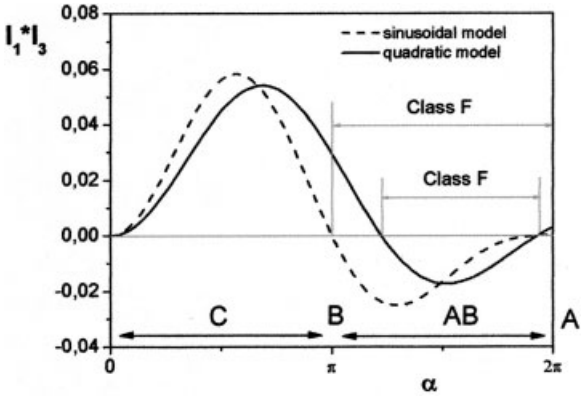

Figure 3. The drain-current harmonic component-phase relationship.

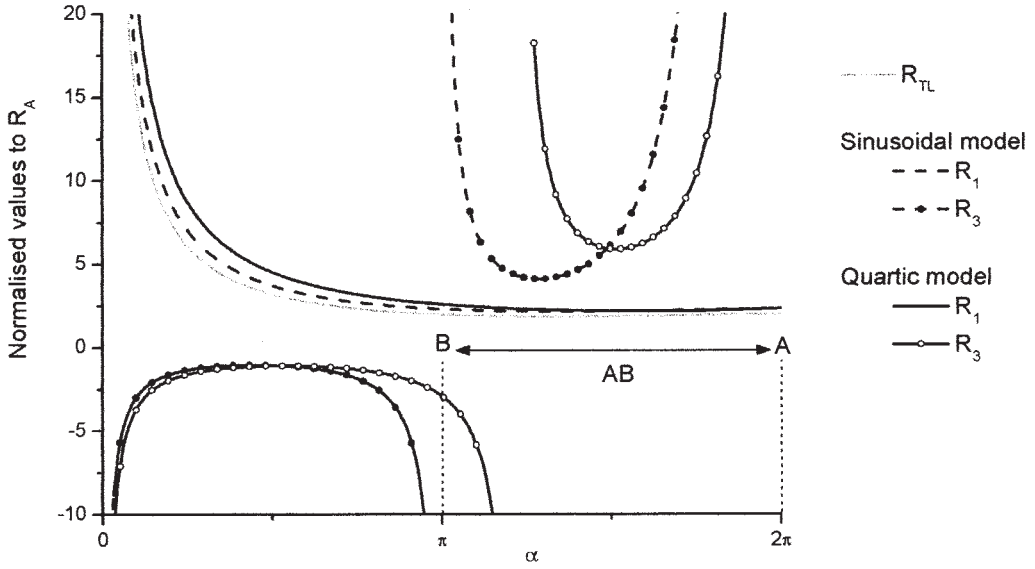

Figure 4. Ideal HF Class-F load impedances at f_o and $3f_o$ inferred by eq. (13) and assuming truncated sinusoid and quadratic models, respectively.

cussed in the following section. The optimum value for the 3rd-harmonic load impedance R_3 tends to become an open circuit when I_3 tends to zero (π and 2π for truncated sine, 3.8 and 6.06 for the quadratic waveform), as expected, according to Snider's theory. Unfortunately, the device output impedance R_{ds} represents an upper limit for R_3 (and eventually R_1) that can be synthesised; therefore, it has to be taken into account, since it modifies also the k_3 value that can be achieved. In this case, fixing R_3 to its maximum allowable value equal to R_{ds}, the following nonlinear equation has to be solved in k_3:

$$k_3 = \frac{R_{ds} \cdot I_3}{R_{TL} \cdot \delta(k_3) \cdot I_1}, \tag{17}$$

and the corresponding design quantities are given by

$$R_1 = \delta(k_3) \cdot R_{TL} \quad R_3 = R_{ds}. \tag{18}$$

As an example, drain efficiency and output power levels parameterized for several R_{ds} values are reported in Figures 7 and 8.

As a consequence, in both cases the maximum improvements achievable in terms of output power

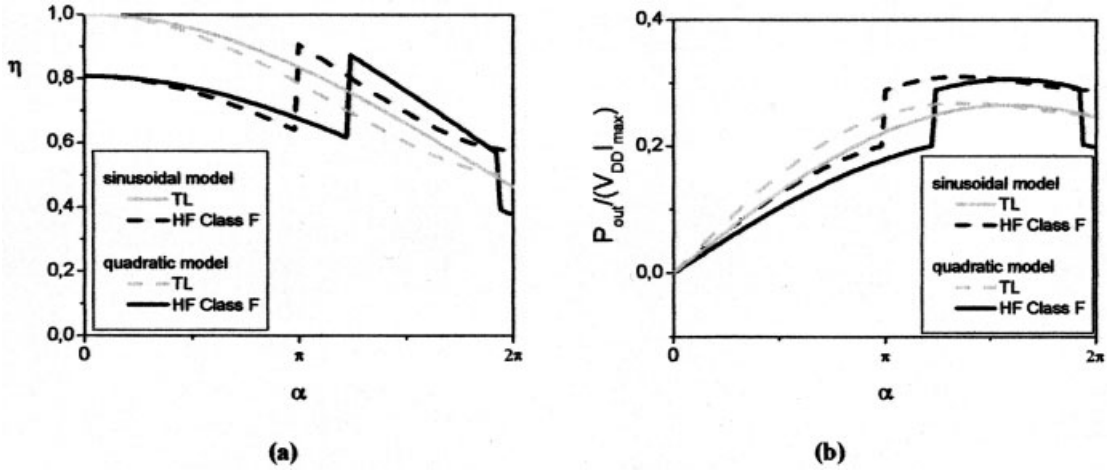

Figure 5. Comparisons between PA performances assuming truncated sinusoid and quadratic models.

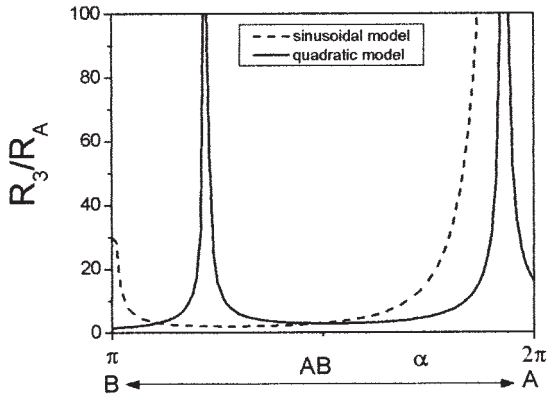

Figure 6. Third-harmonic load-impedance values as a function of the drain conduction angle α for truncated sinusoid and quadratic models.

and drain efficiency are strongly reduced. Moreover, the drain-current conduction angle α and the output conductance G_{ds} appear to be the leading quantities in order to perform an optimum design of an HF Class-F amplifier. For these reasons, in some design charts it is particularly useful to synthesize their combined effect on the main performances of the PA, that is, the output power and the drain efficiency. To this goal, the drain efficiency and output power-contour levels, as functions of the drain-current conduction angle α (and consequently as a function of I_{DC}) and device output conductance G_{ds} are reported in Figure 9.

IV. SIMULATION RESULTS AND IMD BEHAVIOUR

To demonstrate the effectiveness and applicability of the obtained theoretical results, an X-Band (with centre frequency at 9.6 GHz) Class-F power amplifier has been designed and simulated. The selected active device is a 1-mm PHEMT (10×100 μm) from Alenia Marconi Systems, modeled through a full nonlinear neural-based approach [20]. A deep Class-AB bias point has been selected, resulting in $V_{DD} = 8$ V and $V_{GG} = -0.5$ V. A Class-F design approach has been followed for the PA design. The optimum selected loading conditions are reported in Figure 10, at both the fundamental and harmonic frequencies, for the input and output device ports. Such points have been obtained initially by means of the proposed simplified approach and slightly optimized via the available CAD in order to account for device parasitics.

Active device I-V output characteristics are reported in Figure 11 with a superimposed corresponding load curve (that is, the instantaneous plot of the device current and voltage waveforms) simulated at the -1-dB compression point, while the resulting overall PA performances are plotted in Figure 12. The load curve has been obtained considering intrinsic device voltage and current quantities, that is, voltage and current at the intrinsic output voltage-controlled current source terminals.

The dc gate bias voltage has been varied from -0.6 V (deep Class-AB bias condition) to 0 V, leaving the loading conditions unchanged both for the fundamental load and input-output harmonic terminations. The resulting power-added efficiency (PAE) and output power, sampled at -1 dBCP, are reported in Figure 13 and compared with the results predicted according to the approach proposed above. The following device parameters have been assumed:

$$I_{\max} = 440 \text{ mA}, \quad V_k = 1 \text{ V} \quad R_{ds} = 100\Omega. \quad (19)$$

The behavior of the PAE closely matches the one that obtained from eq. (14), regardless of the performed simplifying assumptions. Finally, power-added efficiencies achieved at the 1-dB compression point are reported in Figure 14, fixing the gate bias at $V_{GS} = -0.5$ V and varying the phase only of the input [Fig. 14(a)] or of the output [Fig. 14(b)] reflection coefficient at $3f$ (that is, at 28.8 GHz), while keeping its

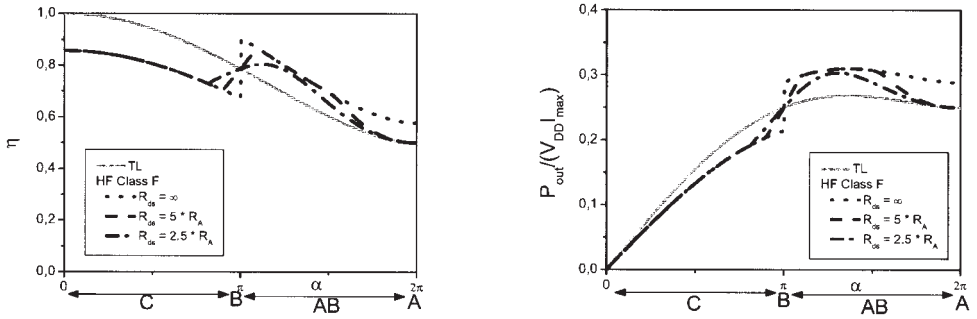

Figure 7. HF Class-F amplifier design assuming a sinusoidal model: (a) achievable drain efficiency; (b) normalized achievable output-power level.

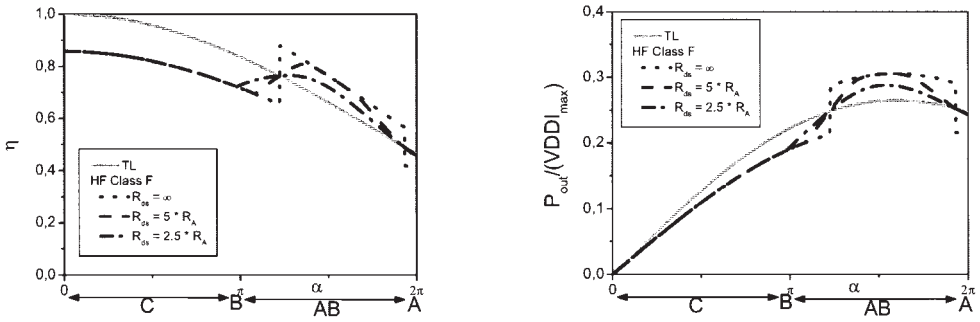

Figure 8. HF Class-F amplifier design assuming a quadratic model: (a) achievable drain efficiency; (b) normalized achievable output-power level.

magnitude fixed to a unitary (purely reactive) value. As is possible to note, the effect of the phase of the input reflection coefficient at $3f$ is basically of minor importance, implying a total potential variation around 2% on PAE performances. On the other hand, as depicted in Figure 14(b), the effect of the output termination at $3f$ may be relevant, implying a total variation of 10% on PAE performances. For these reasons, the design condition has been selected in the "flat" region in Figure 14(b), in order to minimize the detrimental effects of process-parameter variations.

A comparison between the TL and the HF Class-F designs' IMD performances has been carried out and plotted in Figure 15, where the 3rd-order intermodulation power from a two-tone test is plotted as a function of the output back-off.

As is possible to note, the use of harmonic-terminating schemes do not deteriorate in principle the IMD performance with respect to an unmanipulated approach such as the TL one. Nevertheless, IMD improvements to the Class-F approach are feasible by adopting sweet-spot control schemes that are described in the following section.

V. LARGE-SIGNAL SWEET SPOTS ORIGIN

As previously mentioned, large-signal sweet spots are points of the IMD versus input-power characteristic where a minor output-power back-off leads to high levels of power-to-IMD ratio (IMR). For example, the IMR versus P_{in} patterns of a power amplifier biased for classes C, AB, and A (Fig. 16) show that, although Class-A is incomparably more linear for small-signal excitation levels, that situation changes when the PA is driven close to saturation (around 3 dBm $< P_{in} <$ 20 dBm). There, the IMD sweet spots presented by both Class-C and Class-AB overcome the IMR offered by Class-A.

These curious nonlinear effects can be qualitatively explained as opposite phase interactions of small- and large-signal IMD components, typically arising from the mild $i_{DS}(v_{GS})$ nonlinearities of FETs [or $i_C(v_{BE})$ in bipolar-based PAs], and the device's strong nonlinearities, usually associated with the onset of saturation.

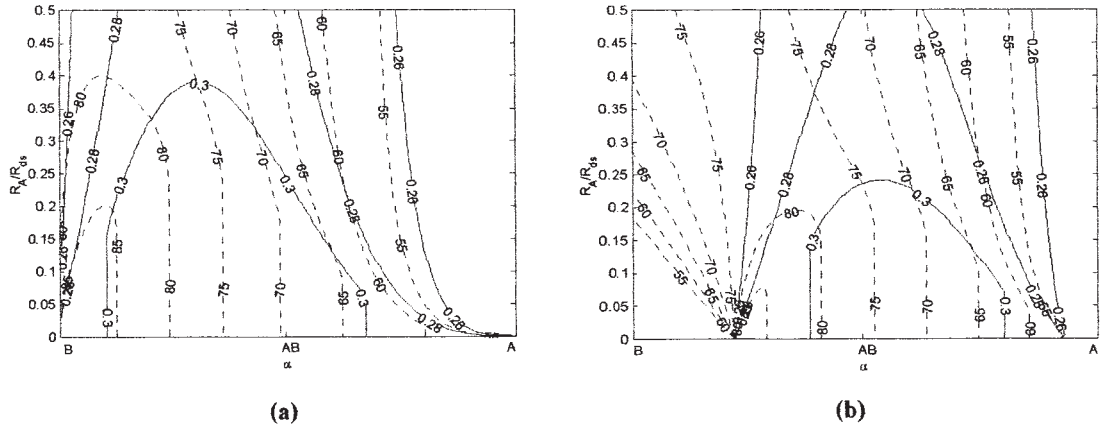

Figure 9. Class-F design charts for drain efficiency (dotted curves) and normalized output power (continuous curves), obtained with a (a) TSM or (b) QM.

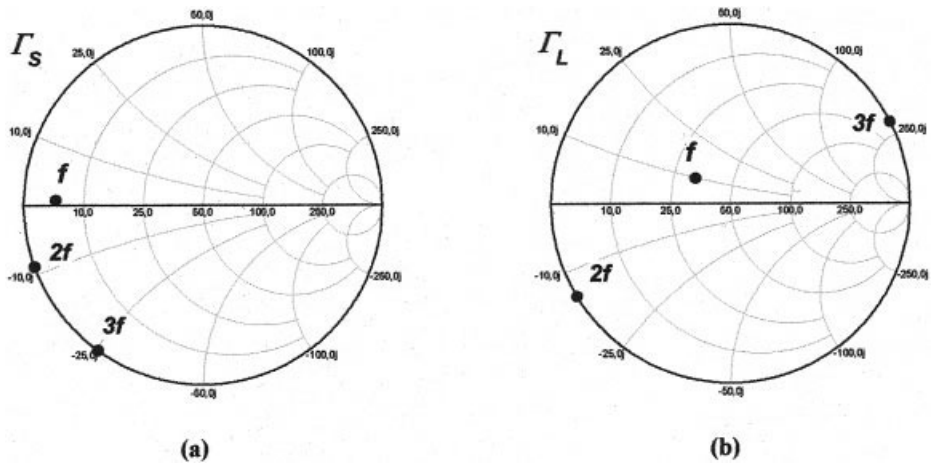

Figure 10. Active-device selected (a) input and (b) output terminations at fundamental f and harmonics ($2f$ and $3f$).

Mild nonlinearities are mainly determined by the device's soft turn-on followed by a region of quasi-linear input-output transfer characteristic. They can be conveniently modeled by a 3rd-order Taylor series expansion around the quiescent point $I_{DS}(V_{GS})$ as eq. (20) below, where the 1st-order coefficient, G_m, determines the fundamental component, and so the linear gain, while the 3rd-order one, G_{m3}, controls the small-signal in-band distortion, and thus IMD and gain versus input drive variation:

$$i_{ds}(v_{gs}, V_{GS}) = i_{DS}(v_{GS}) - I_{DS}(V_{GS}) = G_m(V_{GS})v_{gs} + G_{m2}(V_{GS})v_{gs}^2 + G_{m3}(V_{GS})v_{gs}^3. \quad (20)$$

The FET's strong nonlinearities are imposed by the device's output current limitation, that is, the gate-channel junction conduction or breakdown or, more commonly, the saturation-to-triode region transition.

So, as shown in Figure 17, depending on the device's quiescent point, and thus on the sign of G_{m3}, the mild nonlinearities can lead to either gain expansion (Class-C quiescent point) or gain compression (Class A or AB quiescent points) distortion characteristics.

On the other hand, as the device's strong nonlinearities direct the PA output-power saturation, they always imply gain compression, and thus an in-band distortion whose phase is opposite to the fundamental components. Hence, depending on the quiescent point, we can have a very slight small-signal gain compression followed by strong gain compression, as in the usual Class-A PAs, or a moderate gain expansion followed by, again, the strong compression, if the PA is biased for Class-C, that is, below the threshold voltage V_T. The good news is that any time the nonlinear distortion contributions reverse their phase, because of an opposing interaction between the small-signal—mild—and large-signal—strong—nonlinear regimes, they must pass through a point of theoretically null amplitude, that is, a zero in the IMD versus P_{in} plot, the abovementioned large-signal IMD sweet spot.

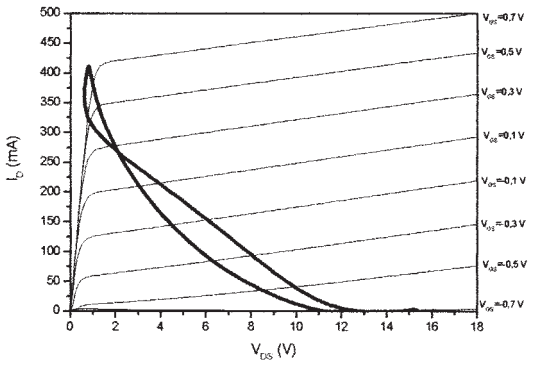

Figure 11. Active-device output I-V characteristics.

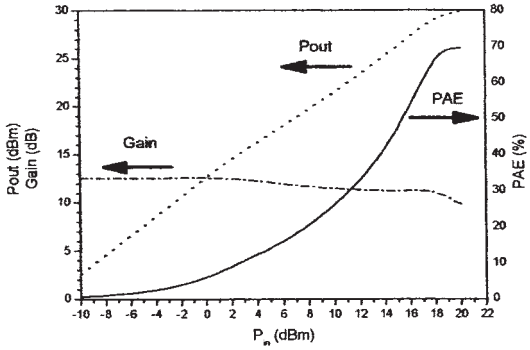

Figure 12. Simulated Class-F PA performances at the bias point $V_{GG} = -0.5$ V and $V_{DD} = 8$ V.

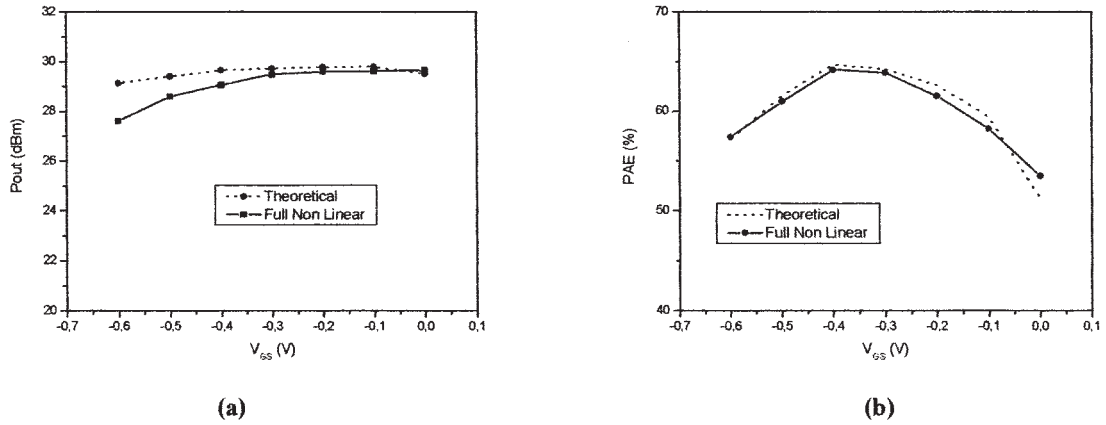

Figure 13. Simulation with (a) full nonlinear-model output power and (b) power-added efficiency at 1-dB compression point for Class-F PA, obtained varying the dc gate bias voltages and compared with the theoretical results, assuming a sinusoidal model and device parameters as reported in eq. (19).

Moreover, if the device is biased slightly above turn-on—the mode usually identified as Class-AB operation—the PA starts by showing again a very shallow gain compression imposed by the negative G_{m3}. Hence, similarly to what was concluded for Class-A operation, no IMD sweet spot should be expected. Nevertheless, depending on the abruptness of turn-on and succeeding linearisation of the $i_{DS}(v_{GS})$ characteristic (typical in LDMOS, MOSFETs, or even in some HEMTs), it can be shown that as the input-signal excursion grows, entering more into the gain-expansion region (positive G_{m3}), the PA ceases to present gain compression and tends to behave as in Class-C [23], generating another IMD sweet spot for moderate signal levels. At this stage, the circuit begins to behave as a Class-C PA with the corresponding gain expansion. Consequently, a new IMD sweet spot will have to occur at large-signal, when gain compression finally takes place. So, depending on the actual device's transfer characteristic and on the adopted quiescent point, Class-AB may be significantly different from Class-A in that it may even present two IMD sweet spots, one for small-to-moderate levels of input power and another for the onset of saturation. This is illustrated by the Class-AB plot in Figure 16.

In summary, low IMD can be either achieved through a largely backed-off Class-A PA, or through the sweet spots of a Class-C or Class-AB PA, close to the onset of saturation. Despite being accomplished in a predetermined zone of excitation level, the PAE provided by the Class-AB or Class-C PA is so high that, unless extremely good figures of the carrier-to-IMD ratio are required, these solutions present a much

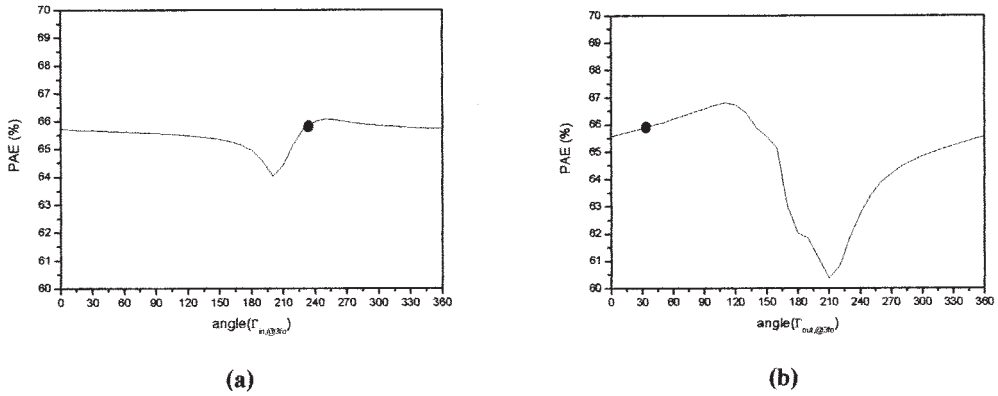

Figure 14. Simulation with full nonlinear model power-added efficiency at 1-dB compression point for Class-F PA, obtained at $V_{GS} = -0.5$ V and varying the (a) input or (b) output phase of the reflection coefficient at $3f_o$ (at 28.8 GHz) on the unit Smith chart circle. In both figures the performed design condition is circled.

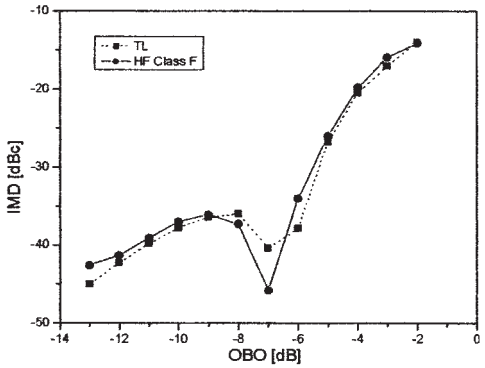

Figure 15. IMD performances of the designed tuned load and HF Class-F amplifiers.

better IMD versus efficiency compromise then the traditional highly linear Class-A amplifier design.

VI. LARGE-SIGNAL SWEET SPOTS CONTROL

Given this large-signal sweet-spot origin, it becomes clear that those parameters capable of controlling the onset of saturation (namely, the biasing voltages and the load termination) can be effectively used to produce a sweet spot at the desired operating power level [22]. By way of illustration, lowering the gate-to-source DC voltage in a class C FET amplifier would move the point of optimum linearity to higher input-power levels, as the required input-voltage excursion, needed for output-current saturation, must be increased. This is shown in Figure 18.

An accurate description of such behavior opens the possibility of automatically conforming P_{in}-IMD profiles with wide or multiple sweet spots. For this, two

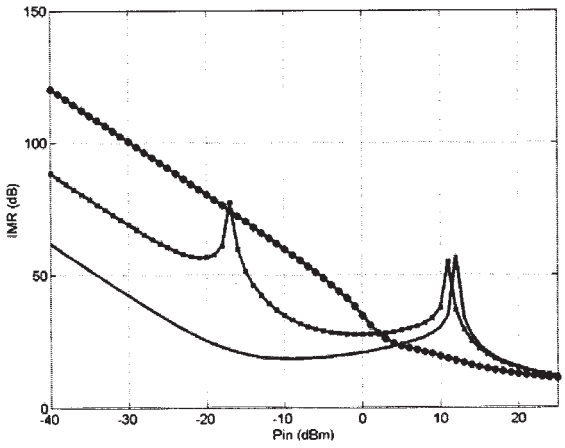

Figure 16. Typical IMR vs. P_{in} plots for three operation classes: C (—), AB (×), and A (○).

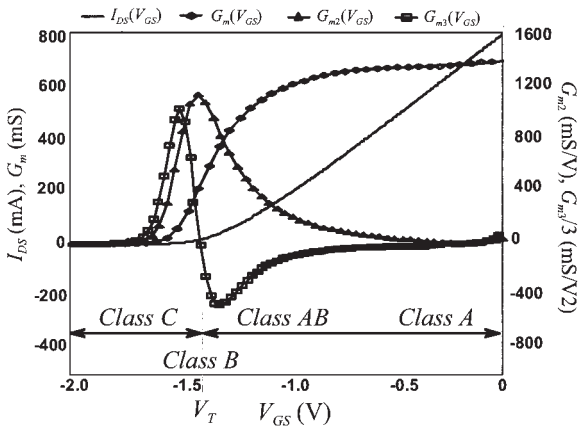

Figure 17. $I_{DS}(V_{GS})$ and its first three Taylor series coefficients, G_m, G_{m2}, and G_{m3}. Note the definition of the PA operation classes, as determined by the FET's quiescent point.

actions would be required: (i) sensing the long time RMS value of the excitation envelope and (ii) using this quantity to modify the device's operating conditions.

For example, a resistor R_G could be added to the gate DC path in order to reduce the sensitivity of the sweet spot to input-power variations in a simple amplifier [24]. In fact, as the gate-channel junction conduction will generate a DC bias current entering the gate (which, flowing through R_G, creates a negative self-biasing effect), it becomes clear that an increase in V_{GS} bias—that would lead to the onset of saturation sooner, and so displace IMD sweet spots towards lower P_{in}—will also lead to gate-channel conduction sooner, thus reducing the actual V_{GS} and restoring the sweet-spot position. In Figure 19, a simplified schematic of the V_{GS} bias-adaptation technique is presented.

On the other hand, a complete bias-adaptation topology can be implemented, if one were also interested in assuring a good linearity versus efficiency tradeoff with constant gain in the output stage of a transmitter with power-control capability [25]. If a reduction in V_{GS} with the input-power level was conveniently accompanied by an increase in V_{DS}, a wide sweet spot could be configured without deterioration in the power-gain characteristic.

The biasing-condition influence over the large-signal intermodulation distortion is also finding application in the development of power-amplifier linearization techniques at the device level. Taking advantage of the distortion-current control in amplitude and sign around the sweet spot, large-signal forms of the derivative superposition have been suggested [26, 27]. The IMD generated in an "auxiliary," parallel-con-

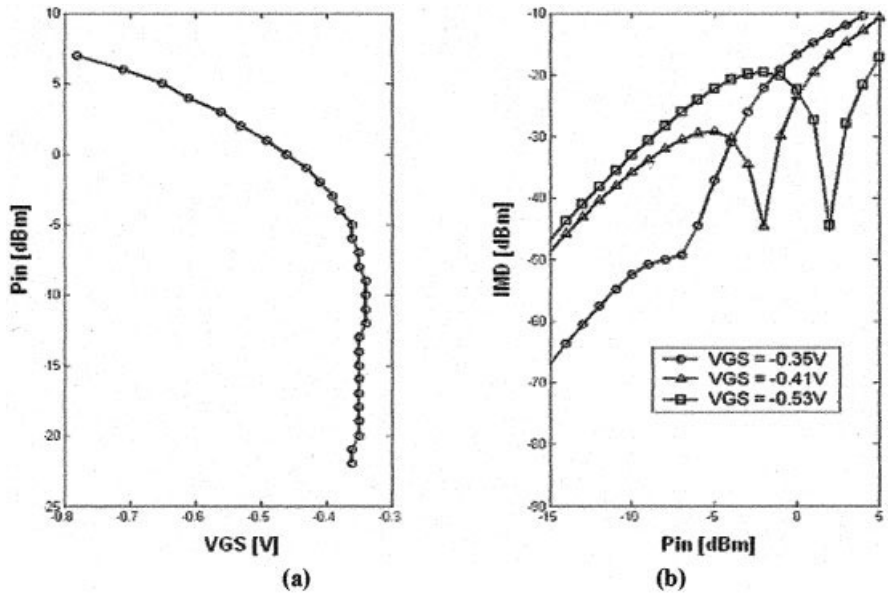

Figure 18. Typical sweet-spot evolution plots with V_{GS} and P_{in}: (a) P_{in} at which an IMD sweet-spot takes place for each V_{GS} bias; (b) a family of IMD vs. P_{in} profiles when V_{GS} bias is used as a parameter.

nected, Class-C power amplifier, operating below the large-signal sweet-spot power level, could be used to cancel the distortion produced by the Class-C "main" amplifier working above its corresponding sweet-spot position.

To close this qualitative analysis, let us mention some issues that may jeopardize the linearity characteristics of these IMD nulls, and thus should deserve particular attention during the PA design and implementation phases.

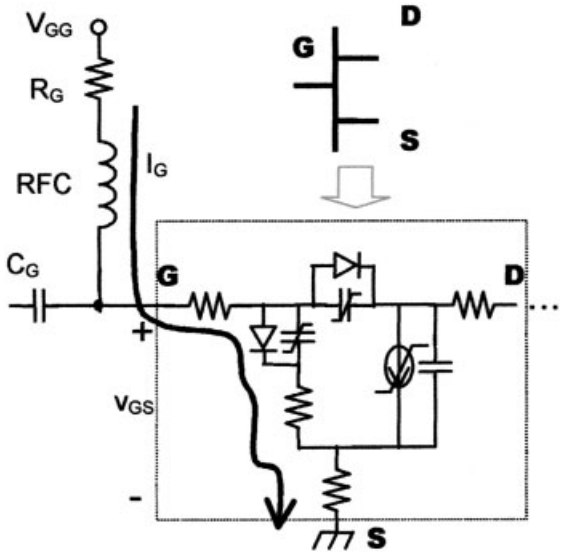

Figure 19. Simplified schematic of the V_{GS} self-biasing technique based on the use of an R_G resistor.

As seen above, large-signal IMD sweet spots are based on the cancellation, at a certain signal level, of small-signal and large-signal IMD components, for example, when 3rd-order IMD at $2\omega_1 - \omega_2$ cancels with 5th, 7th, ..., $(2n + 1)$-order correlated components at $2\omega_1 - \omega_2 + \omega_1 - \omega_1$, $2\omega_1 - \omega_2 + 2\omega_1 - 2\omega_1$, ..., $2\omega_1 - \omega_2 + (n - 1)(\omega_1 - \omega_1)$, or $2\omega_1 - \omega_2 + \omega_2 - \omega_2$, $2\omega_1 - \omega_2 + 2\omega_2 - 2\omega_2$, ..., $2\omega_1 - \omega_2 + (n - 1)(\omega_2 - \omega_2)$. So, this linearization method has its efficacy reduced if some of its preconditions are not met.

First of all, we should recognize that the large-signal IMD sweet spot was referred as the P_{in} amplitude for which 3rd-order components interacted with their higher-order correlated counterparts to create an IMD minimum. In a two-tone test, this means that the IMD sideband at, for example, $2\omega_1 - \omega_2$ will pass through a null. But, as happens to many other PA linearization schemes, this is usually not accompanied by a similar null on, for example, the uncorrelated (with $2\omega_1 - \omega_2$) 5th-order components at $3\omega_1 - 2\omega_2$. Thus, although the overall effect is still an IMD power reduction, the integrated IMD at the 3rd- and 5th-order distortion sidebands will never be exactly zero. Contrary to this simplified two-tone test, in which each of the sidebands only contains correlated components, under a real multicarrier excitation of a large number

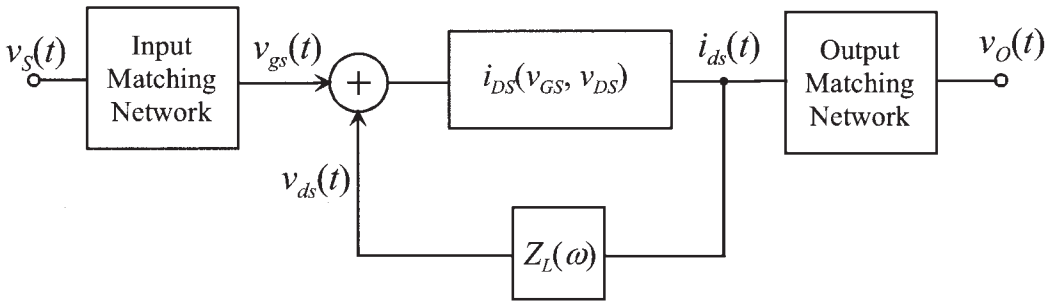

Figure 20. Nonlinear feedback-system model used to qualitatively describe the dynamic IMD sweet-spot dependence on the PA output termination $Z_L(\omega)$.

of tones, the situation is completely different. Each of the adjacent channels, the alternate channel, and so on, contains correlated but now also uncorrelated components of all odd-order IMD components of the form $2\omega_1 - \omega_2$, $3\omega_1 - 2\omega_2$, . . . , $(n + 1)\omega_1 - n\omega_2$. So, the null verified for the correlated components will simply expose the remaining uncorrelated higher-order distortion products, and the previously observed zero in the two-tones case will be converted into a smooth valley [22]. Nevertheless, the overall result is still an IMD improvement.

This effect can also be seen from the time-varying envelope perspective, as the presence of the modulation can be traced to the multitone nature of the signal. Indeed, if the handled signal shows a wide varying-amplitude envelope, and the IMD cancellation can only be perfect at a particular amplitude, we are led to the conclusion that the overall P_{in}-IMD pattern is also likely to depend on the statistics of the signal-amplitude distribution [28], thus smoothing the referred IMD valley [22].

Also, perfect cancellation requires that the IMD correlated components arising from the device's mild and strong nonlinearities are in exact opposite phase. If that condition is not met, the sweet spot will again be converted in a smooth valley, even under the idealized two-tone excitation. As the onset of saturation can generally be attributed to the output-current limitation imposed by the FET's triode zone, a phase deviation from the required 180° is expected to happen anytime the intrinsic load impedance at the fundamental components is not a pure resistance, or because there are out-of-band reactive effects at the baseband and the even harmonics [22].

To understand this process, let us imagine, as a 1st-order approximation, that the FET current does not depend on v_{DS}, in saturation [the assumption used to adopt a 1D Taylor series formulation in (20)], but shows a strong variation with this control voltage when in the triode zone. So, the large-signal i_{ds} in-band distortion effects can now be modeled for combined effects of the input voltage, $v_{gs}(t)$, and output voltage, $v_{ds}(t)$, using the model shown in Figure 20.

This model describes the feedback dependence that exists between $i_{ds}(t)$ and $v_{ds}(t)$ via the load termination. This is due to the fact that i_{DS} strongly depends on v_{DS} in the triode region, while $v_{ds}(t)$ is determined by $i_{ds}(t)$ via the load impedance termination by $V_{ds}(\omega) = Z_L(\omega) \cdot I_{ds}(\omega)$.

The condition regarding the dynamic load impedance at the fundamental refers to a phase shift between the pure in-phase compression due to the hypothetical resistive output and the actual phase the IMD will have in case of a significant output reactive mismatch [22]. In that case, the small-signal distortion at $2\omega_1 - \omega_2$ will be determined by $V_{gs}(\omega_1)^2 V_{gs}(\omega_2)^*$ while the 5th-order components will have distortion products of the form $V_{gs}(\omega_1)^2 V_{gs}(\omega_2)^* V_{gs}(\omega_1) V_{ds}(\omega_1)^*$ and $V_{gs}(\omega_1)^2 V_{gs}(\omega_2)^* V_{gs}(\omega_2) V_{ds}(\omega_2)^*$. In any of these cases, it is obvious that the phase of the higher-order components will depend on the $Z_L(\omega)$ phase, and so the sweet spot cannot be the ideal IMD null.

The second condition concerns the odd-order IMD generated by remixing even-order components with odd-order ones. For example, the IMD components at $2\omega_1 - \omega_2$ that arise by the output remixing of 4th-order $2\omega_1 = 2\omega_1 + \omega_1 - \omega_1$ or $2\omega_1 = 2\omega_1 + \omega_2 - \omega_2$ with the fundamental ω_2—$V_{gs}(\omega_2)^* \cdot V_{ds}(2\omega_1) \cdot |V_{ds}(\omega_1)|^2$ or $V_{gs}(\omega_2)^* \cdot V_{ds}(2\omega_1) \cdot |V_{ds}(\omega_2)|^2$—have a phase that is obviously dependent of the $2\omega_1$ output termination, $Z_L(2\omega_1)$.

Fortunately, since the output current and voltage shaping of high-efficiency PA designs commonly dictate a null 2nd-harmonic $v_{ds}(t)$ component, it may be expected that this $Z_L(2\omega_1)$ may not have a strong effect on the IMD characteristics.

Finally, as even the difference frequency components can be remixed with the fundamentals to create new in-band distortion products, for example,

$V_{gs}(\omega_1) \cdot |V_{gs}(\omega_1)|^2 \cdot V_{ds}(\omega_1 - \omega_2)$ or $V_{gs}(\omega_1) \cdot |V_{gs}(\omega_2)|^2 \cdot V_{ds}(\omega_1 - \omega_2)$, care should be taken to prevent the dynamic effects induced by the bias networks. In fact, it is this bias circuitry, associated with any RF choke or DC blocking capacitor present in the output matching network, that will impose the load impedance at the difference frequency, $Z_L(\omega_1 - \omega_2)$.

Moreover, it is convenient to note that the device's low-frequency dispersion, due to trapping effects and/or self-heating [29], are two more causes of a slow memory-feedback path. Therefore, it is at least theoretically possible to have smooth IMD sweet-spot valleys for PAs presenting matched fundamentals [resistive $Z_L(\omega)$], shorted 2nd harmonics [$Z_L(2\omega) \approx 0$] and well-designed bias networks [$Z_L(\omega_1 - \omega_2) \approx 0$]. Unfortunately, the lack of good nonlinear device models to represent these low-frequency memory effects still constitutes a major difficulty for the accurate computer-aided design of current PA prototypes, especially where detailed P_{in}-IMD patterns are concerned.

VII. CONCLUSION

The HF Class-F PA design strategy has been revised, relating it to the TL approach. The effects of both the driving drain-current shaping and the device output conductance R_{ds} have been stressed, carrying out optimum HF Class-F design statements, while putting into evidence some relevant discrepancies between the ideal case and the practical realization of such an amplifier. Moreover, the crucial role of the biasing point of the amplifier has been evidenced, demonstrating that it must be different from the Class-B theoretical one, in order to obtain the expected improvement. Design charts have been inferred to help designers choose the proper trade-off solutions, depending on the device physical parameters. After presenting the IMD behavior of a sample HF Class-F design, the origin of the large-signal sweet spot in IMD performances has been presented. The possibility of controlling the sweet-spot position has been justified and demonstrated through the proper choice of terminating impedances, at both the relevant fundamental and harmonic frequencies, and at low frequencies, where the validity of commonly adopted large-signal device models is often not verified in the accurate representation of low-frequency memory effects.

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BIOGRAPHIES

Paolo Colantonio was born in Roma, Italy on March 22, 1969. He received his degree in electronic engineering from University of Roma "Tor Vergata" in 1994 and his Ph.D in microelectronics and telecommunications in 2000. In 1999 he became a Research Assistant at the same university. Since 2002 he has been a professor of microwave electronics at the University of Roma "Tor Vergata," Italy. His main research activities are in design methodologies for nonlinear microwave circuits, nonlinear analysis techniques, and modelling of microwave active devices. Currently, he is responsible for the work package activity on "power-amplifier design overview" in the European network of excellence TARGET.

José Angel García was born in Havana, Cuba, in 1966. He received his Telecommunication Engineering degree (with honors) from the Instituto Superior Politécnico "José A. Echeverría" (ISPJAE), Cuba, in 1988, and his Ph.D. degree from the University of Cantabria, Spain, in 2000. From 1988 to 1991, he was a Radio System Engineer at the High-Frequency Communication Center, where he designed antennas and RF circuits. In 1991, he was appointed Instructor Professor in the Telecommunication Engineering Department, ISPJAE. From 1999 to 2000, he was a Radio Design Engineer with Thaumat Global Technology Systems. He also worked as Microwave Design Engineer and Project Manager with TTI Norte from 2000 to 2001, in charge of the research line on software-defined radios while involved in LNA and active antenna design. Since January 2002, he is working as a Senior Research Engineer at the University of Cantabria. His main research interests include nonlinear characterization and modeling of active devices, intermodulation distortion control on RF and microwave applications, reconfigurable terminals, and active antennas. He received one of the prizes from the Spanish Official Board of Telecommunication Engineers to the Best 2000 Doctoral Thesis Work, and was co-recipient of the GaAs Prize for Best Paper at the 2001 European Microwave Week. He has also been a reviewer for several magazines.

Franco Giannini was born in Galatina (LE), Italy, on November 9, 1944, and received a degree in electronics engineering, summa cum laude, in 1968. Since 1980 he has been a professor of applied electronics. Presently, he is at the University of Roma "Tor Vergata." He has been working on problems concerning modelling, characterization, and design methodologies of passive and active microwave components, circuits, and subsystems, including GaAs microwave and millimeter wave monolithic integrated circuits. He is a consultant for various national and international industrial and governmental organizations, including the International Telecommunication Union and the European Union, and has been a member of many committees for international scientific conferences on

GaAs and on microwave and millimeter-wave techniques and applications.

Carmen Gómez was born in Santander, Spain, in 1975. She received her Telecommunication Engineering degree from the University of Cantabria, in 2002. Since that date, she has been working on her Ph.D. with the Communication Engineering Department, also at the University of Cantabria. Her research topics are nonlinear characterization and modeling of active devices, intermodulation distortion control in RF and microwave applications, and active antennas. Currently, she is working for the Cantabrian Regional Development Agency, SODERCAN.

Nuno Borges Carvalho was born in Luanda, Portugal, in 1972. He received his diploma and doctoral degrees in Electronics and Telecommunications Engineering from the University of Aveiro, Aveiro, Portugal in 1995 and 2000, respectively. From 1997 to 2000, he was an Assistant Lecturer and a Professor since 2000. Currently, he is an Associate Professor at the same University and a Senior Research Scientist at the Telecommunications Institute. He has worked as a scientist researcher at the Telecommunications Institute, engaged in different projects on nonlinear CAD and circuits. His main research interests include CAD for nonlinear circuits and design of RF-microwave power amplifiers. He is a member of the Portuguese Engineering Association and an IEEE member. He was the recipient of the 1995 University of Aveiro and the Portuguese Engineering Association Prize for the Best 1995 Student at the Universidade de Aveiro, the 1998 Student Paper Competition (third place) presented at the IEEE International Microwave Symposium and the 2000 IEE Measurement Prize. He has been a reviewer for several magazines and is a member of the *IEEE Transactions on Microwave Theory and Techniques* Reviewer Board. He is co-author of the book "Intermodulation in Microwave and Wireless Circuits" (Artech House, 2003).

Ernesto Limiti was born in Roma, Italy in 1965 and received his degree in electronic engineering from the University of Roma "Tor Vergata" in 1989. In 1991, he became a Research and Teaching Assistant at the same university, where, from 1998, he has been a Professor of Electronic Instrumentation and Measurements. He is currently Full Professor of Electronics. His main scientific interests are in the field of design methodologies for nonlinear microwave circuits, nonlinear analysis methods, and noise characterization and modelling of microwave active devices for high-performance applications. He serves as a reviewer for a number of scientific journals and international conferences. He chaired the INMMiC international workshop in 2004.

José C. Pedro was born in Espinho, Portugal on March 7, 1962. He received his diploma and doctoral and habilitation degrees in electronics and telecommunications engineering from the University of Aveiro, Portugal in 1985, 1993, and 2002, respectively. From 1985 to 1993, he was an Assistant Lecturer at University of Aveiro, and a Professor since 1993. Currently he is a Professor at the same University, and a Senior Research Scientist at the Institute of Telecommunications. His main scientific interests include active-device modeling and the analysis and design of various nonlinear microwave and optoelectronics circuits, in particular, the design of highly linear multicarrier power amplifiers and mixers. He is the leading author of "Intermodulation Distortion in Microwave and Wireless Circuits" (Artech House, 2003), has authored or co-authored several papers in international journals and symposia, and has served the IEEE as a reviewer for the *MTT Transactions* and the *MTT-IMS.* He received the Marconi Young Scientist Award in 1993 and the 2000 Institution of Electrical Engineers (IEE) Measurement Prize.