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DESIGN OF SINGLE ENDED PRIMARY INDUCTOR DC-DC CONVERTER

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DESIGN OF SINGLE ENDED PRIMARY INDUCTOR DC-DC CONVERTER

A Thesis submitted in partial fulfillment of the requirements for the degree of

Bachelor of Technology in "Electrical Engineering"

By

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ODISHA, INDIA-769008

CERTIFICATE

This is to certify that the thesis entitled "**Design of single ended primary inductor DC-DC converter**", submitted by **Soumya Ranjan Behera(109ee0259) and Thabir Kumar Meher(109ee0282)** in partial fulfillment of the requirements for the award of **Bachelor of Technology** in **Electrical Engineering** during session 2012-2013 at National Institute of Technology, Rourkela. A bona fide record of research work carried out by them under my supervision and guidance.

The candidates have fulfilled all the prescribed requirements.

The Thesis which is based on candidates' own work, have not submitted elsewhere for a degree/diploma.

In my opinion, the thesis is of standard required for the award of a bachelor of technology degree in Electrical Engineering.

Place: Rourkela

Dept. of Electrical Engineering
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Assistant Professor

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ABSTRACT

In modern age different portable electronic equipment have benefited from a power converter is able to achieve high efficiency with a wide input and output voltage ranges with a small size. But conventional power converter can't maintain a wide operation range with high efficiency, especially if up-and-down voltage conversion has to be achieved. These characteristics can be obtained in a single ended primary inductor converter (SEPIC). Some limitation in conventional buck boost converter like inverted output ,pulsating input current, high voltage stress make it unreliable for wide range of operation. So to get rid of this SEPIC converter is used.

In this thesis ideal method of designing passive component of SEPIC is described, which is a DC-DC converter that provides a positive regulated output voltage from an input voltage. It also operates as a buck and boost converter. The SEPIC also has a simple controller that provides low noise operation. The experimental result of SEPIC is well studied by designing open loop hardware model and observing the waveforms in oscilloscope.

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CHAPTER 1:

Introduction

SEPIC is a DC to DC converter and is capable of operating in either step up or step down mode and widely used in battery operated equipment by varying duty cycle of gate signal of MOSFET. We can step up or step down voltage .For duty cycle above 0.5 it will step up and below 0.5, it will step down the voltage to required value. Various conversion topologies like buck, boost, buck-boost are used to step up or step down voltage. Some limitation like pulsating input and output current, inverted output voltage, in case of buck converter floating switch make it unreliable for different application. So it is not easy for conventional power converter design to maintain high efficiency especially when it step or step down voltage. All these characteristics are obtained in SEPIC DC to DC power conversion. Different designs are used using active and passive components. Non- inverted output ,low equivalent series resistance(ESR) of coupling capacitor minimize ripple and prevent heat built up which make it reliable for wide range of operation.

CHAPTER 2:

2.1: BASICS OF SEPIC CONVERTER

The basic converter we see in our day to-day life is buck converter. It is so called, because it only step down the input voltage .the output is given by

$$V_o=DV_s \tag{2.1}$$

Where V_o=output voltage

V_{IN}=input voltage

D=duty cycle

By interchanging input and output we get boost converter .which only step up voltage, hence its name boost. The output is always greater than input, but main problem is to get step up and step down voltage from a single device depending on output. We can use two cascaded converters (a buck and a boost).but for this two separate controller and separate switch are required. So it is not the good solution .Buck-boost converter can give required output but here output is inverting .These converters have more component stresses, component sizes and lesser efficiency. To reduce the losses caused by high voltages, a circuit with buck-boost conversion characteristics, small energy storage element required and smaller inductor size is desired .but inductor should not be so less ,such that ripple current is high.

Thus, the optimum converter however should have low component stresses, low energy storage requirements and size and efficiency performance comparable to the boost or the buck converter. One converter that provided required output is the SEPIC (single ended

primary inductor converter) converter.by varying duty cycle of gate signal of MOSFET we can vary the output. If duty cycle is greater than 50%, it will step up.so it is called as boost converter. if duty cycle is below 50% it will step down the voltage and it operate as buck converter. Another advantage of this converter is it provides a positive regulated output voltage from an input voltage that varies from above to below the output voltage. It function as both like a buck and boost converter, the SEPIC also has minimal active components, a simple controller that provide low noise operation.

2.2 : CIRCUIT OPERATION

Single-ended primary inductor converter (SEPIC) is a type of DC-DC converter, that allows the voltage at its output to be more than, less than, or equal to that at its input. The output voltage of the SEPIC is controlled by the duty cycle of the MOSFET. A SEPIC is similar to a traditional buck-boost converter, but has advantages of having non-inverted output, by means of coupling energy from the input to the output is via a series capacitor. When the switch is turned off output voltage drops to 0 V. SEPIC is useful in applications like battery charging where voltage can be above and below that of the regulator output.

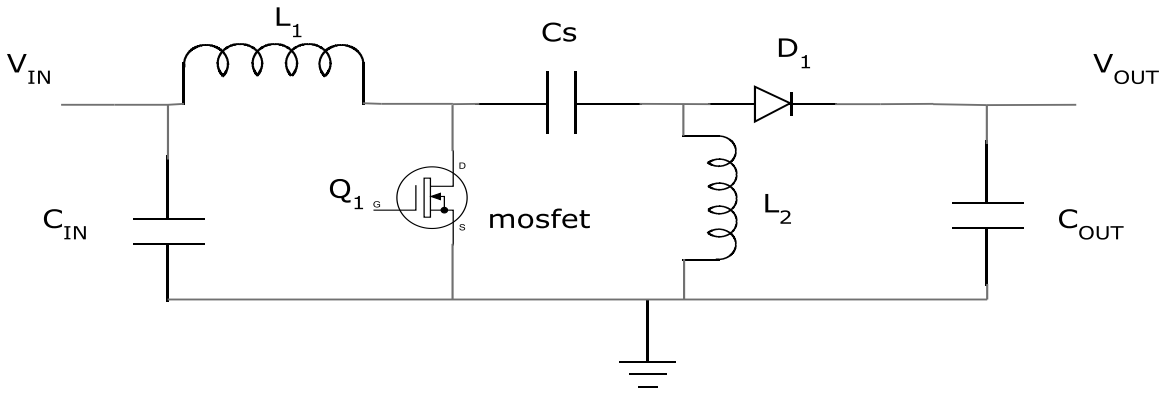


Figure.2.1. Circuit diagram of SEPIC Converter

2.2. A: CONTINUOUS CONDUCTION MODE

A SEPIC is said to be in continuous-conduction mode if the current through the inductor L_1 never go down to zero. During a SEPIC's steady-state operation, the average voltage across capacitor C_s (V_{Cs}) is equal to the input voltage (V_{IN}). Because capacitor C_s blocks direct current, the average current across it (I_{Cs}) is zero, making inductor L_2 the only source of load current. Hence the average current through inductor L_2 is the same as the average load current and hence independent of the input voltage. Looking at average voltages, the following can be written:

$$V_{IN}=V_{L1}+V_{Cs}+V_{L2} \tag{2.2}$$

Because the average voltage of V_{Cs} is equal to V_{IN}

$$V_{L1} = -V_{L2.} \tag{2.3}$$

For this reason, the two inductors can be wound on the same core. Since the voltages are the equal in magnitude, their mutual inductance effect will be zero. Here it is assumed that the polarity of the coil is correct. As the voltages are the equal in magnitude, the ripple currents of the two inductors will be equal in magnitude. The average currents can be summed as follows:

$$I_{D1}= I_{L1} - I_{L2} \tag{2.4}$$

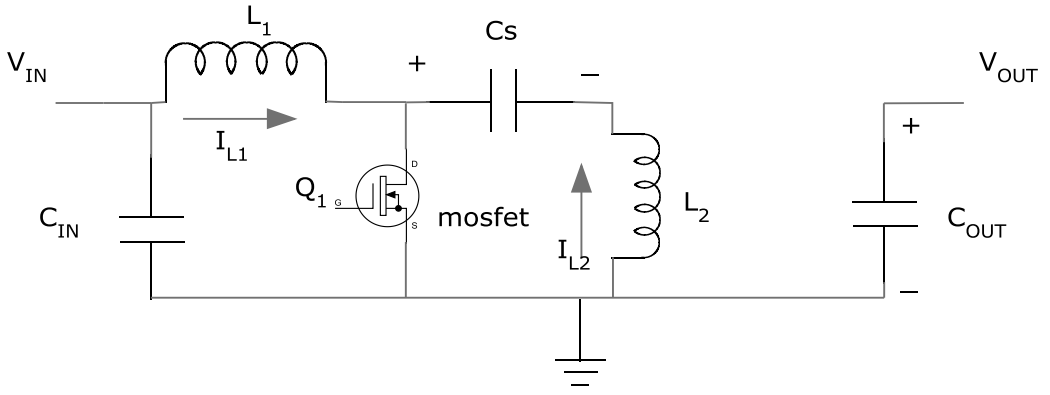


Figure 2.2. SEPIC on state (continuous conduction mode)

When switch Q_1 is turned on, current I_{L1} increases and the current I_{L2} increases in the negative direction. The energy to increase the current I_{L1} comes from the input source. Since Q_1 is a short while closed, and the instantaneous voltage V_{Cs} is approximately V_{IN}, the voltage V_{L2} is approximately $-V_{IN}$. Therefore, the capacitor Cs supplies the energy to increase the magnitude of the current in I_{L2} and thus increase the energy stored in L_2.

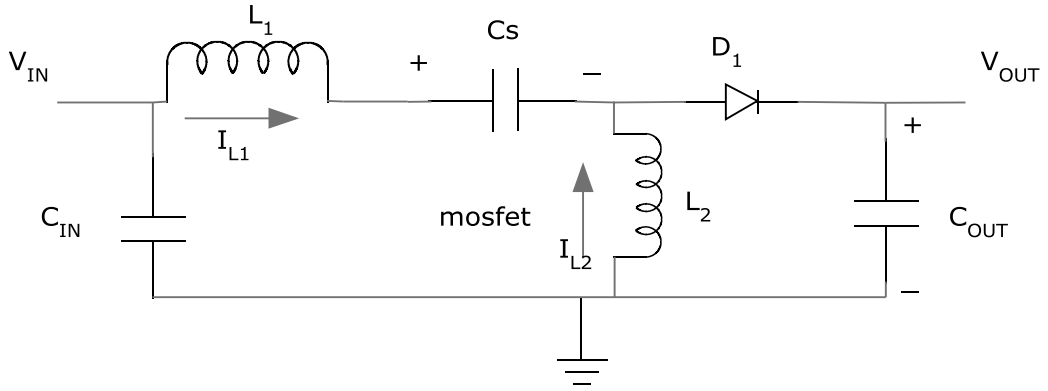


Figure 2.3. SEPIC Off state (Continuous conduction mode)

When switch Q_1 is turned off, the current I_{Cs} becomes the same as the current I_{L1}, as the inductors will not allow instantaneous changes in current. Current I_{L2} will continue in the negative direction, in fact it never reverse direction. It can be seen from the diagram that a negative I_{L2} will add to the current I_{L1} to increase the current delivered to the load. By Using Kirchhoff's Current Law

$$I_{D1} = I_{Cs} - I_{L2}. \tag{2.5}$$

So while Q_1 is off, power is delivered to the load from both L_2 and L_1. Coupling capacitor (C_s), is charged by L_1 during this off cycle, and will recharge L_2 during the on cycle. The boost/buck capabilities of the SEPIC are possible because of capacitor C_s and inductor L_2. Inductor L_1 and switch Q_1 create a standard boost converter, which generates a voltage (V_{Q1}) that is higher than

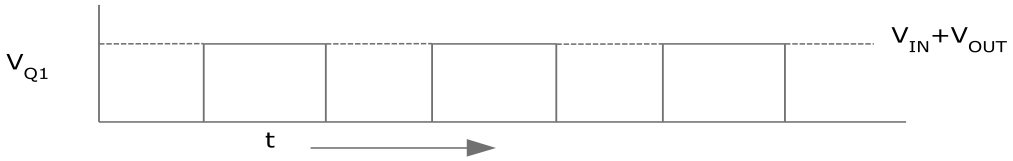
V_{IN}. Its magnitude is determined by the duty cycle of the switch Q_1. Since the average voltage across C_s is V_{IN}, the output voltage (V_{OUT}) is

$$V_{OUT}=V_{Q1}-V_{IN}. \quad (2.6)$$

If V_{Q1} is less than double of V_{IN}, then the output voltage will be less than the input voltage. If V_{Q1} will be greater than double of V_{IN}, then the output voltage will be greater than the input voltage.

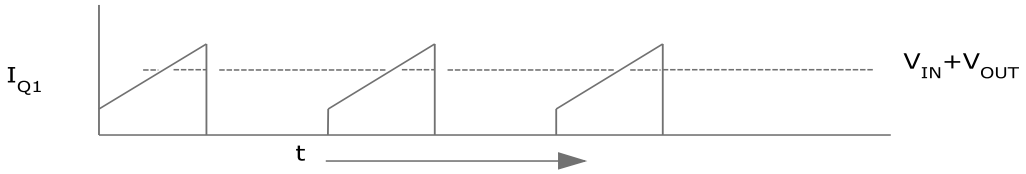
2.2.B:Expected waveforms:

Gate of MOSFET is triggered by squre wave pulse.MOSFET is a switching device,when it turns on voltage across the mosfet is zero means drain to source voltage is zero.When mosfet turns off supply voltage is build up across MOSFET. So according to on off of MOSFET a square wave pulse is obtaind across drain to source,that is also called voltage across MOSFET.



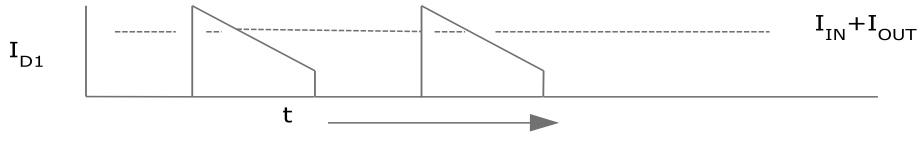
Fig(2.4)voltage across MOSFET vs Time

When MOSFET is turn on inductor1(L1) is start charging through MOSFET.So current through inductor and MOSFET start increasing.When MOSFET is turn off no current will flow through it.



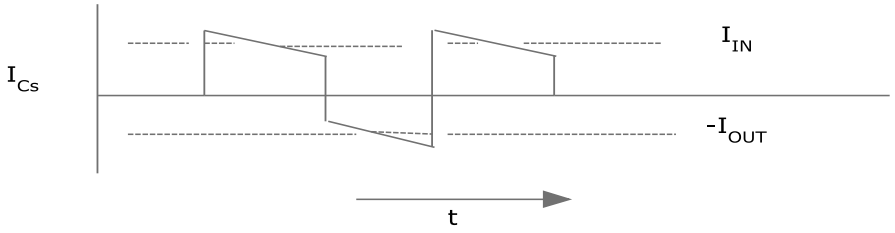
Fig(2.5)current through MOSFET vs Time

Diode is one of the switching device in SEPIC.It turns on ,when anode voltage is more that cathode voltage.It is unidirectional.During MOSFET turns on no current through diode as voltage across diode is negative.When MOSFET is turns off coupling capacitor start charging and inductor(L_2) discharging through diode .So initially current is at peak rate ,then current is slowly decreasing.



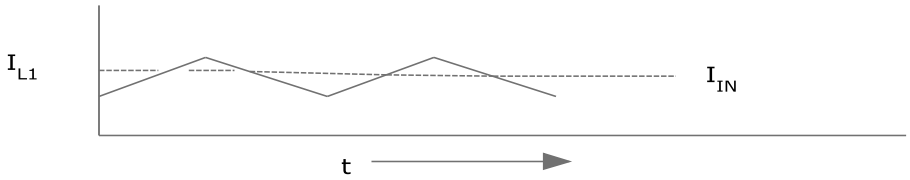
Fig(2.6)current through diode vs time

When capacitor starts charging current through it start decreasing and when it discharge,current through it starts increasing.so during T_{on} period coupling capacitor starts discharing through inductor ,so current in capacitor starts increasing ,but in a reverse direction.So current is negative. During T_{off} capacitor starts charging and current is in forward direction.



Fig(2.7)current through coupling capacitor vs time

When MOSFET is turn on inductor1(L1) is start charging through MOSFET.So current through inductor and MOSFET start increasing to a certain value till switch is turn off.When swith is turns off inductor(L_1) current starts decreasing.Current through both the inductor is same as both the inductor charging and discharging simultaneously.



Fig(2.8)current through inductor (L_1) vs time

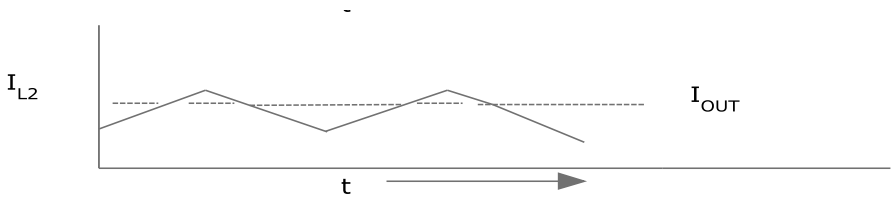


Figure (2.9).current through inductor(L_2) vs time

2.3:VOLT-SECOND BALANCING OF SEPIC

During the MOSFET turn on (Positive slope)

$$V_{IN} = V_{L1(ON)} \tag{2.7}$$

$$\frac{\Delta I_{L1}}{T_{ON}} = \frac{V_{L1(ON)}}{L_1} \tag{2.8}$$

During the MOSFET turn off (Negative slope)

$$V_{L1(OFF)} = V_{Cs} + V_{OUT} - V_{IN} \tag{2.9}$$

$$\frac{\Delta I_{L1(OFF)}}{T_{OFF}} = \frac{V_{Cs} + V_{OUT} - V_{IN}}{L_1} \tag{2.10}$$

Equating the above equations

$$V_{L1\,(ON)} * T_{ON} = V_{L1\,(OFF)} * T_{OFF} \tag{2.11}$$

For Inductor L2 during turn on of MOSFET voltage across inductor L_2 is $V_{Cs.}$

$$\frac{\Delta I_{L2}}{T_{ON}} = \frac{V_{Cc}}{L_2} \tag{2.12}$$

During MOSFET turn off voltage across output voltage is equal to voltage across L_2

$$\frac{\Delta I_{L2}}{T_{OFF}} = \frac{V_{OUT}}{L_2} \tag{2.13}$$

Equating the above equation

$$T_{ON} * V_{L2\,(ON)} = T_{OFF} * V_{L2(OFF)} \tag{2.14}$$

CHAPTER 3

DESIGN OF OPEN LOOP SEPIC CONVERTER:

3. DESIGN SPECIFICATION:

A SEPIC is used in various applications in power electronics field. Given below specification are used for charging a battery

Input voltage (V_{IN}) =12 V

Output voltage (V_{OUT}) =10-14V

Output ripple current=20-30% of load current

Output ripple voltage=3% of load voltage

Switching frequency (F_s) =30 KHz

3.2 POWER STAGE FILTER DESIGN FROM RIPPLE SPECIFICATIONS:

A. INDUCTOR SELECTION:

For determining the inductance peak to peak current is approximately 25% of the maximum input current, at minimum input voltage. The ripple current flowing in equal value in inductor L1 and L_2 is given by

$$\Delta I_1 = I_{IN} * 25\% = \frac{I_{OUT} * V_{OUT}}{V_{IN}} * 25\% \qquad (3.1)$$

The inductor value calculated by

$$L_1 = L_2 = L = \frac{V_{IN}}{\Delta I_L} * D_{MIN} \quad (3.2)$$

The peak current in inductor is given by

$$I_{L1(peak)} = I_{OUT} * \frac{V_{OUT} + V_D}{V_{IN(MIN)}} * (\frac{1 + 25\%}{2}) \quad (3.3)$$

$$I_{L2(peak)} = I_{OUT} * (\frac{1 + 25\%}{2}) \quad (3.4)$$

Here maximum input current=1.25 A

From (3.1),(3.2),(3.3)and (3.4)

$$L_1 = L_2 = \frac{12}{.25} * 0.464 = 0.866\text{mH}$$

$$I_{L1(peak)} = 1 * \frac{14 + .4}{12} * (\frac{1 + 25\%}{2}) = 1.35 \text{ A}$$

$$I_{L2(peak)} = 1 * (\frac{1 + 25\%}{2}) = 1.125 \text{ A}$$

B**: COUPLING CAPACITOR SELECTION:**

The selection of coupling capacitor Cs depends on the RMS current and is given by

$$I_{cs(rms)} = I_{OUT} * \sqrt{\frac{V_{OUT} + V_d}{V_{IN(MIN)}}} \quad (3.10)$$

The coupling capacitor must be rated for a large RMS current relative to output power. This property makes the SEPIC much better suited to lower power application, here the RMS current through the capacitor is relatively small. The voltage rating of it must be greater than the maximum input voltage. Electrolytic capacitor work well for through whole application ,where the size is not limited and they can accommodate the required RMS current rating.

The peak to peak ripple voltage on Cs is

$$\Delta V_{cs} = \frac{I_{OUT} * D_{MAX}}{c_s * F_{sw}} \quad (3.11)$$

A capacitor that meets the RMS current requirement would mostly produce small ripple on Cs. Hence the peak voltage is typically close to input voltage

from (3.10),(3.11):

RMS current through coupling capacitor =I_{Cs}=1.2 A

Peak to peak reverse voltage on Cs=1.81V

C: OUTPUT CAPACITOR SELECTION:

In a SEPIC converter, when the power switch Q_1 is turned on ,the inductor is charging and the output current is supplied by the out-put capacitor.as a result capacitor sees large ripple currents. Thus the selected out-put capacitor must be capable of handling maximum RMS current in out-put capacitor is

$$I_{OUT(rms)} = I_{OUT} * \sqrt{\frac{V_{OUT} + V_d}{V_{IN(MIN)}}} \tag{3.12}$$

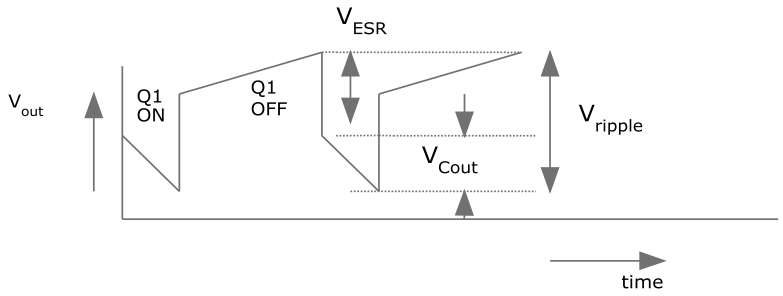


Fig.3.1. Output Ripple Voltage

The ESR, ESL and the buck capacitance of output capacitor directly control the output ripple. As shown in figure, we assume half of the ripple is cause by the ESR and where other half is caused by amount of capacitance. So

$$\text{ESR} \leq \frac{V_{ripple} * 0.5}{I_{L1(peak)} + I_{L2(peak)}} \tag{3.13}$$

$$C_{OUT} \geq \frac{I_{OUT} * D}{V_{ripple} * 0.5 * F_{sw}} \tag{3.14}$$

By calculating using (3.12), (3.13) and (3.14)

RMS current in output capacitor=$I_{C\,(OUT)}$=1.2 A

$\text{ESR} \leq 0.072$

$C_{OUT} \geq 151.3$ UH

D: INPUT CAPACITOR SELECTION:

Input current waveform is continuous and triangular. The inductor ensure that the input capacitor sees fairly low ripple current. The RMS current in the input capacitor is given by

$$I_{CIN(rms)} = \frac{\Delta I_L}{\sqrt{12}} \qquad (3.15)$$

Input capacitor be capable of handling the RMS current. The input capacitor is not much important in a SEPIC application, a 10 uf or higher value, good quality capacitor would prevent impendence interaction with the input supply

So from (3.15) RMS current in input capacitor is :

$I_{CIN(rms)}$ =0.072 A

3.3: SWITCH SELECTION:

There is two switching element in SEPIC. That is diode and MOSFET.

3.3.A: POWER MOSFET SELECTION:

The parameter governing the selection of the MOSFET are :

Minimum threshold voltage $V_{TH\,(MIN)}$

The on resistance $R_{DS\,(ON)}$

Gate drain charge Q_{GD}

Maximum drain to source voltage = $V_{DS(MAX)}$

The peak switch voltage is equal to $V_{IN} + V_{OUT}$ (3.5)

The peak switch current is given by

$$I_{Q1(peak)} = I_{L1(peal)} + I_{L2(peak)} \quad (3.6)$$

The RMS current through MOSFET is given by

$$I_{Q1(rms)} = I_{OUT} \sqrt{\frac{(V_{OUT} + V_{IN(MIN)}) * V_{OUT}}{V_{IN(MIN)}^{2}}} \quad (3.7)$$

The MOSFET power loss P_{Q1} is approximately:

$$P_{Q1} = I_{Q1}^{2} * R_{DS(ON)} * D_{MAX} + (V_{IN(MIN)} + V_{OUT}) * I_{Q1(peak)} * \frac{Q_{GD} * F_{sw}}{I_G} \quad (3.8)$$

P_{Q1} includes conduction loss and switching loss .The $R_{DS(ON)}$ value should be selected at maximum operating junction temperature and is typically given in MOSFET data sheet. conduction loss plus switching loss never exceed the package rating or exceed the overall thermal budget

From (3.5),(3.6) and (3.7) :

Peak swing of voltage= $V_{IN} + V_{OUT}$ = 26 V

Peak swing current = $I_{Q1(peak)} = I_{L1(peal)} + I_{L2(peak)}$ =2.475A

RMS current through switch= $I_{Q1(rms)}$ = 1.2638 A

3.3.B: DIODE SELECTION:

The output diode must be selected to handle the peak current and the reverse voltage. In a SEPIC ,the diode peak current is the same as the switch peak current $I_{Q1\ peak}$ .The minimum peak reverse voltage the diode should withstand is

$$V_{RD1} = V_{IN(\max)} + V_{OUT(\max)} \tag{3.9}$$

The power dissipation in diode is equal to the output current multiplied by the forward voltage drop of the diode. Schottky diode is used to minimize the switching loss.

From (3.9) :

Diode peak current =2.475A

Minimum peak reverse voltage the diode must withstand is $=V_{RD1}$

$$=V_{IN(\max)} + V_{OUT(\max)} = 26\text{V}$$

CHAPTER 4:

RESULTS

4.1 OPEN LOOP SIMULATION RESULT:

Given below is circuit diagram for matlab simulation of SEPIC converter. The aim is to measure output voltage, current waveform in both inductor, capacitor current.

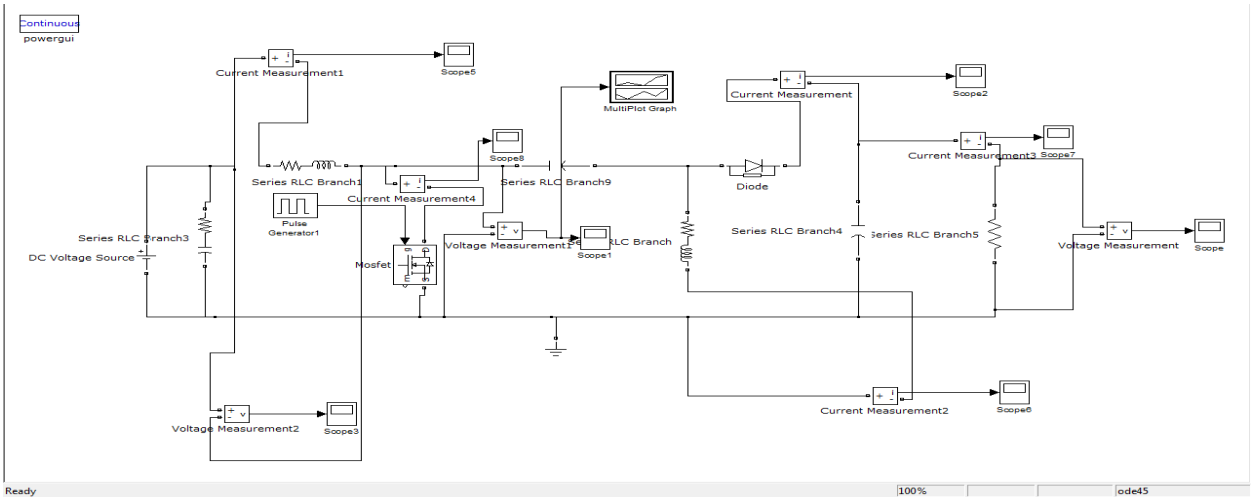


fig 4.1 circuit diagram of simulation of SEPIC

Given below is the waveform of output voltage vs time at 50% duty cycle. The aim is to know about transient and steady state behavior.

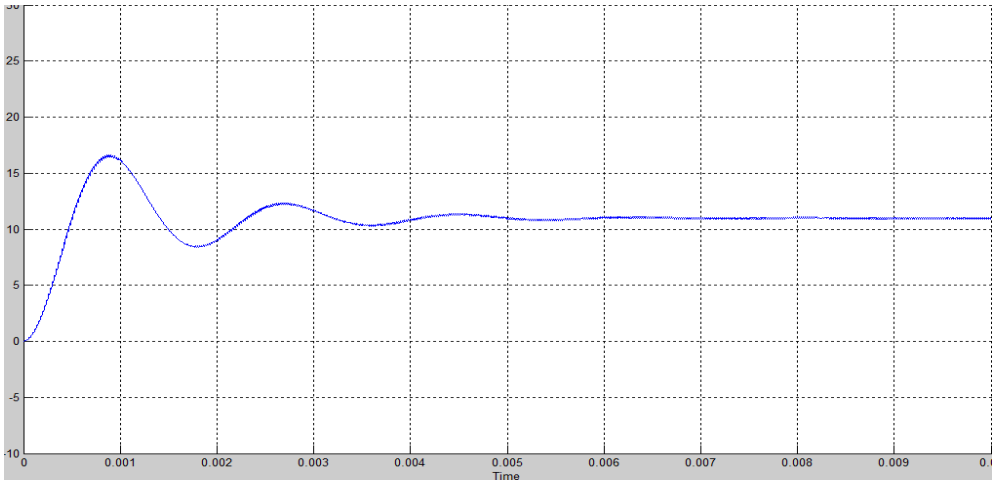


Fig 4.2 V_{OUT}(output voltage) vs Time

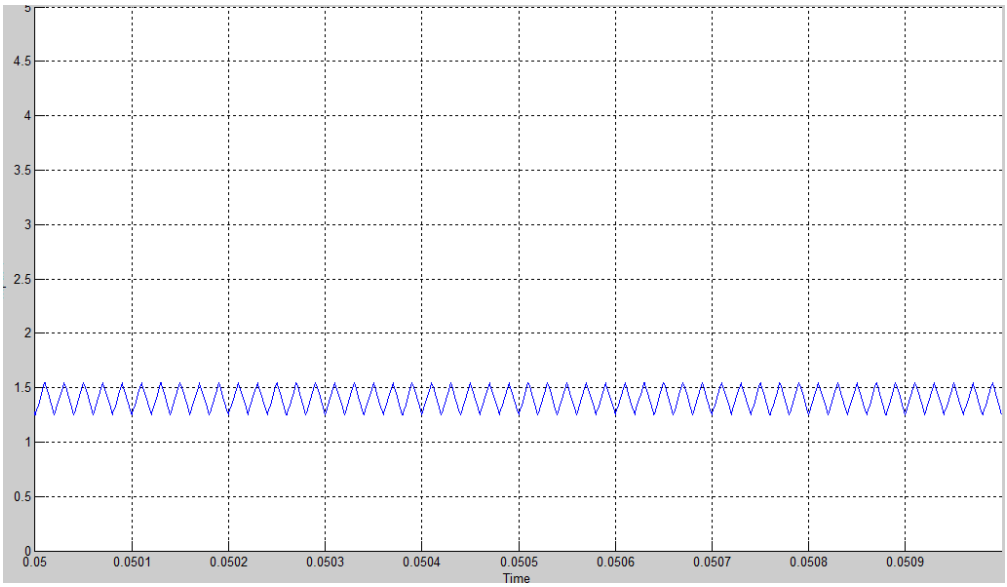


Fig 4.3 I_{L1}(current through inductor l_1) vs Time

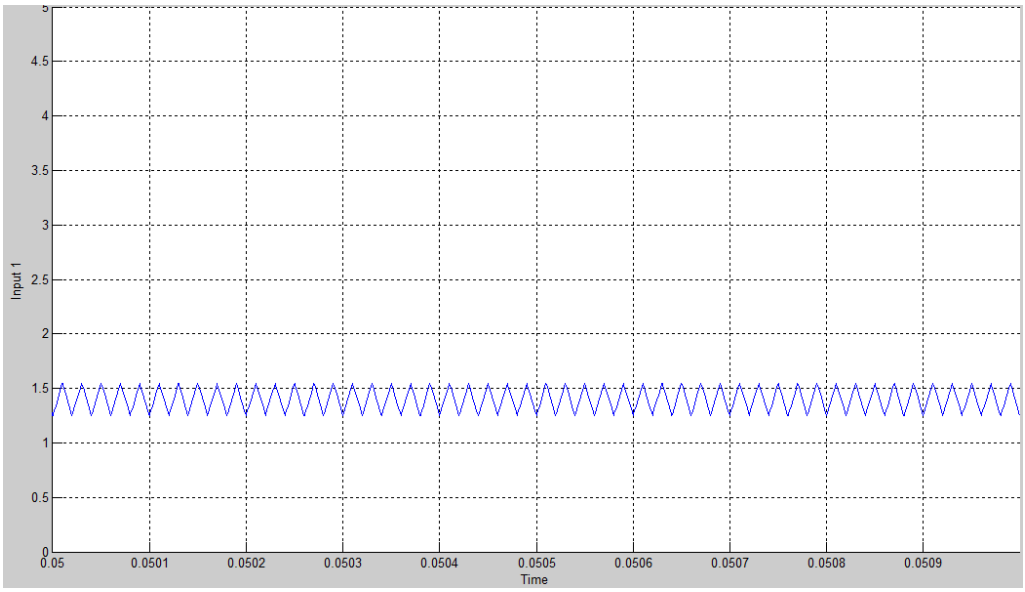
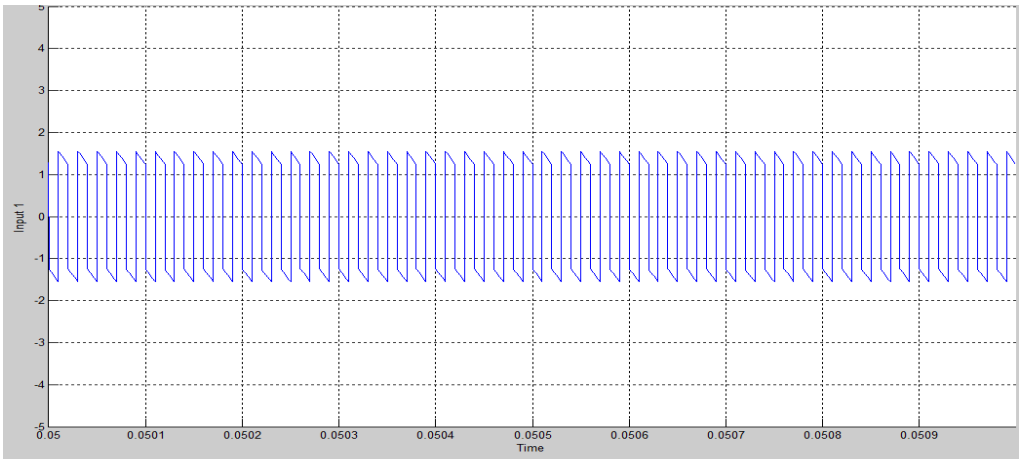


Fig 4.4 I_{L2}(current through inductor l_2) vs Time



Fig(4.5) current through coupling capacitor vs time

4.2 Closed loop simulation of SEPIC converter:

For close loop system we have to know the transfer function of the system.

During $0<t<DT_s$ interval(when MOSFET is turn on) in fig(2.2)

$$V_{IN} + L_1 \frac{dI_{L1}}{dt} = 0 \Rightarrow \frac{dI_{L1}}{dt} = -\frac{V_{IN}}{L_1} \tag{4.1}$$

$$L_2 \frac{dI_{L2}}{dt} - V_{Cs} = 0 \Rightarrow \frac{dI_{L2}}{dt} = \frac{V_{Cs}}{L_2} \tag{4.2}$$

$$C_{CS} \frac{dV_{CS}}{dt} + I_{L2} = 0 \Rightarrow \frac{dV_{CS}}{dt} = -\frac{I_{L2}}{C_S} \tag{4.3}$$

$$C_{OUT} \frac{dV_{C(OUT)}}{dt} + \frac{V_{COUT}}{R} = 0 \Rightarrow \frac{dV_{C(OUT)}}{dt} = -\frac{V_{COUT}}{RC_{OUT}} \tag{4.4}$$

During $DT_s<t<(1-D)T_s$ interval (when MOSFET is turns off) in fig(2.3)

$$V_{IN} + L_1 \frac{dI_{L1}}{dt} + V_{CS} + V_{C(OUT)} = 0 \Rightarrow \frac{dI_{L1}}{dt} = -\frac{V_{CS1}}{L_1} - \frac{V_{C(OUT)}}{L_2} + \frac{V_{IN}}{L_1} \tag{4.5}$$

$$L_2 \frac{dI_{L2}}{dt} + V_{C(OUT)} = 0 \Rightarrow \frac{dI_{L2}}{dt} = -\frac{V_{C(OUT)}}{L_2} \tag{4.6}$$

$$C_S \frac{dV_{C(S)}}{dt} - i_1 = 0 \Rightarrow \frac{dV_{C(S)}}{dt} = \frac{I_{L1}}{C_S} \tag{4.7}$$

$$C_{OUT} \frac{dV_{C(OUT)}}{dt} - I_{L1} - I_{L2} + \frac{V_{C(OUT)}}{R} = 0 \Rightarrow \frac{dV_{C(OUT)}}{dt} = -\frac{V_{C(OUT)}}{RC_{OUT}} + \frac{I_{L1}}{C_{OUT}} + \frac{I_{L2}}{C_{OUT}} \tag{4.8}$$

So when MOSFET is on state space equation is

$$\begin{bmatrix} \frac{dI_{L1}}{dt} \\ \frac{dI_{L2}}{dt} \\ \frac{dV_{C(S)}}{dt} \\ \frac{dV_{C(OUT)}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & 0 \\ 0 & -\frac{1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & -1/RC_2 \end{bmatrix} \begin{bmatrix} I_{L1} \\ I_{L2} \\ V_{C(S)} \\ V_{C(OUT)} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} \begin{bmatrix} V_{IN} \end{bmatrix} \tag{4.9}$$

So $A_1 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & 0 \\ 0 & -\frac{1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & -1/RC_2 \end{bmatrix}$ (4.10)

$B_1 = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix}$ (4.11)

When MOSFET is off, the state space equation is

$$\begin{bmatrix} \frac{dI_{L1}}{dt} \\ \frac{dI_{L2}}{dt} \\ \frac{dV_{C(S)}}{dt} \\ \frac{dV_{C(OUT)}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} & -\frac{1}{L_1} \\ 0 & 0 & 0 & -\frac{1}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ \frac{1}{C_2} & \frac{1}{C_2} & 0 & -1/RC_2 \end{bmatrix} \begin{bmatrix} I_{L1} \\ I_{L2} \\ V_{C(S)} \\ V_{C(OUT)} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} \begin{bmatrix} V_{IN} \end{bmatrix} \quad (4.12)$$

Where

$$A_2 = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} & -\frac{1}{L_1} \\ 0 & 0 & 0 & -\frac{1}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ \frac{1}{C_2} & \frac{1}{C_2} & 0 & -1/RC_2 \end{bmatrix} \quad (4.13)$$

$$B_2 = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (4.14)$$

$$V_{OUT} = [0 \quad 0 \quad 0 \quad 1] \begin{bmatrix} I_{L1} \\ I_{L2} \\ V_{C(S)} \\ V_{C(OUT)} \end{bmatrix} \quad (4.15)$$

so

$$C = [0 \quad 0 \quad 0 \quad 1] \quad (4.16)$$

For state space average model we have to consider

$A=DA_1+ (1-D) A2$
(4.17)

$B=DB_1+ (1-D) B2$
(4.18)

For SEPIC converter the large signal input to output relationship and associated large signal state relationship can be represented as:

$$\frac{V_{OUT}}{V_{IN}} = \frac{D}{1-D}$$
$$I_{L1} = \frac{D^2 V_{IN}}{(1-D)^2 R}$$
$$V_{C(S)} = V_{IN}$$
$$I_{L2} = -\frac{DV_{IN}}{(1-D)R}$$
$$V_{C(OUT)} = \frac{DV_{IN}}{(1-D)} \quad (4.19)$$

So Duty cycle to output relationship can be expressed as

$$\frac{V_{OUT}}{D}(S) = \frac{A_1 S^3 + A_2 S^2 + A_3 S + A_4}{A_5 S^4 + A_6 S^3 + A_7 S^2 + A_8 S + A_9} V_{IN} \quad (4.20)$$

$$A_1 = -L_1 C_S L_2 D$$
$$A_2 = L_1 C_S R D^2$$
$$A_3 = -D^2 L_1$$
$$A_4 = D^2 R$$
$$A_5 = (1-D)^2 L_1 C_S L_2 C_{OUT} R$$
$$A_6 = (1-D)^2 L_1 L_2 C_S$$
$$A_7 = (1-D)^2 R(L_1 C_S (1-D)^2 + L_2 C_{OUT} (1-D)^2 + L_2 C_S (1-D)^2 + L_1 C_{OUT} D^2)$$
$$A_8 = (1-D)^2 (L_2 (1-D)^2 + L_1 D^2)$$
$$A_9 = (1-D)^4 R$$

Input to output voltage relationship can be described as

$$\frac{V_{OUT}}{V_{IN}}(S) = \frac{B_1 S^2 + B_2}{B_3 S^4 + B_4 S^3 + B_5 S^2 + B_6 S + B_7} V_{IN} \tag{4.21}$$

Where

$$A_1 = L_2 C_S R(1-D)$$
$$A_2 = RD(1-D)$$
$$A_3 = L_1 L_2 C_S C_{OUT} R$$
$$A_4 = L_1 L_2 C_S$$
$$A_5 = R(L_1 C_1 (1-D)^2 + L_2 C_{OUT}(1-D)^2 + L_1 C_{OUT} D^2 + L_2 C_S (1-D)^2)$$
$$A_6 = L_1 D^2 + L_2 (1-D)^2$$
$$A_7 = R(1-D)^2$$

Put the calculated value of inductance, capacitance and resistance in equation (4.20) and (4.21) respectively. We consider duty cycle is 0.5.So

$$\frac{V_{OUT}}{D}(S) = \frac{-3.74*10^{-12} S^3 + 38.97*10^{-9} S^2 - 0.2165*10^{-3} S + 4.5}{5400*10^{-18} S^4 + 1.87*10^{-12} S^3 + 331.24*10^{-9} S^2 + 0.108S + 1.125} V_{IN} \tag{4.22}$$

$$\frac{V_{OUT}}{V_{IN}}(S) = \frac{77.94*10^{-9} S^2 + 4.5}{21600*10^{-18} S^4 + 7.48*10^{-12} S^3 + 1324*10^{-19} S^2 + .432S + 4.5} V_{IN} \tag{4.23}$$

For better transient and steady state response of the system a feedback path given to the system. We are using PID controller for feedback..Because propotional controller reduce the rise time, hense transient response is better.we are selecting only PI controller here.Integral conroller reduce the steady state error ,so that a better ouput response will come.In close loop we can change the output by changing the reference signal.

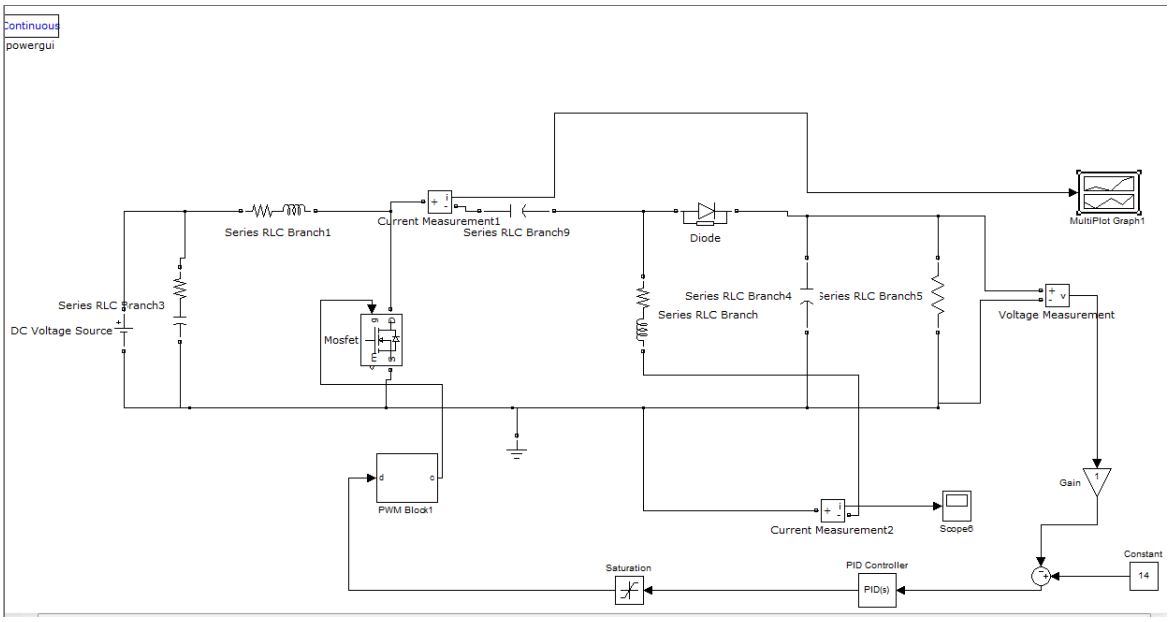


Fig4.6 simulation of closed of SEPIC converter

When reference of 8 volt is given the response of SEPIC converter is given below. Here it act as buck converter.

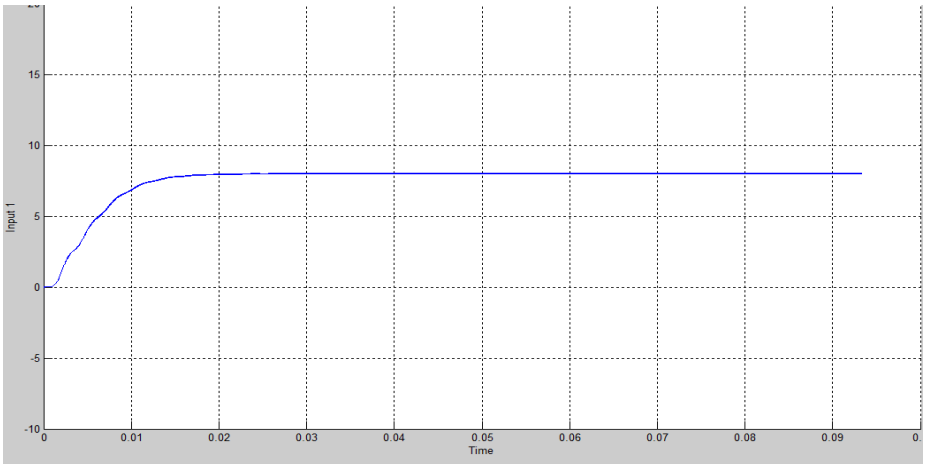


Fig 4.7 SEPIC as buck converter (output voltage vs time)

When a reference of 14 volt is given the response of SEPIC converter is given below. Here it act as buck converter.

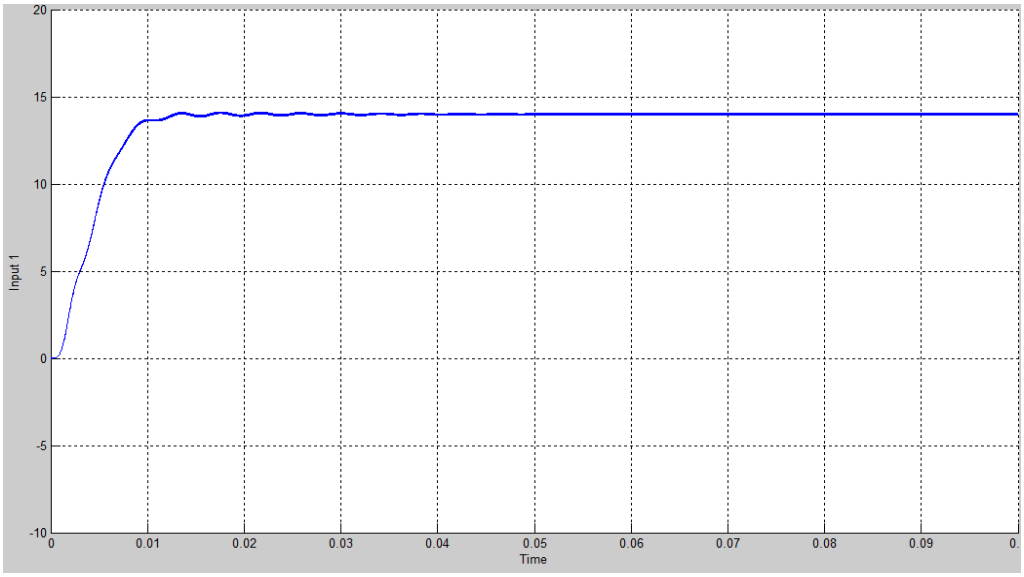


Fig 4.8 SEPIC as boost converter(output voltage vs time)

The inductor current (L1) at steady state is given below. The value fluctuates between 1.25 to 1.35 ampere.

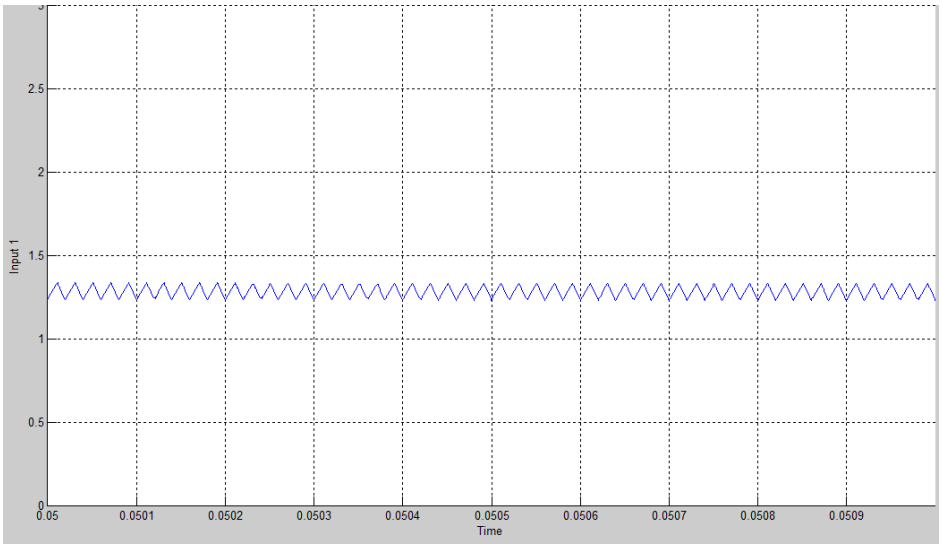


Fig 4.9 Inductor current I_{l1} vs time

Current through coupling capacitor is given below. During on state of MOSFET the current is positive while during off state of MOSFET it is negative.

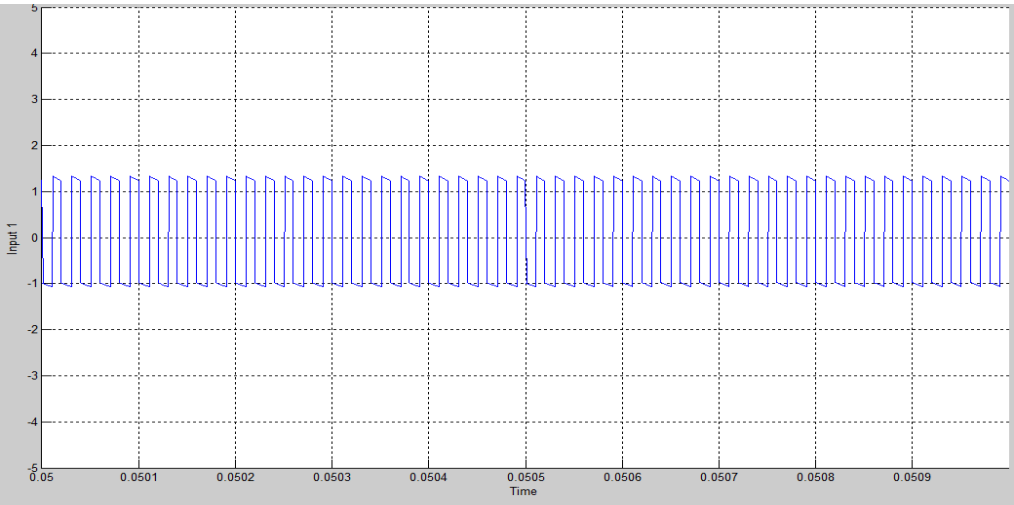


Fig 4.10 capacitor current(I_c) vs time

4.3 EXPERIMENTAL RESULTS:

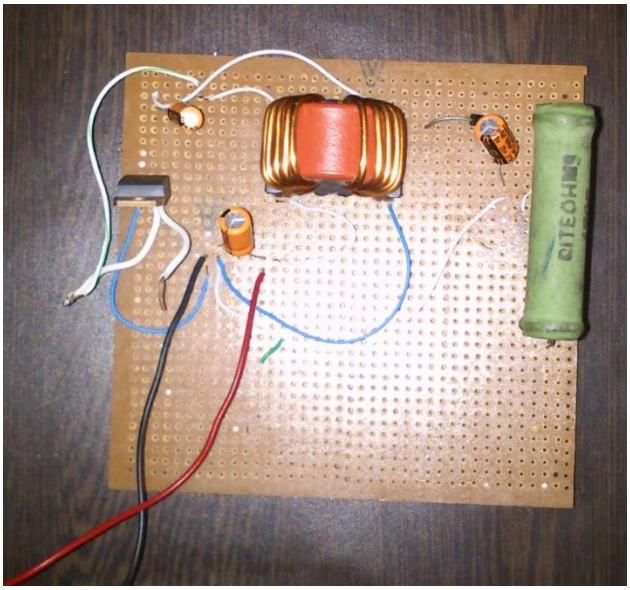
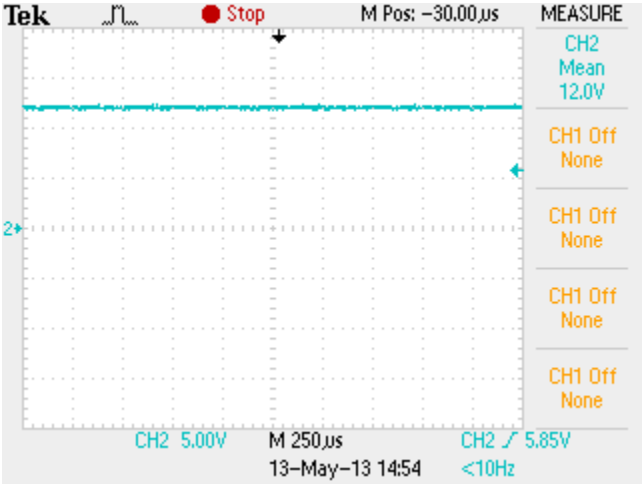
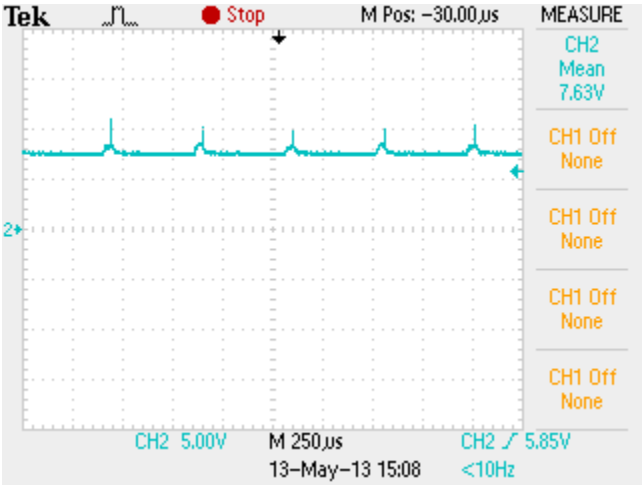


Fig 4.11 Hardware of SEPIC

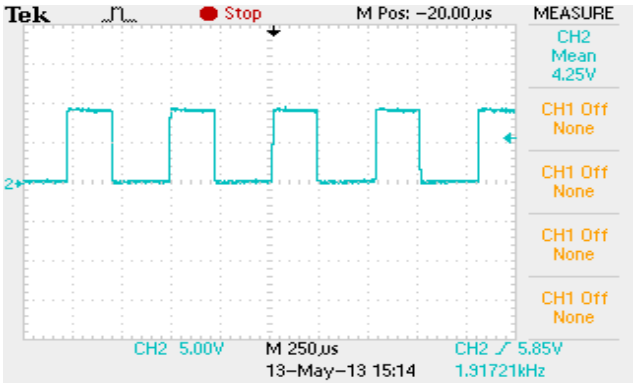
4.3.A. SEPIC AS BUCK CONVERTER



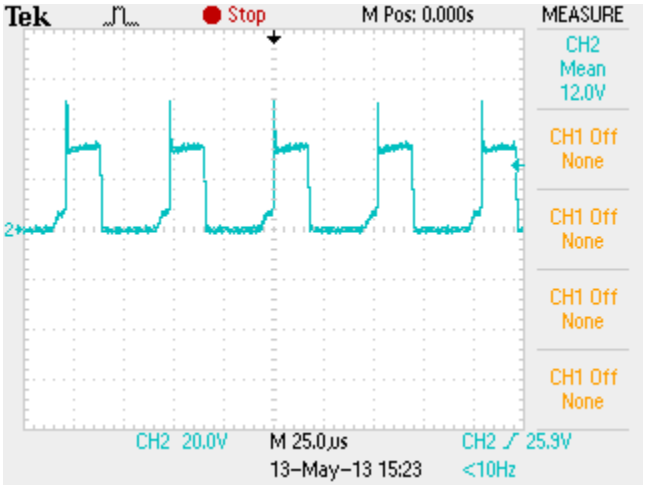
Fig(4.12) input supply voltage vs time



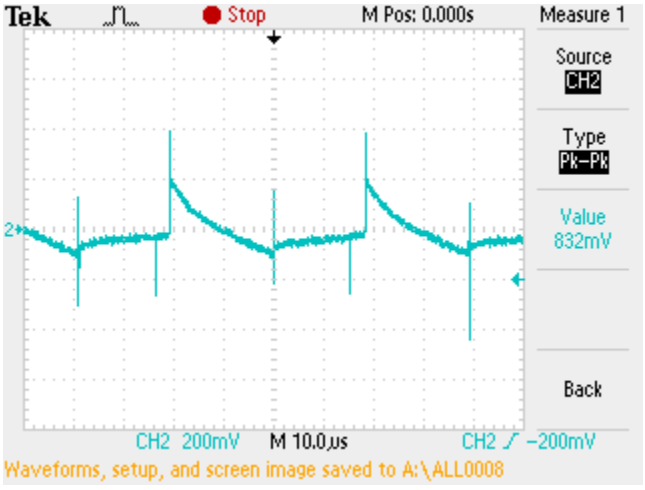
Fig(4.13) Output voltage vs time



Fig(4.14)Gate signal to MOSFET vs time

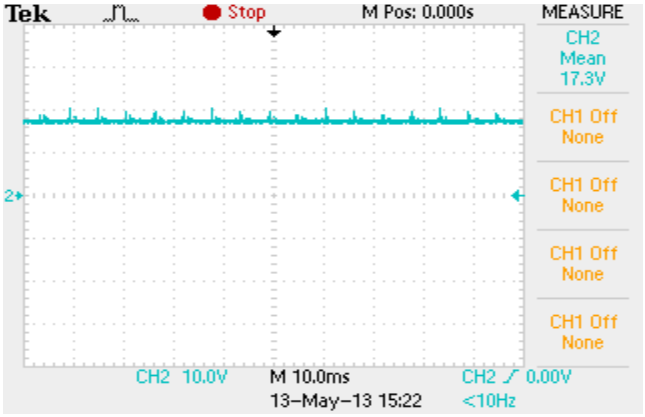


Fig(4.15) Drain to source voltage of MOSFET vs time

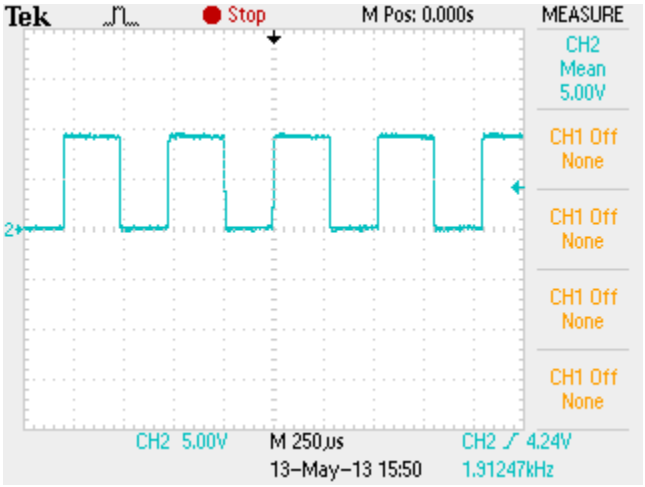


Fig(4.16)output capacitor ripple voltage vs time

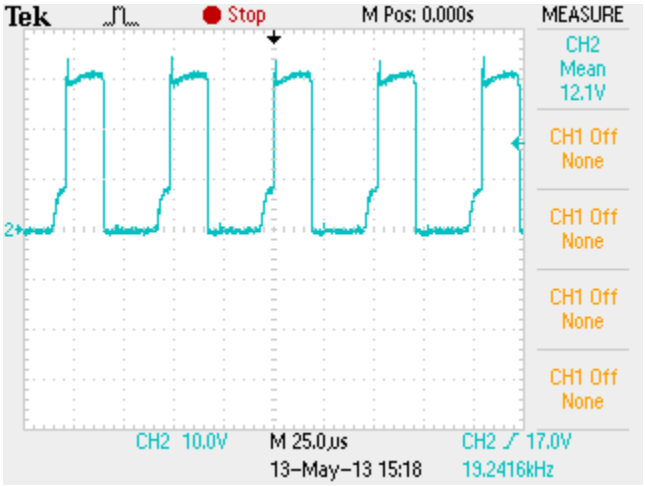
4.3.B SEPIC AS BOOST CONVERTER



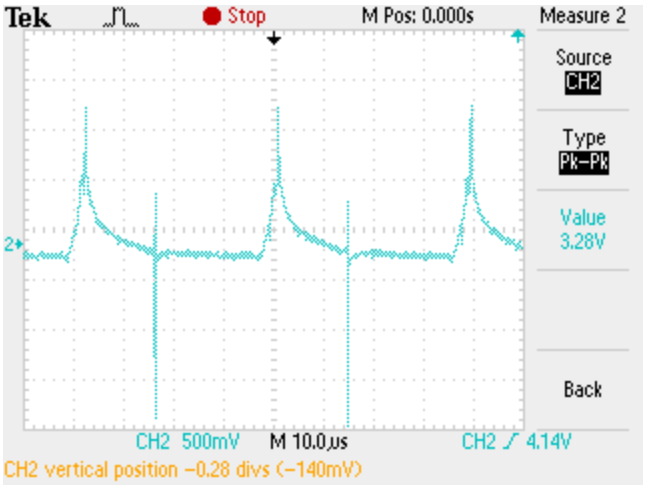
Fig(4.17) Output voltage vs time



Fig(4.18)Gate signal to MOSFET vs time

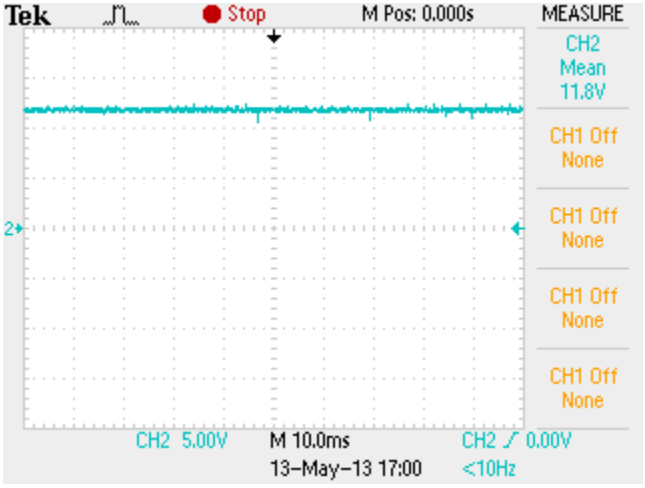


Fig(4.19) Drain to source voltage of MOSFET vs time

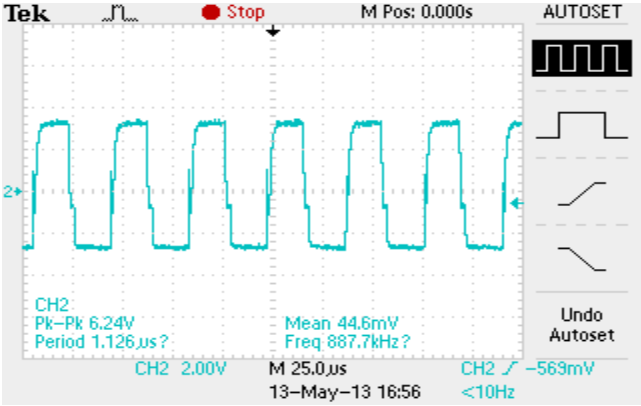


Fig(4.20)Output capacitor ripple voltage vs time

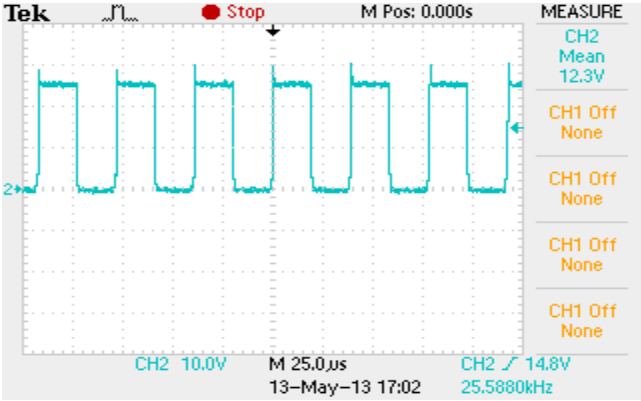
4.3.C SEPIC OUTPUT AT 50% DUTY CYCLE



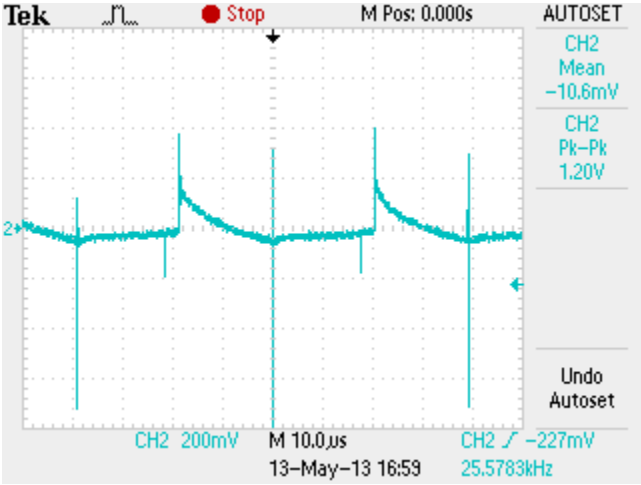
Fig(4.21) Output voltage vs time



Fig(4.22) Gate signal of MOSFET vs time



Fig(4.23) Drain to source voltage of MOSFET vs time



Fig(4.24) Ripple voltage across output capacitor vs time

CHAPTER 5:

CONCLUSION

All the specification and values of passive components for designing of a SEPIC was determined. Matlab simulation using calculated parameters was performed in open loop and closed loop and corresponding waveforms were obtained. From simulation we observed that the output of closed loop system gives more accurate result than open loop system. Hardware design of SEPIC converter was done for open loop. It is observed by varying duty cycle output also changes, duty cycle above 50% it operate as a boost converter and below 50% it act like a buck converter.

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APPENDIX

MOSFET specification sheet: IRF640

V_{DS}	Drain to source voltage	200		V
Q_g	Gate charge total(4.5V)	70		nC
Q_{gd}	Gate charge to gate drain	39		nC
$R_{DS(on)}$	Drain to source on resistance	Vgs=10v	0.18	mΩ
Q_{GS}		13		nC