IMPLEMENTATION OF PWM BASED FIRING SCHEME FOR MULTILEVEL INVERTER USING MICROCONTROLLER

A PROJECT REPORT SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF BACHELOR OF TECHNOLOGY IN "ELECTRICAL ENGINEERING"

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CERTIFICATE

This is to certify that the work in the project report entitled ***"Implementation of PWM based Firing Scheme for multilevel Inverter using microcontroller"*** by **Bhabani Shankar Pattnaik(10502057), Debendra Kumar Dash(10502065), Joydeep Mukherjee(10502063)**, has been carried out under my supervision in partial fulfillment of the requirement for the degree of Bachelor of Technology in **"Electrical Engineering**" during session 2008-09 in the **Department of Electrical Engineering, National Institute of Technology, Rourkela** and this work has not been submitted elsewhere for a degree.

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We would like to thank our department for giving us the opportunity and platform to make our effort a successful one.

ABSTRACT

The power electronics device which converts DC power to AC power at required output voltage and frequency level is known as inverter. Inverters can be broadly classified into single level inverter and multilevel inverter. Multilevel inverter as compared to single level inverters have advantages like minimum harmonic distortion, reduced EMI/RFI generation and can operate on several voltage levels. A multi-stage inverter is being utilized for multipurpose applications, such as active power filters, static var compensators and machine drives for sinusoidal and trapezoidal current applications. The drawbacks are the isolated power supplies required for each one of the stages of the multiconverter and it's also lot harder to build, more expensive, harder to control in software.

This project aims at generation of carrier based PWM scheme using POD strategy through the means of an AT89C51 microcontroller. The salient features are: Firstly, Both the high frequency triangular carrier wave and the sinusoidal reference signal are being generated in the microcontroller. The digital to analog converter(DAC0808)is then employed for converting them into their analog signal forms An opamp based comparator then compares these two carrier & reference signals to give us the desired sinusoidal pulse width modulated signal as the required final-output. The PWM signal thus generated is then used as triggering pulses for the multilevel inverters.

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CHAPTER #1

INTRODUCTION

Ac loads require constant or adjustable voltages at their input terminals. When such loads are fed by inverters, it's essential that output voltage of the inverters is so controlled as to fulfill the requirements of AC loads. This involves coping with the variation of DC input voltage, for voltage regulation of inverters and for the constant volts/frequency control requirement. There are various techniques to vary the inverter gain. The most efficient method of controlling the gain (and output voltage) is to incorporate pulse-width modulation (PWM) control within the inverters. The carrier based PWM schemes used for multilevel inverters is one of the most straight forward methods of describing voltage source modulation realized by the intersection of a modulating signal (Duty Cycle) with triangular carrier wavefroms.The Alternative PWM strategies with differing phase relationships are:

- Alternate phase disposition (APOD): Every carrier wave form is in out of phase with its neighbor carrier by 180 degree.
- Phase Opposition Disposition (POD): All carrier waveforms above zero reference are in phase and are 180 degree out of phase with those below zero reference.
- Phase Disposition (PD): All carrier waveforms are in phase

1.1 PROJECT OUTLINE

This project aims at generation of carrier based PWM scheme using POD strategy through the means of an AT89C51 microcontroller. The salient features are:

- Firstly, both the high-frequency triangular carrier wave & the sinusoidal reference signal are being generated in the microcontroller.
- A digital to analog converter (DAC 0808) is then employed for converting them into their analog signal forms.
- An opamp(KF351) based comparator then compares these two carrier & reference signals to give us the desired sinusoidal pulse width modulated signal as the required final output

1.2 INVERTERS

A device that converts DC power into AC power at desired output voltage and frequency is called an Inverter. Phase controlled converters when operated in the inverter mode are called line commutated inverters. But line commutated inverters require at the output terminals an existing AC supply which is used for their commutation. This means that line commutated inverters can't function as isolated AC voltage sources or as variable frequency generators with DC power at the input. Therefore, voltage level, frequency and waveform on the AC side of the line commutated inverters can't be changed. On the other hand, force commutated inverters provide an independent AC output voltage of adjustable voltage and adjustable frequency and have therefore much wider application.

Inverters can be broadly classified into two types based on their operation:

- Voltage Source Inverters(VSI)
- Current Source Inverters(CSI)

Voltage Source Inverters is one in which the DC source has small or negligible impedance. In other words VSI has stiff DC voltage source at its input terminals. A current source inverter is fed with adjustable current from a DC source of high impedance,i.e;from a stiff DC current source. In a CSI fed with stiff current source, output current waves are not affected by the load.

From view point of connections of semiconductor devices, inverters are classified as under

- Bridge Inverters
- Series Inverters
- Parallel Inverters

1.3 APPLICATIONS

- **DC POWER SOURCE UTILIZATION**

Inverter designed to provide 115 VAC from the 12 VDC source provided in an automobile. The unit provides up to 1.2 Amps of alternating current, or just enough to power two sixty watt light bulbs.

An inverter converts the DC electricity from sources such as batteries, solar panels, or fuel cells to AC electricity. The electricity can be at any required voltage; in particular it can operate AC equipment designed for mains operation, or rectified to produce DC at any desired voltage.

Grid tie inverters can feed energy back into the distribution network because they produce alternating current with the same wave shape and frequency as supplied by the distribution system. They can also switch off automatically in the event of a blackout.

Micro-inverters convert direct current from individual solar panels into alternating current for the electric grid.

- **UNINTERRUPTIBLE POWER SUPPLIES**

An uninterruptible power supply is a device which supplies the stored electrical power to the load in case of raw power cut-off or blackout. One type of UPS uses batteries to store power and an inverter to supply AC power from the batteries when main power is not available. When main power is restored, a rectifier is used to supply DC power to recharge the batteries.

It is widely used at domestic and commercial level in countries facing Power outages.

- **INDUCTION HEATING**

Inverters convert low frequency main AC power to a higher frequency for use in induction heating. To do this, AC power is first rectified to provide DC power. The inverter then changes the DC power to high frequency AC power.

- ## HVDC POWER TRANSMISSION

With HVDC power transmission, AC power is rectified and high voltage DC power is transmitted to another location. At the receiving location, an inverter in a static inverter plant converts the power back to AC.

- ## VARIABLE-FREQUENCY DRIVES

A variable-frequency drive controls the operating speed of an AC motor by controlling the frequency and voltage of the power supplied to the motor. An inverter provides the controlled power. In most cases, the variable-frequency drive includes a rectifier so that DC power for the inverter can be provided from main AC power. Since an inverter is the key component, variable-frequency drives are sometimes called inverter drives or just inverters.

- ## ELECTRIC VEHICLE DRIVES

Adjustable speed motor control inverters are currently used to power the traction motor in some electric locomotives and diesel-electric locomotives as well as some battery electric vehicles and hybrid electric highway vehicles such as the Toyota Prius. Various improvements in inverter technology are being developed specifically for electric vehicle applications.[2] In vehicles with regenerative braking, the inverter also takes power from the motor (now acting as a generator) and stores it in the batteries.

- ## THE GENERAL CASE

A transformer allows AC power to be converted to any desired voltage, but at the same frequency. Inverters, plus rectifiers for DC, can be designed to convert from any voltage, AC or DC, to any other voltage, also AC or DC, at any desired frequency. The output power can never exceed the input power, but efficiencies can be high, with a small proportion of the power dissipated as waste heat.

CHAPTER #2

PULSE MODULATION SCHEMES

2.1 PULSE-AMPLITUDE MODULATION

In PAM the successive sample values of the analog signal *s*(*t*) are used to effect the amplitudes of a corresponding sequence of pulses of constant duration occurring at the sampling rate. No quantization of the samples normally occurs (Fig. 1*a*, *b*). In principle the pulses may occupy the entire time between samples, but in most practical systems the pulse duration, known as the duty cycle, is limited to a fraction of the sampling interval. Such a restriction creates the possibility of interleaving during one sample interval one or more pulses derived from other PAM systems in a process known as time-division multiplexing (TDM).

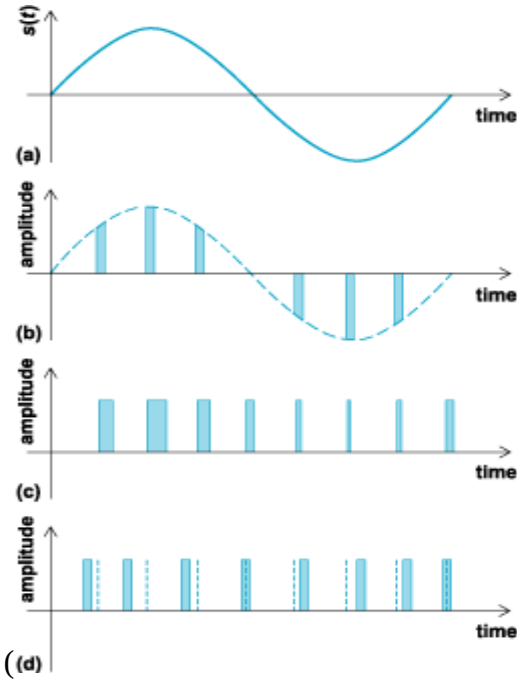


Figure 1*(a)*Analog signal, *s*(*t*). (*b*) Pulse-amplitude modulation. (*c*) Pulse-width modulation. (*d*) Pulse position modulation

2.2 PULSE-WIDTH MODULATION

In PWM the pulses representing successive sample values of $s(t)$ have constant amplitudes but vary in time duration in direct proportion to the sample value. The pulse duration can be changed relative to fixed leading or trailing time edges or a fixed pulse center. To allow for time-division multiplexing, the maximum pulse duration may be limited to a fraction of the time between samples (Fig. 1*c*).

2.3 PULSE-POSITION MODULATION

PPM encodes the sample values of $s(t)$ by varying the position of a pulse of constant duration relative to its nominal time of occurrence. As in PAM and PWM, the duration of the pulses is typically a fraction of the sampling interval. In addition, the maximum time excursion of the pulses may be limited (Fig. 1*d*).

2.4 PULSE-CODE MODULATION

Many modern communication systems are designed to transmit and receive only pulses of two distinct amplitudes. In these so-called binary digital systems, the analog-to-digital conversion process is extended by the additional step of coding, in which the amplitude of each pulse representing a quantized sample of $s(t)$ is converted into a unique sequence of one or more pulses with just two possible amplitudes. The complete conversion process is known as pulse-code modulation. Figure 2*a* shows the example of three successive quantized samples of an analog signal $s(t)$, in which sampling occurs every T seconds and the pulse representing the sample is limited to $T/2$ seconds. Assuming that the number of quantization levels is limited to 8, each level can be represented by a unique sequence of three two-valued pulses

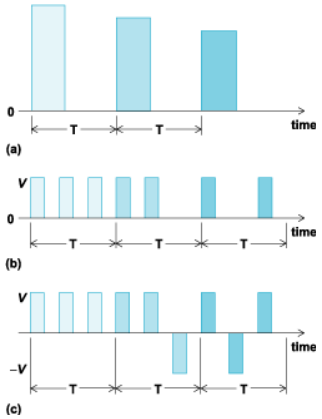


Figure 2(a) ***Three successive quantized samples of an analog signal. (b) With pulses of amplitude V or 0. (c) With pulses of amplitude V or –V***

PCM enjoys many important advantages over other forms of pulse modulation due to the fact that information is represented by a two-state variable. First, the design parameters of a PCM transmission system depend critically on the bandwidth of the original signal $s(t)$ and the degree of fidelity required at the point of reconstruction, but are otherwise largely independent of the information content of $s(t)$. This fact creates the possibility of deploying generic transmission systems suitable for many types of information. Second, the detection of the state of a two-state variable in a noisy environment is inherently simpler than the precise measurement of the amplitude, duration, or position of a pulse in which these quantities are not constrained. Third, the binary pulses propagating along a medium can be intercepted and decoded at a point where the accumulated distortion and attenuation are sufficiently low to assure high detection accuracy. New pulses can then be generated and transmitted to the next such decoding point. This so-called process of repeatering significantly reduces the propagation of distortion and leads to a quality of transmission that is largely independent of distance.

2.5 WHY PULSE WIDTH MODULATION?

Pulse-width modulation (PWM) of a signal or power source involves the modulation of its duty cycle, to either convey information over a communications channel or control the amount of power sent to a load.

2.6 ADVANTAGES OF PWM

Using pulse width modulation has several advantages over analog control.

I. The entire control circuit can be digital, eliminating the need for digital-to-analog converters.

II. Using digital control lines will reduce the susceptibility of your circuit to interference.

III. Finally, motors may be able to operate at lower speeds if you control them with PWM. When you use an analog current to control a motor, it will not produce significant torque at low speeds.

IV. The output voltage control can be obtained without any additional components.

V. With this method, lower order harmonics can be eliminated or minimized Along with its output voltage control.

VI. As higher order harmonics can be filtered easily the higher order harmonics can be minimized.

CHAPTER #3

PULSE WIDTH MODUALTION

There are many forms of modulation used for communicating information. When a high frequency signal has amplitude varied in response to a lower frequency signal we have AM (amplitude modulation). When the signal frequency is varied in response to the modulating signal we have FM (frequency modulation. These signals are used for radio modulation because the high frequency carrier signal is needs for efficient radiation of the signal. When communication by pulses was introduced, the amplitude, frequency and pulse width become possible modulation options. In many power electronic converters where the output voltage can be one of two values the only option is modulation of average conduction time.

Figure

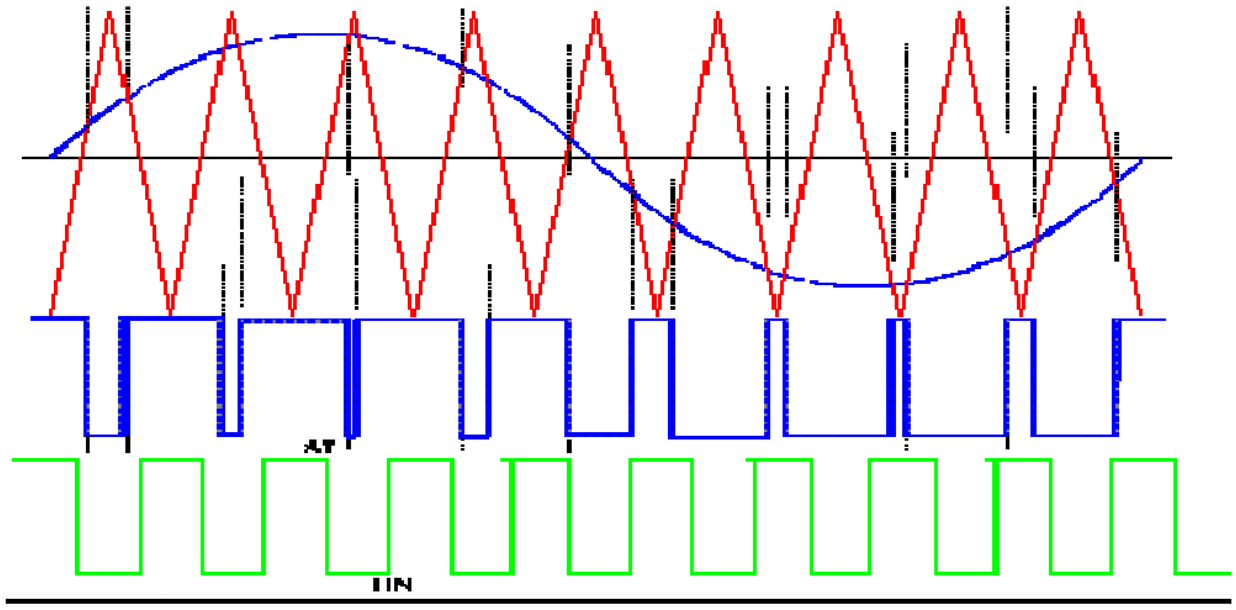
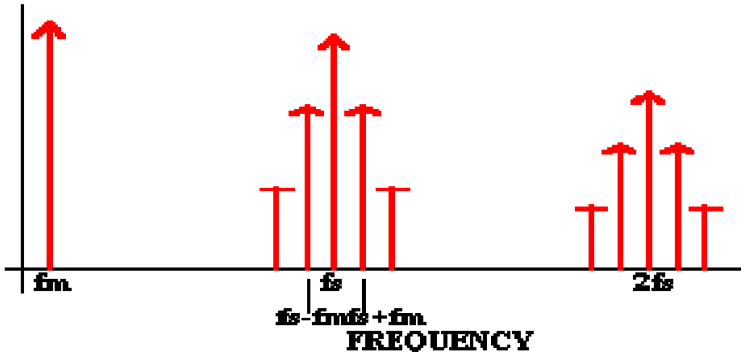


Figure 3 (Sine moodualted, Unmodualted signal)

3.1. LINEAR MODULATION

The simplest modulation to interpret is where the average ON time of the pulses varies proportionally with the modulating signal. The advantage of linear processing for this application lies in the ease of de-modulation. The modulating signal can be recovered from the PWM by low pass filtering. For a single low frequency sine wave as modulating signal modulating the width of a fixed frequency (fs) pulse train the spectra is as shown in Fig 2. Clearly a low pass filter can extract the modulating component fm.

Figure 4



3.2. SAW TOOTH PWM

The simplest analog form of generating fixed frequency PWM is by comparison with a linear slope waveform such as a saw tooth. As seen in Fig 2 the output signal goes high when the sine wave is higher than the saw tooth. This is implemented using a comparator whose output voltage goes to logic HIGH when ne input is greater than the other. Other signals with straight edges can be used for modulation a rising ramp carrier will generate

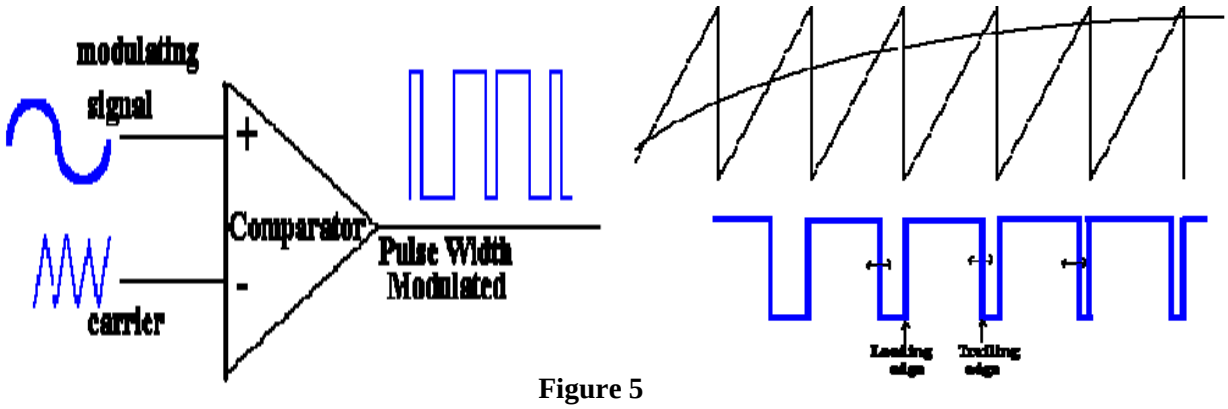


Figure 5

3.3 REGULAR SAMPLED PWM

The scheme illustrated above generates a switching edge at the instant of crossing of the sine wave and the triangle. This is an easy scheme to implement using analog electronics but suffers the imprecision and drifts of all analog computation as well as having difficulties of generating multiple edges when the signal has even a small added noise. Many modulators are now implemented digitally but there is difficulty is computing the precise intercept of the modulating wave and the carrier. Regular sampled PWM makes the width of the pulse proportional to the value of the modulating signal at the beginning of the carrier period. In Fig 5 the intercept of the sample values with the triangle determine the edges of the Pulses. For a saw tooth wave of frequency fs the samples are at 2fs.

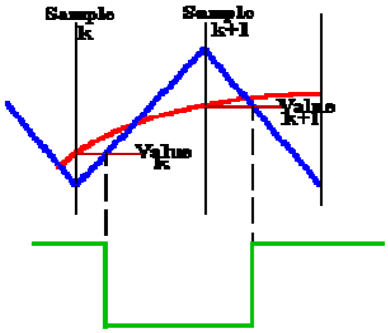
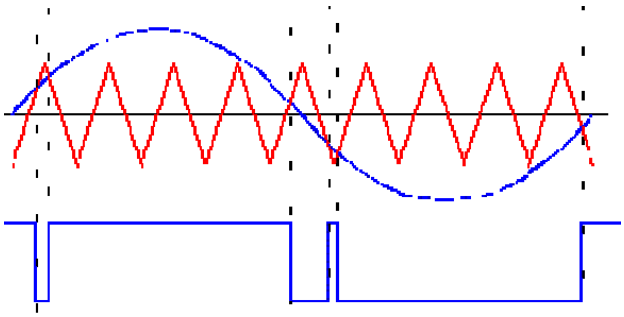


Figure 6 (Regular sampled PWM)

3.4. MODULATION DEPTH

For a single phase inverter modulated by a sine-sawtooth comparison, if we compare a sine wave of magnitude from -2 to +2 with a triangle from -1 to +1 the linear relation between the input signal and the average output signal will be lost. Once the sine wave reaches the peak of the triangle the pulses will be of maximum width and the modulation will then saturate. The Modulation depth is the ratio of the current signal to the case when saturation is just starting. Thus sine wave of peak 1.2 compared with a triangle with peak 2.0 will have a modulation depth

Figure 7



CHAPTER #4

SINGLE PHASE PWM INVERTERS

In many industrial applications, it's often required to control the output voltage of inverters for the following reasons

- To cope with the variations of DC input voltage
- For voltage regulation of inverters
- For the constant volts/frequency control requirement

  There are various techniques to vary the inverter gain. The most efficient method of controlling the gain (and output voltage) is to incorporate pulse width modulation (PWM) control within the inverters. The commonly used techniques are

  I. Single Pulse width Modulation

  II. Multiple Pulse width Modulation

  III. Sinusoidal Pulse width Modulation

  IV. Trapezoidal Pulse width Modulation

  V. Stair case Pulse width Modulation

In PWM inverters, forced commutation is essential. The PWM techniques listed above differ from each other in the harmonic content in their respective output voltages.Thus,choice of a particular PWM technique depends upon the permissible harmonic content in the inverter output voltage. Industrial applications PWM inverter is supplied from a diode bridge rectifier and an LC filter. The inverter topology remains the same for a single phase inverter and for a three phase inverter. But now the devices are now switched ON and OFF several times within each half cycle to control the output voltage which has low harmonic content.

4.1 SINGLE PULSE WIDTH MODULATION

In this control, there's only one pulse per half cycle and the width of the pulse is varied to control the inverter output. The gating signals are generated by comparing a rectangular reference signal of the amplitude A_r with triangular carrier wave of amplitude A_c,the frequency of the carrier wave determines the fundamental frequency of output voltage. By varying A_r from 0 to A_c,the pulse width can be varied from 0 to 100 percent. The ratio of A_r to A_c is the control variable and defined as the modulation index.

4.2 MULTIPLE PULSE WIDTH MODULATION

The harmonic content can be reduced by using several pulses in each half cycle of output voltage. The generation of gating signals for turning ON and OFF transistors by comparing a reference signal with a triangular carrier wave. The frequency F_c, determines the number of pulses per half cycle. The modulation index controls the output voltage. This type of modulation is also known as uniform pulse width modulation (UPWM).

4.3 SINUSOIDAL PULSE WIDTH MODULATION

Instead of ,maintaining the width of all pulses of same as in case of multiple pulse width modulation, the width of each pulse is varied in proportion to the amplitude of a sine wave evaluated at the centre of the same pulse. The distortion factor and lower order harmonics are reduced significantly. The gating signals are generated by comparing a sinusoidal reference signal with a triangular carrier wave of frequency F_c.The frequency of reference signal F_r ,determines the inverter output frequency and its peak amplitude A_r,controls the modulation index M,and rms output voltage V_O.The number of pulses per half cycle depends on carrier frequency .

CHAPTER #5

PWM STRATEGIES WITH DIFFERING PHASE RELATIONSHIPS

This section of the chapter extends the principles of carrier-based PWM that are used for multilevel inverter. One of the most straightforward methods of describing voltage-source modulation is to illustrate the intersection of a modulating signal (duty cycle) with triangle waveforms. There are three alternative PWM strategies with differing phase relationships:

- Alternate phase disposition (APOD) – every carrier waveform is in out of phase with its neighbor carrier by 180.
- Phase opposition disposition (POD) – All carrier waveforms above zero reference are in phase and are 180 degree out of phase with those below zero.
- Phase disposition (PD)- All carrier waveforms are in phase

5.1 ALTERNATE PHASE DISPOSITION (APOD):

In case of alternate phase disposition (APOD) modulation, every carrier waveform is in out of phase with its neighbor carrier by 180 degree. Since APOD and POD schemes in case of three-level inverter are the same, a five level inverter is considered to discuss about the APOD scheme. The rules for APOD method, when the number of level N = 5, are

- The N – 1 = 4 carrier waveforms are arranged so that every carrier waveform is in out of phase with its neighbor carrier by 180
- The converter switches to + Vdc / 2 when the reference is greater than all the carrier waveforms.
- The converter switches to Vdc / 4 when the reference is less than the uppermost carrier waveform and greater than all other carriers.
- The converter switches to 0 when the reference is less than the two uppermost carrier waveform and greater than two lowermost carriers.
- The converter switches to - Vdc / 4 when the reference is greater than the lowermost carrier waveform and lesser than all other carriers.

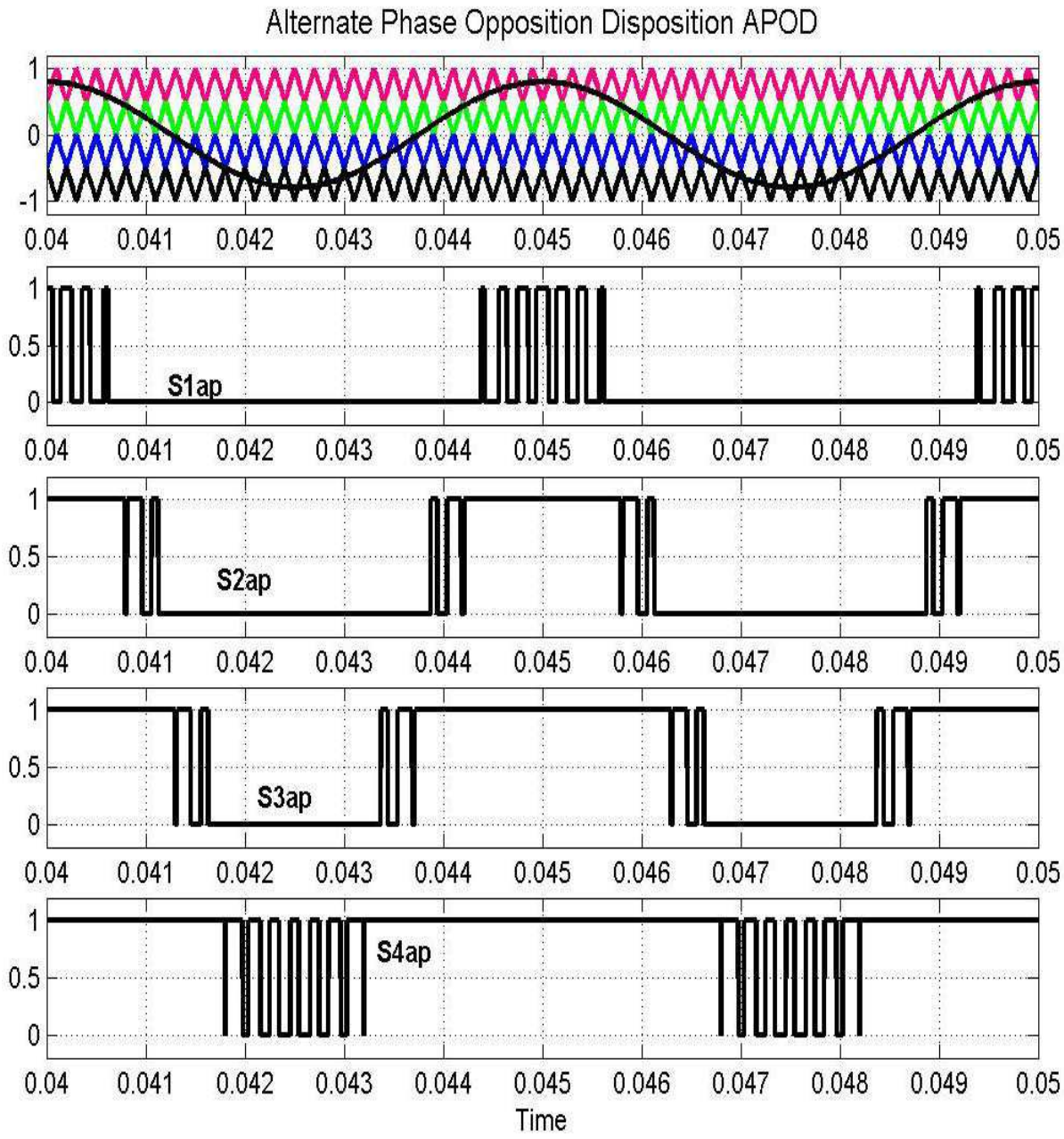


Figure 8 (Switching pattern produced using the APOD carrier-based PWM scheme for a five-level inverter: (a) Four triangles and the modulation signal (b) S1ap (c) S2ap (d) S3ap (e) S4ap.)

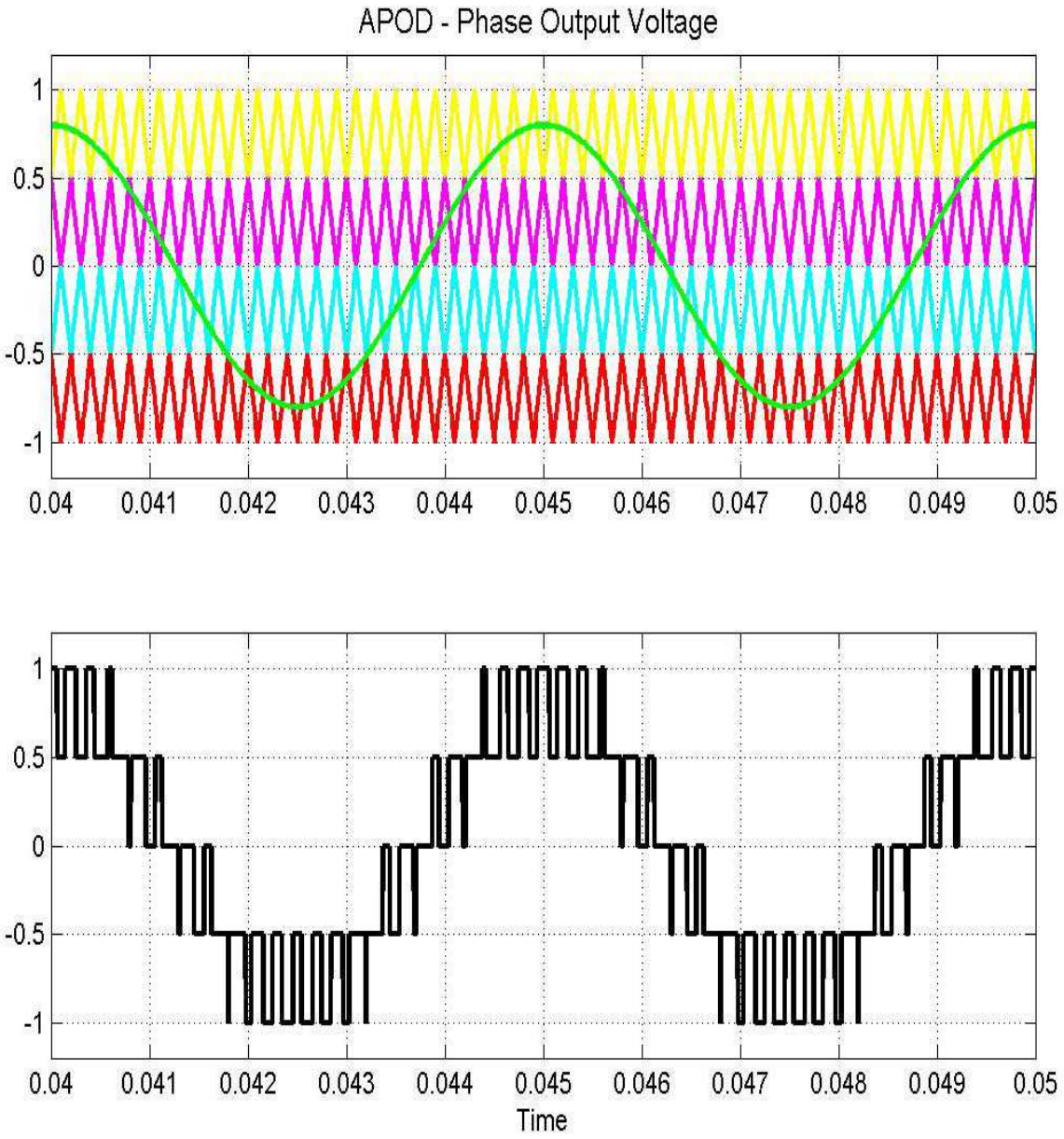


Figure 9.(Simulation of carrier-based PWM scheme using APOD for a five-level inverter. I. Modulation signal and carrier waveforms (II) Phase "a" output voltage.)

Figure . Demonstrates the APOD scheme for a five-level inverter. The figure displays the switching pattern generated by the comparison of the modulation signals with the four carrier waveforms. Figure 9 Shows the output voltage waveform of phase "a" and it is clear the waveform has five steps.

5.2 PHASE OPPOSITION DISPOSITION (POD):

For phase opposition disposition (POD) modulation all carrier waveforms above zero reference are in phase and are 180^0 out of phase with those below zero.
The rules for the phase opposition disposition method, when the number of level N = 3 are

• The N –1 = 2 carrier waveforms are arranged so that all carrier waveforms above zero are in phase and are 180^0 out of phase with those below zero.

• The converter is switched to + V_{dc} / 2 when the reference is greater than both carrier waveforms.

• The converter is switched to zero when the reference is greater than the lower carrier waveform but less than the upper carrier waveform.

• The converter is switched to - Vdc / 2 when the reference is less than both carrier waveforms.

As seen from Figure, the figure illustrates the switching functions produced by POD carrier based PWM scheme. In the PWM scheme there are two triangles, upper triangle magnitude from 1 to 0 and the lower triangle from 0 to –1 and these two triangle waveforms are in out of phase. When the modulation signal is greater than both the carrier waveforms, S_{1ap} and S_{2ap} are turned on and the converter switches to positive node voltage and when the reference is less than the upper carrier waveform but greater than the lower carrier, S_{2ap} and S_{1an} are turned on and the converter switches to neutral point. When the reference is lower than both carrier waveforms, S_{1an} and S_{2an} are turned on and the converter switches to negative node voltage.

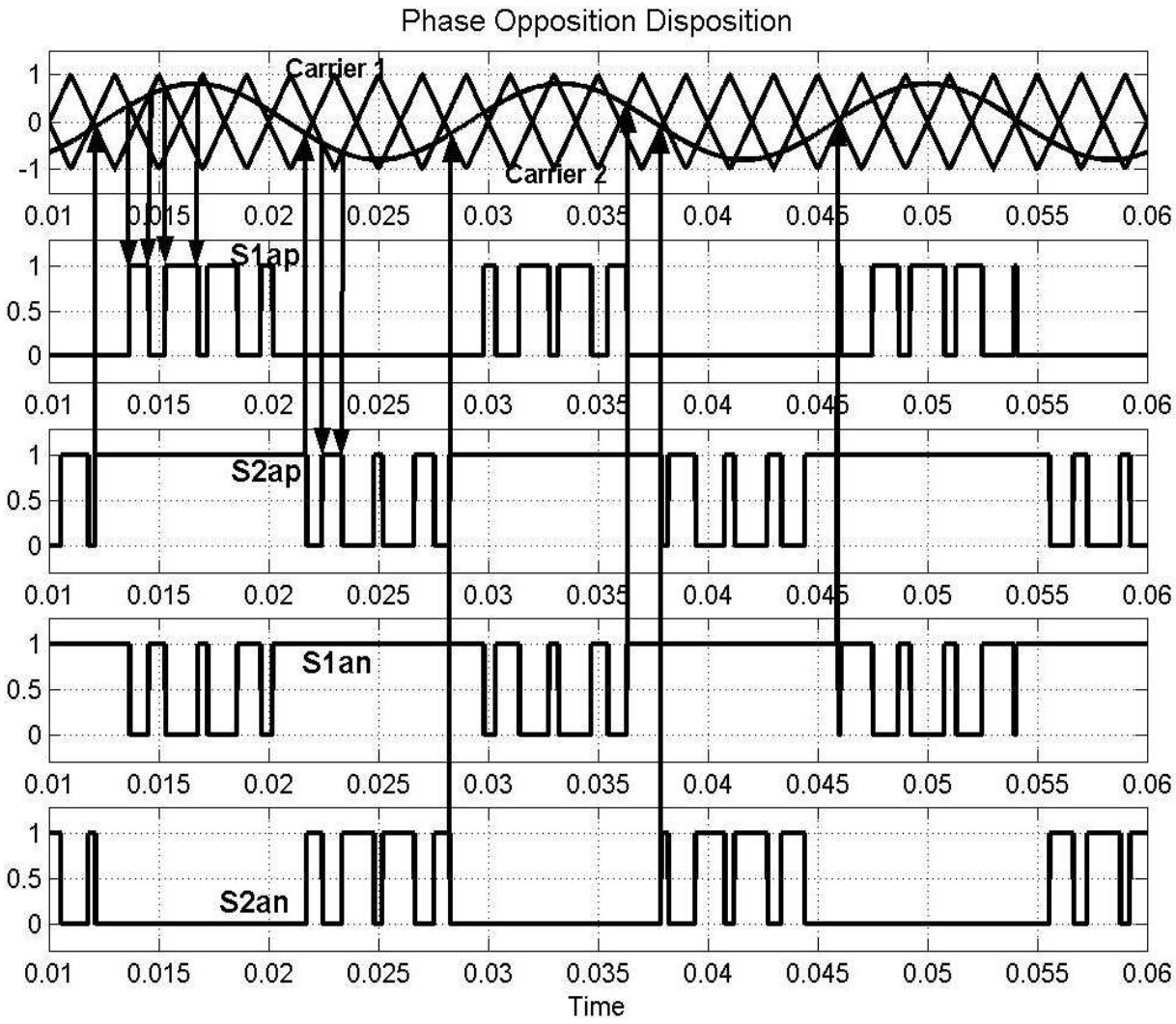


Figure 10.(Switching pattern produced using the POD carrier-based PWM scheme: (a) two triangles and the modulation signal (b) S1ap (c) S2ap (d) S1an (e) S2an

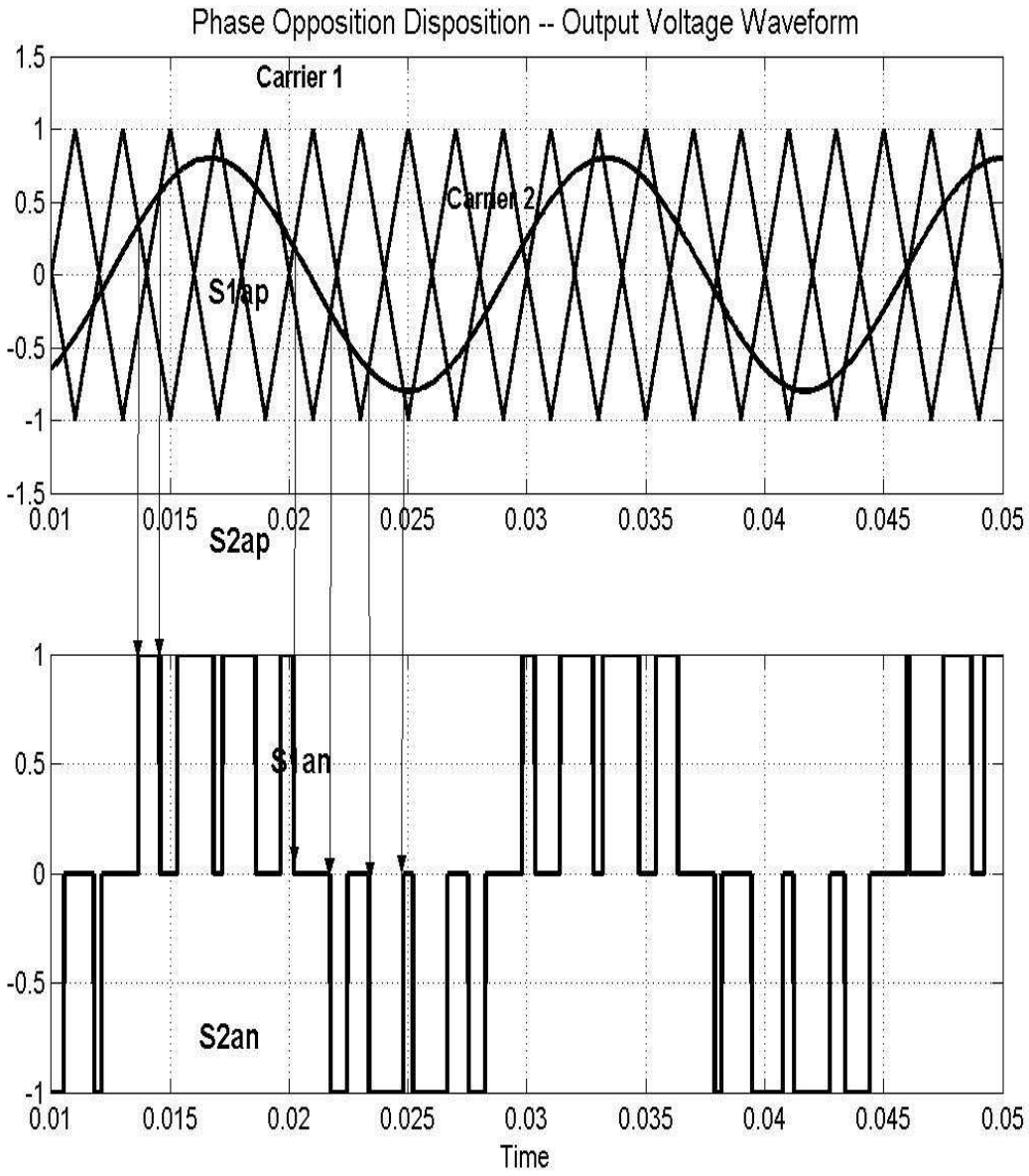


Figure 11.(Simulation of carrier-based PWM scheme using POD. I. Modulation signal and out of phase carrier waveforms (II) Phase "a" output voltage)

Also shows the implementation of the phase disposition (PD) scheme. Shows the carriers waveforms are displaced out of phase and compared with the sinusoidal modulation signal. Figure . (II) Shows the phase "a" output voltage waveform.

5.3 PHASE DISPOSITION (PD):

In the present work, in the carrier-based implementation the phase disposition PWM scheme is used.

Figure demonstrates the sine-triangle method for a three-level inverter. Therein, the a-phase modulation signal is compared with two (n-1 in general) triangle waveforms. The rules for the phase disposition method, when the number of level N = 3, are

• The N –1 = 2 carrier waveforms are arranged so that every carrier is in phase.

• The converter is switched to + Vdc / 2 when the reference is greater than both carrier waveforms.

• The converter is switched to zero when the reference is greater than the lower carrier waveform but less than the upper carrier waveform.

• The converter is switched to - Vdc / 2 when the reference is less than both carrier waveforms.

In the carrier-based implementation at every instant of time the modulation signals are compared with the carrier and depending on which is greater, the definition of the switching pulses is generated.

As seen from Figure, the figure illustrates the switching pattern produced by the carrier-based PWM scheme. In the PWM scheme there are two triangles, the upper triangle ranges from 1 to 0 and the lower triangle ranges from 0 to –1. In the similar way for an N –level inverter, the (N-1) triangles are used and each has a peak-to-peak value of 2/(N-1). Hence the upper most triangle magnitude varies from 1 to (1-2/(N-1)), second carrier waveform from (1-4/(N-1)), and the bottom most triangle varies from (2-2/(N-1)) to –1.

In Figure , the switching pattern of each device can be seen. It is clear from the figure that during the positive cycle of the modulation signal, when the modulation is greater than Triangle 1 and Triangle 2, then S1ap and S2ap are turned on and also during the positive cycle S2ap is completely turned on. When S1ap and S2ap are turned on the converter switches to the + Vdc / 2 and when S1an and S2ap are on, the converter switches to zero and hence during the positive cycle S2ap is completely turned on and S1ap and S1an will be turning on and off and hence the converter switches from + Vdc / 2 to 0. During the negative half cycle of the modulation signal the converter switches from 0 to -Vdc / 2. The phase voltage equations for star-connected, balanced three-phase loads expressed in terms of the existence functions and input nodal voltage.

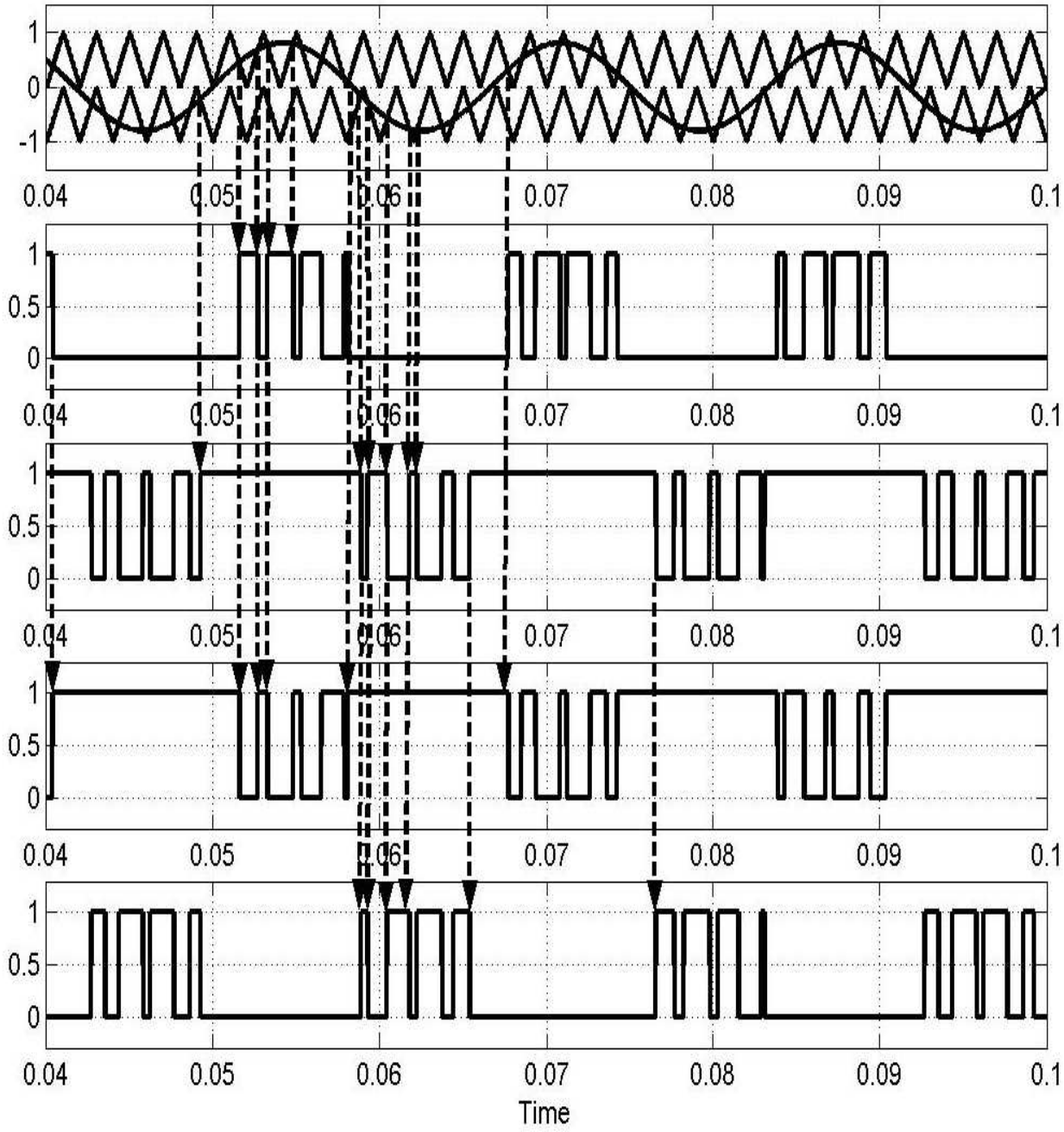


Figure 12(Switching pattern produced using the PD carrier-based PWM scheme: (a) two triangles and the modulation signal (b) S1ap (c) S2ap (d) S1an (e) S2an.)

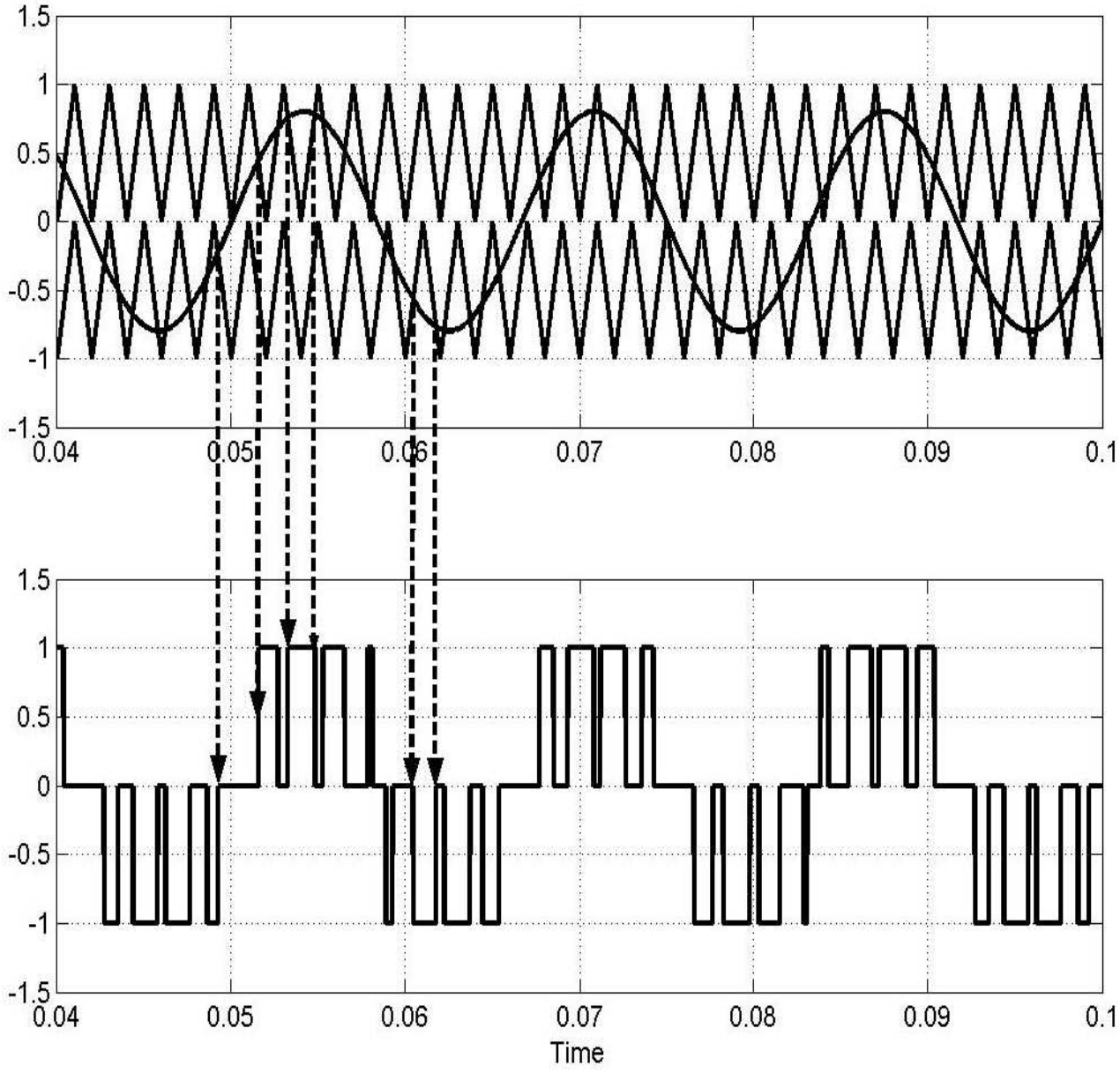


Figure 13(Simulation of carrier-based PWM scheme using the phase disposition (PD).

I. Modulation signal and in-phase carrier waveforms (II) Phase "a" output voltage.)

Figure . Shows the implementation of the phase disposition (PD) scheme.

Figure 13 (I)shows that two carriers waveforms are displaced in phase and compared with the sinusoidal modulation signal. Figure . (II) Shows the phase "a" output voltage waveform.

CHAPTER #6

OVERVIEW OF 8051 MICROCONTROLLER

6.1 DESCRIPTION

The AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K bytes of Flash programmable and erasable read only memory (PEROM). The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard MCS-51 instruction set and pin out. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides a highly-flexible and cost-effective solution to many embedded control applications.

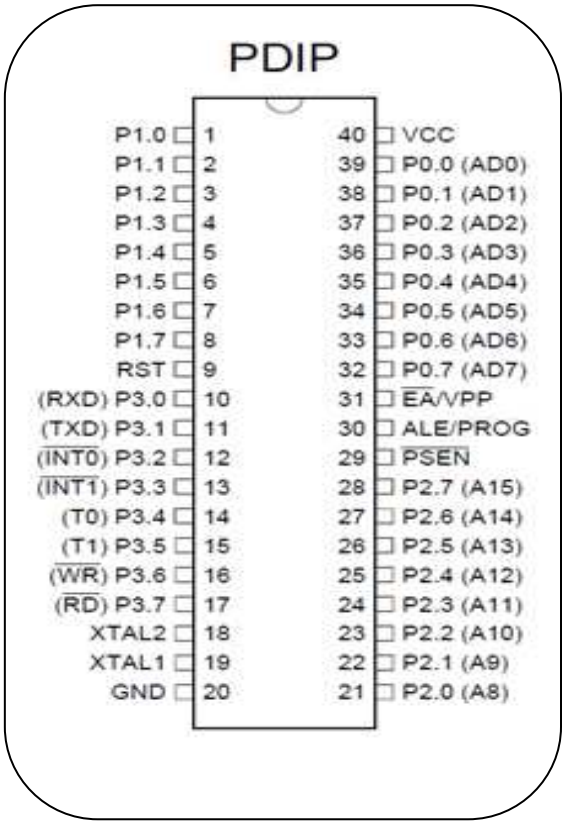


Figure 14 **Pin configuration**

6.2 INTERNAL ARCHITECTURE OF 8051 MICROCONTROLLER

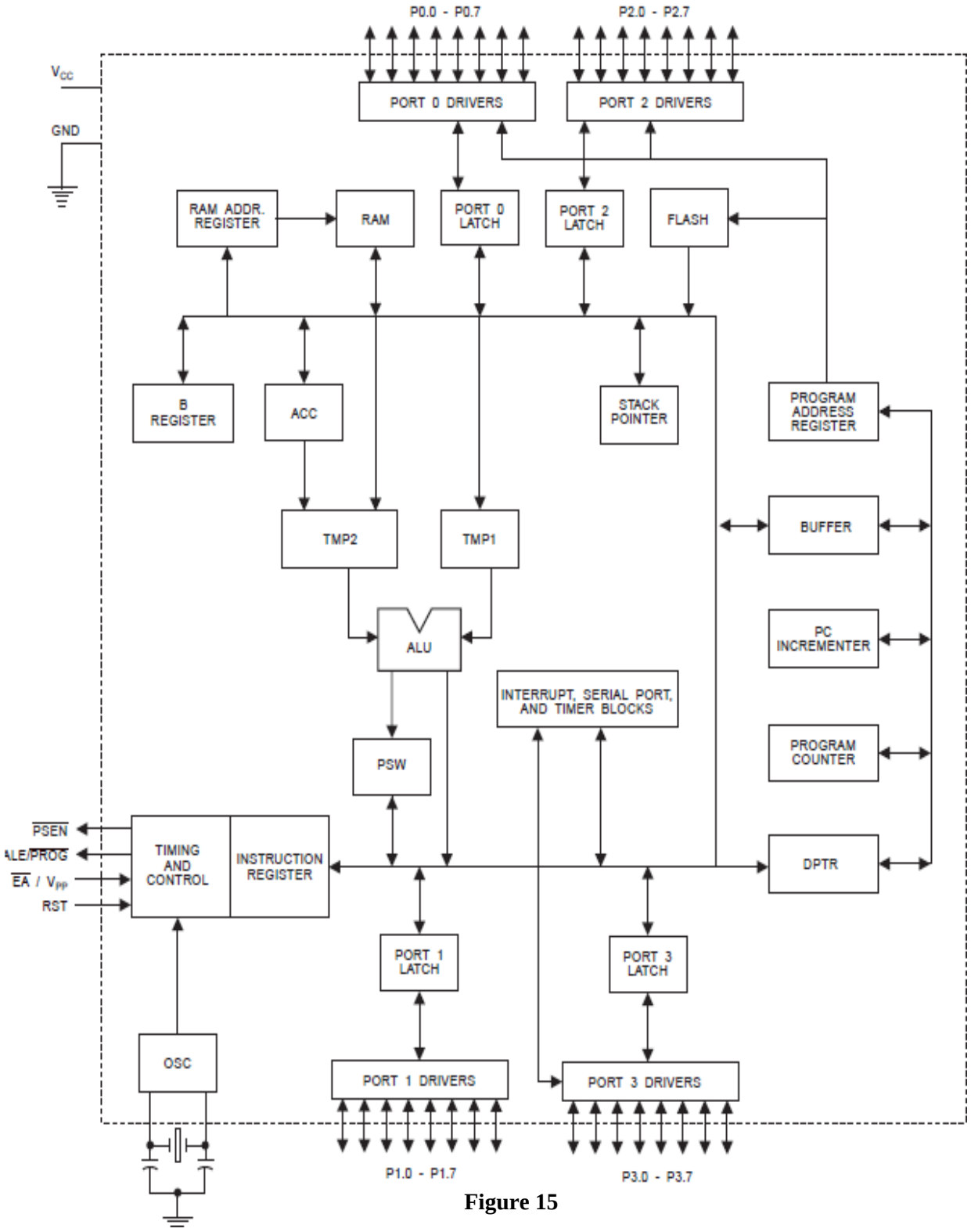


Figure 15

6.3 PIN DESCRIPTION

VCC

Supply voltage. +5.0V

GND

Ground.

Port 0

Port 0 is an 8-bit open-drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high impedance

Inputs. Port 0 may also be configured to be the multiplexed low order address/data bus during accesses to external program and data memory. In this mode P0 has internal pull-ups. Port 0 also receives the code bytes during Flash programming, and outputs the code bytes during program verification. External pull-ups are required during program verification.

Port 1

Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL) because of the internal pull-ups. Port 1 also receives the low-order address bytes during Flash programming and verification.

Port 2

Port 2 is an 8-bit bi-directional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (IIL) because of the internal pullups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register. Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (IIL) because of the pull-ups.

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/PROG

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during Flash programming. In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALEpulse is skipped during each access to external Data Memory. If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

PSEN

Program Store Enable is the read strobe to external program memory. When the AT89C51 is executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.

EA/VPP

External Access Enable. EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset. EA should be strapped to VCC for internal program executions. This pin also receives the 12-volt programming enable voltage (VPP) during Flash programming, for parts that require 12-volt VPP.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

6.4 RAM MEMORY SPACE ALLOCATION IN THE 8051

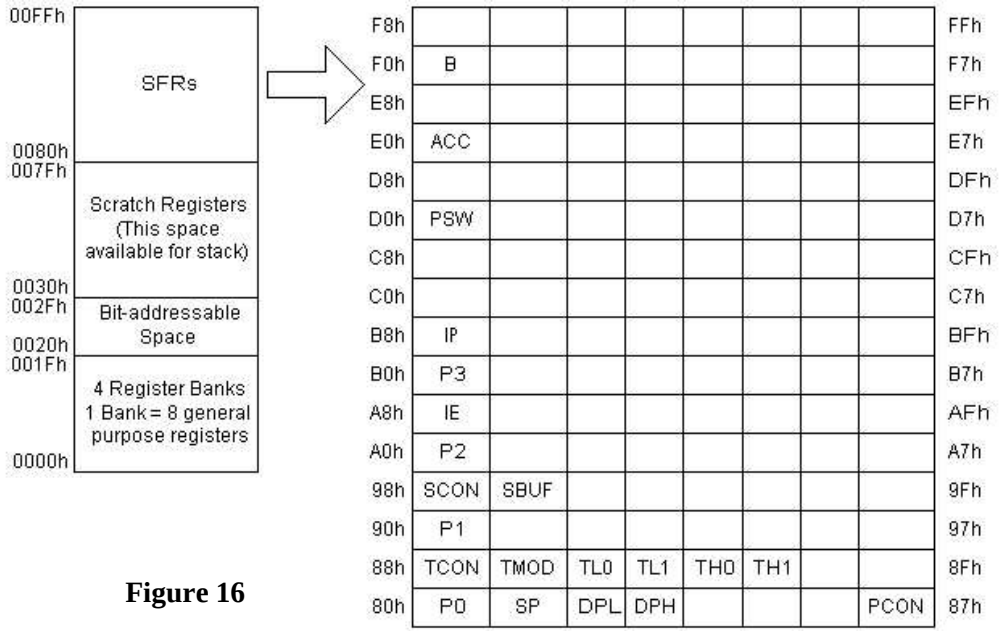


Figure 16

The 8051 microcontroller has a total of 128 bytes of RAM which are assigned address 00 to 7FH.These 128 bytes are divided into 3 different groups as follows.

I. A total of 32 bytes from location 00 to 1FH are set aside for register banks and the stack.

II. A total of 16 bytes from location 20H to 2FH are set aside for bit addressable read/write memory.

III. A total of 80 bytes from location 30H to 7FH are used for read and write storage, or what is normally called a “scratch pad”. These 80 locations of RAM are widely used for the purpose of storing data and parameters by 8051 programmers.

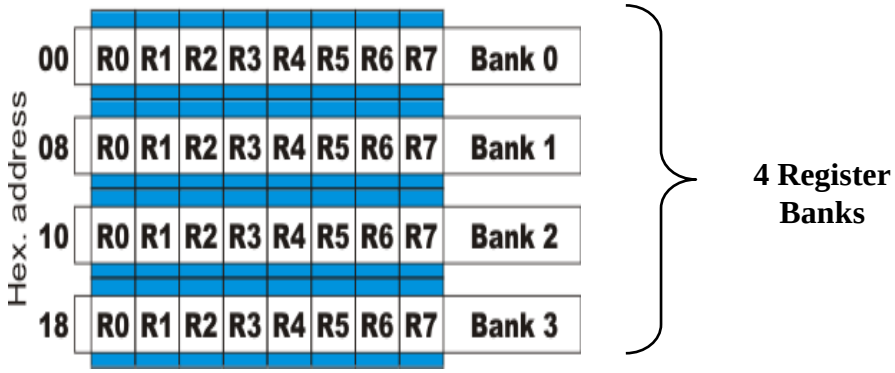
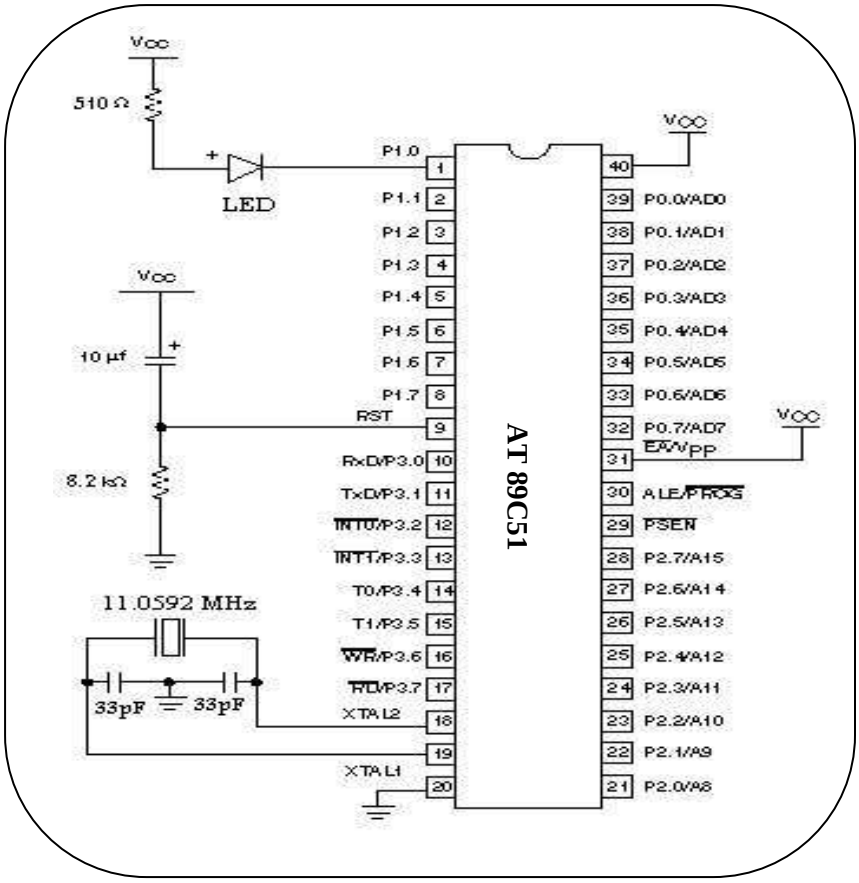
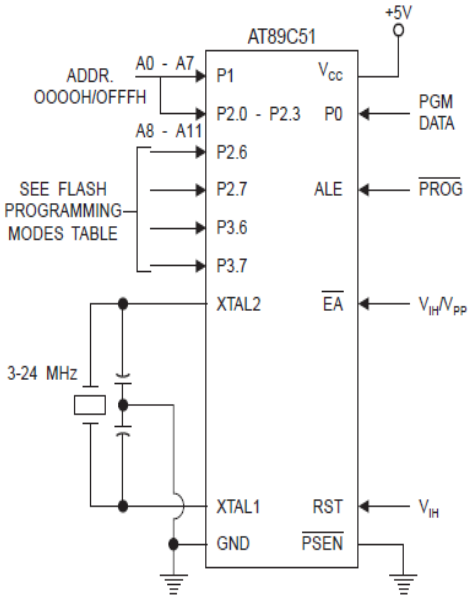


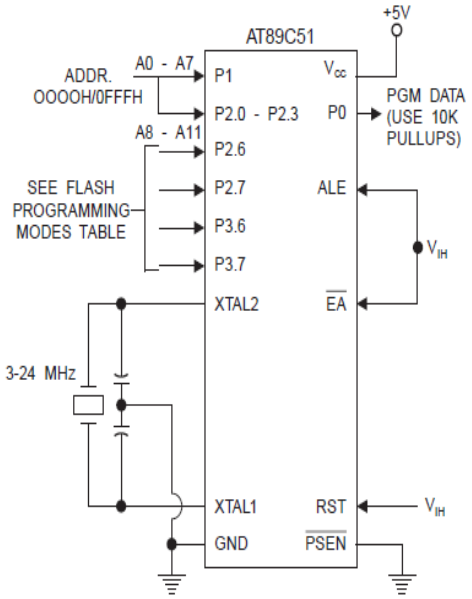
Figure 17

6.5 BASIC POWER CIRCUIT OF AT89C51





Programming the flash



Verifying the flash

Figure 18

CHAPTER #7

MICROCONTROLLER BASED WAVE GENERATION SCHEME

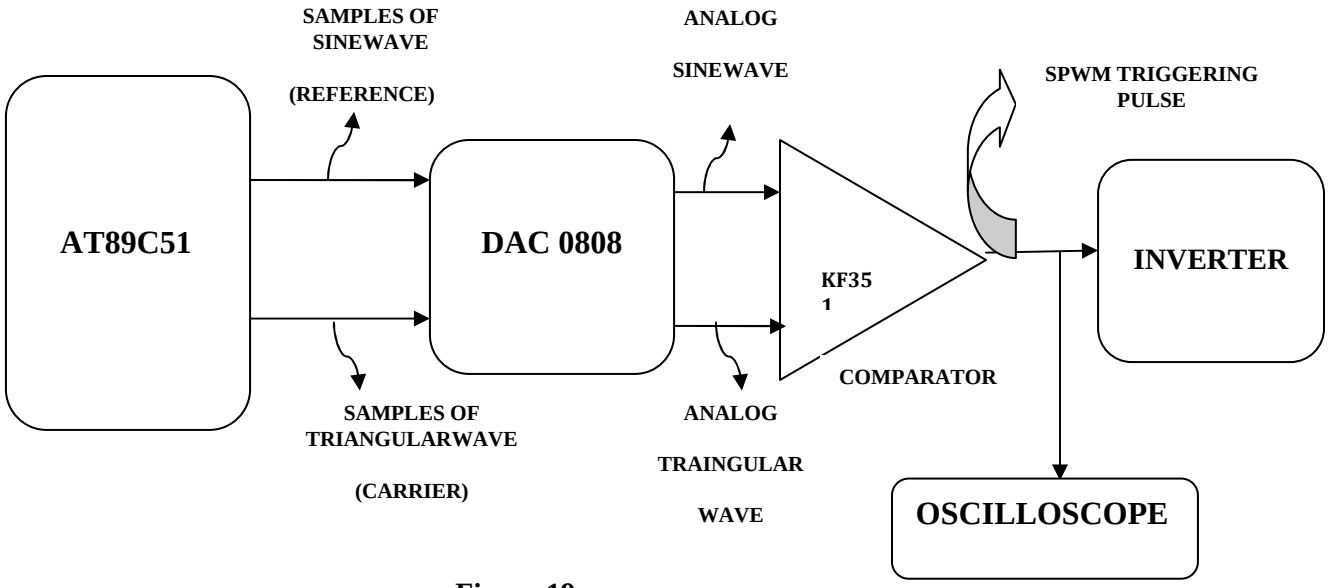


Figure 19

[BLOCK DIAGRAM REPRESENTATION OF WAVE GENERATION SCHEME]

ALGORITHM FOR PWM WAVE GENERATION:

I. Compilation and Simulation of Assembly language program for AT89C51 using "Top view simulator(4.1)"

II. Burning the Program through the "BeeProg universal(48pin Driver) Programmer" into the flash memory of AT89C51

III. Generation of Digital Sample of Sinusoidal and Triangular waves from microcontroller, which is fed into the DAC 0808

IV. Analog output from the DAC 0808 is fed into the comparator KF351

V. Generation of SPWM triggering pulses from KF351 (which is observed through the Oscilloscope) fed to the inverter

7.1 INTERFACING AT89C51 WITH DAC 0808

7.1.1 DAC0808 8-BIT D/A CONVERTER

The Digital to Analog converter is a device widely used to convert digital pulses to analog signal. There are two methods of making the DAC namely, Binary weighted and R/2R ladder. The vast majority of integrated circuit DACs,use the R/2R method.Since,it can achieve much higher degree of precision. The first criterion for judging a DAC is its resolution, which is a function of the number of binary inputs. The common ones are 8,10 and 12 bits. The number of data bit inputs decides the resolution of the DAC since the number of analog output levels is equal to 2^n ,where n is the number of data bit inputs. There are also 16 bit DACs but they are expensive.

The DAC0808 is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with ±5V supplies. No reference current (IREF) trimming is required for most applications since the full scale output current is typically ±1 LSB of 255 $I_{REF}/256$. Relative accuracies of better than ±0.19% assure 8-bit monotonicity and linearity while zero level output current of less than 4 μA provides 8-bit zero accuracy for I_{REF}>=2 mA. The power supply currents of the DAC0808 are independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range.

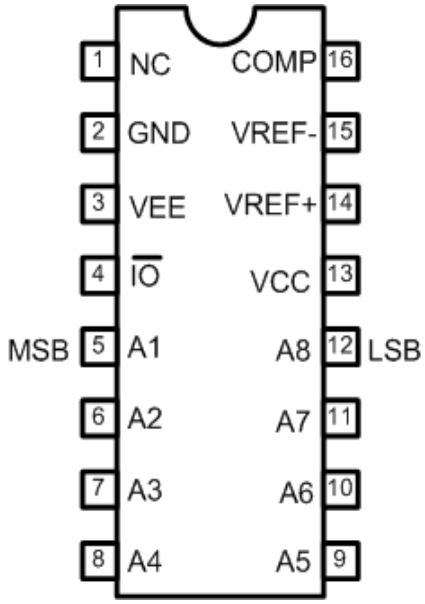
In DAC 0808 the digital inputs are converted to current (I_{out}) and by connecting a resistor to the I_{out} pin we convert the result to voltage. The total current provided by the I_{out} pin is a function of the binary number at D0-D7 inputs of the DAC 0808 and the reference current I_{ref} is as follows.

$$I_{out} = I_{ref} (D7/2 + D6/4 + D5/8 + D4/16 + D3/32 + D2/64 + D1/128 + D0/256)$$

Where D0 is the LSB and D7 is the MSB for the inputs and I_{ref} is the input current that must be applied to pin 14.The output pin I_{out} is connected to resistor and converts this current to voltage and the output can be monitored on the scope.

7.1.2 FEATURES

- n Relative accuracy: ±0.19% error maximum
- n Full scale current match: ±1 LSB type
- n Fast settling time: 150 ns type
- n Non inverting digital inputs are TTL and CMOS
- compatible
- n High speed multiplying input slew rate: 8 mA/μs
- n Power supply voltage range: ±4.5V to ±18V
- n Low power consumption: 33 mW @ ±5V



Pin Description of DAC 0808

Figure 20

7.2 INTERFACING AT89C51 WITH DAC0808

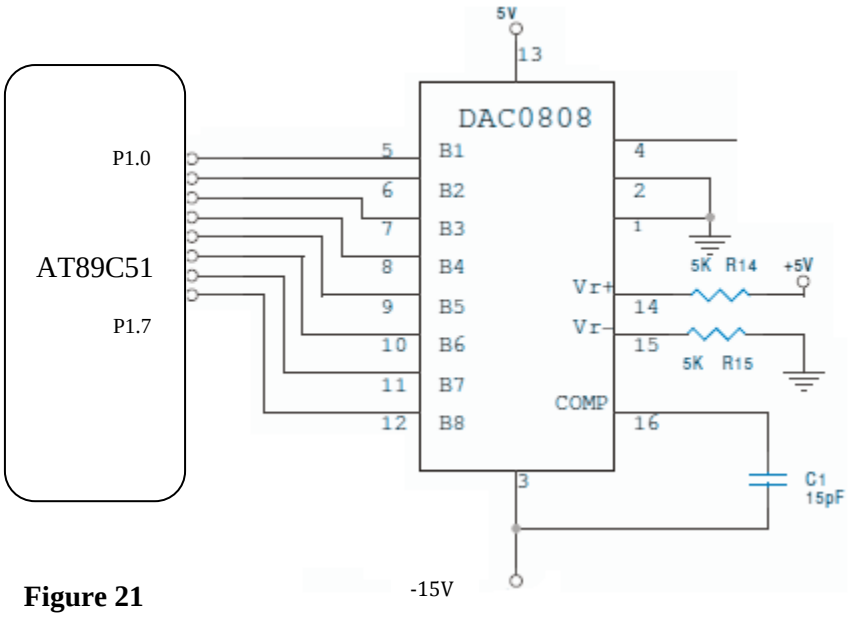


Figure 21

[CIRCUIT DIAGRAM SHOWING INTERFACING AT89C51 WITH DAC 0808]

7.3 INTERFACING DAC0808 WITH KF351 COMPARTOR

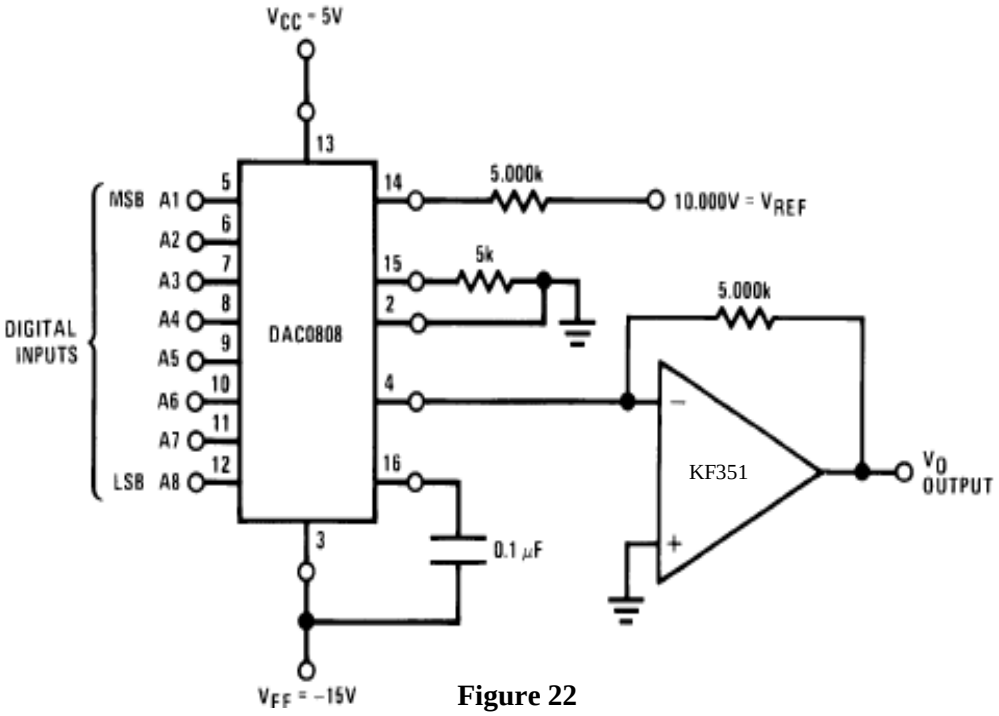


Figure 22

7.4 SOFTWARE IPLEMENTATION

7.4.1 ASSEMBLING AND RUNNING AN 8051 PROGRAM

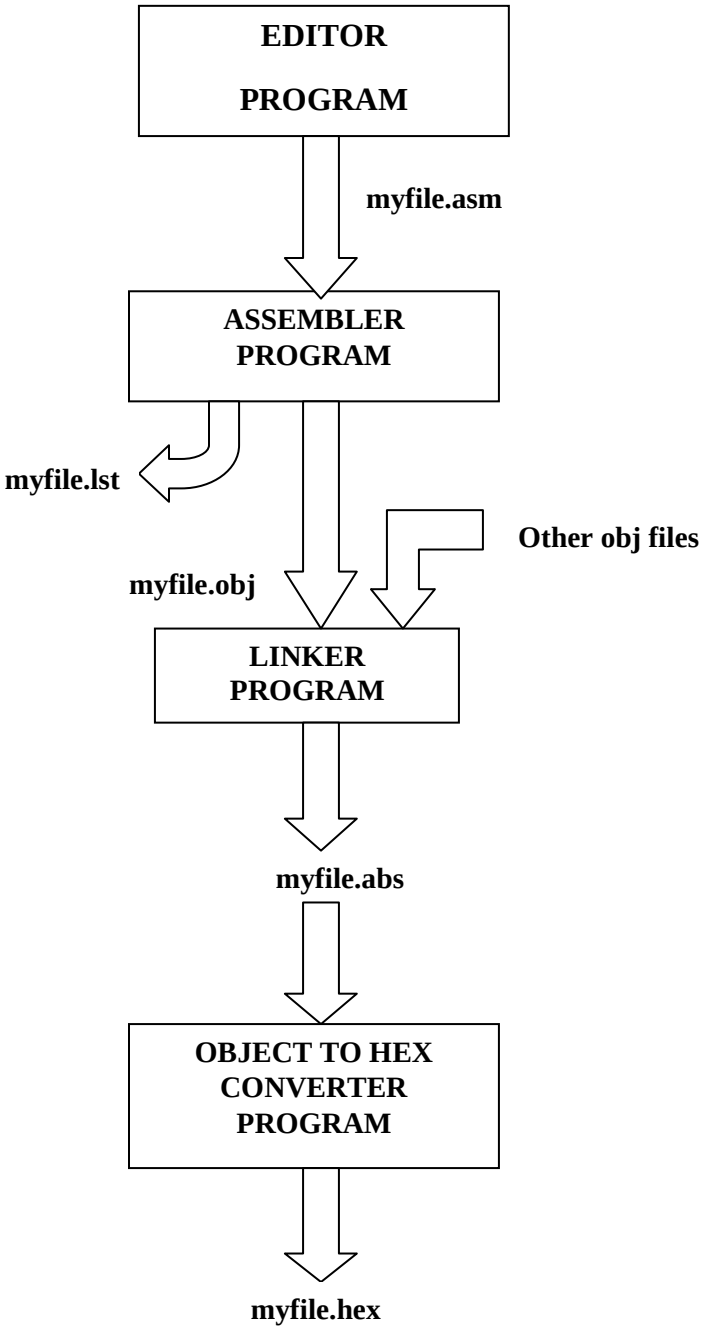


Figure 23

7.5 8051 ASSEMBLY LANGUAGE PROGRAMMING FOR WAVE GENERATION

7.5.1 FLOW CHART

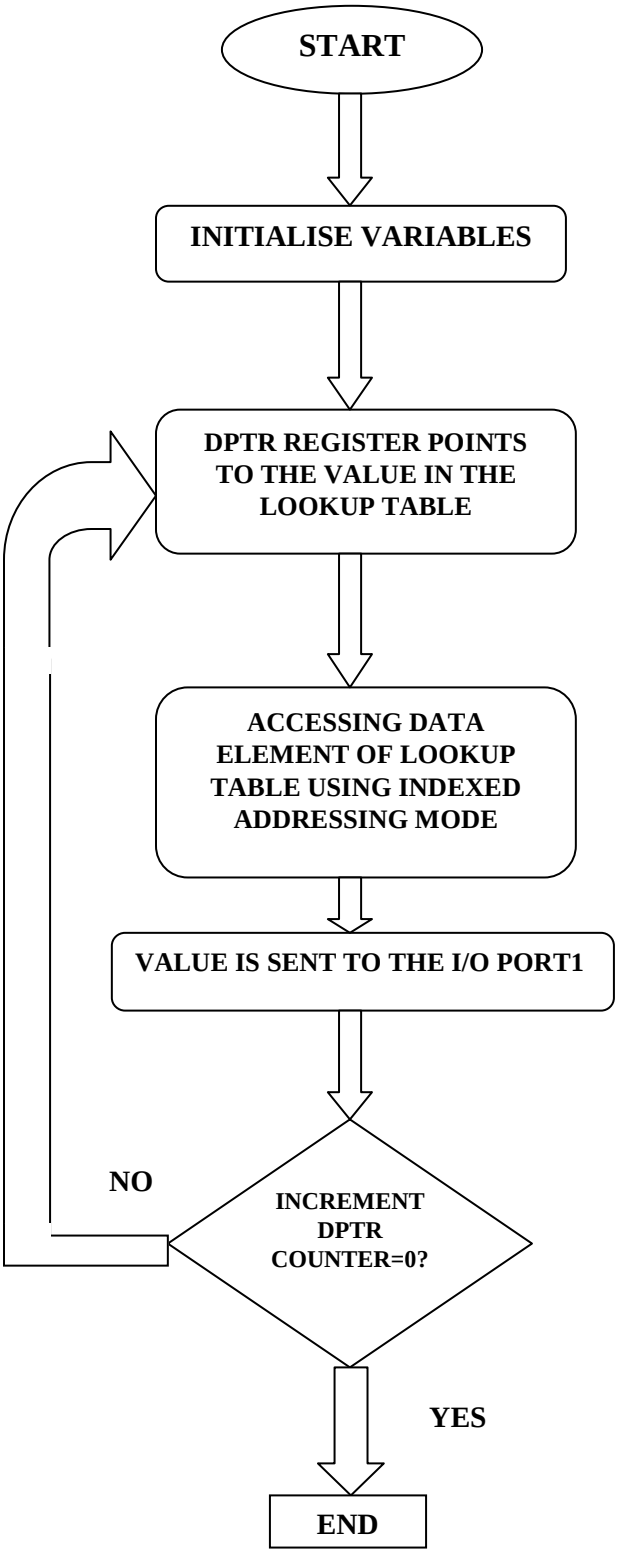


Figure 24

7.5.2 SINE WAVE GENERATION

To generate a sine wave, we first need a table whose values represent the magnitude of the sine of angles between 0 & 360 degrees. The values for the sine function vary from -1 to +1 for 0 to 360 degrees angles. Therefore, the table values are integer numbers representing the voltage magnitude of the sine of thita.This method ensures that only integer numbers are outputted to the DAC(Digital to Analog Converters) by the 8051 Microcontroller. The following table gives the angles, sine values, the voltage magnitudes, the integer values representing the voltage magnitude for each angle (with 30 degree increments). To generate we assumed the full-scale voltage of 10V for DAC Output. Full scale output of DAC is achieved when all the data inputs of the DAC are high. Therefore to achieve the full-scale 10 V output we use the following equation :

$$Vout=5V + 5\times sin\Theta$$

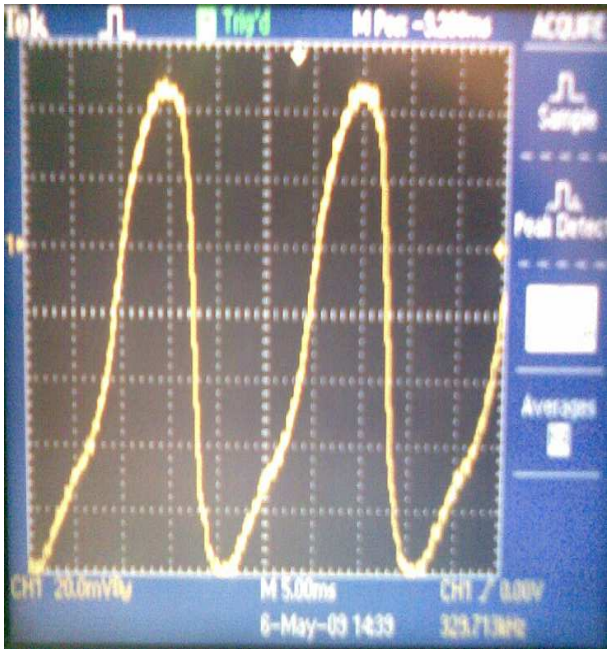
Vout of DAC for various angles is calculated as shown in the table:

AngleΘ	sinΘ	V_{out}	Values sent to DAC
0	0	5	128
30	0.5	7.5	192
60	0.866	9.33	238
90	1.0	10.0	255
120	0.866	9.33	238
150	0.5	7.5	192
180	0	5	128
210	-0.5	2.5	64
240	-0.866	0.669	17
270	-1	0	0
300	-0.866	0.669	17
330	-0.5	2.5	64
360	0	5	128

7.5.3 COMPILED ASSEMBLY CODE FOR SINE WAVE GENERATION USING TOP VIEW SIMULATOR (VERSION 1.2h)

```
SINE
PAGE 1


0000                    1             ORG 0000H
0000 900300             2    AGAIN:   MOV DPTR,#TABLE
0003 7AFF               3             MOV R2,#255
0005 C2E0               4    BACK:    CLR 0E0H
0007 93                 5             MOVC A,@A+DPTR
0008 85E090             6             MOV 90H,0E0H
000B A3                 7             INC DPTR
000C DAF7               8             DJNZ R2,BACK
000E 80F0               9             SJMP AGAIN
0300                   10             ORG 300H
                       11
0300 80C0EEFF          12    TABLE:   DB 128,192,238,255,238,192
0304 EEC0
0306 80401100          13             DB 128,64,17,0,17,64,128
030A 114080
                       14             END



VERSION 1.2h ASSEMBLY COMPLETE, 0 ERRORS FOUND

SINE
PAGE 2


AGAIN. . . . . .  C ADDR  0000H
BACK . . . . . .  C ADDR  0005H
TABLE. . . . . .  C ADDR  0300H
```

7.5.4 GENERATED SINE WAVE



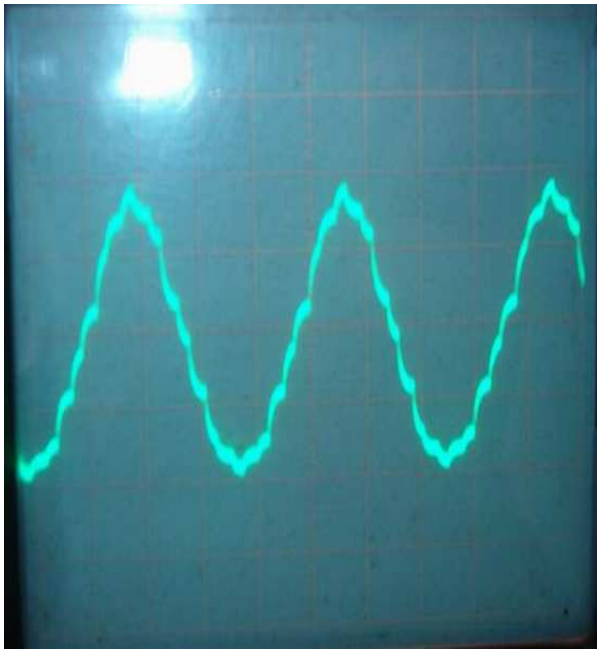


FIGURE (SINE WAVE ON STORAGE OSCILLOSCOPE) FIGURE (SINE WAVE ON CR OSCILLOSCOPE)

Figure 25

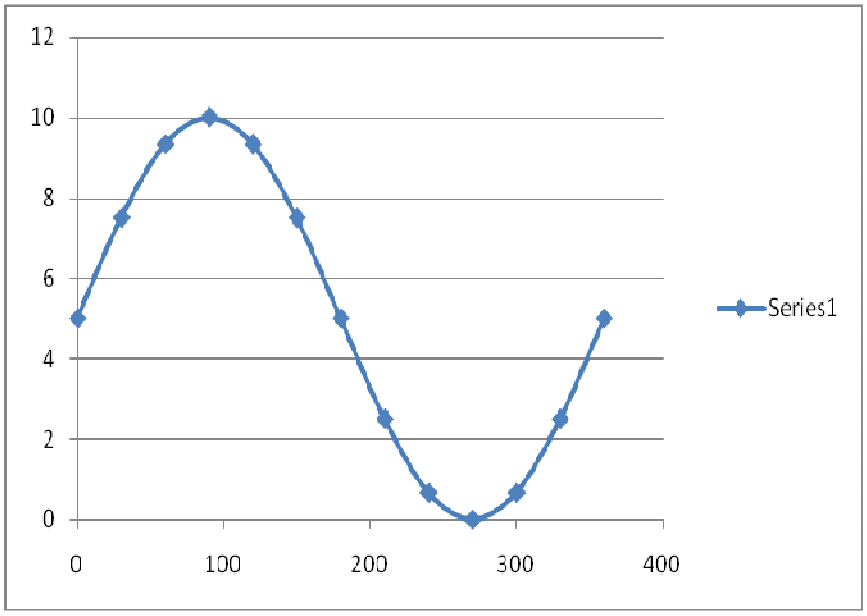


Figure 26 [SIMULATED PLOT OF SINE WAVE (V_{OUT} ~Θ)]

7.5.5TRIANGULAR WAVE GENERATION

If the sequence Y represents triangle wave, the Triangle Wave generates the pattern according to the following equation.

$Y_I = A*tri(phase[I])$

for I = 0, 1, 2, …, N – 1 and where A is amplitude and N is the number of samples**.**

tri(phase[I] is defined by the following equation.

$$Tri(phase[i]) = \begin{cases} P/90 & for\ 0 \le P < 90 \\ 2-P/90 & for\ 90 \le P < 270 \\ P/90-4 & for\ 270 \le P < 360 \end{cases}$$

Angle P (Degrees)	Tri(phase[i])	V_{out}(Voltage Magnitude) 5V+(5V×Tri(phase[i]))	Values sent to DAC(decimal) V_{out}×25.6
0	0	5	128
30	0.3333	6.6654	170
60	0.6666	8.3335	213
90	1.0000	10.0000	255
120	0.6666	8.3335	213
150	0.3333	6.6654	170
180	0	5.000	0
210	-0.3333	3.3333	85
240	-0.6666	1.6765	42
270	-1.0000	0	0
300	-0.6666	1.6765	42
330	-0.3333	3.3333	85
360	0	5.0000	128

7.5.6 COMPILED ASSEMBLY CODE FOR TRIANGULAR WAVE GENERATION USING TOP VIEW SIMULATOR (VERSION 1.2h)

```
TRIANGULAR
PAGE 1


0000                     1           ORG 0000H
0000 900300              2    AGAIN: MOV DPTR,#TABLE
0003 7AFF                3           MOV R2,#255
0005 C2E0                4    BACK:  CLR 0E0H
0007 93                  5           MOVC A,@A+DPTR
0008 85E090              6           MOV 90H,0E0H
000B A3                  7           INC DPTR
000C DAF7                8           DJNZ R2,BACK
000E 80F0                9           SJMP AGAIN
0300                    10           ORG 300H
                        11
0300 80C0EEFF           12    TABLE: DB 128,170,213,255,213,170
0304 EEC0
0306 80401100           13           DB 0,85,42,0,42,85,128
030A 114080
                        14           END


VERSION 1.2h ASSEMBLY COMPLETE, 0 ERRORS FOUND

SINE
PAGE 2

AGAIN. . . . . .  C ADDR 0000H
BACK . . . . . .  C ADDR 0005H
TABLE. . . . . .  C ADDR 0300H
```

7.5.7 GENERATED TRIANGULAR WAVE

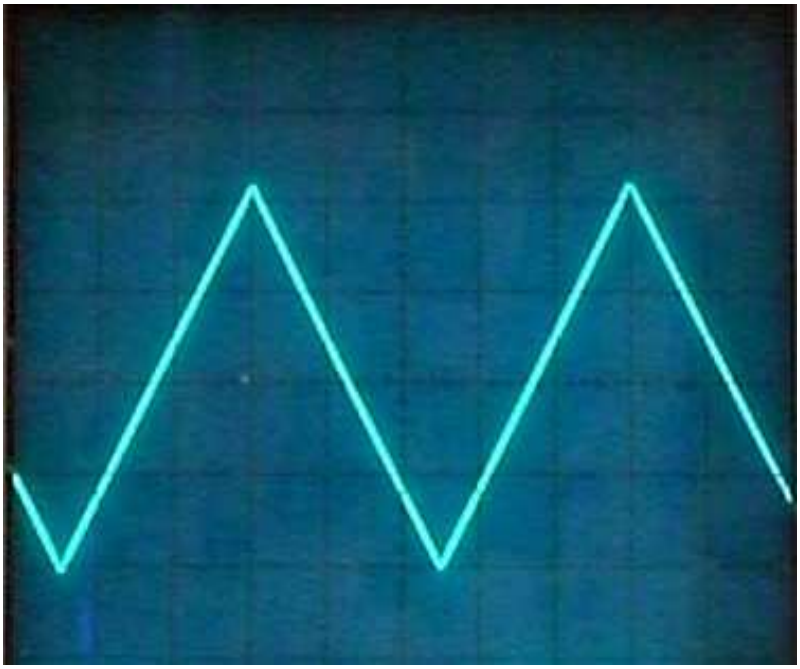


Figure 27 [PLOT OBTAINED ON OSCILLOSCOPE]

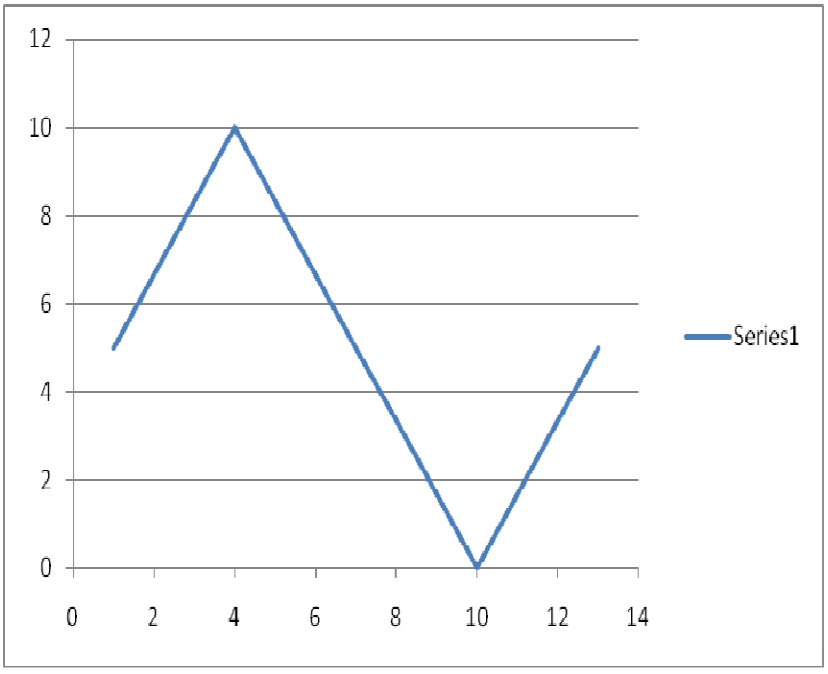


Figure 28 [SIMULATED PLOT OF TRAINGULAR WAVE]

7.5.8 COMPILED ASSEMBLY CODE FOR PWM WAVE GENERATION USING TOP VIEW SIMULATOR (VERSION 1.2h)

```
PWM
PAGE 1
  007F                1    PWM_SWAP            EQU     7FH
  007E                2    PWM_SKN             EQU     7EH
  007D                3    PWM_SKR             EQU     7DH
                      4
  0090                5    PWMKR               BIT     90H
  0091                6    PWMKN               BIT     91H

                      7
0000                  8                        ORG     0000H        ; Reset
0000 020100           9                        LJMP    BEGIN
0003                  10                       ORG     03H           ;INT 0
0003 32               11                       RETI
000B                  12                       ORG     000BH      ; Timer 0
000B 020119           13                       LJMP    PWM_MSAC
0013                  14                       ORG     13H          ; INT 1
0013 32               15                       RETI
001B                  16                       ORG     1BH        ; Timer 1
001B 32               17                       RETI
0023                  18                       ORG     23H     ; Port I/O
0023 32               19                       RETI
                      20
                      21


0100                  22                       ORG     100H
0100 758922           23    BEGIN:             MOV     89H,#22H
                      24
0103 75A892           25                       MOV     0A8H,#10010010B
0106 D28C             26                       SETB    8CH
0108 D28E             27                       SETB    8EH
```

```
010A 759000           28                        MOV     90H,#0000H
                      29
010D C290             30                        CLR     PWMKR
010F C290             31                        CLR     PWMKR
0111                  32                      START:
0111 757DDD           33                        MOV     PWM_SKR,#0DDH
0114 757EFF           34                        MOV     PWM_SKN,#0FFH
                      35
                      36
0117 80F8             37                        SJMP    START
                      38


0119 F57F             39    PWM_MSAC:           MOV     PWM_SWAP,A
011B 758CDC           40                        MOV     08CH,#0DCH
011E DF05             41                        DJNZ    R7,CHECK
0120 D291             42                        SETB    PWMKN


FINALP^1
PAGE 2
0122 D290             43                        SETB    PWMKR
0124 32               44                        RETI
0125 CF               45              CHECK:    XCH     A,R7
0126 B57E02           46                        CJNE    A,PWM_SKN,CHECK1
0129 C291             47                        CLR     PWMKN
012B B57D02           48              CHECK1:   CJNE    A,PWM_SKR,PWM_RET
012E C290             49                        CLR     PWMKR
0130 CF               50              PWM_RET:  XCH     A,R7
0131 E57F             51                        MOV     A,PWM_SWAP
0133 32               52                        RETI
                      53
                      54
                      55                         END
VERSION 1.2h ASSEMBLY COMPLETE, 0 ERRORS FOUND

PWM
PAGE 3
```

7.5.7 GENERATED PWM WAVE

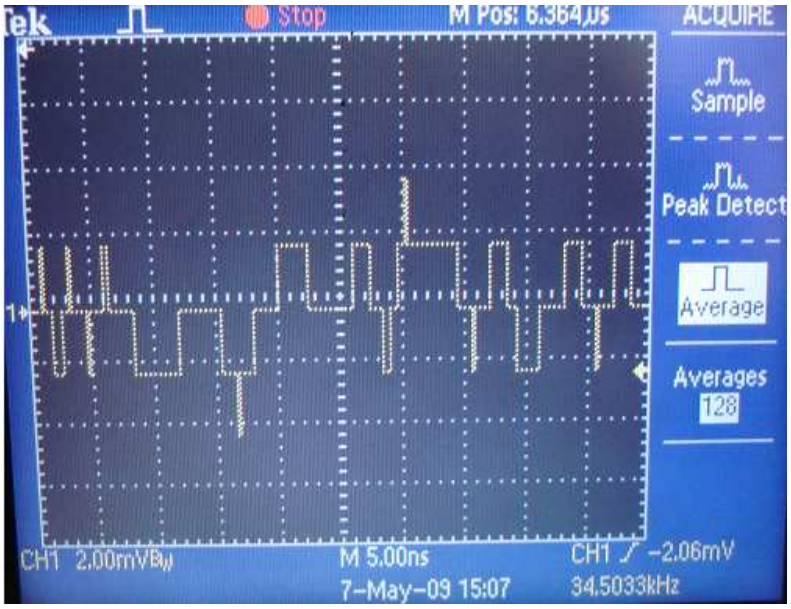


Figure 29 [PWM SIGNALS ON STORAGE OSCILLOSCOPE]

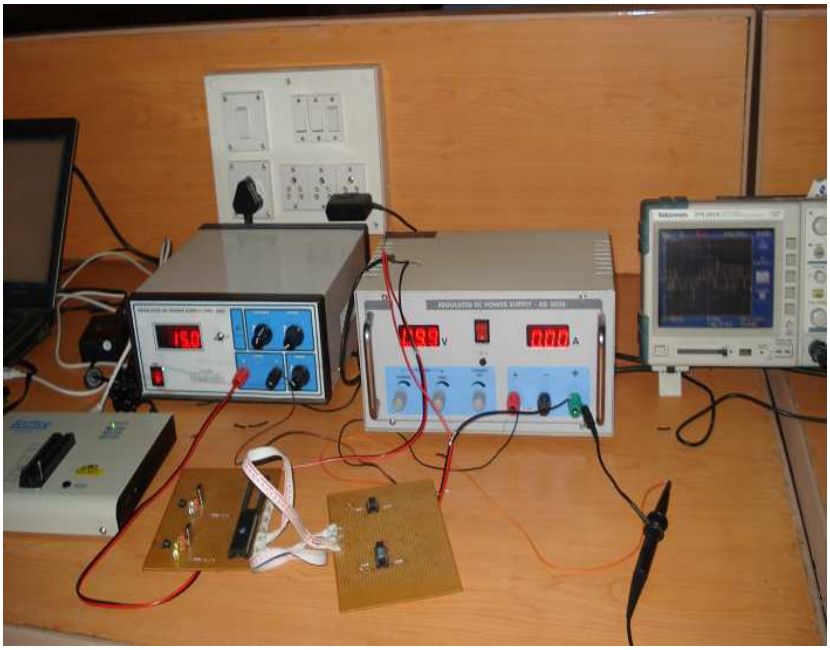


Figure 30 [COMPLETE EXPERIMENTAL SETUP]

CONCLUSION

The background study regarding the various aspects of the PWM firing scheme was studied. The carrier based PWM scheme using the POD strategy based on AT89C51 was simulated with the help of “TOP VIEW SIMULATOR (1.2H)”. Hardware involving the power circuit of AT89C51 was fabricated. Power circuit of AT89C51 was interfaced with DAC0808 for the generation of analog signal. The analog signals (sinusoidal and triangular) so generated were compared using a comparator (KF351) thereby generating PWM waves which is fed as triggering pulses to the inverters.

It’s to be noted that in this entire experiment DAC 0808, an 8 bit D/A converter is used. Thus the resolution of the waves generated is not impeccable. Thus, it’s recommended to use 12 or 16 bit D/A converter to get better wave forms.

REFERENCES AND BIBLIOGRAPHY

[1] P.S. Bhimbra, Power Electronics.

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