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[a] *LPICM, Ecole Polytechnique, CNRS, 91128 Palaiseau, France*
[b] *CEA Saclay, DSM/IRAMIS/SPCSI/LCSI, 91191 Gif-sur-Yvette, France*

Abstract

The organic thin-film transistors (OTFTs) incorporating pentacene/SU-8 interface were fabricated and characterized. SU-8, a reliable epoxy-based photoresist, is tested as a potential highly-stable polymeric gate dielectric for OTFTs. The fabricated devices showed promising electrical performance with on-off ratio up to 10^7 and field-effect mobility up to 0.56 $cm^2/V{\cdot}s$. Several device characteristics are further analyzed. There existed a leakage current path due to the uncontrolled pentacene coverage and we revealed that precise alignment of the evaporation mask of pentacene is critical for eliminating this problem. Pentacene grain formation largely depended on the growth condition on the SU-8 surface and small-grain films offered outstanding performance possibly owing to enhanced inter-domain connections. Natural degradation of the OTFTs is also discussed in terms of environmental stability and the pentacene/SU-8 transistor operated with noticeable air-stability under ambient conditions.

Keywords:

1. Introduction

Organic electronic devices are under consistent progress with its captivating advantages of mechanical flexibility, low-cost processibility, bio-chemical

*Corresponding author. Tel.: +33 1 6933 4321; fax: +33 1 6933 4333. E-mail address: chang-hyun.kim@polytechnique.edu (C. H. Kim).

compatibility, etc. In industrial point of view, some organic devices have already met the requirements for an alternative technology against the silicon-based one. Theoretical interests are also attracting researchers to investigate many peculiar phenomena observed in organic devices.

Organic thin-film transistors (OTFTs) are among the most promising candidates for addressing flexible, next-generation displays and they are theoretically valuable as well for the purpose of understanding charge injection or transport mechanisms in organic materials [1]. Focusing on the device physics, people consider the understanding of semiconductor/insulator interface as a critical issue in OTFTs because the conductive channel forms as a very thin accumulation layer on this interface [2]. In addition, in the case when the organic semiconductor is evaporated on the insulator surface (bottom-gate configuration), the surface interaction determines the microscopic nature of the semiconducting film. Because of these aspects, a great number of materials are under thorough investigation seeking desirable semiconductor/insulator combinations [3].

In this study, we adopted an epoxy resin-based polymeric film as a gate insulator for pentacene OTFTs. SU-8 is a commercially available negative photoresist which has been widely used in MEMS (microelectromechanical systems) technology for many years [4, 5]. Key features of SU-8 comprise excellent coating/planarization properties, high-aspect-ratio patterning results, and mechanical/chemical stability. It can be also used for a permanent application where cured SU-8 remains as a solid structure. Melai *et al.* recently drew attention to the dielectric property of SU-8 [6] and observed high dielectric strength of 4.43 MV/cm, which strongly motivates the utilization of SU-8 as a dielectric of the TFT architecture. With optimized process conditions, we could fabricate high-performance pentacene/SU-8 transistors showing field-effect mobility (μ_{fe}) of 0.56 $cm^2/V{\cdot}s$ and the on-to-off current ratio (I_{on}/I_{off}) of $\sim 10^7$. In order to obtain further insight of the operation, several important device characteristics are analyzed. First, we discuss the effect of pentacene coverage, which critically controls the geometrical leakage current. Next, different morphologies of pentacene films on SU-8 surface are presented with the corresponding electrical characteristics. Finally, aging effect or environmental stability of OTFTs are dealt with by repeatedly measuring the transistor performance under exposure to the ambient conditions.

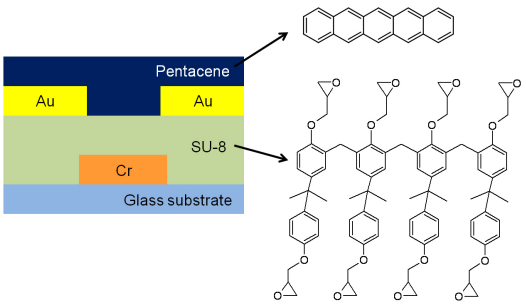

Figure 1: Bottom-gate, bottom-contact pentacene/SU-8 organic transistor with the molecular structures of pentacene and SU-8.

2. Experimental

Figure 1 contains the schematic cross-sectional view of a fabricated OTFT. On the cleaned glass substrate, 100 nm of Cr was deposited by sputtering and photolithograpically patterned as a gate electrode. Then, we spin-coated a diluted SU-8 (SU-8 2050 product of MicroChem) solution followed by a series of patterning process to define gate contact holes. The main component in SU-8 formulation is an epoxy oligomer drawn in Figure 1. During the UV exposure and the post-exposure bake steps, ring-opening reaction of epoxy groups occurs and acid-catalized polymerization takes place [5]. Each monomer has eight reactive epoxy rings (triangular groups with one O and two C atoms) so that high degree of cross-linking could be expected and high mechanical and thermal stability of the film could be achieved. The processed film was cured at 200 °C for 2 min as a final solidification step. The measured thickness of the SU-8 dielectric film is 950 nm. Au source/drain electrodes (150 nm) were patterned after sputtering deposition. Pentacene (99.9+% purity, used as-recieved from Sigma Aldrich), small-molecular p-type organic semiconductor, was finally vacuum-evaporated to form a 50 nm-thick semiconducting film.

Current-voltage (I-V) characteristics were measured using a semiconductor characterization system (Keithley 4200) in the dark under amibient atmosphere. Tapping-mode atomic force microscopy (AFM) images of pentacene films were taken using Veeco Dimension 5000 AFM system.

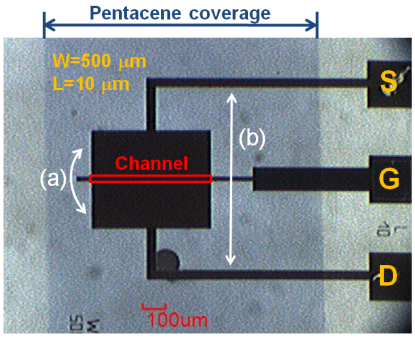

Figure 2: Optical microscopic image illustrating geometrical leakage current path on the pentacene film. S: Source, G: Gate, and D: Drain contact. (a) and (b) are indicated as possible leakage paths

3. Results and discussion

3.1. Geometrical leakage current path

While measuring a number of transistors made on the same substrate, it was found that some of them exhibited high off-current (I_{off}) of the order of 10^{-9} A, whereas the others showed nearly perfect off-state (I_{off} near 10^{-12} A, the lowest range of the detection limit) as shown in Figure 3. From the careful observation of each transistor with the microscopic image, we found that this is due to the geometrical leakage current path (between source and drain) on the pentacene layer.

A representative top-view image of the transistor is shown in Figure 2, which, associated with Figure 1, helps giving a proper interpretation of the geometrical leakages. The basis of the leakage paths originates from the fact that pentacene is evaporated through a shadow mask that has a larger opening than the channel area. Accordingly, the pentacene film covers an area that largely exceeds that of the channel. The pentacene coverage corresponds to the blue area in Figure 2, while uncovered regions look more transparent. Two possible source-drain leakage paths can be thought of, path (a) and path (b) in Figure 2. Path (a) is located at left hand side, where a high source-drain fringe field takes place [7]. Path (b) spreads over a wide area delineated by the source and drain leads. We note that path (b) is unlikely to significantly contribute to the drain current because the distance between the source and drain leads is much larger than the channel length (L).

Figure 3 shows that the leakage current is strongly influenced depending on the presence of pentacene beyond the left border of the source-drain elec-

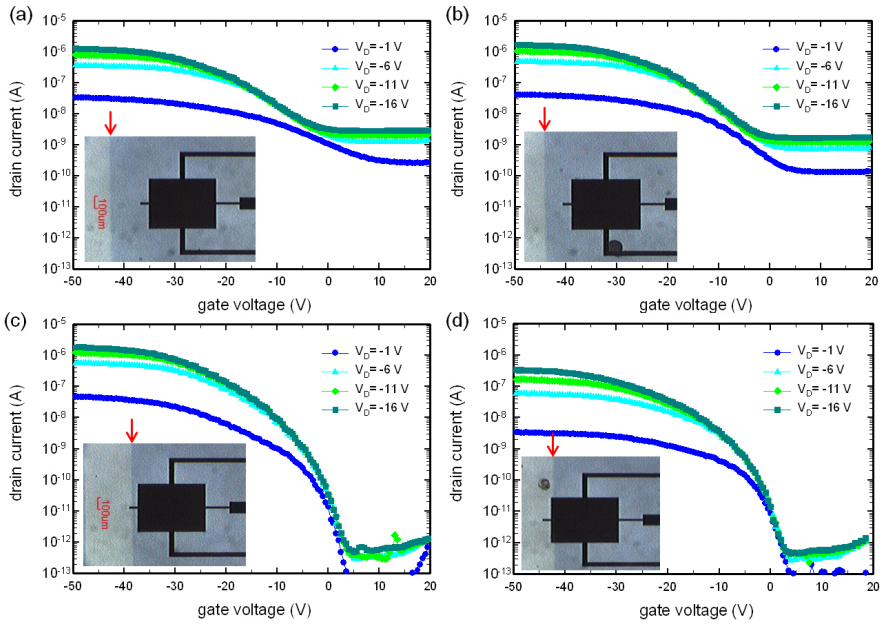

Figure 3: Transfer curves of four different transistors with the same channel geometry (W = 500 μm and L = 10 μm). (a) and (b): transistors with geometrical leakage path. (c) and (d): transistors without leakage path. Each inset is the microscopic picture of the near-channel region.

trodes. The insets show that the coverage of pentacene may largely change due to an imperfect mask alignment. When pentacene coverage exceeds the source-drain edges (Figures 3a and 3b), there exists a floating pentacene layer on path (a) that is not affected by the gate voltage (V_G) but is influenced by the fringe field between source and drain. The transfer curves confirm this argument; when V_G is positive (off-state), a substantial drain current (I_D) flows that increases with the drain voltage (V_D), which would correspond to an increase of the fringe field. Conversely, Figures 3c and 3d show that in the case when the edge of the pentacene layer is aligned with that of the source-drain electrodes, I_{off} is much lower and can now be attributed to the leakages through the insulator. In this case, I_{on}/I_{off} amounts to 10^6. This finding emphasizes the importance of precise mask alignment and/or the necessity of mask design that avoids geometrical paths to get rid of parasitic leakages.

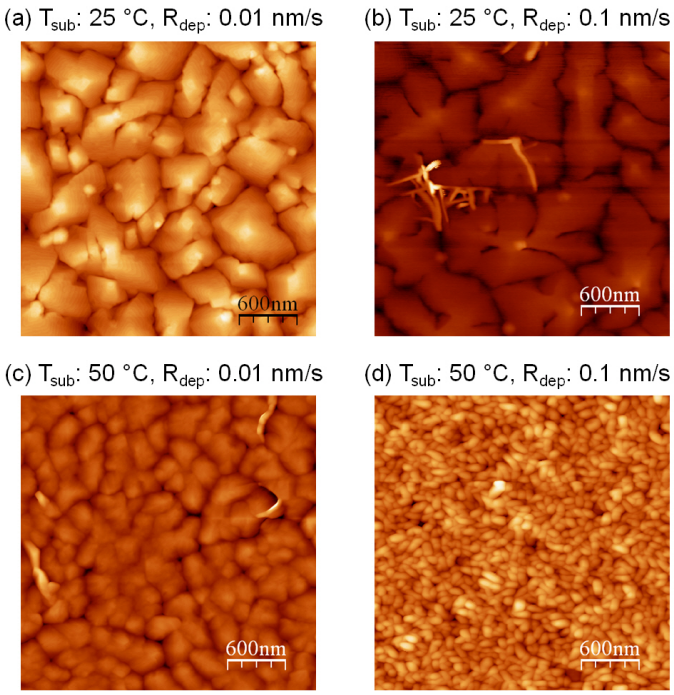

Figure 4: AFM images of the pentacene layers with different deposition parameters (scan size: 3×3 μm^2).

3.2. Morphology of pentacene films

Pentacene is known for its ability to form highly-ordered film on a variety of surfaces and this is regarded as a key feature that results in a high field-effect mobility in thin-film phase [8]. Both surface material and growth condition can significantly affect the film-forming process and the final morphology of polycrystalline thin film.

In order to investigate the morphological variation of pentacene on SU-8 surface, we controlled two critical deposition conditions, namely substrate temperature (T_{sub}) and deposition rate (R_{dep}), and scanned each film with AFM. In spite of the difficulty in understanding the correlation between the deposition condition and the film property of pentacene [8], a general rule in vacuum evaporation is that grain (or domain) size tends to increase with increasing T_{sub} and decreasing R_{dep}. Representative data can be found in the article of Yanagisawa *et al.* with the AFM morphology of pentacene films on SiO_2 substrate [9]. Our results shown in Figure 4 seem to be at variance with this rule. High T_{sub} (50 °C) led to much smaller grains. However, a

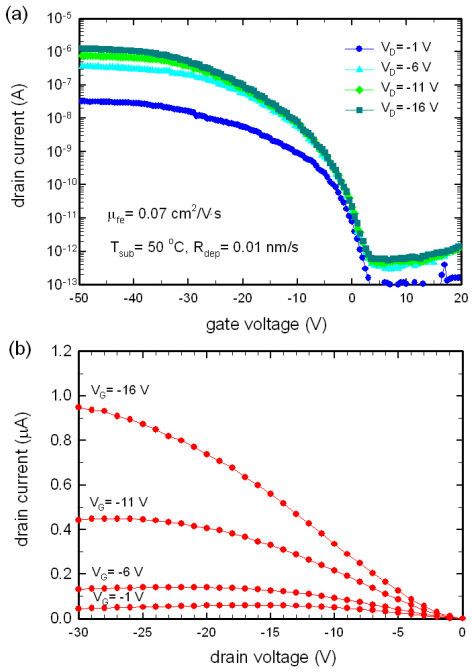

Figure 5: (a) Transfer and (b) output characteristics of an OTFT with pentacene evaporated with T_{sub} = 50 °C and R_{dep} = 0.01 nm/s (W = 500 μm and L = 20 μm).

careful observation of the grain shapes infers that the growth mode itself change with the temperature. The films with T_{sub} = 25 °C (Figures 4a and 4b) exhibit pyramidal or dendritic grains [9] that are often observed in the case of layer growth of pentacene with relatively large domains. By contrast, 50 °C-deposited films (Figures 4c and 4d) contain very small and uniform grains. Taking into account the low surface energy of our SU-8 film (measured water contact angle of 84 °), high T_{sub} could enhance pentacene-pentacene aggregation favoring island-mode growth of densely-packed grains [10]. We fabricated two sets of transistors with fixed T_{sub} (50 °C) and different R_{dep} (0.01 and 0.1 nm/s). The measured electrical characteristics are shown in Figures 5 and 6 and they support the above argument on the island growth. Even though the grain boundaries can normally contain trapping sites with energy barrier [11], the TFT with the smallest grains (Figures 4d and 6) showed improved transistor performance when compared to the case of middle-size grains (Figures 4c and 5). We can explain this morphological effect on the electrical performance as follows; when the island

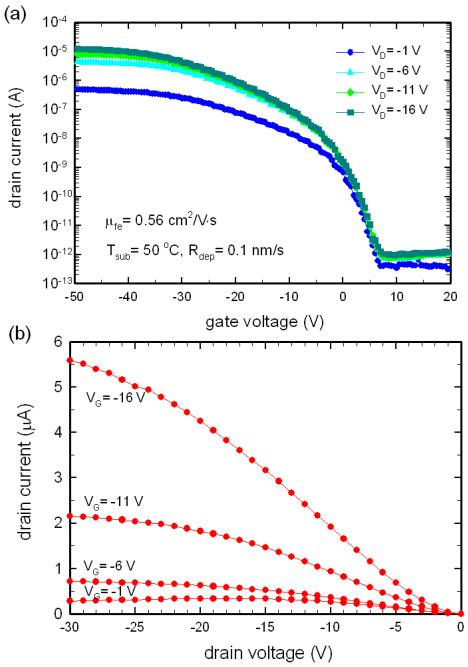

Figure 6: (a) Transfer and (b) output characteristics of an OTFT with pentacene evaporated with T_{sub} = 50 °C and R_{dep} = 0.1 nm/s (W = 500 μm and L = 20 μm).

mode dominates the initial growth, the grains tend to expand their volume from the first stage so that they can be closely linked to one another [10]. As a consequence, the small-grain film probably could have well-connected domains on the conducting channel with less inter-domain voids.

The field-effect mobility μ_{fe} of each TFT is extracted from the slope of square-root I_D in saturation regime [1] by using

$$\sqrt{I_{D,sat}} = \sqrt{\frac{W}{2L} C_i \mu_{fe} |V_G - V_T|} \tag{1}$$

where W is the channel width, L the channel length, C_i the insulator capacitance per unit area, and V_T the threshold voltage. Extracted field-effect mobility values are 0.07 cm^2/V·s (R_{dep} = 0.01 nm/s) and 0.56 cm^2/V·s (R_{dep} = 0.1 nm/s) respectively. The best performance shown in Figure 6 makes certain of the potential of SU-8 as a reliable dielectric material for OTFTs. It provides hydrophobic surface for well-ordered organic film (high μ_{fe}) and the gate insulation is excellent (I_{on}/I_{off} reaching 10^7). Slight upward bending

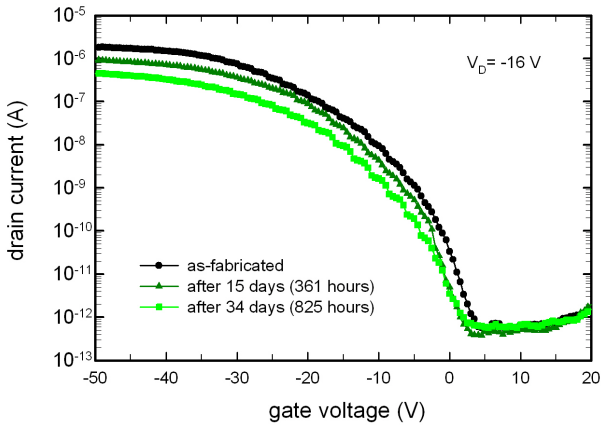

Figure 7: Change in the transfer curve showing degradation of the electrical performance of pentacene/SU-8 TFT. Data obtained with a test device with $W = 500$ μm and $L = 10$ μm.

of the output curves at low V_D (linear regime) can be accounted for by the contact-resistance effect that is usually observed in OTFTs with the coplanar type device geometry (bottom-gate, bottom-contact) [12, 13].

3.3. Environmental stability

Long-term stability of OTFTs has been often pointed out as a critical factor for practical electronic products because of its inherent chemical reactivities that normally degrade the electrical performance upon operation in ambient atmosphere. In general, fast degradation of organic transistors originates from the chemical reaction of organic semiconductors with O_2 and H_2O [14]. Many studies are thus devoted to the encapsulation/passivation techniques in order to maintain the initial performance of OTFTs [15].

To estimate the environmental stability of unpassivated pentacene/SU-8 transistors, we monitored the degradation of its electrical performance with time. The test device was left at ambient condition right after the initial measurement and the I-V characteristics were repeatedly measured. Figure 7 shows selected time-varying transfer curves of the test transistor. Even though I_{off} remains stable during the period, degradation of the transistor is clearly seen as a reduction of I_{on}. From the extracted μ_{fe} and V_T of each data, we could realize that the major cause of the degradation is the decrease of μ_{fe} (V_T does not change significantly).

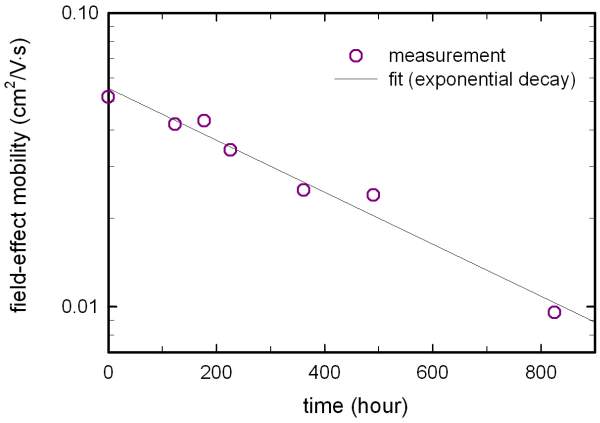

Figure 8: Decrease of the field-effect mobility drawn in semi-log plot as a function of air-exposure time. Experimental data (circle) was fitted to the exponential decay function (solid line).

The variation of μ_{fe} as a function of time is presented in Figure 8. Measured data could be well fitted to an exponential function as assured by the linearity of the graph in semi-log plot. Time-dependence of the field-effect mobility is then expressed as

$$\mu(t) = \mu_0 \exp\left(-\frac{t}{\tau_d}\right) \tag{2}$$

where $\mu(t)$ is the time-varying mobility, t is the air-exposure time, μ_0 the initial mobility, and τ_d the degradation lifetime. Fitted parameters in Equation (2) are $\mu_0 = 0.055$ cm^2/V·s and $\tau_d = 490$ hours. Exponential decay of the mobility in pentacene TFTs is often reported. Our extracted degradation constant τ_d compares favorably to other results with different dielectric materials [14, 16] and this feature can also be attributed to the chemical stability of SU-8. Fully cross-linked SU-8 film is chemically inert so that it could resist well the diffusion of contaminating molecules into the insulator and the pentacene/SU-8 interface. The origin of decreasing mobility is explained by trap-state modeling in [17]; the aging effect could be related to the additional tail states induced by reaction of pentacene molecules with adsorbed water or oxygen.

The subthreshold swing S is another important device parameter. It is a measure of how much V_G is required to switch on a transistor from the

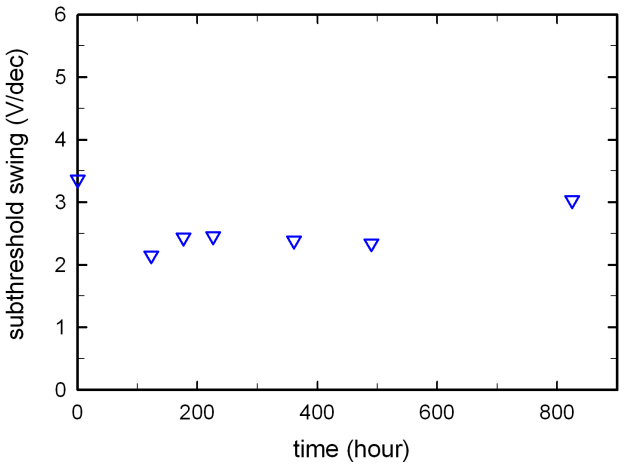

Figure 9: The subthreshold swing S as a function of air-exposure time. The values were extracted from the transfer characteristics measured at $V_D = -16$ V.

off-state [18] and can be estimated by

$$S = \frac{dV_G}{d\log(I_D)}. \tag{3}$$

Figure 9 shows that the substhreshold swing S remained relatively stable during the entire test period. The physical meaning of the subthreshold swing can be explained by the density of deep trap states [18, 19]. Therefore, we can infer that there is no significant increase of deep trap states in pentacene or SU-8/pentacene interface, which is advantageous in terms of operational stability of OTFTs.

4. Conclusion

The pentacene OTFTs with SU-8 polymeric insulator were fabricated and analyzed. Highly stable epoxy resin, SU-8, could be successfully adopted as a dielectric layer showing very low gate leakage current. Excessively wide pentacene layer provided geometrical leakage path that resulted in abnormally high off-state drain current. Precise control of the mask alignment is emphasized with this point. Pentacene films with different deposition conditions (substrate temperature and deposition rate) were imaged by AFM and showed significant changes in film morphology. It was found that small-size, compact pentacene grains are of great advantage to the charge transport at

the channel owing to enhanced inter-domain connections on low-energy SU-8 surface. Environmental stability of pentacene/SU-8 transistor was finally discussed by monitoring degradation of the electrical performance. Unpassivated OTFT could operate steadily with small reduction in field-effect mobility during the test period of 34 days after fabrication. Time-dependent degradation of the field-effect mobility was fitted to the empirical exponential decay function with the degradation lifetime of 490 hours. We believe that high quality SU-8 film can be widely adopted for OTFTs making use of its well-known mechanical/chemical stability and also its reliable dielectric property presented in this study.

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