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An architecture for ultra-low-voltage ultra-low-power compressed sensing-based acquisition systems

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***Abstract*—Compressed Sensing (CS) has been addressed as a paradigm capable of lowering energy requirements in acquisition systems. Furthermore, the capability of simultaneously acquiring and compressing an input signal makes this paradigm perfectly suitable for low-power devices. However, the need for analog hardware blocks makes the adoption of most of standard solutions proposed so far in the literature problematic when an aggressive voltage and energy scaling is considered, as in the case of ultra-low-power IoT devices that need to be battery-powered or energy harvesting-powered. Here, we investigate a recently proposed architecture that, due to the lack of any analog block (except for the comparator required in the following A/D stage) is compatible with the aggressive voltage scaling required by IoT devices. Feasibility and expected performance of this architecture are investigated according to the most recent state-of-the-art literature.**

I. Introduction

The development of ultra-low-voltage circuits has received increased attention in recent years. To mention just an example, we can consider the Internet-of-Things (IoT) paradigm, which makes use of a plethora of autonomous (i.e., battery-powered or harvester-powered) sensors connected to a (typically wireless) communication network [1], [2]. In this context, the requirement of having these sensors as autonomous sets a limit not only to the available power, but also to the supply voltage, that can be limited in many cases to small fractions of Volt.

Nevertheless, the design of circuits operating at such a low supply voltage is critical. MOS circuits needs to be designed to operate in the near- and sub-threshold regime, with the cost of an increased design complexity and of an operating speed (or bandwidth) reduced to the order of kHz, or even lower. Anyway, this option has been shown to allow minimum-energy operations for low-performance applications [3]–[5], being the ideal choice for this class of use-cases.

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Indeed, differences can be observed according to the hardware blocks of interest. As an example, the design of digital logic [4], [6], [7] and memory cells [8], [9] has been pushed to supply voltages down to a few hundred millivolts, and a large number of solutions can be found in the recent Literature with circuits operating with a supply voltage between $200\,\mathrm{mV}$ and $300\,\mathrm{mV}$.

Conversely, the design of analog hardware blocks at such a supply level, with particular reference to operational transconductance amplifiers (OTAs), appears to be more critical. Many solutions can be actually found [10], but performance is typically low. The most common techniques are the inverter-based topology approach [10]–[12], where pseudo-differential pairs only are achievable, and the bulk-driven approach [10], [13], [14], based on the bulk transconductance g_{mb} instead of the much higher gate transconductance g_m. These limitations strongly affect performance and, to the best of the authors' knowledge, complex analog systems such as biomedical front-ends [15] or demodulators for communications systems [16] still requires a supply voltage in the order of 0.6–$0.8\,\mathrm{V}$.

Instead, if we focus on analog-to-digital (A/D) conversion only, a very large numbers of A/D converters (ADC) prototypes designed to operate with a supply voltage between $200\,\mathrm{mV}$ and $300\,\mathrm{mV}$ can be found [17]–[19]. This is possible mainly thanks to the very simple architecture required by a capacitive array-based successive approximation register (SAR) topology [20], that relies on a simple comparator (that can also be implemented in the time domain as in [19]) as the only required analog block (excluding pass transistors), allowing to operate without the need of complex power-management circuitry.

The aim of this paper is to investigate the possibility to implement an ultra-low-voltage autonomous sensor whose acquisition system is based on the Compressed Sensing (CS) paradigm. CS is a signal processing technique [21]–[23] that, by replacing the standard ADC with a more generic Analog-to-Information converter (AIC), allows to simultaneously acquire and compress a signal directly in the analog domain, hence resulting in a lower number of acquisitions per unit time required to correctly reconstruct the input signal. This paves

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the way to sub-Nyquist sampling, with a potentially large energy saving at the sensor node, under the assumption that energy required by the analog circuitry (pre-processing and ADC) is relevant.

Nevertheless, the pre-processing of the input signal required by CS, despite being very simple (a linear combination by means of random-like coefficients, locally generated or stored into a digital memory, is enough), typically requires additional analog hardware, reducing the compliance towards an ultra-low-voltage implementation.

With this aim in mind, we analyze the most important AICs proposed so far in the literature, exploring their architectures and identifying possible issues when targeting implementation in an ultra-low-voltage environment. As a fundamental assumption of this paper, based on the above short literature survey, we consider a SAR architecture (including all its circuital blocks) easily implementable in an ultra-low-voltage design, whereas OTA not easily implementable. Even if this is a strong simplification of such a complex problem, it allows us to easily distinguish between compliant and non-compliant CS architectures.

The result is that standard approaches do not well-fit the requirements of an aggressive voltage scaling. Conversely, an innovative architecture we recently proposed, constructed as a standard charge-redistribution SAR architecture with a few additional pass transistors, fits these requirements extremely well. By considering performance and limits of a state-of-the-art implementation of a low-voltage SAR architecture, we can also extrapolate performance and limits of a CS-based low-voltage acquisition system.

The paper is organized as follows. In Section II we introduce the basic concepts of the CS paradigm. Then, we propose in Section III a survey analyzing the architecture of the most important CS-based acquisition system proposed so far in the Literature, and their disadvantages in a low-voltage implementation. Conversely, the innovative architecture we recently proposed in [24], and that fits well the low-voltage paradigm, is described in Section IV. The feasibility and theoretical performance of this architecture assuming a design based on the state-of-the-art low-voltage SAR technology is described in Section V. Finally, the conclusion is drawn.

II. Compressed Sensing fundamentals

Coherently with common sense, when the informative content of a signal is much lower than what its bandwidth would suggest, the signal is known to be *compressible*. In this context, many algorithms can be applied to reduce the number of scalars needed to correctly represent the original signal [25].

The main difference between CS and a traditional compression scheme is the distribution of computational complexity between encoder end decoder stage. Whereas in the standard approach, based on the assumption that the signal is compressed only once and decompressed many times, the most complex and power-hungry stage is the encoding one, the situation is specular for a CS setup. Here, encoding and compression are obtained as a single and very simple operation, whereas complexity is transferred to the decoding stage. This fits perfectly the IoT scenario, where acquisition is required on a small, low-power sensor node, while reconstruction is typically completed in the cloud, with no energy constraints.

More formally, the compressibility condition for CS is the following one. Let us consider an input signal $x \in \mathbb{R}^n$, that could be either the discrete-time representation $\{x(T), x(2T), \ldots, x(nT)\}$ of a signal over a time window $0 \leq t \leq nT$ and sampled with a period T, or the collection of samples $\{x_1(\tau_0), x_2(\tau_0), \ldots, x_n(\tau_0)\}$, taken at a given time τ_0, of a n-dimensional signal $\boldsymbol{x}(t)$. Let us simply indicate each signal sample within the collection as x_k, with $k = 1, 2, \ldots, n$.

CS theory can be applied if the following assumptions are satisfied: i) let $D \in \mathbb{R}^{n \times n}$ be an arbitrary, typically orthonormal, basis; ii) let $\xi \in \mathbb{R}^n$ be the representation of x in terms of D, i.e., the vector such that $x = D\xi$; iii) let $s \in \{0, 1\}^n$ the *support* of x, i.e., the vector such that $s_j = 0$ if $\xi_j = 0$, and $s_j = 1$ otherwise; iv) x is *sparse* in D, i.e., s has at most $\kappa \ll n$ non-null elements. The latter assumption can formally be written as $\|s\|_1 \leq \kappa$, or equivalently, $\|\xi\|_0 \leq \kappa$, where the notation $\|\cdot\|_p$ refers to the standard ℓ_p norm.

Note that the last assumption is the most critical one, as very few real signals are truly sparse. More commonly, real signals can only be approximated as sparse, i.e., they concentrate most of their energy (but not *all* their energy) on a few elements of D. In this case, CS can still be used as a *lossy* compression algorithm.

In the compression phase, the signal x is encoded into a set of m scalar quantities called *measurements*, and arranged in the vector $y \in \mathbb{R}^m$. The required operation is a simple linear combination (or *projection*) according to the coefficients stored in the sensing matrix $A \in \mathbb{R}^{m \times n}$

$$y = Ax = AD\xi. \tag{1}$$

that can be reformulated component-wise as

$$y_j = \sum_{k=1}^{n} A_{j,k} x_k, \quad j = 1, \ldots, m \tag{2}$$

with $A_{j,k}$ is the element of A at the intersection of the j-th row and k-th column.

Traditionally, the efficiency in compression is defined by the Compression Ratio $CR = m/n$.

In this paper we focus on the encoding process, and we consider the reconstruction problem, as well as reconstruction performance, out of scope.

Suffice it to say that recovering x from y is an ill-posed problem. In fact, many vectors ξ exist satisfying $y = AD\xi$. In standard CS theory [21], [26], assuming CR is not too low, the correct reconstruction is obtained by looking for the sparsest $\hat{\xi}$ among all possible ξ satisfying equation (1). Many algorithms have been proposed to solve this problem either in an exact or an approximated way [27]–[32].

Performance in terms of quality of the reconstructed signal depends on many factors. The correct choice of n, A and CR according to the class of input signal is fundamental for

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any system, and many trade-offs have been proposed so far [33] for ensuring correct reconstruction. A topic that is still open is the resolution required to sample the y_j measurements, as a relation with overall reconstruction quality is complex due to the strong non-linearity of the reconstruction algorithm [34]. Yet, it is possible to observe that most of the solutions proposed in the literature [35]–[37] use a resolution of 10 or 11 bits.

At the same time, trade-offs capable of reducing hardware complexity have been proposed. As an example, one of the most common options is to limit $A \in \{-1,1\}^{m\times n}$ or $A \in \{0,1\}^{m\times n}$ to reduce the complexity of a four-quadrant multiplication to a simple sign inversion (trivially obtainable in a fully differential implementation) or a pass/block signal, respectively. Another way is to design, using a methodology such as in [38], the elements of A to maximize their *rakeness* [39], i.e., the energy collected by CS samples, in a way similar to what a rake receiver does in a communication system [40], [41].

Obvious to say that, with the notation $A \in \{-1,1\}^{m\times n}$ or $A \in \{0,1\}^{m\times n}$, we do not want to say that the gain has to be exactly 1 or -1, but we indicate a *class* of modulations only. For example, the $A \in \{0,1\}^{m\times n}$ stands for any systems that can multiply input samples either by zero or by non-zero values. The non-zero values can be even different element by element, as the fundamental assumption for the CS to work is that $A_{j,k}$ are shared between encoder and decoder, and that are randomly drawn, but there are no constraints on the particular distribution to be used.

Therefore, the second, fundamental assumption of this paper is that parameters of a CS system can be tuned to allow it to correctly work. This assumption allows us to focus on the circuital architecture only, and investigate which hardware implementations of (1), among all known ones, are suitable for a low-voltage implementation, without the need for considering reconstruction performance of each architecture.

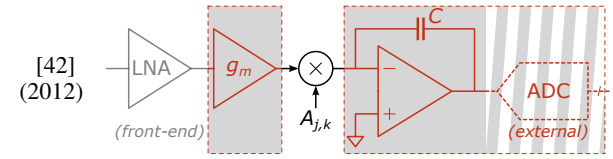
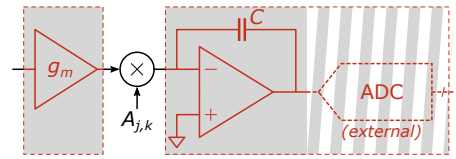
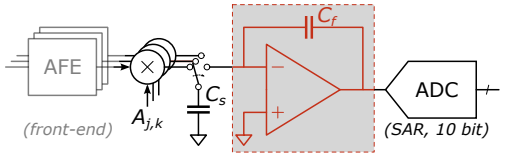
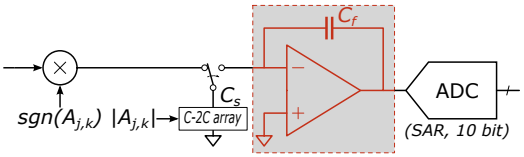
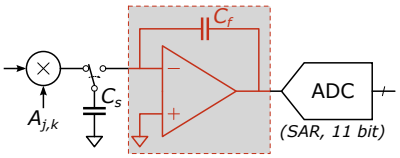
III. Architectures of AIC in the State-of-the-Art

Many prototypes have been proposed so far in the Literature for implementing a CS encoder capable of approximating (1). We focus here on fully *analog* implementations. The reason is that, even if it is possible to implement (1) in the digital domain by first digitizing all x_k and then computing the linear combination [44], this would be equivalent to a standard acquisition-and-compression approach, whose lower energy bound is given by the n digital conversions, with no advantages from the sub-Nyquist capabilities of the CS.

All prototypes are extremely different in operating frequency, input signal families, and target value of n. None of them prevails under every operating condition; here we would like to focus only on their architecture, identifying why an implementation in an ultra-low voltage would be critical.

Furthermore, we also focus on the hardware block required to compute (2) and to get a single measurement. All other measurements can be either computed reusing the same circuital block in a time-interleaving approach, or on additional instances of the considered block.

TABLE I
Summary of solutions proposed to implement a CS encoder exploiting (2), highlighting hardware blocks (mainly, amplifiers) that could be critical in a low-voltage application.

Ref.	Schematic
[42] (2012)	
[43] (2012)	
[35] (2014)	
[36] (2014)	
[37] (2016)	

A visual comparison of integrated solutions recently proposed in the literature is shown in Tab. I. For each architecture considered, a simplified schematic is drawn, highlighting the hardware block that may be problematic in a low-voltage implementation, according to the two main assumptions of this paper: i) we consider SAR-based architectures suitable for a low-voltage implementation, but not OTA-based ones; and ii) a set of parameters allowing CS to correctly operate can always be found. Note that a few among the considered solutions embed also an analog front-end. We neglect it as, technically, it does not strictly belong to the AIC. Hence, for a fair comparison, we focus only on the hardware part computing (2) and the following ADC.

In [42] and in [43] two AICs designed for radio-frequency (RF) signals are presented. The prototype in [42] is a sub-Nyquist rate receiver for radar pulse signal, whereas in [43] a data acquisition system for multi-tone RF communication is presented. The two architectures are very similar: both embed a passive mixer that limits $A_{j,k} \in \{-1,1\}$ by exploiting the differential structure. However, they also require an OTA-

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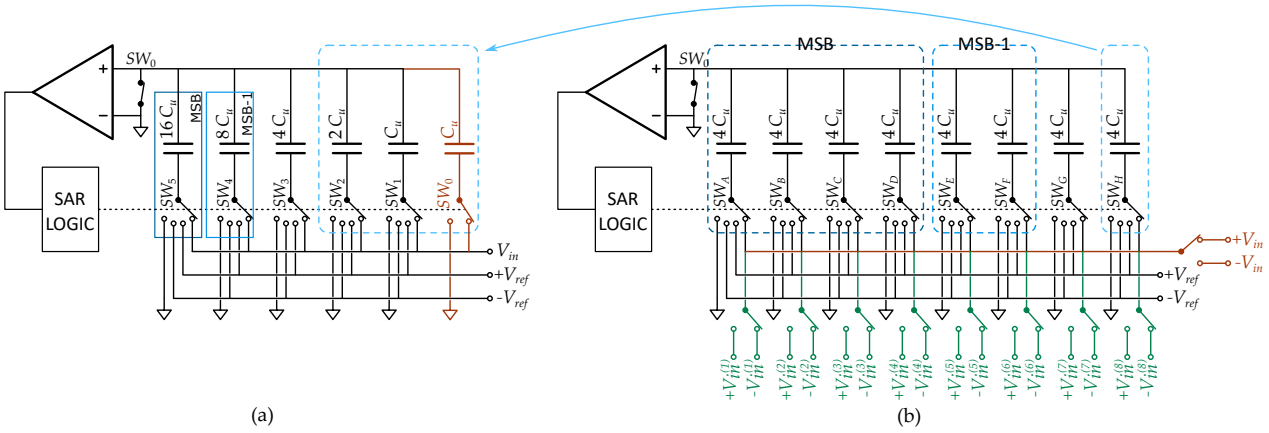

Fig. 1. Proposed low-voltage compliant CS architecture. (a) Basic architecture of a simple SAR architecture, featuring a capacitive array. (b) Rearrangement of the capacitive array in order to allow the SAR converter working as CS based AIC.

based continuous-time integrator, that could be critical in a low-voltage setting. The prototype in [42] is designed in 90 nm CMOS technology, running at 1.5 V; that in [43] is designed in 90 nm CMOS technology, but the operating voltage in undeclared. Both implementations rely on an external ADC, for which no considerations can be provided.

Solutions targeting lower frequency signals typically rely on a switched-capacitors, OTA-based integrator architecture, followed by a SAR converter. In [35] the target application is given by multi-lead intracranial EEG signals. CS is not applied by integrating the signal in the time domain; instead, the x_k samples in (1) refer to values obtained sampling the k-th lead. A passive mixer is adopted, implementing $A_{j,k} \in \{0, 1\}$ by means of simple pass-transistors. The most problematic part in terms of low-voltage implementation is, again, the OTA-based integrator, whereas both the SAR and the pass-transistor based mixer do not represent a problematic hardware. The prototype, designed in 0.18 µm CMOS, is operating with a 1.2 V power supply.

The architectures proposed in [36] and [37] are similar to that in [35], except that they consider a 1-D input signal, and the x_k in (2) are sampled at different time steps. The prototype in [36] is an analog front-end for ECG signals. The mixer is passive, and approximates $A_{j,k} \in \mathbb{R}$. The differential architecture is exploited to implement the sign change, and a 6-bit multiplying DAC relying on a C-2C array that replaces the sampling capacitor is used. This solution is based on pass-transistors only and is suited for almost any voltage supply. Nevertheless, an integrator is still required, that is based on an OTA that, according to authors, is designed to work in the sub-threshold region but still requires a power supply between 0.9 V and 1.2 V. The prototype is implemented in 0.13 µm CMOS.

The last architecture we consider is that described in [37]. By constraining $A_{j,k} \in \{-1, +1\}$, the architecture embeds a fully passive mixer exploiting the fully differential architecture. However, the architecture shares the same problems identified in the last two solutions, given by the OTA used in the switched capacitor integrator. The prototype is implemented in 0.18 µm CMOS and is operated at a 1.8 V power supply voltage.

In conclusion, all these solutions (including that based on a pass-transistor multiplier and on a SAR converter) rely their hardware implementation on an OTA. This represents the most important issue in a low-voltage implementation.

IV. Proposed Architecture

We recently proposed [24] an innovative architecture, whose working principle is detailed in Fig. 1.

In part (a) of the figure, a standard capacitive array-based SAR is depicted. For the sake of simplicity, a 5-bit one is considered, with a weighted array whose capacitors range from $16C_u$ down to C_u. In the figure we have also included, depicted in red, the additional C_u capacitor closing the array, that ensures that the weights implemented by the capacitance ratios are truly powers of two. Sometimes this capacitance is not used, leading to a small variation in the input range of the conversion. Other times this capacitance is replaced either by a binary-weighted secondary array (connected by means of an attenuation capacitance C_a) or to a C-2C secondary array. Both solutions allow to increase the precision of the SAR without exponentially increasing the size of the capacitive array.

Referring to the simplest structure of the figure, the working principle can be described as follows. The array is first used to sample the input signal V_{in}; after that, all switches SW_5 downto SW_0 go to ground and SW_0 opens, so that the voltage at the non-inverting node of the comparator goes to $-V_{\text{in}}$. Then, switches are changed sequentially to move the voltage at the inverting node the closest possible to ground. The final position of the switches gives the digital conversion of the $-V_{\text{in}}$ voltage [20].

The basic idea to turn the SAR converter into a AIC with $A_{j,k} \in \{-1, 1\}$ is sketched in Fig. 1(b). Basically, we can split and/or recombine (by an appropriate driving of the respective switches) the capacitors within the array to obtain capacitors of

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equal size, $4C_u$ in the example. The structure thus obtained can be used to sample different values on each capacitive element.

In a time-interleaving fashion (red modifications in the figure), at time t_1 the switch SW_A samples either $V_{\rm in}(t_1)$ or $-V_{\rm in}(t_1)$ on the first capacitance, then it goes to high impedance; at time t_2, the switch SW_B samples either $V_{\rm in}(t_2)$ or $-V_{\rm in}(t_2)$ on the second, and so on. At the end of the sampling phase, all switches go to ground, and due to charge redistribution, the voltage at the non-inverting node (playing the role of $-V_{\rm in}$ in the conversion) goes to

$$-\sum_{k=1}^{8} A_{j,k} V_{\rm in}(t_k) \tag{3}$$

with $n = 8$, $A_{j,k} = \pm 1/8$, $k = 1, \ldots, 8$, as either $V_{\rm in}(t_k)$ or $-V_{\rm in}(t_k)$ is sampled over a $4C_u$ capacitance, and then the corresponding charge redistributed over a $32C_u$ capacitance. This matches (2) if we replace the generic input signal x with the voltage signal $V_{\rm in}$.

In a multi-lead setting (green modifications), at $t = \tau_0$, the first capacitance is charged by SW_A either to $V_{\rm in}(\tau_0)$ or $-V_{\rm in}(\tau_0)$ and so on. When all switches go to ground, the voltage at the non-inverting node goes to

$$-\sum_{k=1}^{8} A_{j,k} V_{\rm in}^{(k)}(\tau_0) \tag{4}$$

that, as in the previous case, matches (2) with $n = 8$, $A_{j,k} = \pm 1/8$, $k = 1, \ldots, 8$.

The working principle described above can be easily extended for the case $A_{j,k} = \{0, 1\}$, and even to cover the presence of a binary-weighted or C-2C secondary array. As an example, we would like to consider the simple case when the additional C_u is not included in the array. Equations (3) and (4) are slightly changed as follows. The overall size of the array is now $31C_u$, and the charge is redistributed on capacitors with different size (the last of them for $k = 8$ is now $3C_u$). So, $A_{j,k} = \pm 4/31$, $k = 1, \ldots, 7$, and $A_{j,8} = \pm 3/31$. Indeed, this is not an issue for a CS system, as already observed in Section II.

This suggests that whatever the actual SAR configuration is (e.g., independently of the size of the array and of the presence of any secondary array of any type), it is always possible to reassemble capacitors to get a charge redistribution similar either to (3) or to (4).

V. Feasibility of a low-voltage CS-based design

The only transistor-based blocks in the proposed architecture are switches, a comparator and the digital control logic. So, based on the two assumptions that *i*) a SAR-like architecture is feasible for low-voltage operations; *ii*) the CS can always be tuned to work properly; the proposed architecture is feasible for a low-voltage implementation.

In more details, let us consider a standard CS architecture like that described in [35], where a 8-lead signal is acquired by means of a CS system with $A_{j,k} \in \{0, 1\}$. The architecture for computing the generic j-th measurement y_j has been sketched in Fig. 2(a).

The aim of this section is to investigate the feasibility and to indicate some performance limits, of an ultra-low-voltage implementation of this schematic.

As a reference technology, we consider the SAR described in [18]. This ADC has a single-ended architecture and operates down to 0.2–0.25 V with a sampling rate between 100 Hz and 500 Hz. The critical parts of this architecture are:

- a capacitive array consisting of a 6-bit binary-weighted primary (MSB) array and a 4-bit binary-weighted secondary (LSB) array;
- a double-boosted and low-leakage, T-shaped switch to sample input voltage on the capacitive array;
- a temperature-stabilized ultra-low-voltage comparator.

The overall architecture is depicted in Fig. 2(b). Mainly, even if the architecture is standard, some arrangements are required to enable low-voltage operation, as detailed in the following.

i) A boosted switch S_B is required to sample the input voltage $V_{\rm in} \in [0, V_{DD}]$ The double boost architecture is commonly used in low-voltage approaches for reducing the on-resistance [17], [18]. All other switches are used to connect capacitance plates either to GND or to V_{DD}, and standard topologies are used.

ii) The non-inverting input terminal of the comparator is fixed to V_{DD}, whereas the inverting one is first pre-charged to $V_{\rm in}$ during the sampling phase, and then raised to $V_{\rm in} + V_{DD}/2$ (by connecting the bottom plate of C_9 to V_{DD}) at the first conversion cycle. At successive conversion cycles, the switches connected to the bottom plates of C_9 to C_0 are moved to approximate the negative input terminal voltage to V_{DD}. This ensure that, at any conversion step, the voltages of the input terminals of the differential pair used as first stage of the comparator is biased with the highest possible voltage.

Just a few modifications are required to ensure this circuit to implement the desired system of Fig. 2(a). The most important modification is that the boosted switch S_B has to be replaced by at least 8 boosted switches to sample all input voltages $V_{\rm in}^{(k)}(\tau_0)$, $k = 1, \ldots, 8$. A solution, among the several possible ones, is to *i*) precharge all top plates of capacitors C_4–C_9 to V_{DD}; and *ii*) connect boosted switches to all bottom plates for sampling the $V_{\rm in}^{(k)}(tau_0)$.

For the sake of simplicity, the secondary array is grounded during the sampling phase. This, as observed in the previous section, is not critical and leads only to a small deviation in the $A_{j,k}$ coefficients with respect to the expected values $\pm 1/8$.

At the end of the sampling phase $t = \tau_0$, the bottom plates of C_4–C_8 are grounded, whereas C_9 is connected to V_{DD}. The voltage at the inverting terminal of the comparator rises to

$$\left(V_{DD} - \sum_{k=1}^{8} A_{j,k} V_{\rm in}^{(k)}(\tau_0) \right) + \frac{V_{DD}}{2}$$

so that the voltage that is converted into a digital word is actually $V_{DD} - \sum_k A_{j,k} V_{\rm in}^{(k)}(\tau_0)$, that is nothing more that the complement to V_{DD} of the desired measurement.

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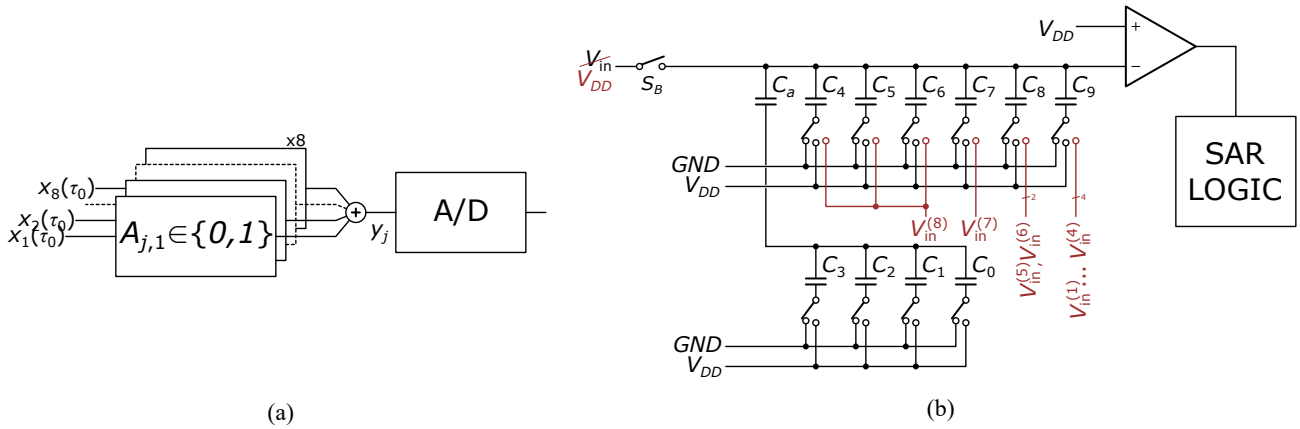

(a) (b)

Fig. 2. (a) CS system considered for an ultra-low-voltage implementation. (b) Architecture for the SAR in [18] and arrangements (in dark red) to allow to operate as the system in (a).

This suggests the feasibility of the considered system in an ultra-low-voltage environment. The only issue to be reported is the replication of the double-boosted switch, that is a critical component in [18].

Regarding system performance, it is quite hard to extrapolate performance of the overall CS system, as this may depend on many factors. Indeed, it is possible to estimate the performance of the computation and of the A/D conversion of the single measurement y_j. The prototype in [18], operating at $0.225\,\mathrm{V}$ has a maximum sampling frequency of $450\,\mathrm{samples/s}$ and a power consumption of $0.85\,\mathrm{nW}$. The feasibility with the same supply voltage is proven. We also expect a similar behavior in terms of sampling frequency. In fact, the configuration in conversion mode in unchanged and we expect the same transient time for all steps. We expect also the same transient time when charging the capacitive array (the sampling phase), since the charge, in both cases, is operated through the series of a standard switch (with source to ground or V_{DD}) and a double-boosted switch. Indeed, we are expecting a slightly higher power consumption due to the higher number of switches, but we cannot estimate it as the power requirements of the double-boosted switch only is not indicated in [18].

VI. Conclusion

In this paper we have considered the feasibility of the implementation of an AIC based on Compressed Sensing as an ultra-low-voltage circuit. A survey of AIC architectures proposed so far in the literature suggests that most common topologies may present many issues mainly due to the several analog blocks required. Indeed, an innovative architecture we recently proposed appears to be perfectly compatible with the hardware solutions used in state-of-the-art ultra-low-voltage SAR A/D converters. By considering a 0.2–$0.25\,\mathrm{V}$ 10 bit SAR converter as reference design, we have proposed a few modifications required to allow the SAR to operate as an ultra-low-voltage AIC. Since required modifications are very small, performance is expected to be aligned with that of the original design.

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