Silicon nanowires for hybrid solar cells

Mingxuan Zhu

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Mingxuan Zhu

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Frédéric Chandezon	Rapporteur
Philippe Knauth	Rapporteur
Jacques Liandrat	Examinateur
Johann Bouclé	Examinateur
François Flory	Directeur de Thèse
Judikaël Le Rouzo	Co-directeur de Thèse
Marielle Eyraud	Membre invité

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Introduction

The objective of the 3rd generation of photovoltaic solar cells technology[1–3] is to achieve high efficiency devices but still use thin-film deposition methods. This concept is not only to enhance conversion efficiency to approach or even overcome Shockley-Queisser limit, but also to keep areal costs low. Various approaches are attempted to improve efficiency in thin-film solar cells especially with the use of nanostructures. The advantage of using these structures for optoelectronic devices is now widely accepted. Indeed these nanostructures have the distinction of having different physical properties from those of macroscopic structures. Of these, one can notice changes in the bandgap, the refractive index, the rate of recombination of carriers and a large surface-to-volume ratio.

Different materials and solar cell structures based on nanostructures have been studied. Both new photovoltaic mechanisms and new concepts for solar cells are thus expected such as multijunction solar cells[4], hot carrier solar cells[5], intermediate band solar cells[6], hybrid solar cells[7], frequency conversion[8], and multiple-exciton generation[9].

Among these attempts silicon nanowires is an active research subject in photovoltaic application as we will see in the first chapter (Nanowires Photovoltaic solar cells). Firstly because its diameter is at the length scale of wavelength of light which gives its unique properties in light trapping; secondly because its radial dimension is below the photogenerated excitons diffusion length which makes core-shell structure advantageous in carriers collection; thirdly because the unconstrained dimension along the wire length allows to transport the electrons or holes. In addition the high aspect ratio makes it rather reactive in chemical behavior[10].

Light absorption is always a major concern to improve energy conversion efficiency in solar cells. The first generation of bulk silicon solar cells face two problems: a theoretical limitation of the conversion efficiency and high manufacturing cost. The second generation thin film solar cells also sacrifices absorption loss because of its thin thickness. In this context, due to light trapping effect, SiNWs may provide a way for high light absorption at a low cost. For example, a large area of SiNWs can be easily realized on an entire wafer surface with the electroless metal-assisted chemical etching (EMACE) method that is simple and inexpensive. The light trapping effect exhibits itself as a very low reflection in SiNWs. The reflection is related to the wire areal density on the wafer surface, which can be tuned by KOH tapering process. The EMACE technique for SiNWs etching and the KOH tapering to tune the areal density of the wires will be presented in the second chapter (Silicon nanowires fabrication).

Besides the strong light trapping effect, nanowire is promising for solar cells also due to its effectiveness to collect carriers if a core-shell junction can be fabricated in wire. But one of major difficulty is the junction fabrication surrounding or in the wire with a nanometer-scaled diameter. In our study a real core-shell junction wrapping individual single silicon nanowire is realized with electrochemical deposition method with etched SiNWs as electrode. It is first time, to our knowledge, that PEDOT is polymerized on chemical etched SiNWs with electrochemical method. Illumination during fabrication is necessary for polymerization. The core-shell morphology is dependent on the competition between EDOT diffusion to wire bottom space and PEDOT growth on wire tips. In the third chapter (PEDOT electrochemical deposition), we will describe the PEDOT electrochemical deposition and the competition mechanism to get such a core-shell structure.

The major problem restricting hybrid solar cells is the high recombination rate of charge-trapping interfacial states resulted from the lattice mismatches of the two different materials. The Si-C bond can eliminate surface recombination centers to passivate SiNWs[11]. PEDOT:PSS as a kind of thiophene-based conducting polymer can also passivate SiNW[12]. But the PEDOT:PSS polymer forms a layer on top of SiNWs and coats only a fraction of wire surface, because of the large particles of commercial PEDOT:PSS difficult to penetrate into the bottom of SiNWs array. Compared with spin-coated PEDOT/SiNWs cell, the most remarkable feature of our PEDOT/SiNWs hybrid cell is its ultralow leakage current density and ultrahigh leakage resistance. The large resistance parallel to diode suggests a good passivation effect to remove interfacial states which constitutes the pathway for charge transport at reverse bias. In the fourth chapter (Characterization of SiNW/PEDOT solar cell), we will discuss the characterization of the PEDOT/SiNWs cell made with the EMACE method and the electrodeposition technique.

Finally, we conclude this work and propose some perspectives to go further in the study of solar cells based on silicon nanowires.

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Glossary

AAM	Anodic Alumina Membrane
AM	Air Mass
a-SiN_x:H	Amorphous hydrogenated silicon nitride
a-Si:H	Amorphous hydrogenated Si
CdS	Cadmium sulfide
CdTe	Cadmium telluride
CH^{3-}	Methyl group
CNMW	Co-integrated Nano and Micro Wires
CVD	Chemical Vapor Deposition
EMACE	Electroless Metal-Assisted Chemical Etching
EQE	External Quantum Efficiency
FDTD	Finite-Difference Time-Domain
GaAs	Gallium Arsenide
H_2O	Dihydrogen oxide (water)
HF	Hydrofluoric acid
IQE	Internal Quantum Efficiency
IR	Infrared
LIBC	Laser Induced Beam Current
MW	Micro-Wire
NW	Nano-Wire
O_3	Ozone
O_2	Oxygen
PEDOT	Poly(3,4-ethylenedioxythiophene)
PSS	Poly(styrene sulfonate)
RIE	Reactive Ion Etching
RTA	Rapid Thermal Annealing
RSH	Read-Shockley-Hall
SEM	Scanning Electron Microscope
SRH	Shockley-Read- Hall
Si	Silicon
SiO_2	Silicon dioxide
SiNWs	Silicon Nano-Wires
TF	Thin Film
TMM	Transfer Matrix Method

List of symbols

Symbol	Description	Unit
A_{pj}	Projected area of an object	m^{-2}
c	light speed	$m\ s^{-1}$
C_{abs}	Absorption cross-section	m^{-2}
E_f	Final energy of electron	eV
E_g	Bandgap energy	eV
E_i	Initial energy of electron	eV
E_{ph}	Energy of phonon	eV
FF	Fill factor	-
G	Generation rate	cm^{-3}
h	Planck's constant	J s
H	Embedded length of CdS nanopillar	nm
I	Current	mA
I_0	Intensity of incident light	$cm^{-2}\ s^{-1}$
I_{max}	Current at maximum power	mA
I_{ph}	Photogenerated current	mA
I_s	Saturation Current	mA
I_{sc}	Short circuit current	mA
k_B	Boltzmann's constant	$J\ K^{-1}$
k_{ph}	Wave vector of phonon	nm^{-1}
N_0	Number of photons incident on cell surface	$cm^{-2}\ s^{-1}$
P_c	Collection probability	-
P_{in}	Power incident on solar cells	$mW\ cm^{-2}$
q	Electronic charge	C
Q_{abs}	Absorption efficiency	-
R_{nrad}	Rate of non-radiative recombination	cm^{-3}
R_{rad}	Rate of radiative recombination	cm^{-3}
R_s	Series resistance	Ω
R_{sh}	Shunt resistance	Ω
T	Absolute temperature	K
T_A	Temperature of the absorber	K
T_s	Temperature of the sun	K
T_0	Temperature of the environment	K
V	Applied voltage on solar cell	V
V_{max}	Voltage at maximum power	V
V_{oc}	Open circuit Voltage	V
x	Distance under material surface	cm
α	Absorption coefficient	cm^{-1}
η	Energy conversion efficiency	-
λ	Light wavelength	nm

μ_h	Mobility of charge hole	$cm^2V^{-1}S^{-1}$
ν	Frequency	Hz
ν_{ph}	Frequency of phonon	Hz
Ω_{emit}	Solid angle of photons emission	sr
Ω_{sun}	Solid angle of sun light absorption	sr

1.1. Solar cell principle

1.1.1. Solar spectrum

Almost all the energy used by human beings comes from the solar energy resource. For example, fossil fuels, petrol or coal, used for transportation and electricity generation, are plant matter that stored solar energy million years ago. Wind energy resulted from air current in fact is created by solar heated atmosphere and the rotation of the earth. Hydroelectricity is also originally a form of solar energy, as hydropower is dependent on the evaporation of water by the Sun, and its subsequent return to the earth as rain to provide water in dams. Photovoltaic is a simple and elegant way to utilize solar energy by directly converting it into electrical power.

The sun can be viewed as a blackbody with the temperature a little below 6000 K. Therefore the peak of its irradiance spectrum is in the visible range according to Planck's radiation law[13]. When solar irradiance arrives on the earth through the air atmosphere, part of its energy is absorbed by dusts and molecules like O_3, O_2, H_2O, etc., and part is reflected. Up to 45% solar energy is lost. The solar irradiation spectrum can be seen in Figure 1-1. AM 1.5 is the standard spectrum used for solar cells performance evaluation[14]. It is estimated that the amount of solar energy in one day exceeds the total energy consumption in the entire world in one year.

The photon energy E_{ph} in eV is related to its wavelength λ in nm as the following equation:

$$E_{ph} = \frac{hc}{\lambda} = \frac{1240}{\lambda} \qquad 1\text{-}1$$

where *h* is Planck's constant and *c* is the light speed. The production of *h* and *c* is 1240 eV nm. The solar visible range of wavelength is from 400 to 700nm, or the energy range from 1.8 to 3.1eV. Nearly half of the solar energy is in the visible range. This range is just a little beyond the bandgap energy 1.12eV of silicon, which makes silicon a good candidate material for solar energy convertor, because the theoretical solar energy conversion efficiency is actually a function of semiconductor's bandgap, as will be discussed next.

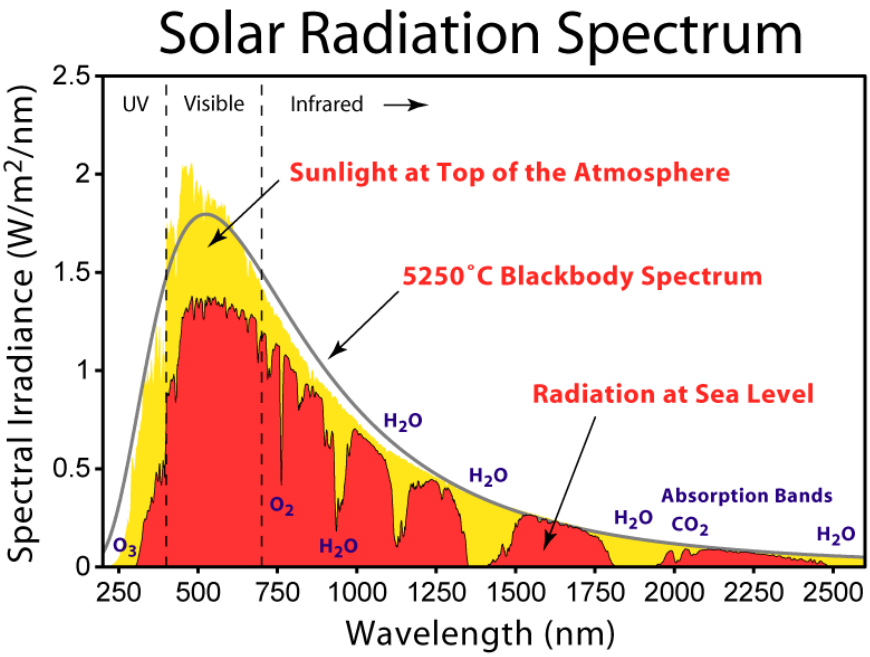

Figure 1-1 Radiation spectra of sunlight at top of the atmosphere, blackbody spectrum and radiation at sea level (Air Mass 1.5 solar spectrum)

1.1.2. Theoretic limitation of efficiency

The maximum efficiency 85% is determined by the second law of thermodynamics[13]. The theoretical consideration about the efficiency limitation is obtained from the equation as follows:

$$\eta = \left(1 - \frac{T_A^4}{T_S^4}\right)\left(1 - \frac{T_0}{T_A}\right) \qquad 1\text{-}2$$

where T_A is the temperature of ideal absorber for solar energy, the sun temperature T_s = 5800K, T_0 is the environment temperature of 300K. In Equation 1-2 the first term in the round brackets on the right side is a ratio of the extracted energy from the solar power which is the difference between the incident energy and that emitted back to the sun. The second term represents the maximum efficiency to utilize the extracted energy with Carnot engine to generate electricity. Equation 1-2 gives the maximum efficiency 85% at T_A= 2478K.

The second law of thermodynamics limits the efficiency of a solar energy converter in an ideal case without considering concrete materials. When a single junction solar converter is taken into account, the efficiency maximum is reduced to 31% known as Shockley- Queisser efficiency limit, or detailed balance limit.

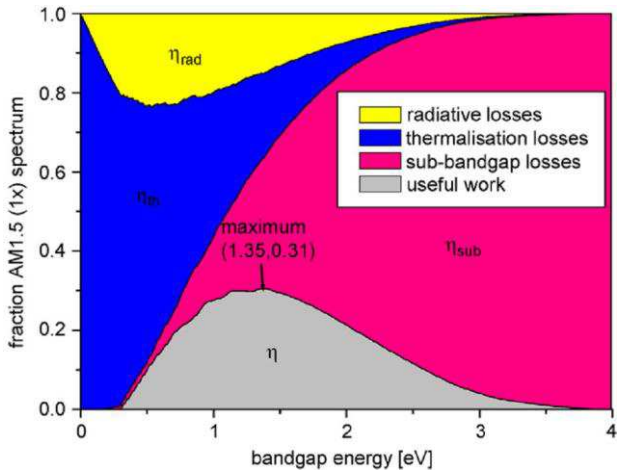

Figure 1-2 Theoretical one sun AM 1.5 spectra fractional intensity losses and limiting efficiencies for different ideal bandgap devices (at 300K) . Lower bandgaps have higher thermalisation losses, whereas higher bandgaps have large sub-bandgap losses[15].

In the analysis on the solar cell composed of only one single pn junction[16], only one electron-hole pair is generated by one incoming photon under unconcentrated sunlight. The photon with energy lower than band gap has no contribution to the converted power. The part of energy loss is called sub-bandgap losses as seen in Figure 1-2. The absorbed photon energy will lose the part of energy higher than band gap by thermal relaxation. This is called thermalisation losses. The real contributing energy just equals the band gap of chosen materials, as it is shown in Figure 1-2. So the efficiency maximum is actually the function of band gap. The maximum efficiency for silicon of 1.12ev bandgap is around 29%.

The thermodynamics determined efficiency is the ultimate efficiency that any solar cell can achieve, while Shockley-Queisser limit sets the working boundary of the first generation solar cells. The gap between the two efficiency limits spurs researchers to fill in it by creating new ideas and employing more sophisticated devices.

Breakthrough of efficiency beyond Shockley-Queisser limit may take place against the assumptions used in this theoretical limit. The assumption of one single pn junction is most broken by tandem solar cells which employs multiple junctions trying to cover the solar spectrum as much as possible. The recent world efficiency record of 44.4% is created by Sharp with its triple-junction solar cells. Concentrator configuration helps boom the conversion efficiency by providing more photon flux. Quantum dots are also hot in science community at least because it provides possibility to generate more than one pair of excitons by one photon[17],[18]. Thermo-electronic conversion performance can be improved by silicon nanowires to save the energy loss in infrared spectrum.[19] It is also possible to break down one high-energy photon into several low-energy photons by fluorescence materials[20] which are under research to overcome thermalisation losses.

It is the main objective of the 3rd generation of photovoltaic solar cells technology[1–3] to achieve high efficiency devices but still use thin-film deposition methods. This concept is not only to enhance conversion efficiency to approach and even overcome Shockley-Queisser limit, but also to keep areal costs low. Various approaches are attempted to improve efficiency in thin-film solar cells[21][22]. For example, quantum dots are added in thin film to improve optical absorption[23], and metal nanostructures can also be used in thin film cell to increase absorption with plasmon resonance effect[24].

However, nowadays the widely used photovoltaic technology in industry is the bulk silicon solar cells, and its application growth is established on the thorough and solid understanding of silicon properties in chemistry, optics, electronics, mechanics and so on. The large amount of knowledge on silicon becomes basic background to understand the working mechanism of solar cells and also supports the photovoltaic research to go further.

1.1.3. Basics on bulk silicon solar cells

The photovoltaic effect was first observed by French physicist A. E. Becquerel in 1839[25]. When the sunlight or any other light is incident upon a material surface, the electrons present in the valence band absorb energy and, being excited, jump to the conduction band and become free. These highly excited, non-thermal electrons diffuse, and some reach a junction where they are accelerated into a different material by a built-in potential (Galvani potential). This generates an electromotive force, and thus some of the light energy is converted into electric energy. Generally speaking, solar cells work on photovoltaic effect through carriers generation and collection.

The formation of photogenerated current mainly includes four processes as illustrated in Figure 1-3: (1) light absorption, (2) electron-hole pairs diffusion to and separation in a pn junction, (3) electrons diffusion in n type material and holes diffusion in p type, (4) the current circuit completion at rear contact. The key processes are the first two processes: light absorption in cell and exciton pairs separation at pn junction, which are described in detail into the next two sections.

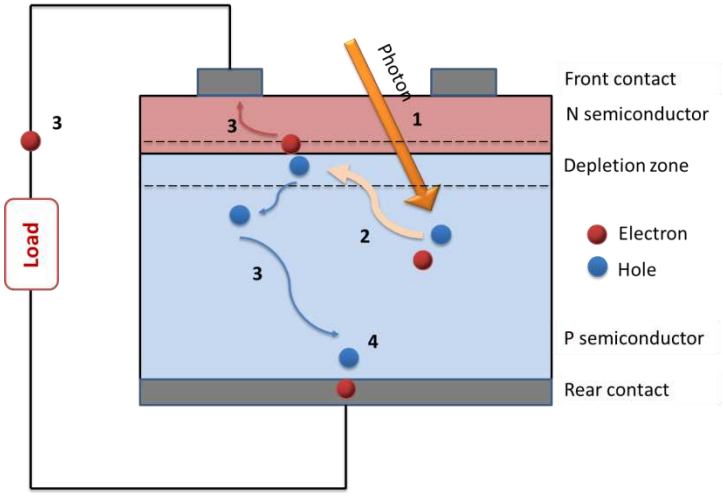

Figure 1-3 Schematic of circuit flow of electron and hole at a pn junction. Process (1): photon absorption and electron-hole pair generation; Process (2): diffusion and separation of electron-hole pair in depletion zone; Process (3): electron diffusion in n type semiconductor and load, and hole diffusion in p type semiconductor; Process (4): meeting of electron and hole at rear contact to complete a circuit.

Carriers generation

The incident light on the surface of a solar cell is reflected back to the air, or absorbed by the cell's body, or transmitted through the cell. The reflection and transmission of incident light are viewed as the loss of energy which will not contribute to the light current or electric power from the cell. Only the absorption can be utilized by the solar cell to excite carriers of electron and holes.

Absorption coefficient α is a property parameter of solar cell's material that determines how far into solar cell's body a photon of a particular wavelength can penetrate before being absorbed. The absorption coefficient is dependent on the material. Figure 1-4 presents several semiconductor materials' absorption coefficient as a function of wavelength.

Only when the photon energy is larger than bandgap of a material, the photon can be absorbed. When the energy is larger than the bandgap, the probability of a photon being absorbed is dependent on the likelihood of interaction between a photon and an electron in such a way to move the electron from one band to another. For the photon with energy just equal to the bandgap, only the electrons at the valence band edge can interact with the photon, and therefore the relative low number of electrons at the valence band edge causes the low probability of the photon absorption. While the photon energy is larger than bandgap, a much larger amount of electrons not just close to the band edge can be involved into the interaction with the photo, and thus the absorption of such a photon is increased

greatly. That is why, as can been seen from Figure 1-4, absorption coefficient decreases sharply with increasing wavelength.

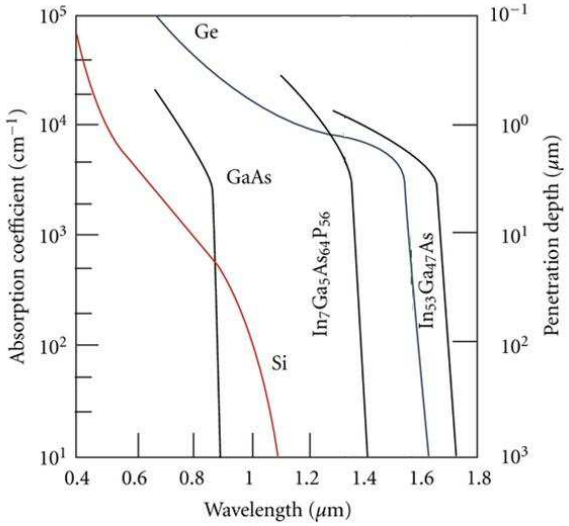

Figure 1-4 Absorption coefficient and penetration depth of various bulk materials as a function of wavelength [26] **.**

In fact silicon is not a good candidate to convert energy due to its indirect bandgap. The light absorption process can be seen in Figure 1-5. The indirect transition of electrons from valence band to conduction band requires phonons emission/scattering with photos to conserve lattice momentum, so the absorption is much less possible in silicon than in other direct semiconductor material. The energy and momentum conversation equations are [27]:

$$h\nu = E_f - E_i + h\vartheta_{ph} \qquad 1\text{-}3$$

$$k = k_f - k_i + k_{ph} \qquad 1\text{-}4$$

where *h* is the Planck's constant; ν and *k* are the frequency and wavevector of the photon; *i* and *f* denote the initial and final states of the electron, respectively; ν_{ph} and k_{ph} are the frequency and wavevector of the phonon. In this case the theory results in a second order relation between absorption coefficient and photon energy which takes into account the energy of the phonon.

$$\alpha \sim (h\nu - E_g - h\vartheta_{ph})^2 \qquad 1\text{-}5$$

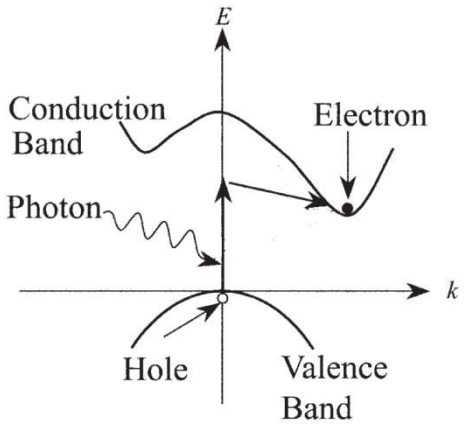

Figure 1-5 Schematic of photon absorption in indirect bandgap semiconductor

The absorption coefficient of a cell material is closely related to the generation rate. Generation rate *G* gives the number of generated electrons at any point per unit time in the device due to photon generation. Generation rate in the device can be calculated from the loss of intensity of incident light. Neglecting the reflection, the incident light intensity *I* at any point in the device is given by Beer-Lambert law as follows:

$$I = I_0 e^{-\alpha x} \qquad 1\text{-}6$$

where I_0 is the intensity of incident light on the surface of a cell, α is the absorption coefficient of the cell's material, and x is the distance into the cell at which the intensity is being calculated. Since the loss in light intensity, or absorption of light causes the electrons generation, the generation rate can be calculated by finding the change in light intensity at any point in the device. The generation rate can be derived by differentiating Equation 1-6 and then given as

$$G = N_0 \alpha e^{-\alpha x} \qquad 1\text{-}7$$

Where N_0 is the number of incident photons at the surface of the cell.

From Equation 1-7 we know that the generation rate at a particular wavelength is exponentially reduced with penetration distance into the surface, and has its maximum at the surface of the cell. By summing up the generation rates for all the wavelengths in a standard solar spectrum AM 1.5, the net generation rate as a function of penetration distance into a slice of silicon is shown in Figure 1-6. The profile features that the highest generation rate appears at the surface of silicon slice and further that the generation rate becomes constant when the distance is deep into the body of the device. The characteristics in generation rates profile suggest that the collection region should be as close to the surface as possible in order to get the largest amount of generated electrons. Of course the efficiency of carriers collection should take into account the mechanisms how the generated electrons or holes are collected in a cell.

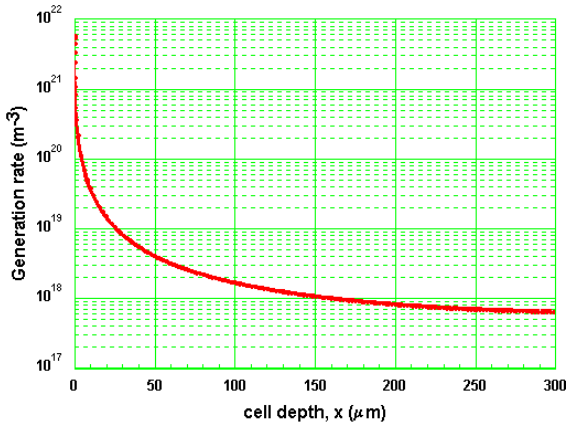

Figure 1-6 Generation profile in silicon due to the Am1.5 spectrum

Carriers collection

A generated carrier is just in metastable state. An electron as minority created in p type semiconductor will recombine with a hole, while a hole produced in n type material will recombine with an electron. The recombination types can be seen in Figure 1-7. The electron jumps back from conduction band to valence band and recombines with a hole while a photon is emitted. This process is called band-to-band recombination, or radiative recombination. Reed-Shockley-Hall (RSH) recombination is assisted by trap energy level in band gap. Auger recombination is a process in which an electron and a hole recombine in a band-to-band transition, but now the resulting energy is given off to another electron or hole.

All of these recombination mechanisms limit the lifetime of charge carriers. If the carrier is recombined, the light-generated exciton pair is lost and no current or power is generated.

In the case of hybrid solar cell mismatch of different crystal lattices may cause a large number of dangling bond at the interface between two different materials. The interface recombination can be viewed as a type of RSH recombination because it also depends on the interface states in bandgap, and the interface becomes major limiting factor resulting in rather high interface recombination velocity which thereby lowers the lifetime of carriers.

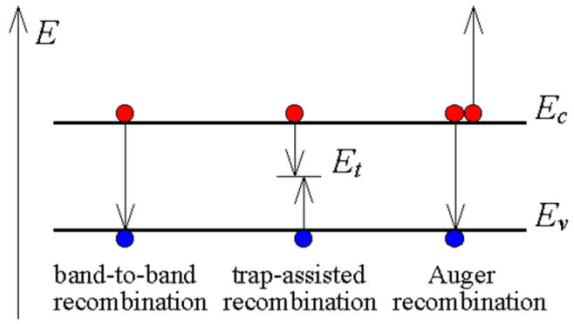

Figure 1-7 Schematic of recombination types in bandgap. E_t, E_c and E_v denote the trap energy level, the conduction band edge level, and the valence band edge level, respectively.

The separation of generated electron-hole pairs saves the life of carriers by preventing their recombination at a pn junction. Across the interface in the pn junction there is a build-in electric field pointing from n type semiconductor side to p type side, due to the requirement of Fermi level alignment between p and n semiconductor. Once an electron-hole pair diffuses or is generated in the junction, due to the built-in electric field the carrier of electron is swept towards n type side and the hole moves to p type side. In the n type semiconductor, the electron as majority is much less possible to be recombined than as minority. It is the same for hole in p type semiconductor. So the collection of light generated carriers of charge is determined by the separation process at the pn junction.

Collection probability P_c is a definition describing the probability that a photo-generated carrier in a certain region of the device will be collected by the pn junction and therefore will contribute to the photo-generated current. This collection probability at any point in the cell equals the normalized excess minority carrier concentration at the same point in the dark [28–31].

Collection probability is dependent on the diffusion distance that the carrier should travel to reach the junction- see Figure 1-8. In the pn junction the collection probability is unit since the carrier there can be swept and collected immediately after being generated. The collection probability drops as the distance becomes far from the junction. When the travelling distance is longer than the diffusion length, the probability is rather low. The collection probability is also dependent on the surface recombination velocity. If the surface is full of capturing centers for carriers, few photo-generated carriers would be collected and therefore low photon current is generated.

So the photogenerated current I_{ph} is determined by the photo-generation rate and the carrier collection probability. It is the integration over the entire thickness of the device of a

carrier collection probability P_c at a particular point x in the device, multiplying the generation rate G at that point. The definition is as follows:

$$I_{ph} = q \int_0^W G\,(x) P_c(x) \mathrm{d}x \qquad 1\text{-}8$$

Where W is the thickness of the device, and q is the electron charge.

One of the advantages of radial pn junction, a shell of one type semiconductor surrounding the core of the other type semiconductor, is that it can reduce the travelling distance of generated carriers and thus increase the collection probability. This will be discussed in the section of state of the art in this chapter.

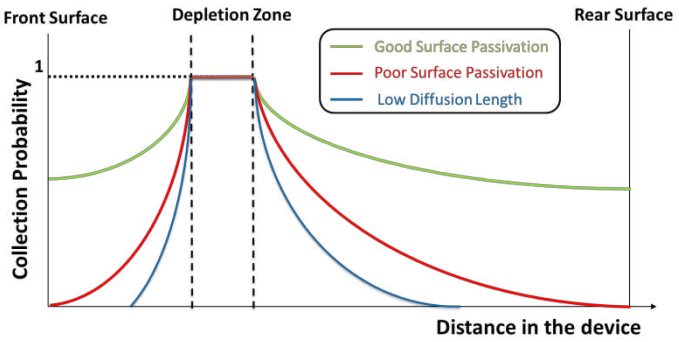

Figure 1-8 Schematic of surface passivation and diffusion length influence on collection probability

Photogenerated voltage

The voltage in solar cell is generated by the photovoltaic effect. When the separation of electron-hole pairs occurs at the junction, electrons move to n type semiconductor while holes travel to p type semiconductor. Under the condition of short circuit i.e. the front and rear contacts are connected without any resistance, the swept carriers exit the cell as photo-generated current. If there is any resistance existing in the solar cell circuit as the load presented in Figure 1-3, the resistance as energy barrier will prevent electrons or holes from leaving the cell and thus cause the accumulation of electrons on the n type side and holes on the p type side of the junction. The increase in the number of accumulated carriers creates a new voltage that is called photovoltaic voltage. The new photovoltaic electric field is opposite to that already existing there, and thereby the net built-in electric field is lowered. As the built-in electric field is the barrier against the flow of the forward bias current, the reduction in the field intensity leads to an increase in the forward bias current. The forward bias current flows in opposition to the photo-generated current. The net current from the cell is the difference between the photogenerated current and the forward bias current. With the increase of accumulated carriers across the junction, the photovoltaic voltage

reaches a point where the photogenerated current is balanced by the forward current, and the net current is zero. This condition is called open circuit condition and the photovoltaic voltage at that moment is called $V_{oc.}$

Equivalent circuit of bulk silicon solar cells

The equivalent electronic circuit of silicon pn junction solar cells can be simplified as in Figure 1-9, and the dependence of current on applied voltage is given by

$$I = I_s\left\{exp\left[\frac{q(V-IR_s)}{nk_BT}\right]-1\right\}-\frac{V-IR_s}{R_{sh}}-I_{ph} \qquad 1\text{-}9$$

Where q is the electronic charge, k_B is the Boltzmann's constant, T is the absolute temperature, and V is the applied potential across the diode, R_{sh} is the shunt resistance, and R_s is the series resistance. n is a dimensionless parameter involved in the IV characteristics to take into account the non-ideal behavior. I_s is the saturation current, and I_{ph} is the photogenerated circuit current.

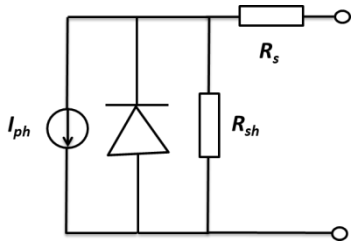

Figure 1-9 Equivalent electric circuit for solar cells

The important parameters that characterize a solar cell are shown in Figure 1-10, including V_{oc} I_{sc} V_{max} and I_{max}. The short circuit current I_{sc} is usually equal to the photo-generated current I_{ph} which has been presented in the previous content as well as open circuit voltage V_{oc}.

Fill factor *FF* is defined as the maximum power divided by the product of I_{sc}*V_{oc} i.e. as

$$FF = \frac{I_{max} \times V_{max}}{I_{sc}V_{oc}} \qquad 1\text{-}10$$

Where I_{max} and V_{max} are the current and the voltage when the maximum power is generated from the solar cell, as shown in Figure 1-10.

The efficiency η of a solar cell is defined as:

$$\eta = \frac{I_{sc} \times V_{oc} \times FF}{P_{in}} \qquad 1\text{-}11$$

where P_{in} is the power incident on the solar cell.

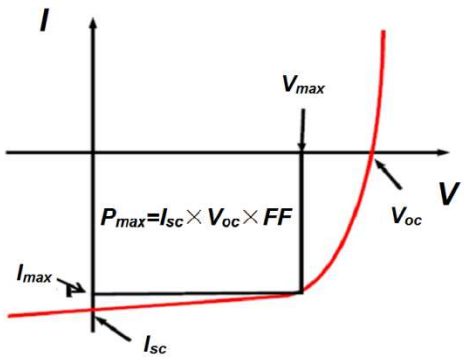

Figure 1-10 Normal IV of a solar cell including important parameters

The series resistance R_s is caused firstly by resistance to movement of current through the emitter and base of the solar cell, secondly by the contact resistance between metal and silicon, and last by the resistance of the top and rear contacts. The series resistance has an impact both on photo-generated current I_{ph} and on fill factor *FF*. But it has little influence on V_{oc}, because no current through the series resistance under open circuit condition.

The shunt resistance R_{sh} is caused mainly by the defects during manufacturing for silicon solar cells. It will result in the reduction in V_{oc}, because it provides an alternative way to generated photons and therefore leads to the weak photovoltaic effect.

After understanding the principle how solar cells works, the next sections describe how to improve the solar cells performance by light trapping to absorb more photons and through well-designed junction geometry to collect more photogenerated carriers.

1.2. Light trapping strategies

The generation analysis above is based on Beer-Lambert law with the assumption that the light is absorbed in one pass through solar cell material as shown in Figure 1-11(b). However, the generation rate can be increased if the light is trapped in the cell. So the light management is a fundamental study to improve solar energy conversion efficiency.

1.2.1. Ray optics limit

The surface texturing is widely used for bulk silicon solar cells and can be greatly increased the light absorption[32]. As presented in Figure 1-11(a), when the light at the back side of solar cell sheet is reflected at an angle exceeding the critical angle for total internal reflection, the light returns to the front surface and no fraction leaks out of the cell. Multiple total internal reflections occurring on the both sides of the sheet of solar cell cause an increase in the path length of light passing through the cell, and therefore enhancement in the absorption efficiency.

When the cell geometric size is much larger than wavelength of illuminating light, the antireflection effect follows a theoretic limit first derived by Yablonovitch and Cody[32]. The absorption will be enhanced at most by a factor of $4n^2$ where n is the film material's refractive index. For example, based on this theory, silicon solar cells with antireflective layer on both sides can only have the maximum absorption enhanced by 62 times at 590nm wavelength (n=3.96 at 590nm[33]). Since in their theory the geometric details of antireflective layer shape is relatively unimportant, it is quite possible that this light trapping effect contributes to light absorption in solar cells covered by SiNWs array on the front surface.

However when a solar cell's dimension is on a sub-wavelength scale or comparable to wavelength of incident light, the appropriate theory to describe light propagation is wave optics rather than ray optics, and the ray optic limit of $4n^2$ can be surpassed. The next will be a short introduction to another strategy of light trapping beyond the limit.

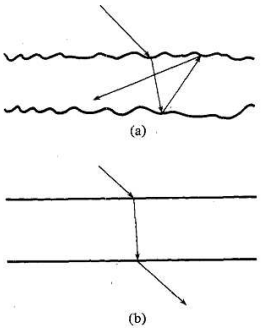

Figure 1-11 Two optical sheets with qualitatively different surface textures. (a) Angular randomization and intensity enhancement do occur. (b) In a plane-parallel slab, there is no angular randomization and no intensity enhancement [32] **.**

1.2.2. Light trapping in individual nanowire

The matter is composed of discrete electric charges such as electrons and protons. When the incident light encounters an object, the charges in the object will be set in oscillation where the net effect manifests itself as the emission of secondary radiation known as light scattering. The incident light can also be scattered because of its diffraction on randomly distributed defects. In addition to scattering, part of the incident power is absorbed within the object because of the excitation of oscillating dipoles. The absorption is taken into account with the imaginary part of the refractive index. The scattering or absorption of incident light can be analogous to a virtual cross section around the object. As soon as the illuminating light hits this area, the interaction between incident electromagnetic wave and electronic charges occurs. According to Mie theory, the absorption cross section area C_{abs} is proportional to the absorbed power. Therefore, the absorption in the object can be described by absorption efficiency Q_{abs} that is defined as the ratio of absorption cross section C_{abs} to the projected area under illumination.

$$\mathrm{Q}_{abs} = \frac{C_{abs}}{A_{pj}} \qquad 1\text{-}12$$

Within the limits of ray optics, i.e. the object size is much larger than the concerned wavelength, for a perfect absorbing black body, its absorption cross section C_{abs} is equal to the projected area, and therefore the absorption efficiency is 1. For an imperfect absorber, the cross section C_{abs} is smaller than the projected area and the absorption efficiency is lower than 1. For larger objects, the absorption efficiency is in general resides between 0 and 1. But on the scale of sub-wavelength, absorption efficiency has been evidenced to be larger than 1[34][17,35].

For example, Krogstrup et al presented the experimental measurements on p-i-n GaAs nanowire solar cell[34]. The nanowire structure can be seen in Figure 1-12(a). The photogenerated current can be as high as 180 mA/cm^2 and the apparent conversion efficiency was estimated to be 40% beyond Shockley-Queisser limit of 31% for GaAs semiconductor. They attributed the ultrahigh photogenerated current to resonance trapping effect due to the geometry of nanowire on the sub-wavelength scale.

They spatially mapped the photocurrent generated by the p-i-n nanowire solar cell for three different excitation laser wavelengths of 488nm, 676nm and 800nm as can be seen in Figure 1-12 (b) (c) (d), respectively. The results presented in Figure 1-12 (b), (c), and (d) are

deconvoluted with the point-spread function of the diffraction-limited laser spot. As seen in Figure 1-12 (b) (c) (d), a photocurrent from an area much larger than the size of the laser spot appears for all three wavelengths of laser. The effective absorption areas for the three cases are about one order of magnitude larger than the physical cross-section of the vertically standing GaAs nanowire with diameter of 425nm, see the SEM image in Figure 1-12(a). The absorption efficiency Q_{abs} is about 8 times higher than is predicted from the Beer-Lambert law. In other words, the single nanowire can collect photons outside its physical body boundaries.

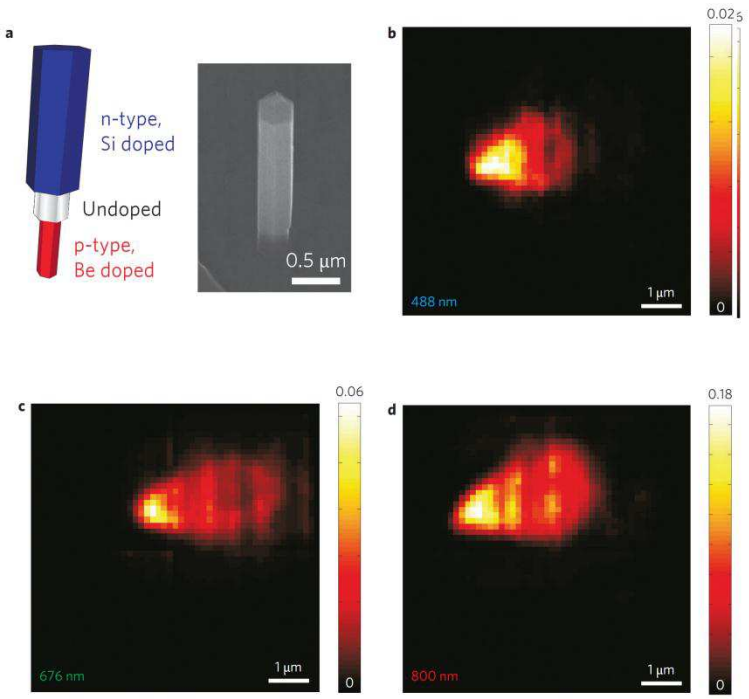

Figure 1-12 Mapping of photocurrent scanning on GaAs nanowire: a, left: The p-i-n radial doping structure of GaAs nanowire by epitaxial growth; right: SEM image of the nanowire solar cell. b-d Scanning photocurrent measurements on the single vertical nanowire device for three different excitation laser wavelengths 488, 676, and 800nm, normalized to the incident photon flux. Adapted from Reference [34].

The effect of enhanced absorption efficiency can be explained with Lorenz-Mie theory. In the article by Cao et al[36] a nanowire was viewed as small scaled microcylinder resonator that can trap light in resonant leaky modes by multiple total internal reflections. The measured absorption spectrum on the single individual germanium nanowire lying on the substrate was in quite good agreement with the predicted spectra according to Mie theory see Figure 1-13. The absorption peaks in measurement were believed to be related to the Leaky-Mode Resonances. They further pointed out that the absorption efficiency was sensitive to diameter and the radiation wavelength.

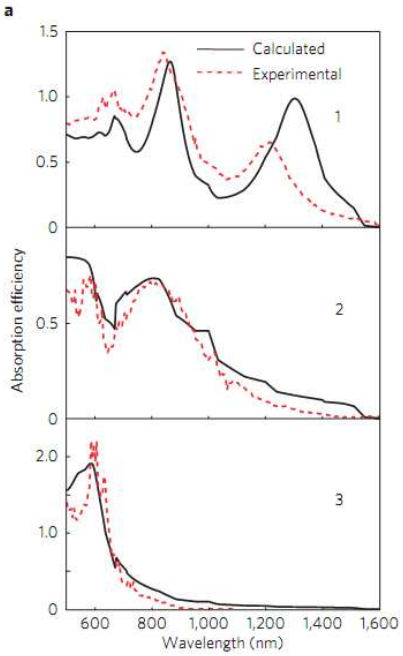

Figure 1-13 Comparison between experimental and calculated absorption efficiency Q_{abs} spectra for Ge nanowire radii of (1) 110nm, (2) 25nm, (3) 10nm [36].

Individual silicon nanowire was also examined by Brönstrup et al[37] in a experimental and theoretical work. They observed the reflection spectrum of the individual silicon nanowire was well consistent with the predicted scattering effect. They also found that the peak in scattering spectrum was dependent on the diameter, which can also be explained with Mie theory.

In Figure 1-14 , for the wavelength that is smaller than 360nm corresponding to the minimum direct band gap of silicon[38], the absorption efficiency is independent on the diameter of silicon nanowire, because the absorption is caused by the intrinsic absorption due to a higher extinction coefficient. In the case of wavelength larger than 360nm, the silicon is indirect band gap semiconductor, and the absorption efficiency becomes dependent on the geometry of nanowire. And the absorption is enhanced due to the resonance effect in the silicon nanowire. The resonance is restricted to certain wavelength and diameter, so the branched structure of absorption efficiency spectra appears. The branched structure is almost straight as a line, and its slope decreases as diameter increases and wavelength decreases.

For the spectrum of chief interest 380 to 1100nm in silicon solar cells, there is a trend that larger diameter has higher absorption efficiency. In the case of diameter smaller than 120nm and wavelength larger than 700nm, although the absorption efficiency is smaller than 7%, it is enough for silicon nanowires array to absorb the light[37].

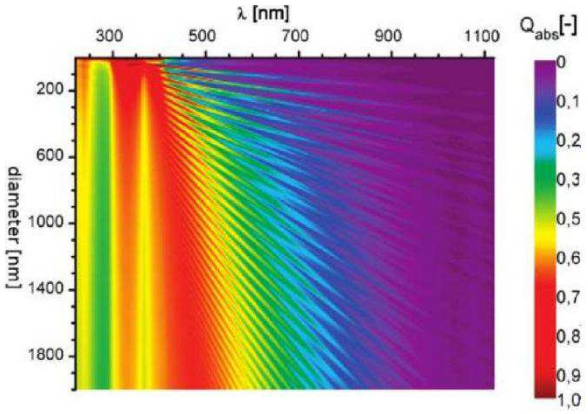

Figure 1-14 Mapping of absorption efficiency Q_{abs} for a single Si nanowire with a diameter d = 2nm and 2000nm and λ = 220 and 1120nm for nonpolarized light. Adapted from Reference [37]**.**

On the contrary to the intuition that optical properties of nanostructure are strongly dependent on the shape of structure, simulation results from the article by Brongersma et al[39] showed weak correlation between absorption and cross sectional shape. In their simulation, four shapes of cross section of single nanowire, rectangle circle hexagon and triangle, respectively, are employed with FDTD method. The similar curves of absorption efficiency vs. wavelength suggest the same mode of resonance occurs in amorphous silicon nanowire, see Figure 1-15(b). The authors further point out that there are two field maxima in all the four plots in Figure 1-15(c), similar to the low-ordered mode of resonance. This similarity suggests that the low ordered mode resonances are less sensitive to the morphology.

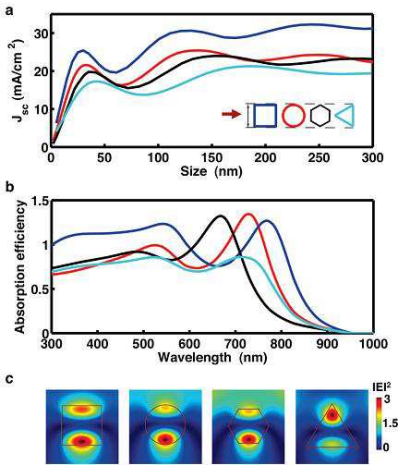

Figure 1-15 Generality of the optical resonance and short-circuit current enhancement to one-dimensional nanostructures. Adapted from the literature[39]**.**

1.2.3. Light trapping in nanowires array

Compared with single nanowire, the nanowires array are much more complicated. The reflectance of silicon nanowires array can be very low less than 3% in the range of wavelength from 400nm to 1100nm. Although the mechanisms are still unclear, many experiments and calculations have been made to understand this unusual physical phenomenon.

Garnett et al.[40] measured the enhancement factor of path length when one photon is scattered in nanowires array in a paper published in 2010, where they stated that the ordered silicon nanowires array has the ability to provide a light-trapping enhancement of ~73 times compared with the planar bulk silicon, beyond the ray optics limit for silicon about 31 times with one side of antireflective layer.

Similar to individual nanowire, some simulation results confirm the enhancement of light trapping in silicon nanowires array.

Gang Chen et al. have studied optical properties of periodic silicon nanowires array by simulation with the transfer matrix method (TMM)[41]. In this paper the model of periodic structure, shown in Figure 1-16, is determined by three key parameters: length *L*, pitch *a*, and diameter *d*. The illuminating light is set as normal to the x-y plane.

Compared with thin film with thickness of 2.33μm, the nanowires array with the same thickness has higher absorption efficiency in the high photon-energy regime but lower absorption in the low photo-energy regime - see Figure 1-16(b). Longer length favors larger absorption in the range of lower frequency. All the three nanowires array share the same absorption plateau for higher energy photons.

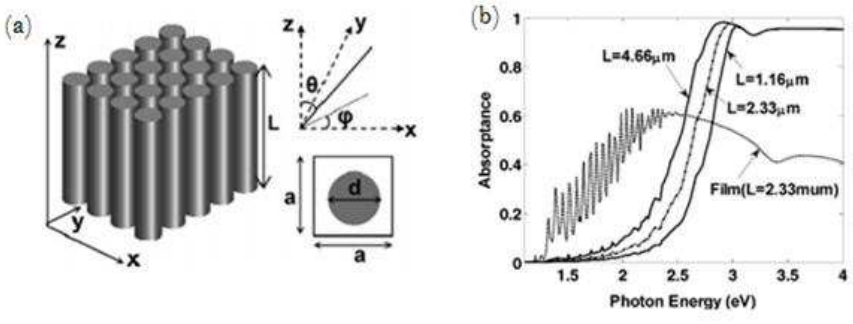

Figure 1-16 Optic simulation on the periodic silicon nanowire structure: (a) Schematic drawing of the periodic silicon nanowire structure. (b) Absorptive properties of nanowire structures with various thicknesses L = 1.16, 2.33 and 4.66 μm (d = 50 nm and a = 100 nm)[41]**.**

1.2.4. Light management contribution to V_{oc}

The contribution to the enhancement of photogenerated current is clear due to light trapping effect, but for V_{oc} it is still not clear how light management can affect the V_{oc}. Polman and Atwater[35] gave the relationship in the article in the framework of thermodynamics as follows:

$$qV_{oc} = E_g\left(1 - \frac{T}{T_s}\right) - k_B T\left[\ln\left(\frac{\Omega_{emit}}{\Omega_{sun}}\right) + \ln\left(\frac{4n^2}{I}\right) - \ln(QE)\right] \qquad 1\text{-}13$$

Where q is the electron charge, E_g is the bandgap energy, T and T_s are the temperatures of the solar cell and the sun, k_B is Boltzmann's constant, Ω_{emit}, Ω_{sun} are the solid angles related to photons emission from the solar cell and absorption into the solar cell, n the solar cell refractive index, I is the enhancement factor of light intensity, QE is the quantum efficiency.

The first term on the right side of Equation 1-13 is related to Carnot efficiency as we stated in the section of Shockley-Queisser efficiency limit. The second term in the square brackets includes three entropy-related terms. The first term in them accounts for the loss in V_{oc} due to the solid angle difference between photon absorption and spontaneous emission. While the solar radiation is incident on the cell from the solid angle Ω_{sun} = $6*10^{-5}$ steradians, the spontaneous emission in solar cell emits outgoing photons into the solid angle Ω_{emit} up to 4π. The loss in V_{oc} is as large as 315mV.

The second term in the brackets gives the description on how light trapping influences V_{oc}. As we talked above $4n^2$ is the maximum value that the enhancement of light intensity trapped in a solar cell can achieve, if the cell is considered much larger than the wavelengths of illuminating radiation. However in the case of cell's dimension on the sub-wavelength or wavelength scale, the local intensity enhancement factor I in cell can exceed the limit substantially[42,43], and therefore the light trapping effect in SiNWs for example will lead to a rise in V_{oc}.

The last term in the brackets describes the reduction in V_{oc} due to the quantum efficiency QE, which is defined as:

$$QE = \frac{R_{rad}}{R_{rad} + R_{nrad}} \qquad 1\text{-}14$$

where R_{rad} and R_{nrad} are the rates of radiative and non-radiative recombinations. The quantum efficiency is related to the non-radiative recombination mechanisms such as Auger recombination and RSH recombination due to defects in cell's body or carrier trapping states on the surface or interface. Obviously the QE can be increased by reducing the non-radiative recombination rates as we will present later in the section of state of the art. An alternative way may be to increase the radiative recombination rate. The light management helps to

increase the local density of optical states which in turn causes an increase in radiation recombination rate. The enhanced QE then directly improves V_{oc}.

All the three terms in the brackets are relevant for the light management strategies. SiNWs at least will work on the second term about V_{oc} by increasing the local light intensity in cell. According to Yang's estimation about path length enhancement factor of 73[40], the V_{oc} of SiNWs solar cell can be increased by 109mV with respect to the case without any enhancement. It is interesting to study the third term about the optical states enhancement in SiNWs, because silicon is an indirect bandgap which causes very low radiation recombination rate, and therefore the increased optical states in SiNWs solar cell might be also very useful to increase V_{oc} further by optimizing its structure.

Besides the strong light trapping effect, nanowire is promising for solar cells also due to its effectiveness to collect carriers if core-shell junction can be fabricated in wire. But one of major difficulty is the junction fabrication in nanowire. Next will be the introduction to development of pn junction fabrication in SiNWs.

1.3. SiNWs solar cells state of the art

We are trying our best to construct a core-shell heterojunction by depositing a PEDOT layer wrapping individual SiNW to form hybrid solar cell. This cell would take the advantages of the light trapping effect in SiNWs, the high collection efficiency due to core-shell structure, and also the passivation effect. Since light trapping effect has been discussed earlier, the core-shell structure and passivation effect will be presented in the following content.

As we stated before the key process of charge collection is based on the junction, and the effective carrier collection in nanowire results from its junction configuration. The junction can occur following in different ways: perpendicular to the length as shown in Figure 1-17 (a) of axial junction, or along the length of a nanowire corresponding to Figure 1-17 (b) of radial junction (core-shell junction), or within the substrate as in Figure 1-17 (c) of substrate junction. The substrate junction and axial junction can have the benefit of the light trapping effect but lose the benefit of efficiently carrier separation and collection. Unlike them, radial junction owns efficient collection of carriers as will be presented in the next subsection.

1.3.1. Junction category in geometry

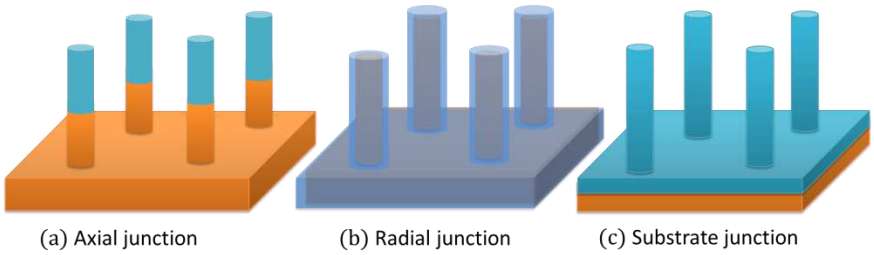

Figure 1-17 Three kinds of junction geometry in nanowires. (a) Axial junction, (b) radial junction, (c) Substrate junction. Different colors represent different carrier types of semiconductor.

1.3.2. Charge carriers separation and collection in radial junction

The reason for effective carrier collection was given in the report by Kayes et al [44]. The configuration of core-shell pn junction in nanowire, see Figure 1-18, makes possible the decoupling of light absorption and carriers extraction. The absorption of light is along the length of nanowire. The longer the wire is, the more possible the photons scattering with the surface, and the more photons are absorbed. So the absorption is mainly in the axial direction. On the other hand, immediately after photons absorption, electron and hole pairs are generated and separated in the depletion area. And then holes are collected in p-typed

semiconductor, while electrons in n type semiconductor. In general the separation and the collection of electron and hole occur in the radial direction. So it is possible for us to produce longer wires to absorb more photons and at the same time to produce thin wire to make sure carriers are collected as much as possible. Therefore the nanowire solar cell provides a possible way to improve carrier collection efficiency.

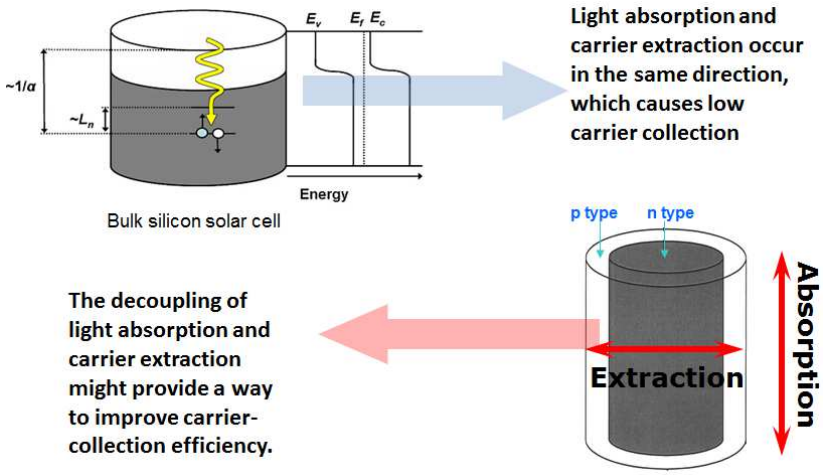

Figure 1-18 The core-shell junction has the advantage to decouple light absorption and carriers extraction

The effectiveness of the geometric configuration is independent on the used materials, and the efficiency in carrier collection can be increased just due to the geometry. This point was examined experimentally by Fan et al [45]. They first grew n-CdS nanopillar in the ordered pores of an anodic alumina membrane (AAM). The top portion of AAM was selectively etched in order to expose the n-CdS nanopillar out of the AAM. The exposed n-CdS nanopillars were then embedded in polycrystalline thin film of p-CdTe to form a n-CdS/p-CdTe core-shell radial junction. The embedded length *H* of CdS nanopillar can be well controlled by tuning the etching time of AAM.

They found that the energy conversion efficiency monotonically increases with *H*, as evident in Figure 1-19(a). They gave this explanation by theoretically calculating the effect of geometric configuration on efficiency. In Figure 1-19 (c), the junction area is confined on the top contact between CdS and CdTe as *H = 0*. In this case the electron-hole separation is conducted just in a small contacting region. Most of the generated carriers are lost on the defects of CdTe film through SRH (Shockley-Reed-Hall) recombination. On the contrary, as *H* = 900nm in Figure 1-19 (d), the carrier separation region of junction along the length of pillar is much more largely extended than the case of *H = 0*, and the larger junction region enhances probability that electron-hole pairs will be separated and then collected. Therefore the device conversion efficiency is increased by more than one order of magnitude. Because the separated charges are concentrated near the junction, the SRH

recombination becomes correspondingly concentrated in the region near the junction rather than in the CdTe film.

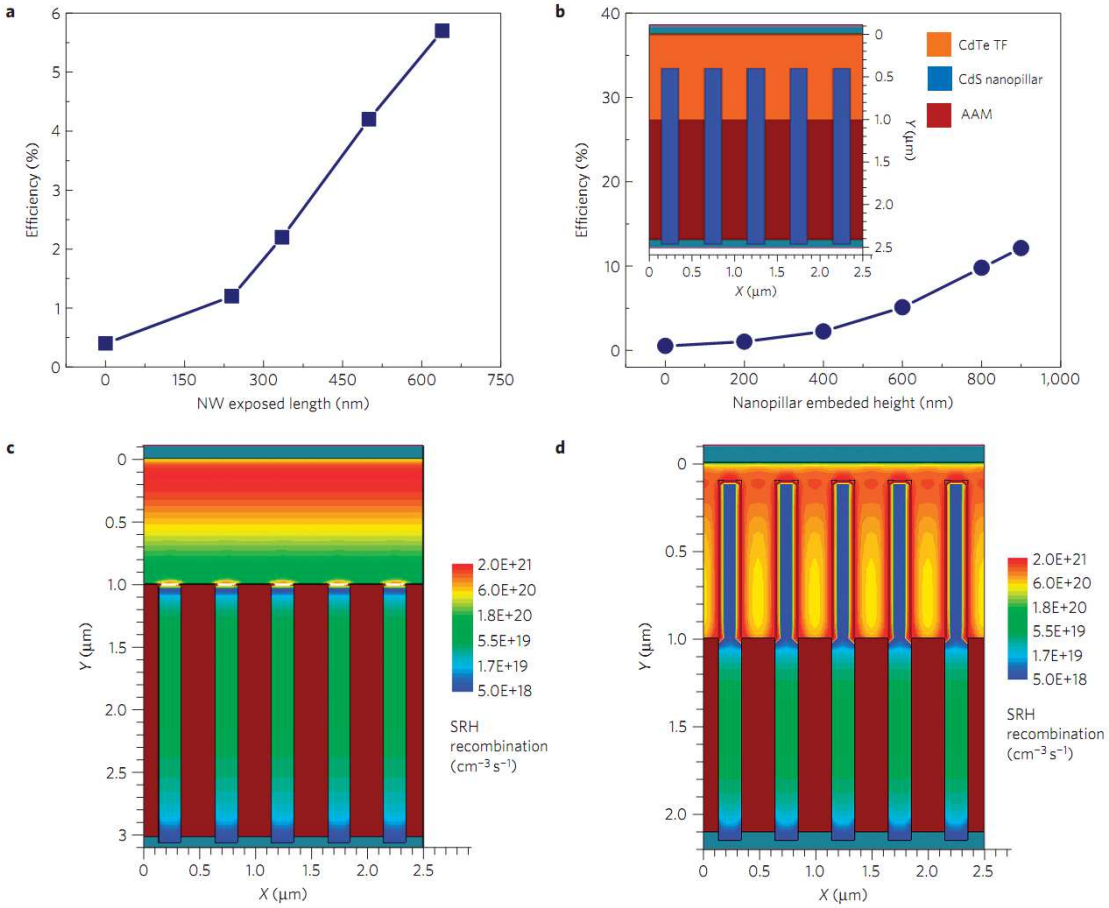

Figure 1-19 Effects of the nanopillar geometric configuration on the device performance. a, Experimentally obtained efficiency of SNOP (solar nanopillar) cells as a function of the embedded nanopillar height, *H*. NW: nanowire. b, Theoretical simulation of the SNOP efficiency as a function of *H*. TF: thin film. Inset: Schematic diagram of the SNOP cell used for simulation. c,d, Visualization of the Shockley-Read-Hall (SRH) recombination in SNOP cells with *H* = 0 (c) and 900nm (d). Adapted from Reference [45].

1.3.3. Realization of radial junction in nanowire

However the realization of radial junction in nanowire is not an easy work. One type of such a junction can be realized with a single semiconductor material known as homojunction. The junction is formed either by diffusion or by depositing a thin film surrounding the nanowire.

In the case of diffusion, for example, Jung et al[46] used spin-on-dopant method and attempted to create a core-shell junction in nanowire, as seen in Figure 1-20. The boron or phosphorus precursor liquid was first covered on the target wafer and the subsequent diffusion was carried out in a furnace at 1050℃ for 5 min. As seen in Figure 1-20(b) and (d),

the core-shell junction can only be formed in the wire with larger diameter. If the diffusion duration is too long, or temperature too high, the radial junction type would be converted to a substrate junction and the benefit of carrier collection is lost.

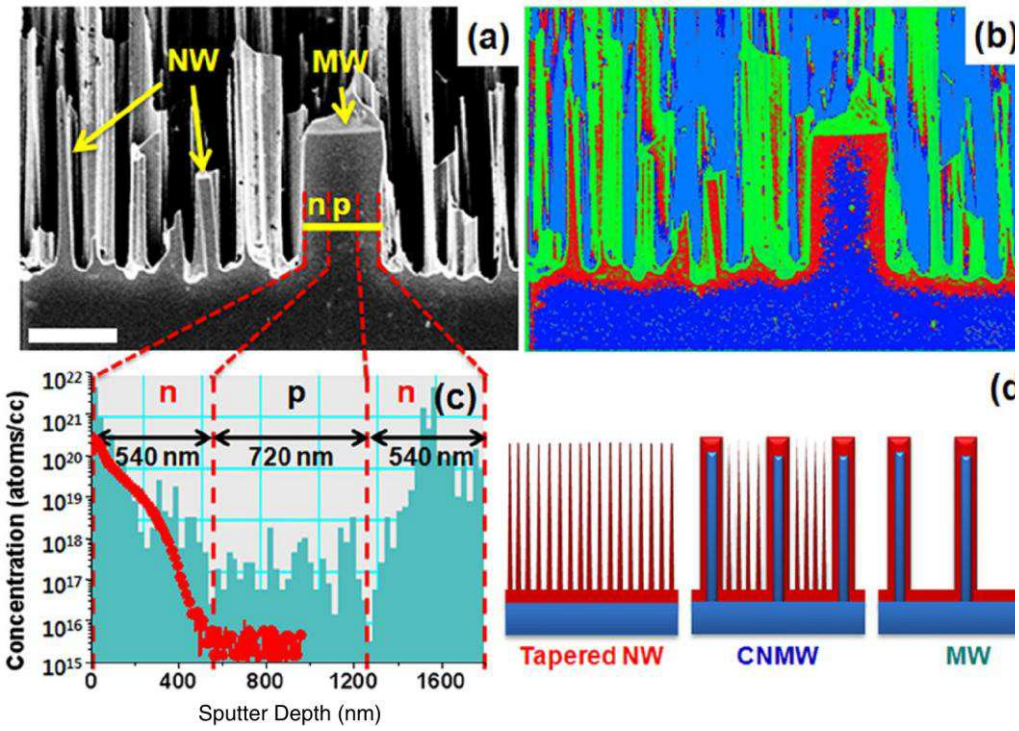

Figure 1-20 Diffusion doping for core-shell junction in nano and micro silicon wires. (a) Low voltage SEM image showing the two-dimensional doping profile by contrast difference of a typical co-integrated nano and micro wires (CNMW) structure. The scale bar is 2 μm. The image in (b) shows the formation of a radial junction (red for the n-type shell and blue for the p-type core). (c) Secondary ion mass spectroscopy variation shows phosphorus concentration along the yellow line denoted in the panel. (d) Schematic of the tapered NW (bulk p–n junction), MW (radial p–n junction), and CNMW (bulk and radial p–n junctions) structures. Adapted from Reference[46]**.**

In the case of depositing method, Garnett et al[47] successfully obtained a SiNWs array with core-shell structure with low pressure chemical vapor deposition method to deposit a layer of amorphous silicon onto SiNWs array. The subsequent crystallization process with rapid thermal annealing (RTA) created a polycrystalline of p type shell surrounding n type core.

However the low performance of this SiNWs solar cell is induced by the roughness of silicon wire surface and the high recombination rate on the surface. Because numerous carrier traps exist on the surface which is in proximity to the pn junction, the dark current and ideality factor of the diode are both very high, leading to a reduction in V_{oc}.

Therefore they concluded that the surface passivation is essential to improve the quality of solar cell based on SiNWs, as we will see in Chapter 4 about PEDOT/SiNWs hybrid cell.

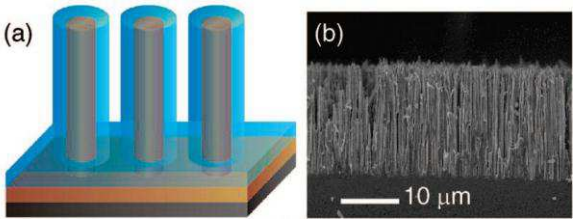

Figure 1-21 CVD deposition for core-shell junction in SiNWs array. (a). Schematic cell design with the single crystalline n-SiNW core in brown, the polycrystalline p-Si shell in blue, and the back contact in black. (b). Cross-sectional SEM of a completed device. Adapted from Reference [47]

1.3.4. Passivation on silicon

Kelzenberg et al[48] investigated the passivation effect of H-termination, SiO_2, a-SiN_x:H, a-Si:H. on the surface of wire by comparing photocurrent intensity. They demonstrated that the good passivation effect causes an increase in energy conversion efficiency.

An alternative way to eliminate surface recombination centers is methyl (CH_3) termination on silicon surface. Sailor et al[49] reported that solar cells of bulk silicon terminated with methyl reaches V_{oc} theoretical limit. In the metal/silicon diode the V_{oc} is limited to 200~300 mV due to Fermi level pinning which is caused by a large number of interfacial states between silicon and metal. However, the conjugated polymer (poly-$(CH_3)_3$Si-cyclooctatetraene)) coated n type silicon diode shows that the photovoltages are at the theoretic limit, much higher than the metal/Si diode. Its V_{oc} is only dependent on the diffusion and recombination in bulk silicon, suggesting that the carrier trapping on the interface between polymer and bulk Si can be negligible. They believed that the trapping defects elimination is due to the passivation effect of methyl termination.

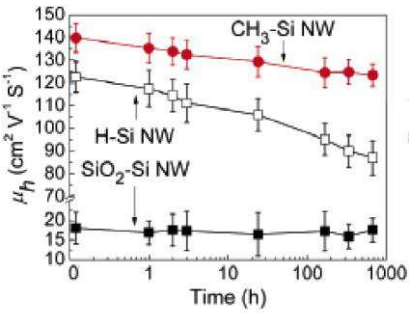

Figure 1-22 Average hole mobility (μ_h) of SiO_2-Si NW, H-Si NW, and CH_3-Si NW samples versus exposure time to air. Adapted from Reference[11].

In addition, the passivation effect of covalent Si-CH_3 on SiNWs surface was identified by measuring charge carrier hole's mobility [11]. The mobility of CH_3-SiNW is larger than H-SiNW, and much larger than SiO_2-SiNW, as seen in Figure 1-22. Different from H termination, the passivation effect of methyl termination maintains stable after long time exposure to air. This trend of mobility can be explained with the density of surface states. The passivation via CH_3 decreases the number of surface states and therefore reduces probability of electron-hole recombination rate, in turn leading to an increase in nanowire's mobility.

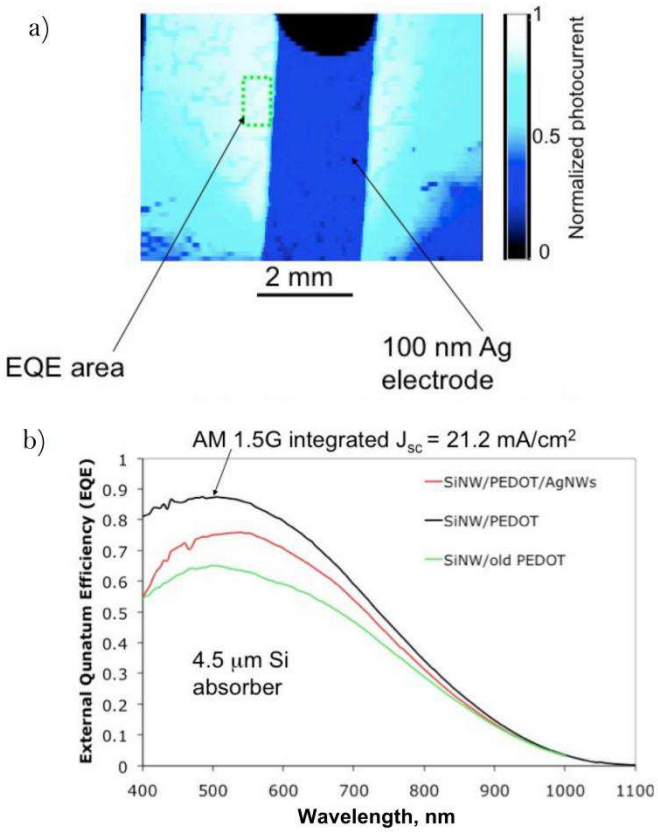

Figure 1-23 LIBC and EQE of SiNWs passivated with PEDOT. a) Laser beam induced current map of silicon nanowire/PEDOT solar cell. b) External quantum efficiency of silicon nanowire/PEDOT solar cells. Adapted from Reference [12].

PEDOT as a kind of thiophene-based conducting polymer can also passivate SiNW, as reported by Garnett et al[12]. They spin-coated PEDOT onto SiNWs array to form a Schottky junction solar cell. The measured EQE of the cell is at the maximum 88% and above 80% over the visible spectrum, as can be seen in Figure 1-23. Considering the reflection of their SiNWs array about 10~20%, the internal quantum efficiency IQE was estimated to 100%, demonstrating the perfect passivation effect in their solar cells.

However, the low EQE in IR and red wavelength spectrum is caused by the short silicon nanowires length and the failure of PEDOT penetrating into the bottom of SiNWs array. Because of the low absorption coefficient of silicon, the light with energy just above

bandgap of silicon, i.e. the light in red or IR spectrum, might be absorbed after multiple scattering deep into the array. However, the poor covering condition of PEDOT on Si wire causes the dramatically reduction in EQE.

1.3.5. SiNWs/PEDOT hybrid solar cell

Indeed many researchers took part in fabricating PEDOT/Si hybrid solar cells [50–60]. Besides the advantage of light trapping effect of nanowire, the carrier collection benefit of radial junction and the passivation effect of PEDOT stated above, spin coating of PEDOT:PSS solution onto SiNWs array is very simple and has no need of either high temperature or expensive equipment.

Among them the record efficiency achieves as high as 11% in such a hybrid solar cell[58]. In their work, periodic silicon nanocones array were fabricated with reactive ion etching (RIE) method using SiO_2 spheres periodic arrangement as mask. And heterojunction is realized by spin coating PEDOT on the surface of nanocones.

Even though the efficiency of PEDOT/SiNWs cell can reach over 10%, there is still room for improvement in efficiency if the limiting factors could be well solved.

The major limiting factor is the bad coating of PEDOT onto Si wire surface. As seen in Figure 1-24 of cross section of PEDOT/Si hybrid SEM images, the PEDOT:PSS polymer forms a layer on top of SiNWs and only a fraction of wire surface is coated by PEDOT, because the large particles of commercial PEDOT:PSS are difficult to penetrate into the bottom of SiNWs array and thus fail to cover the entire surface. Because of the bad contact between the two materials, the carrier collection and passivation advantages cannot be fully achieved with this spin coating method. In order to reduce the limitation caused by spin coating method, a tradeoff has to be made to lower the length of SiNW which sacrifices the benefit of light trapping effect.

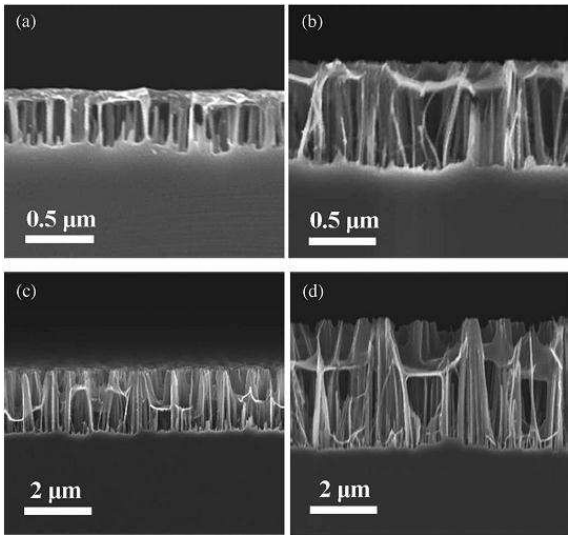

Figure 1-24 Cross-sectional SEM images of SiNWs coated with PEDOT:PSS. The wire lengths are (a) 0.35, (b) 0.9, (c) 2.2, and (d) 4.1 µm. Adapted from Reference [53]**.**

An alternative method maybe overcomes this limitation, which is the electrochemical deposition of PEDOT with SiNWs as electrode. In chapter 3, we will describe the PEDOT electrochemical deposition with etched SiNWs as electrode. The innovative method can get a real core-shell junction. Before that we will present the SiNWs fabrication processes. The light trapping effect exhibits itself as a very low reflection in our SiNWs with electroless metal assisted chemical etching (EMACE) method.

Chapter 2. Silicon nanowires fabrication

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Glossary

2D	Two-dimension
AAO	Anodic Aluminum Oxide
Ag	Silver
$AgNO_3$	Silver nitrate
Au	Gold
CH_3COOH	Acetic acid
CVD	Chemical Vapor Deposition
EDX	Energy-Dispersive X-ray
EMACE	Electroless Metal-Assisted Chemical Etching
FF	Fill factor
HF	Hydrofluoric acid
H_2O_2	Hydrogen peroxide
H_2SO_4	Sulfuric acid
HNO_3	Nitric acid
IPA	Iso-Propyl Alcohol
KOH	Potassium hydroxide
PEDOT	Poly(3,4-ethylenedioxythiophene)
RIE	Reactive Ion Etching
Ref	Reference
SEM	Scanning Electron Microscope
SHE	Standard Hydrogen Electrode
Si	Silicon
SiNWs	Silicon nanowires
TEM	Transmission Electron Microscope
ZnO	Zinc oxide

2.1. Introduction to electroless metal-assisted chemical etching

There are two different strategies to fabricate silicon nanowires array: bottom-up methods of catalytic growing silicon wires and top-down methods by etching bulk silicon.

Based on CVD method, the silicon wires can be catalytically grown with nanometer-scaled diameter[61]. The sub-10nm diameter in cross section attracts interest in scientific community because quantum confinement effect would bring forth new electronic and optic properties of SiNWs by altering the energy band structure of silicon[62] . For the application in photovoltaics, the calculation shows that efficiency might achieve as high as 48% for the tandem structure consisting of SiNWs with various band gaps[4]. However, CVD grown SiNWs suffer several limitations: first the catalyst noble metallic atoms diffusing into wire body become deep energy level recombination centers that reduce greatly minority lifetime[63]; second, it is still hard to control the wire's growth direction, position and filling ratio of each wire in array[62],[64] , and it is also difficult to make wires array covering large area[62]; third, the high cost is another barrier limiting its application in industry.

A large number of top-down methods are used for SiNWs fabrication such as reactive ion etching (RIE), electrochemical etching, or electroless metal assisted chemical etching (EMACE) method. In particular, EMACE method allows control of the doping type, doping level, crystallographic orientation, and the orientation of Si nanowire relative to the Si substrate[65] . The etched SiNWs array can cover a large area on a centimeter scale with uniform antireflection. Using lithography technique, the morphology of silicon wire and filling ratio of individual wire in the array are tunable by selecting appropriate mask. In addition, the technique of electroless chemical etching is cheap and simple, without need for sophisticated equipment.

Although the report[66] said 5 nm diameter can be achieved with AAO mask, most researches with EMACE are focused on fabricating SiNWs with diameter above 20nm, and no quantum confinement effect has been reported for EMACE etched SiNWs. The barrier to make a solar cell may rise in the fabrication of the pn junction in each wire due to the wire's small size, more or less than 100nm.

Both the top-down and bottom-up routines to fabricate SiNWs are facing the same problem of surface recombination because of increased aspect ratio with decreasing diameter.

This chapter will concentrate on the method of electroless metal assisted chemical etching (EMACE) that we used in detail.

2.1.1. Mechanism of electroless metal-assisted chemical etching (EMACE)

General introduction

The EMACE method is an easy and inexpensive method to fabricate nanowire array on a centimeter scale. The whole process is mainly divided into two steps. In Figure 2-1(a) Step 1 is the catalyst metal electroplating, in which silicon wafer is dipped into a solution containing HF and $AgNO_3$. In Figure 2-1(b) Step 2 is the chemical etching of silicon. At this step the deposited Ag serves as catalyst. On these catalytic sites the H_2O_2 is reduced to water (without any deposit), and under these sites the Si atoms are oxidized, and then etched away by HF. The Ag catalysts are finally dissolved in HNO_3 during the sample immersion in HNO_3 for 30 minutes, and the reaction follows formula 2-1.

$$3Ag + NO_3^- + 4H^+ \rightarrow 3Ag^+ + NO + 2H_2O \qquad 2\text{-}1$$

The nanowires array being the remaining part of Si wafer after etching, some properties of the mother Si wafer are passed over to SiNWs, such as crystallinity, and doping level.

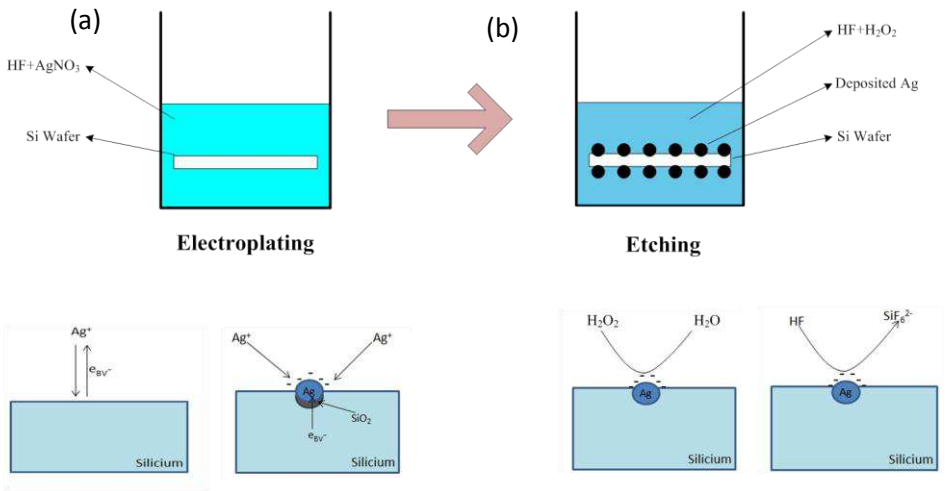

Figure 2-1 Schematic of electroless metal-assisted chemical etching processes for SiNWs: (a) electroplating step, (b) etching step.

All the energy levels related to SiNWs etching are presented in Figure 2-2 (a) with the vacuum energy level as reference. In the middle is the standard hydrogen electrode (SHE) axis. On the left to the SHE axis is the p type silicon energy band diagram with conduction band E_c, valence band E_v and Fermi level E_{Fp}. The redox energy levels of H^+/H and Ag^+/Ag are also positioned in comparison with silicon band diagram. On the right to the SHE axis stands the band diagram of quasi Schottky junction. The band bending curves in solid line is corresponding to Ag/Si contact, while dashed curves illustrate the contact between silicon and Ag^+/Ag couple.

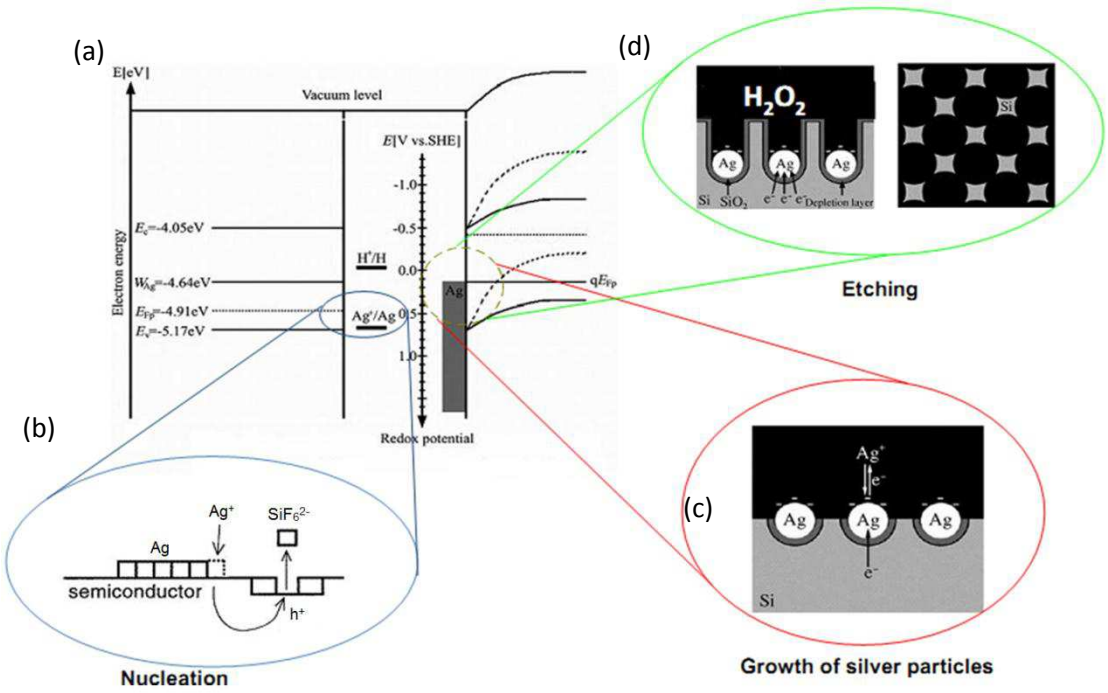

Figure 2-2 Schematic of working principle of SiNWs etching: (a) Energy band diagrams; (b) Mechanisms of silver nucleation; (c) Growth of silver particles; (d) Etching processes. Revised according to the literature[67].

Ag electroplating process

The electroplating process can further be broken down into two stages (See Figure 2-2). The first is the nucleation stage shown on the lower left highlighted in blue ring in Figure 2-2, and the second stage is the growth of Ag particles on the lower right in red ring of Figure 2-2. The principles for the two stages are different.

Ag nucleation stage

During the stage of nucleation, the principle is galvanic displacement reaction between Ag^+ and Si. From the comparison between Si and Ag^+/Ag couple in the band diagram, the Ag^+/Ag redox level is close to the valence band of silicon. It is probable that the charge holes are directly injected into the valence band of silicon from the solution[68].The displacement reaction takes place on the silicon substrate as shown in the nucleation schematic in Figure 2-2 (b). The global chemical reaction can then be formulated as reaction 2-2 [17].

$$4Ag^+(aq) + Si(s) + 6F^-(aq) \rightarrow 4Ag(s) + SiF_6^{2-} \qquad 2\text{-}2$$

which can be separated into two half-cell reactions 2-3 and 2-4

$$4Ag^+(aq) + 4e \rightarrow 4Ag(s) \quad E^\circ = 0.779V \qquad 2\text{-}3$$

$$\mathrm{Si(s)} + 6\mathrm{F^-(aq)} \rightarrow \mathrm{SiF_6^{2-}} + 4\mathrm{e} \quad E° = -1.24V \qquad \text{2-4}$$

When Ag^+ is reduced and Ag nucleates on silicon surface, the injected charge hole may transport to some nearby area and takes part in the oxidation of silicon. The nucleation of Ag and the corrosion of Si may not occur at the same place. The cathode reaction of silver ion is formulated in Equation 2-3, while the anode reaction of silicon is presented as Equation 2-4. Because this stage is caused by the overlapping between silicon valence band and Ag^+/Ag redox level but not associated with Fermi level, both p type and n type silicon can be electroplated with silver particles[65].

Ag growth stage

In the stage of Ag growth, immediately after the clusters of Ag nucleate on the surface, a quasi Schottky junction between silicon and silver is formed as shown in band diagram in Figure 2-2 (a). Different from the displacement mechanism for nucleation stage, the catalytic mechanism of silver nuclei plays the major role in the stage of silver growth. Because Ag has larger electronegativity than silicon[67], electrons diffuse from silicon to silver and accumulate on the silver nuclei surface. This allows Ag^+ in solution to obtain electrons and get reduced on the nuclei surface much more easily and to get them reduced on the nuclei surface than on Si atoms surface. So the deposition is operating preferentially on the nuclei, resulting in the growth of silver particles.

Simultaneously the anode reaction, when it is in the nucleation stage, happens to the silicon area in contact with silver particles as it is in the nucleation stage. Because of releasing electrons to silver, silicon atoms, being oxidized, are attacked and corroded by HF and eventually dissolved in the form of fluoride into the solution, as can be seen in Equation 2-4 of anode reaction. The removal of silicon under the silver catalytic site leads to a pit appearing at the site which traps the silver particle and prevents it from moving horizontally[67]. The trapping effect causes the site-specific etching of silicon under the catalytic silver.

The cathodic Ag reduction on the nuclei leads to the growth of nuclei, as seen in Figure 2-2(c). In the initial time of electroplating, small Ag particles form. With the electroplating, Ag deposits grow to larger particles, isolated patches, and a network with pores. After a long time of electroplating, some trapped small silver particles sink deep into Si substrate as Si atoms under them are removed by HF, while those which do not enter into pits grow to dendrite structure and consume a large fraction of silver ions in the solution.[67]

Si etching process

For the etching process, the mechanism in Figure 2-2(d) is also catalytic behavior of Ag particles. Similar to the growth stage of Ag deposits, the cathodic reduction of H_2O_2 provides charge holes for anodic oxidation of silicon via the Ag/Si Schottky junction, as described in Equation 2-5.

$$H_2O_2 + 2H^+ \rightarrow H_2O + 2h^+ \qquad 2\text{-}5$$

$$Si + 6HF + nh^+ \rightarrow H_2SiF_6 + nH^+ + \frac{4-n}{2}H_2 \qquad 2\text{-}6$$

Equation 2-6 presents that the silicon oxidation is caused in fact not only by the injected holes provided from H_2O_2 reduction but also by chemical reduction of H^+, because the hydrogen evolution is observed during the SiNWs etching. Equation 2-6 is a mixture of anodic oxidation and chemical oxidation (hydrogen ion reduction and hydrogen evolution). The proportion of anodic reaction involved in silicon oxidation is determined by the molar composition HF/ ($HF+H_2O_2$) [69]. When the molar composition is in low regime, the concentration of H_2O_2 is so high that the galvanic current meets the need of the charges for silicon oxidation and no hydrogen is evolved. On the contrary, when the molar composition is in high regime, the concentration of H_2O_2 is too low to cover the total oxidation charges, and the H^+ is involved in oxidation.

Chartier et al[69] divided the ratio ρ = HF/(H_2O_2 + HF) into four ranges according to different morphologies of polished surface, craters on surface, microporous and porous silicon, and only porous silicon - see Figure 2-3.

When the ratio ρ is larger than 80%, H_2O_2 proportion will influence on the surface of silicon nanowires[70][71]. The highly doped p type or n type silicon nanowires etched by EMACE show porous surface at high H_2O_2 concentration. The increasing concentration of H_2O_2 leads to high porosity of surface, which has stronger photoluminescence intensity.

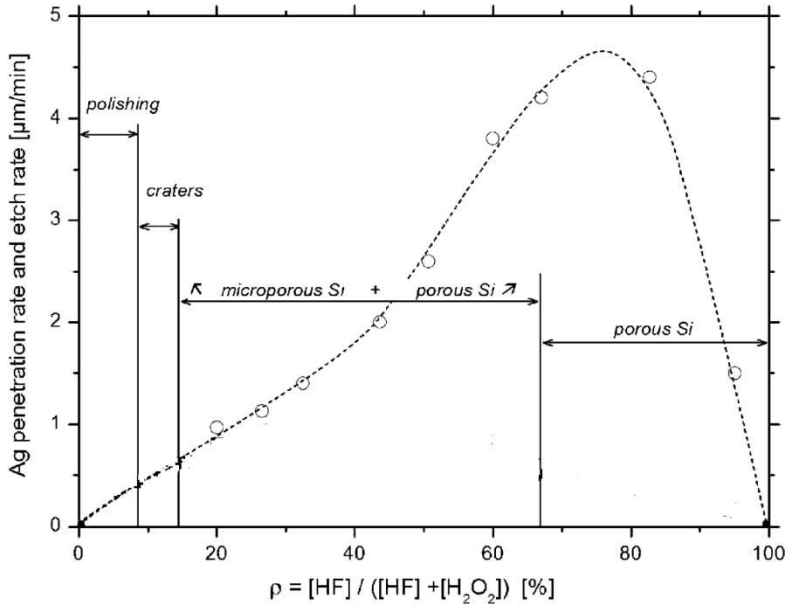

Figure 2-3 Relationships of HF/H_2O_2 ratio on silver catalytically etching rate. Open circles: penetration rate of the Ag nanoparticles. [69]

Wire shape determination

A critical current density J_{ps} - see Figure 2-4- is introduced in order to reveal the mechanism determining the morphology of silicon after etching[69]. The current density J_{ps} is the characteristic anodic current density of silicon electrode measured in electrolyte containing HF, and it is corresponding to the crossover of anodic oxidation of silicon from charge supply control to mass transfer control.[72] When the injected cell current J_{tip} is below J_{ps} ($J_{tip}<J_{ps}$), the supply of charge holes is short for the local silicon oxidation underneath the silver catalytic site, and therefore the etching is confined in vicinity to the silver particles. The pores are formed with diameter matching the size of silver particles at the bottom. When the cell current density J_{tip} is above J_{ps} ($J_{tip}>J_{ps}$), the excess current J_{wall} of holes over the demand of local oxidation diffuses along the silicon wall and take part in the oxidation and the etching of silicon at the wall. If the diffusion current density J_{wall} is still lower than J_{ps}, a microporous (diameter < 2nm) silicon morphology is formed at the wall. In the case that the diffusion current density J_{wall} is much larger than J_{ps}, the silicon wafer surface can be polished without nanostructure. [69]

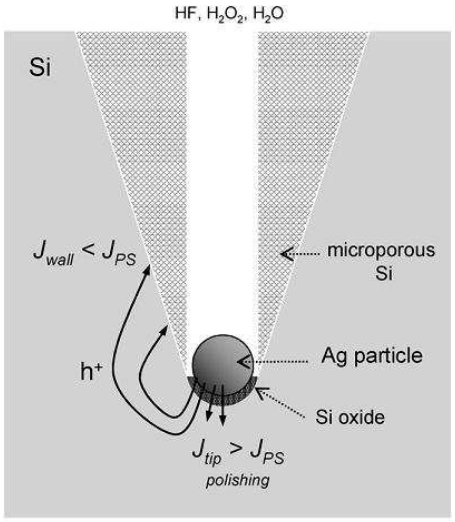

Figure 2-4 Schematic mechanism of HF/H_2O_2 ratio influence on SiNW morphology [69]

2.1.2. Wafer properties: doping type, doping level, and crystalline orientation

The conclusion about relationship between etching and doping type or doping level is not determined. Some researches observe Si nanowires become rougher and finally evolve into nanowires containing micro- and macro-pores[19,73]. It is suggested that the porous structure in highly doped Si substrates might originate from the diffusion of holes from the etching front at the Si/noble metal interface to the substrate without a noble metal during exposure to the etchant[65].

A rough surface should be avoided in order to get a solar cell of quality, because the rough surface may be more likely to increase surface recombination velocity which is a detrimental factor to decrease performance of a cell such as V_{oc} or FF [48][47].

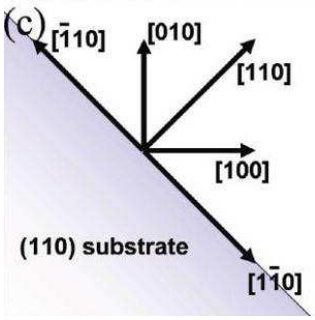

Figure 2-5 Illustration of different orientations on the surface of (110) substrate

The anisotropy etching is faster in the (100) orientation [65]. This can be explained by the back bond theory[74]. The oxidation and dissolution of silicon on the surface is allowed when the back bond of surface silicon atoms is broken, which connects them to the underneath atoms. For (100) surface plane, each atom has two back bonds, while an atom on (110), or

(111) surface has three back bonds. Due to the lower strength of back bond, the atoms on the surface (100) are easier to be removed and the etching direction is preferred along the 100 direction. As a consequence the nanowires form in the <100> direction that is non-vertical to the substrate surface if the substrate orientation is not (100) direction. An example is shown in Figure 2-6, for which the deposited catalyst film forms by displacement reaction in a solution of HF and Ag^+ on the (110) substrate and the etching occurs in a inclined manner to the substrate surface[75] .

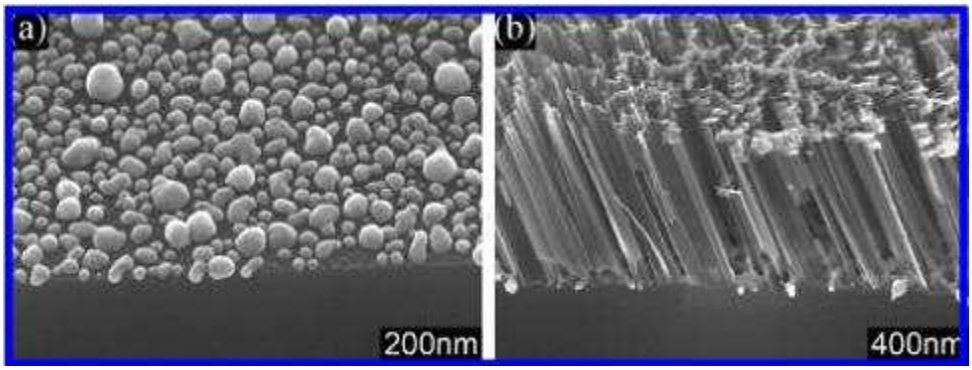

Figure 2-6 SEM images of EMACE etching on (110) silicon wafer: (a) Bird's-eye view SEM image of the electroless deposited silver particles on a (110) substrate. (b) Bird's-eye view SEM images of the substrate etched with electroless deposited silver particles[75]**.**

2.1.3. Etching time and temperature

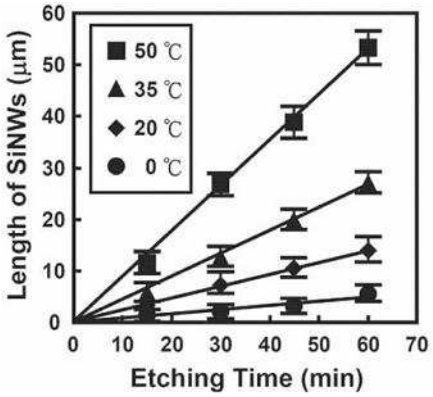

Figure 2-7 Temperature and etching time influence on SiNWs length [65]

In Figure 2-7 the length of SiNWs has a nearly linear relationship with etching duration. The bath temperature can also speed up Ag electroplating because activation energy is lowered. So it is easy to control the length of SiNWs with etching time, and this is one of the advantages of EMACE technique to fabricate solar cell. As stated by Yang et al[40] that the length of SiNWs can be prolonged in order to enhance the photo-trapping effect, another effect that should be taken into account is surface recombination that is proportional to the

length. The tradeoff between the two effects would require the optimal length that can be easily achieved by tuning etching duration.

2.1.4. Lithography technique

Although we didn't present our research on SiNWs made with the lithography method, it is necessary to mention this technique because the well-controlled morphology in diameter, length and filling ratio may allow studying light trapping effect in SiNWs by comparing with simulation results, and thus optimal morphology diameter can be determined to improve solar cells quality.

Electroless metal-assisted chemical etching of Si allows fabrication of SiNWs with the same doping level as the mother substrate. The key point in controlling SiNWs pattern is the deposition of a noble metal film containing position and size-defined pores, which determines the position and size of the remaining structures after etching. The combination of lithography and electroless etching is a simple method to fabricate highly ordered Si nanowires, enabling to control the diameter and length of nanowire, as well as the density of nanowire arrays.

Take Peng's work for example[76]. The processes are shown in **Figure 2-8**. The approach starts from self-assembly of a monolayer of silica spheres array on the Si substrate. Subsequently, size reduction of the silica spheres is achieved by being sintered at 1273K for 180 minutes and chemically etched in 50:1 HF solution, transferring the close-packed silica spheres into non-close-packed ones. In the next step, a noble metal film is deposited by physical vapor deposition onto the Si substrate with the non-close-packed template as a mask. This process results in a continuous layer of noble metal with an ordered array of pores. The diameter of the pores is determined by the remaining diameter of the silica spheres. The Si substrate covered with the continuous metal film with pores is etched in an etchant containing HF and H_2O_2. During the etching, the noble metal porous film sank vertically into the Si substrate. The unetched Si protrudes from the etched surroundings on the porous film, exhibiting itself as a Si nanowire array.

The nanosphere lithography method enables the control of the diameter of Si nanowires in a wide range from 50 nm to several micrometers. The length of Si nanowires varies linearly with the etching time, allowing easy control of their length.

AAO mask in combination with EMACE can also be used to fabricate SiNWs[66] with diameter as small as sub-10nm. It is very interesting to do research on the properties of SiNWs array with such a small diameter.

However, neither monolayer nor AAO mask fabrication is an at-hand technique, and it would take a large amount of time to master them well. Our attempt failed to make a large area of self-assembled monolayer of polystyrene spheres. The best way to get high quality of silica monolayer is to use Langmuir trough, which is not available in our lab. So we didn't pay a lot of time and energy in mask making, because after all our target is to study SiNWs solar cells rather than lithographical pattern designing, and also because the SiNWs array etched without mask works well to build heterojunction with PEDOT, which is the main content of the next chapter.

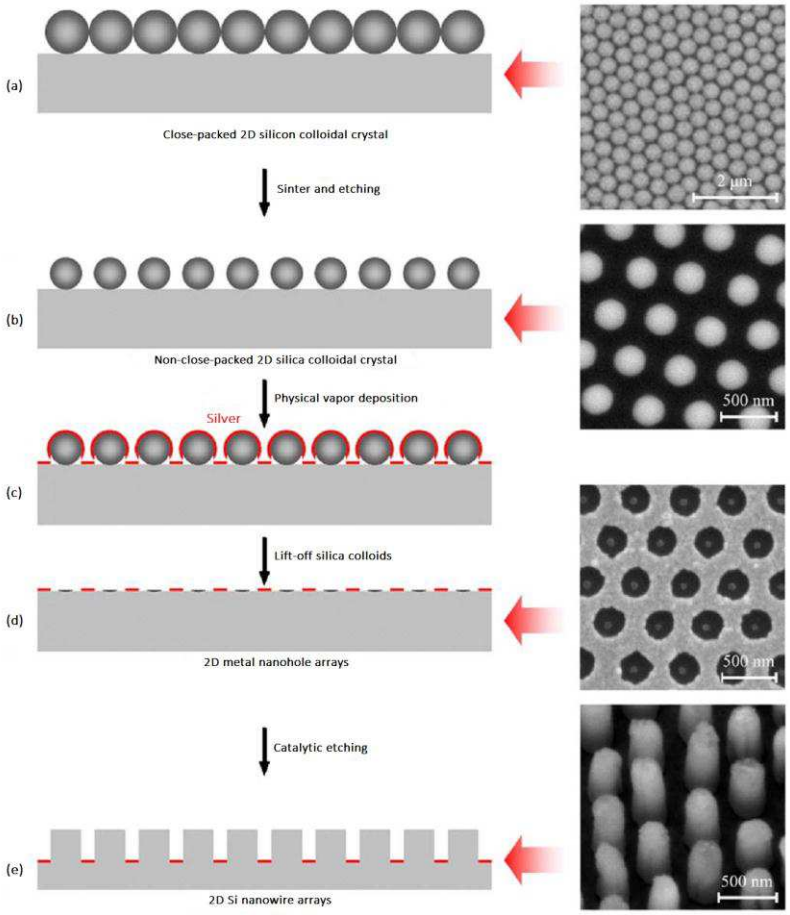

Figure 2-8 Schematic illustration of the experimental procedures for fabricating large-area arrays of ordered SiNWs: (a) deposition of monolayer silica colloidal crystal template on silicon surface; (b) fabrication of 2D non-close-packed silica colloidal crystals on silicon surface; (c) deposition of silver layer on silicon surface through the non-close-packed colloidal crystal template; (d) formation of regular silver nanohole arrays by removing silica colloids by brief ultra-sonication in water; and (e) formation of SiNWs by catalytic etching[76]**.**

2.1. Experiment and characterization

2.1.1. Experiment procedures

Silicon wafer parameters

The Si wafers for EMACE study, both n and p type, were purchased from BT electronics. The n type and p type wafers have the same parameters including diameter of 50.8 mm, resistivity of 1-10 Ω cm, and one polished side. The thicknesses of n type and p type are 280μm and 250μm, respectively. The n type silicon is doped with phosphorus, while p type with boron. Both p and n type silicon wafers have a <100> orientation.

The SiNWs made in our lab was conducted in the following sequence:

1. Division of Si wafer: each wafer was cut into 4 pieces of sample.
2. Si sample is immersed in the following solvent in sequence:
    1) acetone for 15 minutes
    2) ethanol for 15 minutes
    3) deionized water, being rinsed for 2-3 times
    4) piranha solution with volume ratio as H_2SO_4(97%)/H_2O_2(30%) = 3:1 for 15 minutes
    5) deionized water 15 minutes
    6) 40% HF for 1 minute
3. Electroplating: the cleaned silicon sample is immersed into the HF and $AgNO_3$ prepared with deionized water for 1 minute at room temperature. Various $AgNO_3$ concentrations from 5 to 50mM are tested to fabricate SiNWs for the purpose of antireflection measurement. HF concentration is fixed at 4.8M.
4. Chemical etching: the electroplated silicon sample is dipped into the HF and H_2O_2 in dark at room temperature. 0.512M and 0.808M H_2O_2 concentrations are tested in our experiment. The durations are 30 minutes for SiNWs on p type and 2 minutes on n type, respectively. HF concentration is fixed at 4.8M.
5. Removal of silver: the etched sample is placed in a vessel containing HNO_3 (69 wt%) for 30 minutes at room temperature.

2.1.2. Characterization methods

One of the advantages of SiNWs is its antireflective property that is related to diameter of the wire and filling ratio of wire in array. The aim of SiNWs fabrication for solar cells is to absorb more visible light. Thus the desired SiNWs should have very low reflection, considering zero transmission of visible light through silicon. The antireflection requirement gives a facile operational criterion to select good silicon nanowires: the surface of SiNWs should be as black as possible. With this criterion we can determine the optimal parameters even with naked eyes by recognizing as-prepared sample's color, even if an accurate optical measurement is also performed with an integrating sphere to collect the reflection spectrum.

The reflection spectrum in visible range is measured in a 3-port sphere configuration provided by Sphereoptics®. The setup is shown in Figure 2-9 consisting of an integrating sphere with three main openings and an external light source. The entrance port allows the source light to enter into the spherical cavity. The inner surface of sphere is coated with an almost Lambertian reflecting materials. The ideal Lambertian surface and the spherical geometry make sure the input light spread evenly over the entire surface area of the sphere after multiple scattering. The sample was mounted first on the holder at back port and then at side port, when reflectance is to be measured. The principle for calculation can be found in Reference [77].

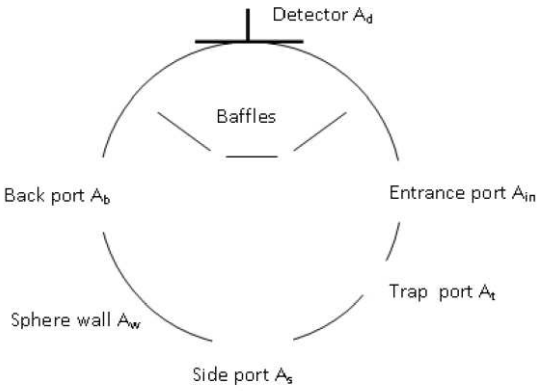

Figure 2-9 Schematic of the integrating sphere

The images of SiNWs and EDX analysis were recorded on a Philips XL ESEM scanning electron microscope (SEM) in Aix-Marseille University at PRATIM (Plate forme de recherche analytique, technologique et imagerie) center.

2.1.3. Morphology of SiNWs

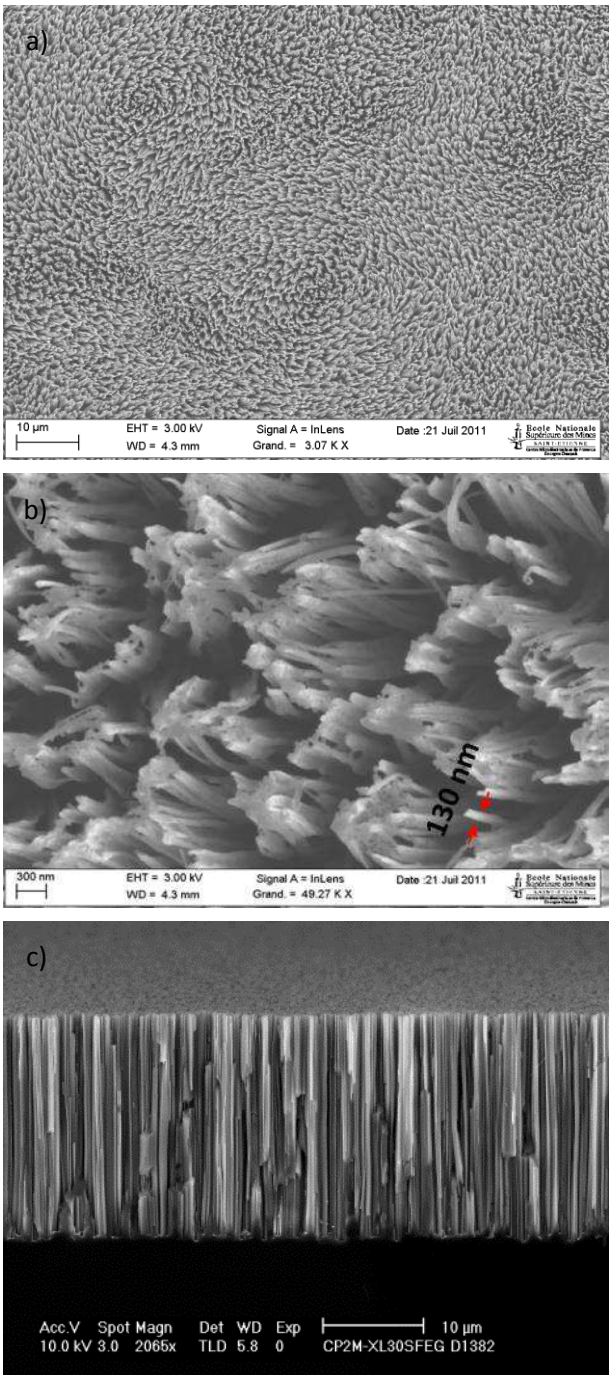

Figure 2-10 SEM images of EMACE etched p type SiNWs: (a) Top view, (b) tilted view, and (c) cross-section. The samples are fabricated on p type, [100] oriented silicon wafer with resistivity 1~10 ohm cm. The fabrication is conducted in 13mM $AgNO_3$ for 1 minute electroplating and then in 0.512M H_2O_2 for 30 minutes etching.

The morphology of our samples can be seen in SEM observations in Figure 2-10 and in Figure 2-11. In Figure 2-10 the SiNWs are made from a p type, (100) oriented silicon wafer with

resistivity 1~10 ohm cm. The fabrication is conducted in 13mM $AgNO_3$ for 1 minute electroplating and then in 0.512M H_2O_2 for 30 minutes etching. From Figure 2-10(a), the wires occupy a large faction of the total volume on the wafer. The diameter of a single wire is about 130nm as shown in Figure 2-10(b). The top tips of wire agglomerate to a bundle, and this can be attributed to surface tension forces exerted between wires during the sample drying[65]. Both the high filling ratio of wires and the agglomeration effect will lead to difficulty in pn junction fabrication especially for the purpose of core-shell junction construction by introducing foreign materials into interspace.

In Figure 2-10(c) of cross section view, the wire has the length of about 15μm after 30 minutes etching. The etching rate is estimated as 500nm/min. It is easy to control the length of SiNWs with etching time due to the linear dependence of etched length on duration, as mentioned in the introduction section.

In order to make PEDOT/SiNWs junction, the n type SiNWs etching is needed to study, because the PEDOT is a kind of p type semiconductor. The quality of hybrid cell is determined by the n type SiNWs properties. For example, the desired low reflection, thus high absorption, is determined by the pattern of SiNWs; the surface recombination is highly dependent on the surface morphology as an etching result; the following PEDOT electrodeposition is also dependent on etching because SiNWs works as electrode. So we will present the etching results of n type SiNWs, although some researchers[65][71][78] demonstrates similarity of etching between p type and lightly doped n type silicon.

The lightly doped n type wafer is used for SiNWs etching with the resistivity 1~10 ohm cm. These SiNWs are fabricated in 4mM $AgNO_3$ for 1 minute electroplating and then in 0.3M H_2O_2 for 2 minutes etching. It is not necessary to keep the same 30 minutes etching duration as p type silicon. In n type SiNWs fabrication, on one hand we find that 2 minutes duration is enough to get a rather low reflection, see the next section of KOH tapering. On the other hand, the wire length should be as short as possible to avoid large surface recombination. So we control the etching duration to be unvaried 2 minutes for all the hybrid cells made by electrodeposition of PEDOT.

The morphology of etched n type SiNWs can be seen in Figure 2-11. The length of wire is estimated from Figure 2-11(c) as 1.5μm. So the etching rate is 750nm/min, faster than p type etching. The EDX spectrum in Figure 2-11(d) proves that there are only silicon and silica in our sample, and silver particles have been removed after HNO_3 treatment.

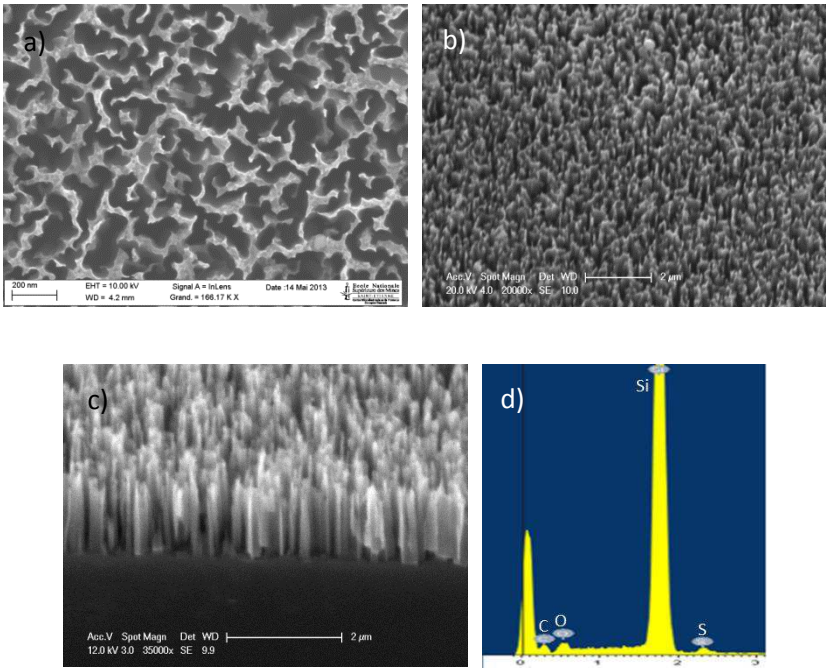

Figure 2-11 SEM images of EMACE etched n type SiNWs: (a) top view, (b) tilted view, and (c) cross-section. Panel (d) is the EDX analysis of the sample. The samples are fabricated on n type, <100> oriented silicon wafer with resistivity 1~10 ohm cm. These SiNWs are fabricated in 4mM $AgNO_3$ for 1 minute electroplating and then in 0.3M H_2O_2 for 2 minutes etching.

Another benefit coming from the short etching duration is that the agglomeration effect can be avoided. The SEM image in Figure 2-11(a) shows the agglomeration phenomenon doesn't appear in this nanostructure, compared with Figure 2-10 of 15µm SiNWs. One reason might be the short length of etched Si wire. The tension due to liquid evaporation is harder to make short Si to bend. Another reason may be the shape of wire: the n type SiNWs is more like belt rather than wire. The large belt-like wires are more difficult to bend than string-like wires.

The shape of SiNW and the pattern of SiNWs in array are determined by concentrations of $AgNO_3$ used in etching, which is the main topic in the next subsection.

2.1.4. Concentration of $AgNO_3$

The reflection spectrum of silicon nanowires can be determined by $AgNO_3$ concentration. The antireflection property of SiNWs should be attributed to the scattering photo-trapping effect of nanometer-scaled wire and space filling ratio of wire[79][37], as discussed in Chapter 1. The concentration of $AgNO_3$ is a key parameter for low reflection because it controls the distribution of silver particles during the electroplating process. Like the negative lithography method, the pattern of Ag network being imprinted into silicon substrate, the remaining part

of substrate becomes SiNWs array. So generally speaking, the $AgNO_3$ concentration determines the reflection of SiNWs through the pattern of deposited Ag network.

In Figure 2-12, various $AgNO_3$ concentrations from 5mM to 50mM are tested to identify the optimal concentration range for low reflection. The SiNWs fabrication is conducted for 1 minute electroplating and then in 0.512M H_2O_2 for 30 minutes etching. The lowest reflection can be ca. 1% at 13mM $AgNO_3$ from 500 to 800nm, as seen in Figure 2-12(a). The mapping in Figure 2-12 (b) shows clearly in the intermediate range from 13mM to 16mM that the SiNWs array has an average reflection as low as 2% throughout the visible spectrum.

To be more specific, the illustrations in Figure 2-12(b) show the influence of $AgNO_3$ concentration on final pattern of SiNWs.

If the surface density of silver particles is too low, caused by low concentration of $AgNO_3$ with the same electroplating duration, the mirror-like surface of silicon wafer would not be changed a lot after etching and therefore the reflection is high. See the schematic illustration on the upper left in Figure 2-12(b).

On the other hand, if the concentration is too high, the SiNWs occupy only a small fraction of the entire surface and the optimal scattering effect cannot be achieved with such a surface density of SiNWs. And this also leads to high reflection. See the illustration on the lower left in Figure 2-12(b).

The optimal concentrations lie in the intermediate range from 13mM to 16mM. The reason might be the strong light trapping effect due to appropriate wire dimension and space between wires. The comparison between Figure 2-10 and Figure 2-11 can also give an idea of the $AgNO_3$ concentration influence on SiNWs morphology. In Figure 2-10 (b) and (c) the nanostructure made at high concentration of 13mM $AgNO_3$ has the shape of string or stick, while at low $AgNO_3$ concentration of 4mM $AgNO_3$ the silicon nanostructure is closer to nanohole arrangement in Figure 2-11(a), and the remaining silicon is more like a wall or belt.

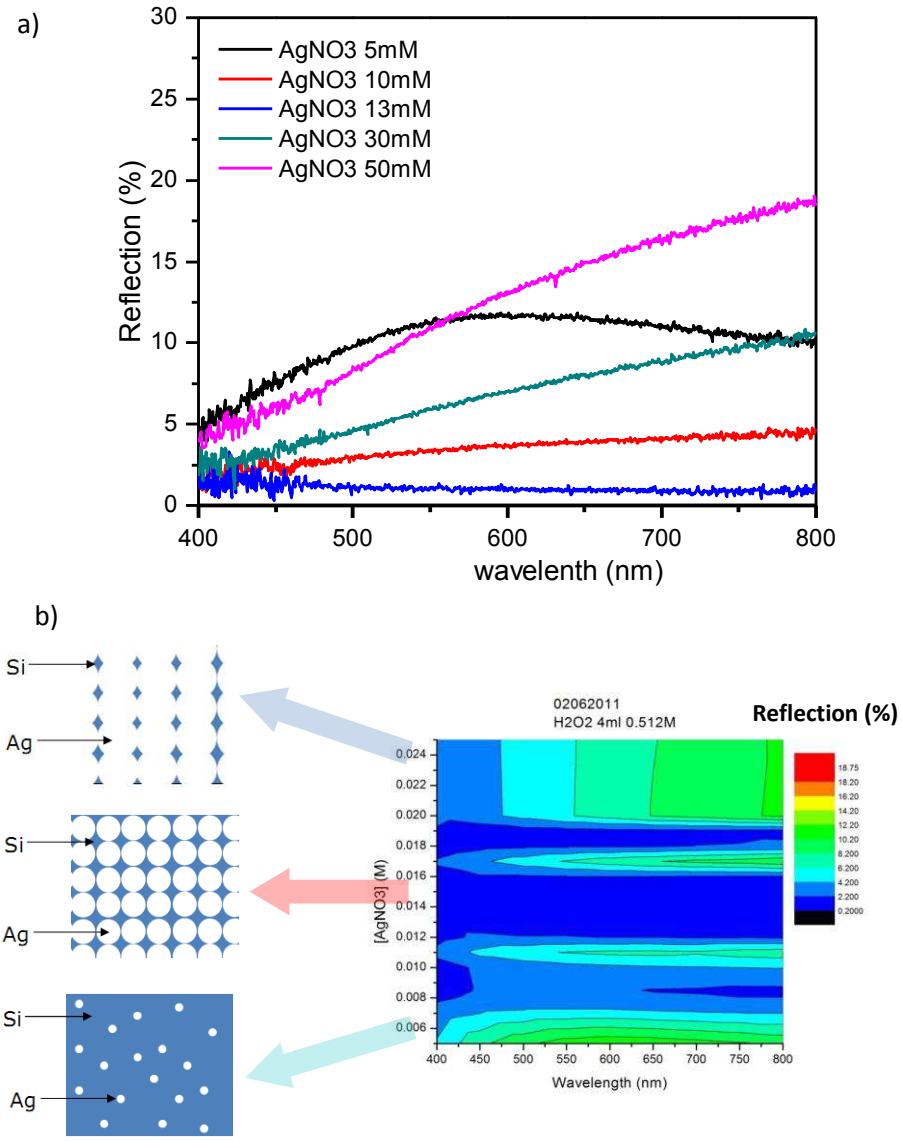

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Figure 2-12 Influence of $AgNO_3$ concentration on reflection spectra of SiNWs: (a) Reflection spectrum of SiNWs fabricated on p type silicon wafer with $AgNO_3$ concentration of 5, 10, 30 and 50mM. (b)The mapping on the right presents the measured reflection spectrum in visible range with varied $AgNO_3$ concentration at 0.512M H_2O_2. The three schematic illustrations on the left from top to bottom describe silver deposits with the $AgNO_3$ concentrations in low, intermediate and high range, respectively. This SiNWs are fabricated with electroplating for 1 minute and then with etching for 30 minutes.

This difference in morphology can be accounted by the EMACE mechanism stated above. The low concentration of $AgNO_3$ with the same duration of electroplating produces Ag isolated patches, but not a connected mesh or network. As the etching faithfully follows the pattern of Ag network, the etched structure is similar to nanohole rather than nanowires. Some simulation result[80] presents that nanohole structure may also have good

antireflection property. This might account for the low reflectance of SiNWs made at the relative low $AgNO_3$ concentration.

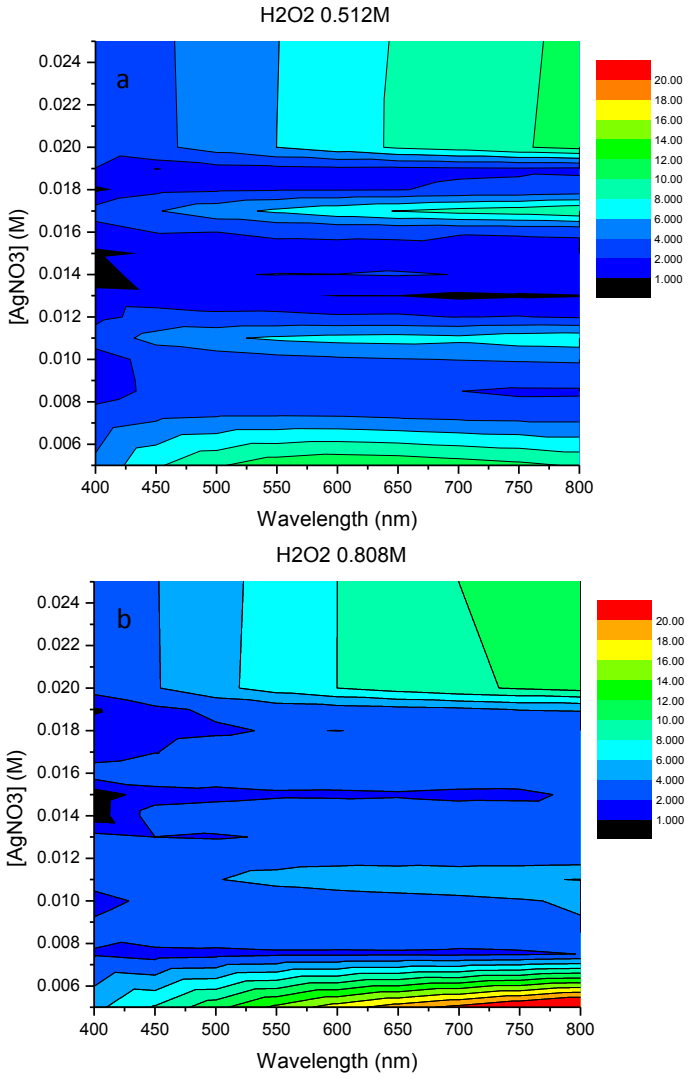

Figure 2-13 Reflection spectra map as a function of $AgNO_3$ concentration at tow H_2O_2 concentrations: (a) H_2O_2 0.512M, (b) H_2O_2 0.808M. The SiNWs array is fabricated from p type lightly doped silicon (resistivity 1-10 Ω cm) with <100> orientation. This SiNWs are fabricated with electroplating process for 1 minute and then with etching process for 30 minutes.

Figure 2-13 (a) (b) present the visible reflection maps in function of $AgNO_3$ concentrations for two concentrations of hydrogen peroxide while HF concentration is fixed at 4.8M: a low H2O2 in Figure 2-13 (a) and a higher in Figure 2-13 (b). The SiNWs array is fabricated from p type lightly doped silicon (resistivity 1-10 Ω cm) with <100> orientation. The difference between the reflection maps in Figure 2-13 is obvious but not significant. By varying the concentration of $AgNO_3$, the SiNWs array has a changed reflectance spectrum in visible range of 400-800nm. As stated previously, the $AgNO_3$ concentration range of 13-16mM at

0.512M H_2O_2 corresponds to the lowest reflectance which is desired for solar cells for the purpose of maximum absorption. The higher 0.808M H_2O_2 broadens the $AgNO_3$ concentration range of lowest reflectance to 12-19mM. The reason might be related to SiNW surface condition, since much rougher surface etched at higher H_2O_2 proportion might cause stronger photon scattering and therefore enhance absorption probability.

2.2. KOH tapering

As described in the chapter of introduction, because it is hard to fabricate radial pn junction within single wire with diameter more or less than 130nm, we decide to try radial heterojunction of PEDOT/SiNWs structure. Furthermore, since PEDOT is commonly used as p type semiconductor, silicon nanowires should be n type and therefore EMACE on n type silicon was explored in our work. In order to avoid huge surface recombination velocity, we attempted to reduce the length of etched SiNWs to 1.5µm, which also has low reflectance.

For PEDOT/SiNWs structure, our aim is to achieve a conformal layer of PEDOT surrounding each silicon nanowire. However, the as-prepared SiNWs are so dense that the space between the wires is too narrow to realize good quality conformal layer. Therefore KOH tapering is selected to vary the volume filling ratio of wire occupation on substrate by increasing the space between wires. The tunable filling ratio allows foreign materials to penetrate more easily between the wires and therefore provides the chance to get optimal heterojunction quality. This will be discussed in the chapter on PEDOT heterojunction fabrication.

In addition, the tapering technique might offer the opportunity to further lead to a decrease in reflection. In the reference[81], the authors believe that the tapering process in 30wt% KOH aqueous bath is able to make sharper the tip of wire. As a consequence the gradual increasing areal density from wire top-ends to bottom makes a gradual increase of effective refractive index from are (n=1) to silicon (n=3.42), as shown in Figure 2-14. This could be the reason for further reflectance reduction.

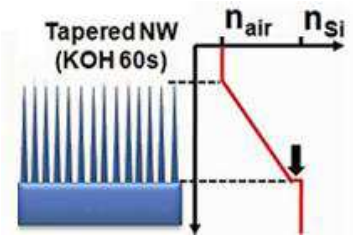

Figure 2-14 Schematic of relevance between wire morphology and the effective refractive index profile. Adapted from the reference[81].

However, such a lowered reflection might not be easy to be obtained on n-type SiNWs with KOH tapering, because of the condition-dependent nature of KOH corrosion reaction against silicon.

In Figure 2-15 the etching of KOH on (100) silicon appears under mass-transfer controlled[82], and consequently the etching rate can be increased by stirring. This causes the difficulty to get repeatable etching results, because any slight shaking of sample immersed in KOH

etchant bath may vary the etching speed. The etching rate is still rather fast when the KOH solution is diluted, which means that during the rinsing process in deionized water the etching might be still going on due to the remaining of KOH liquid.

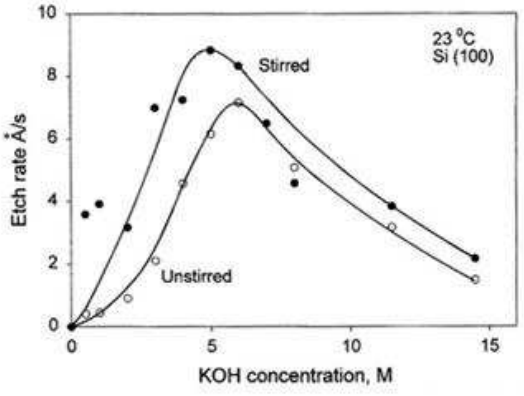

Figure 2-15 KOH etch rate versus molarity for 23℃ on the (100) surface [82]

In order to overcome these hurdles in SiNWs tapering process, we add isopropyl alcohol (IPA) into KOH aqueous solution. As shown in Figure 2-16, when 250ml isopropyl alcohol is added into 1L of 20wt% aqueous solution, the etching rate on the crystal plans (100) and (110) can be decreased by 20% and 90%, respectively[82]. Furthermore, the KOH etching reaction with IPA is less affected by mass transportation and thus stirring or shaking would not affect etch rate[82] .

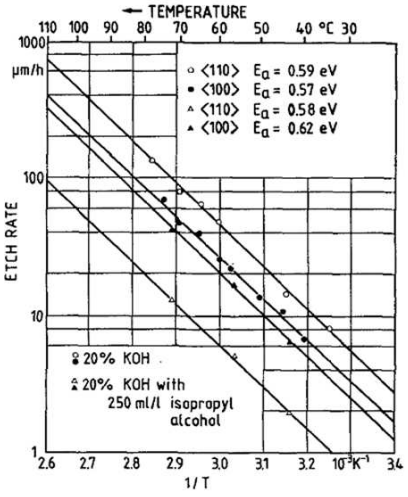

Figure 2-16 (100) and (110) silicon etch rate for a 20% KOH solution with and without the addition of isopropyl alcohol [82]

Besides, n-type SiNWs with 2 minutes etching are observed to disappear within 10 seconds in a tapering in 30wt% (6.3M) KOH aqueous solution. The reason might be high-energy defects on the silicon wire wall. So it is hard to get repeatable and stable tapered results by exactly controlling the duration of tapering within a few seconds.

We chose then to realize our tapering experiments in KOH aqueous solution containing IPA to slow down the rate of tapering on SiNWs and to get a reproducible tapering result. 31.2g KOH and 25ml IPA are added in 100ml deionized water. The KOH molar concentration is 4.0M, and its weight concentration is 20%. This SiNWs for tapering test have been fabricated in 4mM $AgNO_3$ for 1 minute electroplating and then in 0.3M H_2O_2 for 2 minutes etching. At last the samples are all immersed in HNO_3 69wt% for 30 minutes to remove Ag catalysts.

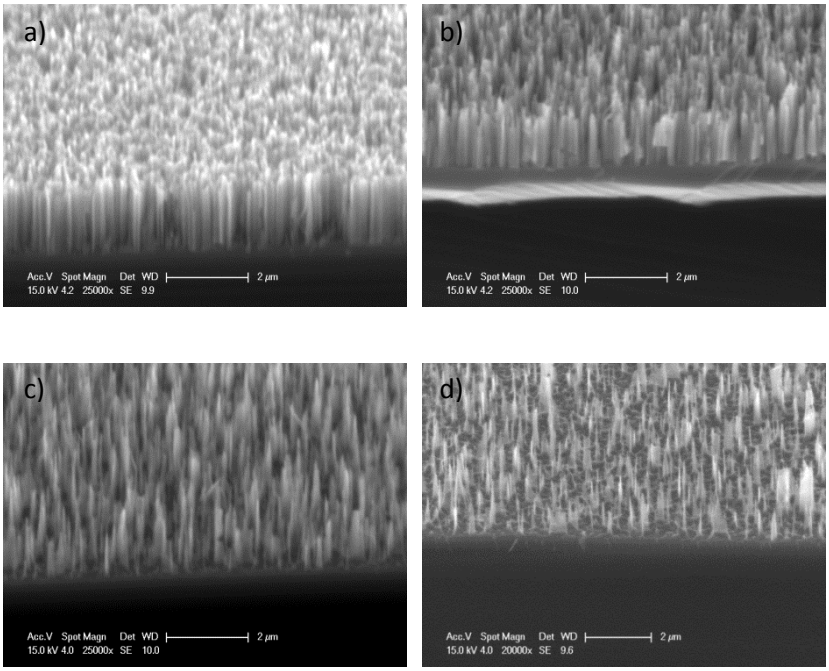

Figure 2-17 SEM observations of SiNWs treated without KOH and with various durations of KOH tapering. (a) without KOH, (b) KOH tapering for 10 seconds, (c) 30 seconds, and (d) 50 seconds. All the silicon nanowires samples are made from n-type silicon wafer, electroplated in 4mM AgNO3+ 4.8M HF aqueous solution for 1 minute, etched in 0.3M H_2O_2 + 4.8M HF bath for 2 minutes, and immersed in HNO_3 69wt% for 30 minutes. They then tapered in a 100ml 20wt% KOH aqueous solution added with 25ml IPA.

Tapering experiments are then performed on the n-type SiNWs for 4 durations from 0 to 50 seconds, without any stirring. The SEM observations are presented in Figure 2-17. KOH tapering not only reduces the filling ratio of wires occupying in array, but also shortens the aligned height of the array. The initial dimensions of the wires before tapering (see Figure 2-17(a)) are 1.6 µm long, 100nm wide with a density of ca. 25 wires/µm². After 10 seconds of tapering (Figure 2-17(b)) the length is decreased to 1.3 µm while the shape becomes more sharpened with more spacing between wires at the sample surface. That can be related to a preferential etching from the tip of the wires. After 30 seconds Figure 2-17(c), the remaining length is 1 µm with an apparent density at the surface of about 12 wires/µm², half of that of the beginning. After 50 seconds of etching (see Figure 2-17(d)) the wires are between 0.7 and 0.8 µm long still with more pores or less packed together, with a mean density of ca. 10

wires/μm². The reduced lengths of SiNWs are summarized in Figure 2-18 and the tapering rate is estimated as 20nm/s.

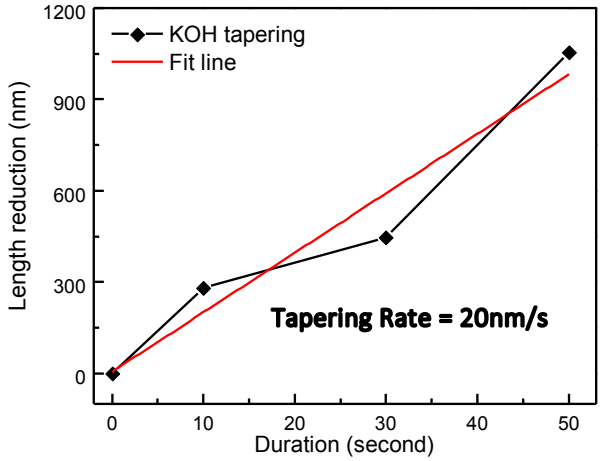

Figure 2-18 Relationship of reduced length of SiNWs with tapering duration. The tapering rate is estimated as 20nm per second.

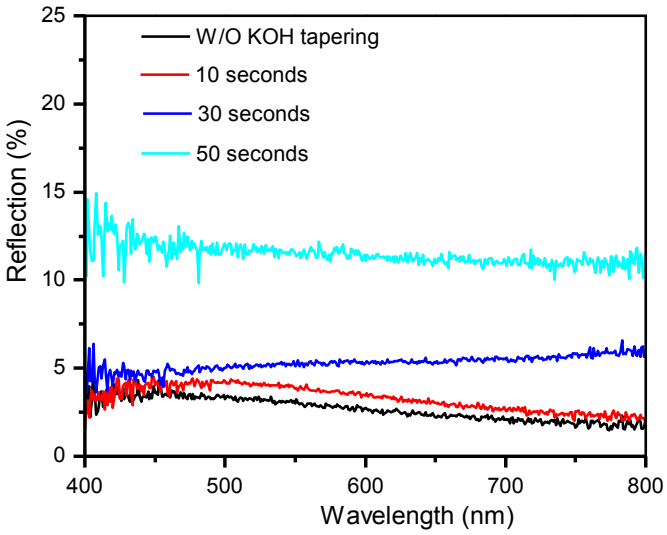

Figure 2-19 Reflection spectrum of SiNWs treated without KOH and with various durations of KOH tapering. The reflection for SiNWs without KOH tapering is in black, and those tapered for durations of 10 seconds, 30 seconds, and 50 seconds are shown in red, blue, and cyan, respectively. The tapering solution is 100ml 20wt% KOH aqueous solution added with 25ml IPA. All the silicon nanowires samples are made from n-type silicon wafer, electroplated in 4mM $AgNO_3$+ 4.8M HF aqueous solution for 1 minute, and etched in 0.3M H_2O_2 + 4.8M HF bath for 2 minutes.

The corresponding reflectance spectra of SiNWs with and without KOH+IPA tapering are shown in Figure 2-19. The 50 seconds tapering causes the spectrum largely lifted above 10% in the entire visible range, while the visible reflection is increased to 5-7% after 30 seconds

tapering, and the spectrum of 10s doesn't change greatly compared to the SiNWs without KOH treatment.

From the SEM images in Figure 2-17, the areal density of wires occupying in array is greatly decreased by 60% and the wire length is reduced by 50% after 50 seconds tapering, the trapping effect may be weakened due to the reduction in both areal density and length, leading to a rise in reflection 2-3 times higher than SiNWs without KOH tapering.

In the case of tapering time shorter than 30 seconds, although the areal density and the length of wires in array decrease with duration, the reflectance doesn't show an obvious increase. This suggests there is still a strong trapping effect in the array with larger interspace between wires. This tolerance gives the chance to make a good core-shell junction structure in array.

2.3. Active area selection

The active area of SiNWs can be easily defined by protecting the targeted SiNWs with goudron, and the unwanted area of SiNWs can be removed with CP4 solution (18mL 40%HF +57ml 69% HNO_3 + 25ml 90% CH_3COOH). The procedure is as follows:

1. The solid goudron is dissolved into an appropriate volume of trichloroethylene to make sure the dilution is suitable for area definition.
2. The targeted area is defined by covering the dissolved goudron.
3. Place the sample into an oven for baking at 35℃ until the goudron becomes solid again.
4. Immerse the sample into CP4 solution 2~3 minutes to remove unprotected SiNWs
5. Rinse the sample thoroughly in acetone, trichloroethylene, and deionized water in sequence.

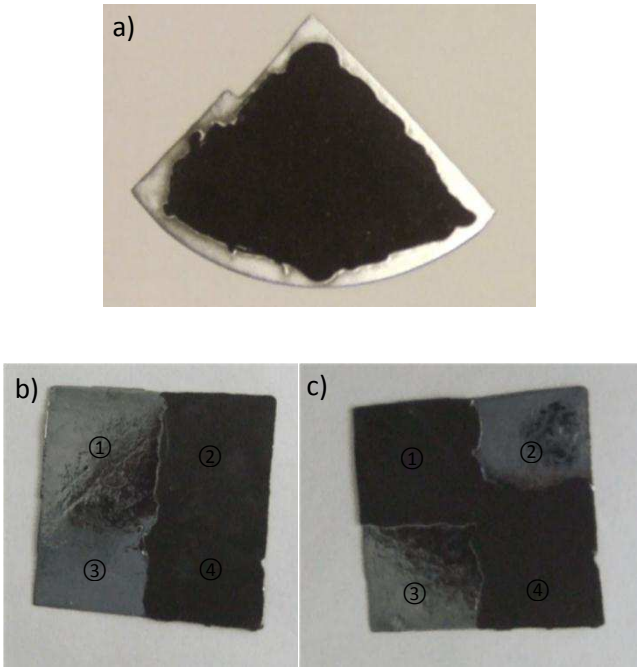

Figure 2-20 Photographs of SiNWs treated with area selection. a) Image of the sample with SiNWs on edge being removed. b) Image of the sample with SiNWs on the left half being removed. c) Image of the sample with SiNWs on two corners being removed.

The effectiveness of area definition in this way can be seen in Figure 2-20. The sample in Figure 2-20 (a) is defined to remove the SiNWs on the edge, and this may help avoid the shunt current pathway between front and back contact due to thermal diffusion doping process. The images in Figure 2-20 (b) and (c) show the front side and the back side of one

identical sample, and the entire sample is divided into four regions: ①,the front without SiNWs and the back with SiNWs; ②, the front with SiNWs and the back without SiNWs; ③, the front without SiNWs and the back without SiNWs; ④, the front with SiNWs and the back with SiNWs, as denoted in Figure 2-20.

But the goudron protection may bring contamination into SiNWs, if the samples are not cleaned thoroughly. This should be considered not to affect the quality of hybrid cell, since in the following step PEDOT will be deposited onto SiNWs.

Conclusions

To sum up, the relationship between $AgNO_3$ concentration and SiNWs reflection is studied, and the 13-16mM $AgNO_3$ range has been found to lead to low reflection. At 13mM $AgNO_3$ the reflection can be as low as 1% in the wavelength range of 500nm to 800nm. The explanation is given based on the pattern of deposited Ag in the electroplating step.

N type SINWs fabrication was also conducted at 4mM $AgNO_3$ for 2mins etching. The relative low $AgNO_3$ 4mM may results in the morphology more like wall or belt, while SiNWs made at higher concentration has the shape of wire. The tip agglomeration effect that occurs in the SiNWs made at high $AgNO_3$ concentration is avoided in this n type Si nanostructure, due to short length as well as belt-like morphology.

H_2O_2 concentration has no significant influence on SiNWs reflectance, but its effect on surface morphology is unknown yet. The length of SiNWs can be easily controlled with etching duration, and the etching rates are estimated as 750nm/min for n type SiNWs and 500nm/min for p type SiNWs.

KOH tapering process helps to enlarge the inter-room between wires by reducing the areal density of wires. 4 different tapering durations were tested. The SEM images confirm the space enlargement effectiveness of the tapering technique. More significantly, the strong trapping effect is still maintained in SiNWs if the tapering is shorter than 30 seconds.

The active region definition can be realized on SiNWs surface by using goudron protection and CP4 etching.

Chapter 3. PEDOT electrochemical deposition

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Glossary

1D	One-dimension
2D	Two-dimension
3D	Three-dimension
AAO	Anodic Aluminum Oxide
ACN	Acetonitrile
Ag	Silver
AgCl	Silver Chloride
$AgNO_3$	Silver Nitrate
BSi	Bulk Silicon
CE	Counter Electrode
ClO^{4-}	Perchlorate
CV	Cyclic Voltammetry
CVD	Chemical Vapor Deposition
EDOT	3,4-ethylenedioxythiophene
EDX	Energy-Dispersive X-ray
EMACE	Electroless Metal-Assisted Chemical Etching
GaAs	Gallium Arsenide
GaIn	Gallium–Indium eutectic
HF	Hydrofluoride acid
H_2O_2	Hydrogen peroxide
H_2SO_4	Sulfuric acid
IPA	Iso-Propyl Alcohol
KOH	Potassium hydroxide
OCP	Open Circuit Potential
PEDOT	Poly(3,4-ethylenedioxythiophene)
PF^{6-}	Hexafluorophosphate
PSS	Poly(Styrene Sulfonate)
PS	Potentio-Static
Pt	Platinum
RE	Reference Electrode
SEM	Scanning Electron Microscope
SHE	Standard Hydrogen Electrode
Si	Silicon
SiNWs	Silicon Nanowires
TiO_2	Titanium dioxide
VC	Vitreous Carbon
WE	Working Electrode

3.1. Introduction to PEDOT

3.1.1. PEDOT structure and its conductivity

Poly(3,4-ethylenedioxythiophene) (PEDOT) is a kind of conducting polymer. The conductivity of the polymer is dependent on its conjugated structure - see Figure 3-1(a). The backbone of polymer is formed by σ-bonded carbon atoms, while the remaining p orbital of carbon overlaps each other across σ-bond to engage in the conjugated π system. In fact the carbon-carbon bonds in the conjugated structure are not equally long. Some carbons are much closer to each other to form a repeat unit. The external distance between repeating units is longer than the internal distance within unit. The geometry inequality causes a result of energy bandgap between a completely filled π band and an empty π* band. The bond-alternating structure is typical for all conducting polymer[83].

The PEDOT in its neutral state, molecule shown in Figure 3-1(a) on the left, has low conductivity, because there is no partially filled band in polymer. This is similar to inorganic semiconductor. However, the concept of doping in conducting polymer is different from its inorganic semiconductor. Doping in inorganic semiconductor is the introduction of foreign atoms, while doping process in polymer is the oxidation reaction of polymer chain as shown in Figure 3-1(a). During the oxidation, the polymer becomes positive charged and counterbalanced electronically by anions like PSS^-, ClO_4^-, PF_6^- and so on. The model of PEDOT polymer with the counter-ions is shown in Figure 3-1(b).

The oxidation of polymer causes carbon chain deformation and creates new electronic states in the bandgap of polymer. With the extent of oxidation, polaron, bipolaron and soliton appear in the bandgap in sequence - see Figure 3-2. Like inorganic semiconductor, the newly created states increase the conductivity of polymer because of the charges stored in these levels.

The additional states in bandgap make polymer not only more conductive but also more transparent. In the Figure 3-3, the absorption spectrum of PEDOT varies with its state. In its oxidized state, for example, 0V and 0.5V, the PEDOT can be highly transparent in visible spectrum[84]. Due to the advantage of high transparency in the PEDOT conductive states, PEDOT is widely studied for its application in the field of organic solar cells[85].

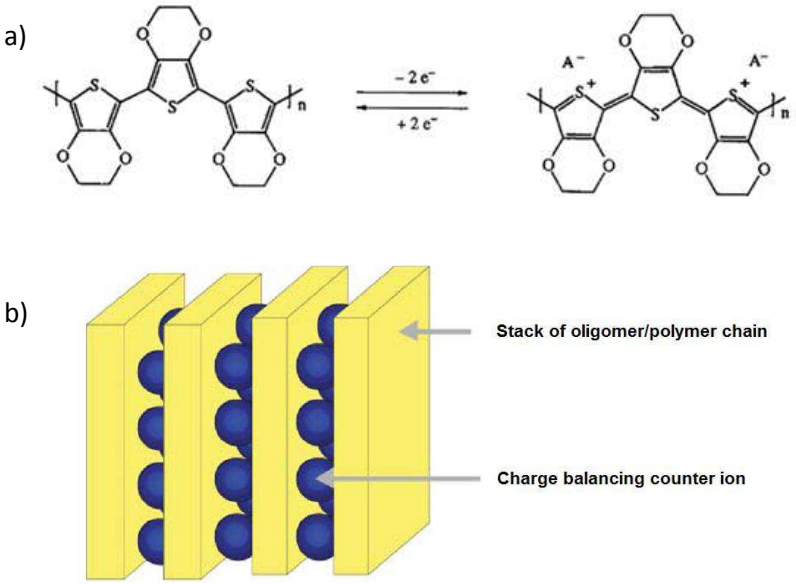


Figure 3-1 Schematic illustration of PEDOT structure: (a) Reversible transformation between neutral state (molecule on the left) to oxidized state (molecule on the right) with electrochemical methods, adapted from Reference [86]. On the oxidation state (molecule on the left) the charge on the backbone is balanced with an anion that may be either a small molecule or a macromolecule such as poly(styrene sulfonate) (PSS). (b) PEDOT stack structure. PEDOT chains are stacked with repeating distance. The doping counter ions are incorporated between the stacks. Extracted from Reference [87].

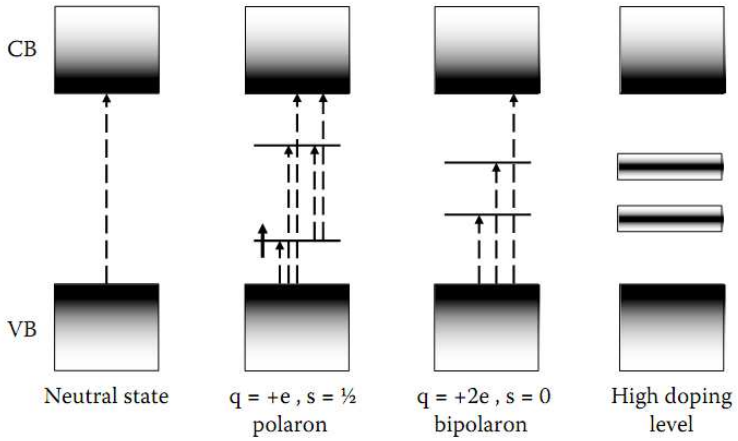


Figure 3-2 Diagram of energy level for conductive polymer. Dashed arrows indicate possible electronic transitions caused by photon absorption. Extracted from reference [88].

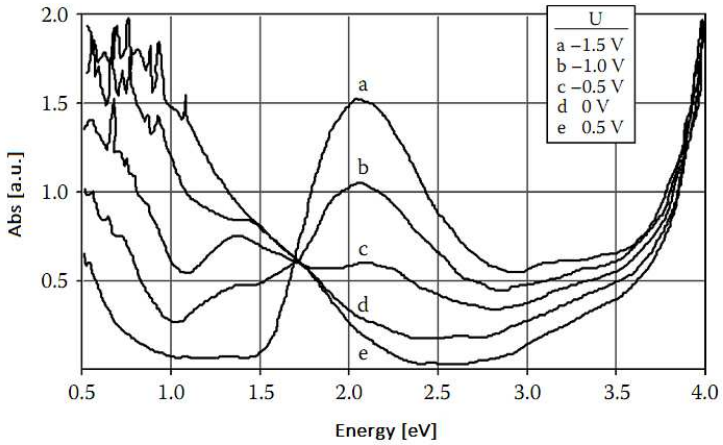


Figure 3-3 Optical absorption spectra of a PEDOT cell at different applied voltage. (a) -1.5V, (b) -1.0V, (c) -0.5V, (d) 0V, (e) 0.5V. [84]

The mechanism of charge transport in PEDOT is still not clear[88]. But at least two factors are directly linked to the conductivity of PEDOT. The one is the doping level that has already been stated above. The other is the ordering degree of PEDOT morphology. Generally speaking, disorder results in the localization of charges, and has a strong effect on electronic property. But in an ordered system the charge transport can be increased if the charges can hope or diffuse from one chain to another [88].

In this chapter we will present PEDOT synthesis and polymerization on SiNWs as electrode with electrochemical methods. Therefore the basic knowledge in semiconductor electrochemistry is necessary to understand the performance of SiNWs in PEDOT fabrication.

3.1.2. Fundamentals of semiconductor electrochemistry

In Figure 3-4 the electrolyte has the redox energy level E_{redox} which can be identified as the Fermi level of electrolyte[89]. When a semiconductor is immersed into the electrolyte, in equilibrium the semiconductor Fermi level E_F and E_{redox} are aligned across the interface through the flow of charges from one phase to the other. The band bending and the built-in voltage turn on in the depletion layer of semiconductor. The bend moving direction, downwards or upwards, and the extent of bending are dependent on the relative positions of E_F and E_{redox} in the band structure[89]. On the side of the electrolyte part, the Helmholtz layer is formed with ions absorbed onto the surface (protons on an amphoteric surface, for instance). The concentration of these ions defines the potential drop across the Helmholtz layer $\Delta\phi_H$ and controls the contact potential at the surface of the solid, defined as flatband potential ϕ_{fb}. This potential can thus be shifted up and down by changing the solution composition.

Considering the relative disposition of energy levels with respect to the band edge potential of semiconductor at the interface $\Delta\phi_H$, see Figure 3-4, the total potential difference can be given by

$$\Delta\emptyset_t = \Delta\emptyset_{DP} + \Delta\emptyset_H + \Delta\emptyset_G$$

$\Delta\phi_t$ is the potential as measured between an ohmic contact on the rear surface of the semiconductor electrode and the reference electrode. $\Delta\phi_H$ is the potential difference across the Helmholtz layer. $\Delta\phi_G$ is the potential drop across Gouy region which extend from outside the Helmholtz layer deep into the solution. The part $\Delta\phi_G$ is usually neglected if the electrolyte is concentrated. In the ideal case of no surface states and neglecting Gouy region, the equivalent circuit of the interface essentially collapse to its most simple form of depletion layer capacitance C_{DP} in series with Helmholtz layer's capacitance C_H[89].

One of the distinctions of semiconductor from metal electrode is the potential distribution of applied potential. Part of the potential is added on semiconductor making the analysis of the reaction in solution more difficult than conductive electrode.

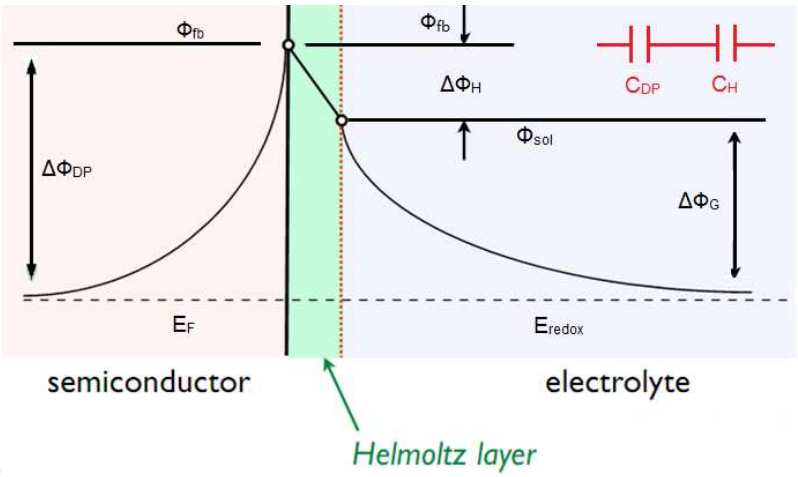


Figure 3-4 Energy band schematic of electrostatics at a semiconductor-electrolyte interface. The simplest equivalent circuit on the upper right represents the interface between semiconductor and electrolyte, when the Gouy region is neglected[89]**.**

Under illumination in Figure 3-5 the built-in electric field at the semiconductor-electrolyte junction allows for the charge separation of carriers generated by light absorption. In the case of a depletion layer in n-doped material, photogenerated electrons will migrate towards the interior of the solid. Holes will accumulate at the surface, where they can react with a donor in the electrolyte. In the bulk of the solid, far from the junction, no field exists to ensure charge separation. Electrons and holes produced there will diffuse to the depletion zone while undergoing the process of recombination.

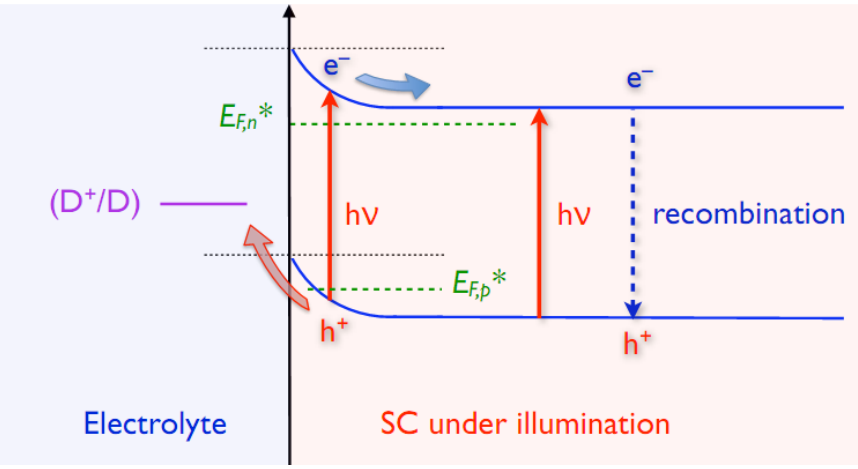


Figure 3-5 Photogeneration of electron-hole pairs in the field free region and depletion layer for a n-type semiconductor-electrolyte interface

The illumination is necessary for PEDOT electrodeposition. In Figure 3-6 of the band diagram, n type silicon band bends upward because the silicon Fermi level is higher than the redox level 5.96eV in EDOT solution (estimated from EDOT oxidation potential 1.3V VS. Ag/AgCl). The built-in electric field has the ability to sweep photogenerated holes from silicon body to EDOT solution across the interface. The high energized holes can oxidize EDOT monomer and trigger the further polymerization step, as will be presented in the next subsection. On the contrary, without illumination it is hard for n type silicon to oxidize EDOT and synthesize PEDOT because of the low concentration of holes in it.

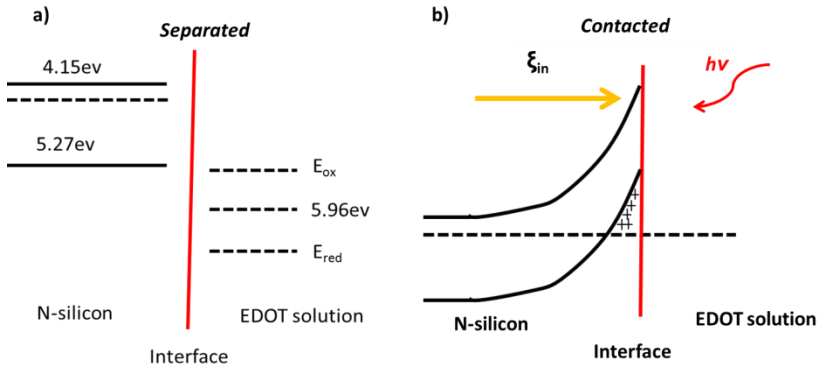


Figure 3-6 Schematics of band structure across the interface between silicon electrode and EDOT electrolyte: a) separated state and b)contacted state.

3.1.3. PEDOT electrochemical synthesis

The fabrication of PEDOT can be summarized into two steps: 1) oxidative polymerization of EDOT to neutral PEDOT and 2) oxidative doping of the neutral polymer to conductive state[87].

As can be seen in Figure 3-7, the reaction first begins with EDOT monomer oxidation to a radical cation. This step is the slowest and thus is a determining step. The cations combine with each other to dimer and finally to oligomer or polymer. At the end, the oligomer or polymer are further doped by oxidation. The anion A^- counterbalances positive charge and stabilizes the bipolaron state of polymer.

According to the literature[90] in the electrochemical method of PEDOT polymerization and deposition, monomer EDOT first oxidized and then diffuses towards the interface between electrode and solution. When oligomerization happens, a high region of oligomer appears. After super-saturation is attained, clusters are deposited on the electrode to become growing nuclei. The further 2D or 3D growth mechanism is dependent on deposition conditions.

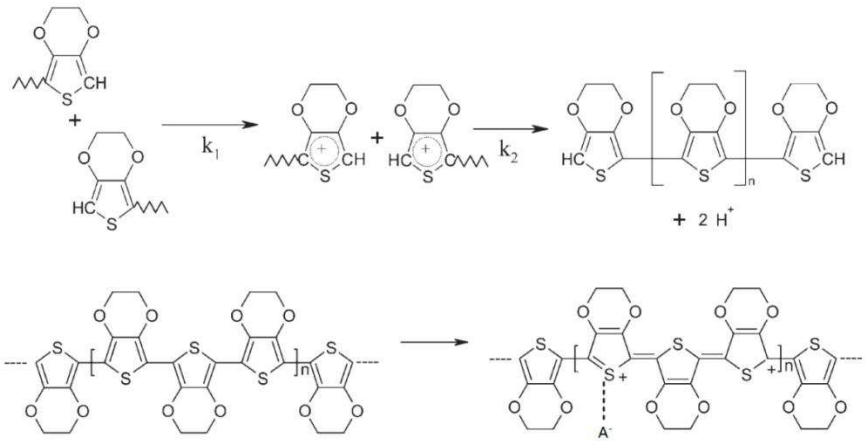


Figure 3-7 Proposed reaction mechanism for EDOT oxidation to conductive PEDOT [87]

What is interesting is the PEDOT synthesis and growth in nanometer scale. PEDOT nanostructure can be polymerized and deposited electrochemically on nanostructured semiconductors of ZnO[91], TiO_2,[92] GaAs[93]. Also the PEDOT morphology can be changed from nanotube to nanofiber according experimental conditions with AAO template[94]. Silicon nanowires array as template is really a new research field. Only CVD grown silicon nanowires[95],[96] have been studied for PEDOT preparation with electrochemical deposition method.

The interaction between the wall surface and polymer might be the mechanism for polymer being deposited and growing along the wall. One component to this interaction is solvophobic, that is, the polycationic form of polymer is insoluble in the solvent. The other component to this interaction is the on the wall [97]. The electrostatic attraction between cationic polymer and anodic sites leads to the nucleation and growth of polymer on the electrode surface.

One benefit from the growth in 1D nanometer scale, nanowire or nanotube, is the enhancement in polymer conductivity, because the chains on the outer surfaces of polymer film are aligned, leading to reduction in the number of conjugated interrupting defect sites. This alignment is caused by polymer stretching, crystallizing or both.[98]

3.1.4. PEDOT electrochemical characterization

As we mentioned about PEDOT conductivity earlier, it is to a large extent dependent on carbon chain deformation, and can be tuned reversibly by electrochemical polarization. Take the CV plot in Figure 3-8 for example, a PEDOT layer had first been deposited on Pt as electrode, and then the characterization of PEDOT layer was conducted on the Pt electrode. By calculating the charge involved during the oxidative process of PEDOT, the doping level of PEDOT can be determined [90].

The doping process of great interest is related to PEDOT oxidation in the forward sweep towards positive potential in Figure 3-8. The oxidation starts at -0.6V, reaches the first anodic peak at -0.3V. This corresponds to the appearance and accumulation of polaron states in the band gap of PEDOT- see Figure 3-2. The second current peak is at 0.25V. The amplitude of the second peak is much larger than the first one. This peak is related to the states of bipolaron formed in band gap as shown in Figure 3-2. After that, the current reaches a plateau. In the forward sweep from -1.3V to 1.2V, the polymer is transformed from neutral state to quasi-metallic state through polaron and bipolaron steps, and each step involves one electron transfer.

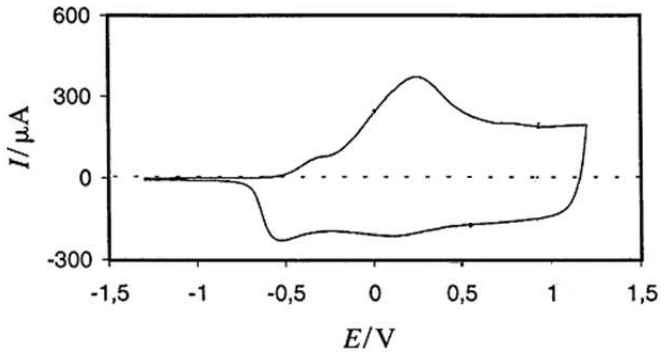


Figure 3-8 Cyclic voltammogram of PEDOT films in 0.1 mol/L TBAP + acetonitrile on a Pt electrode. The scan rate is 0.2V/s[90]**.**

The CV method shows its power not only in PEDOT fabrication but also in PEDOT characterization. The normal CV technique for electrochemical analysis is rather accurate on metal electrode. The accuracy is based on the fact that the applied potential is entirely added on the solution, and the current dependence on potential can give the useful and precise information about chemical reactions occurring in solution.

However, this technique may not be so precise on semiconductor electrode because part of the potential is partitioned on semiconductor, and the faction may vary with applied potential. The imprecision might be even worse since SiNWs properties as electrode is far to be known thoroughly. Although it is more difficult to give an accurate quantitative analysis about PEDOT synthesis on SiNWs, a qualitative description has been given in this chapter. Next is the section on PEDOT fabrication.

3.2. PEDOT electrochemical deposition on SiNWs

3.2.1. Apparatus

The device of three-electrode configuration in Figure 3-9 is used for PEDOT fabrication or characterization. The working electrodes (WE) we use are BSi, SiNWs or vitreous carbon. The counter electrode (CE) is platinum plate, and an Ag/AgCl is selected as reference. The synthesis of PEDOT here is conducted either using cyclic voltammetry (CV) or potentiostatic (PS) techniques. The use of such electrochemical cell allows to control the WE potential with respect to RE (that has a fixed potential and a high impedance), and to record current between WE and CE, vice versa. All the potential in this work are related versus Ag/AgCl electrode.

In the CV measurement, the scan in WE potential varies linearly with time from a beginning potential to a vertex potential, and then the potential sweep is reversed to the beginning. This ramp in potential can be repeated multiple times. When a new anodic or cathodic reaction is triggered at a specific potential, the recorded current would be changed correspondingly. Therefore the variation of current with sweeping potential, featuring in inflection point, peak current, and peak potential, may provide important information about the reaction of interest. The PEDOT polymerization was carried out with the three-electrode apparatus Solartron SI 1287 controlled by a computer running CorrWare software. The entire experimental working configuration can be seen in Figure 3-10.

When the substrate is the n type silicon, to improve its conductivity in anodic potential zone, an illumination on the surface is necessary. A 150w halogen lamp is employed, connected to a variable resistor to tune its output power. The illumination intensity is dependent on the lamp power, and the dependence has been measured as in Figure 3-11 by placing the monitor at a 10cm away from it. In order to evaluate the illumination intensity influence on PEDOT polymerization and characterization, two power output percentages of 70% and 100% are used.

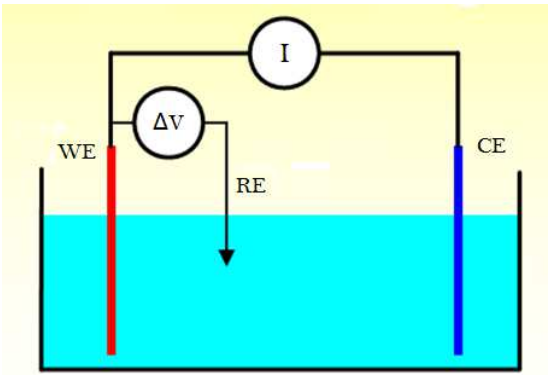


Figure 3-9 Schematic of electrochemical device in a three-electrode configuration

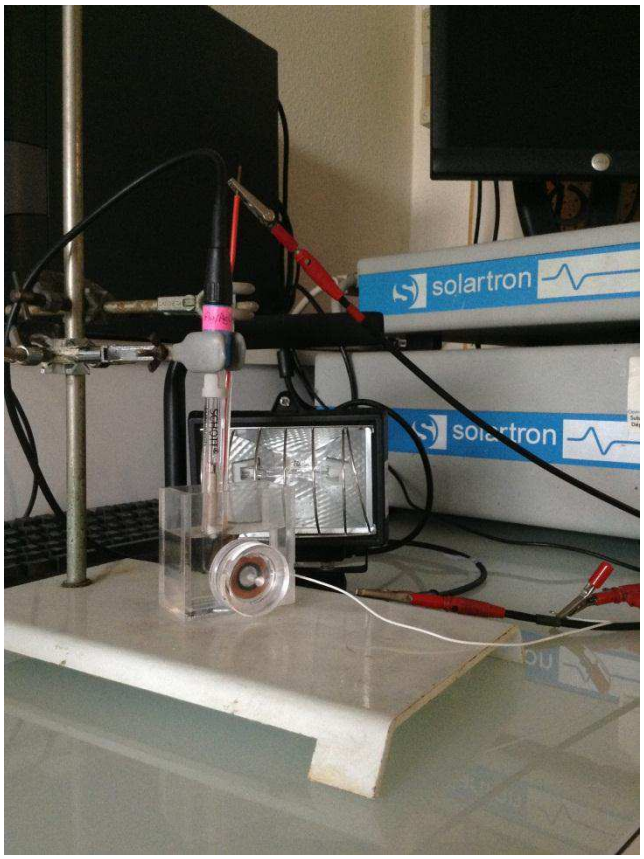


Figure 3-10 Picture of the three-electrode working cell for PEDOT polymerization in connection with the electrochemical workstation Solartron, including the halogen lamp.

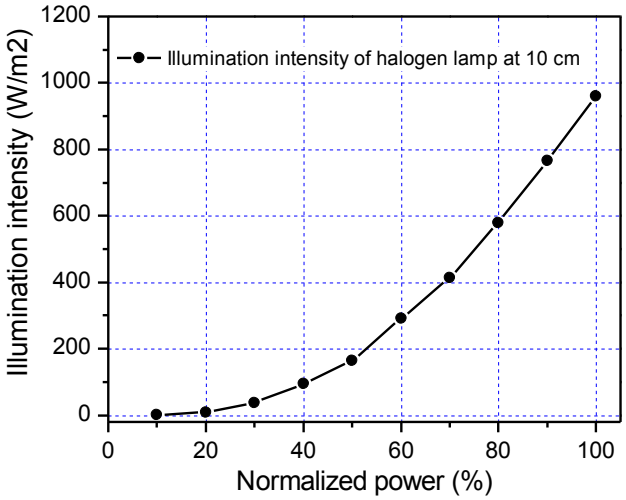


Figure 3-11 Relationship between light illumination intensity and normalized lamp power

3.2.2. PEDOT fabrication

Procedure

The total procedure is shown in Figure 3-12, and the details are as follows:

1. The n type SiNWs are fabricated with EMACE technique as presented in the previous chapter. All the SiNWs are fabricated first by the electroplating process in 4mM $AgNO_3$ 4.8M HF aqueous solution for 1 minute, and then by the etching process in 0.3M H_2O_2 4.8M HF aqueous solution for 2 minutes. The Ag catalysts in SiNWs are removed by be immersed in HNO_3 for 30 minutes.

2. The SiNWs electrode is immersed for 5 minutes in 5% HF of ethanol solution to remove native silicon oxide layer on the surface.

3. SiNWs on the back side surface of the sample are scratched off in order to improve back contact conductance. The back side of the substrate is then placed on a copper ring that is connected via an electronic wire to the working electrode plug of the measurement controlling equipment Solartron, as seen in Figure 3-10 . In order to increase the quality of the electrical contact between the Si substrate and the copper ring, GaIn is spread between them.

4. The SiNWs sample is placed on the working cell's surface that has a circular opening with 1.1cm in diameter which allows $1cm^2$ of the substrate be easily exposed to the solution. A cap is then screwed to keep all the pieces in contact and facing the opening of the solution. The cell picture is in Figure 3-10.

5. PEDOT is polymerized from a 10mM EDOT ACN solution containing 0.1M $LiClO_4$ electrolyte for all the experiments presented in this chapter.

6. After the electrodeposition, the sample is rinsed with acetonitrile for several times to remove EDOT monomer, rinsed thoroughly with ethanol and then dried with air stream.

For the bulk silicon WE electrode, we begin the procedure from step 2 above. For vitreous carbon, a 1.8 cm^2 disc of carbon is first polished with 6 µm diamond pastes and then put in an ultrasonic bath to remove all the particles coming from polishing. The vitreous carbon disk is then placed in an appropriate Teflon holder that lets a 1 cm^2 useful surface exposed to the electrolyte. A classical three electrode cell is used here, without illumination, and the experimental procedure begins from Step 5 above.

The morphology of PEDOT on SiNWs is usually dependent on the fabrication conditions. Path A in Figure 3-12 is a continuous deposition that corresponds to cyclic voltammetry or

potentiostatic deposition experiments. The other way of path B in Figure 3-12 is a step-wise deposition, which favors EDOT monomer diffusion into space between wires and thus results in conformal layer. The discussion will begin first on continuous deposition and then the step-wise technique.

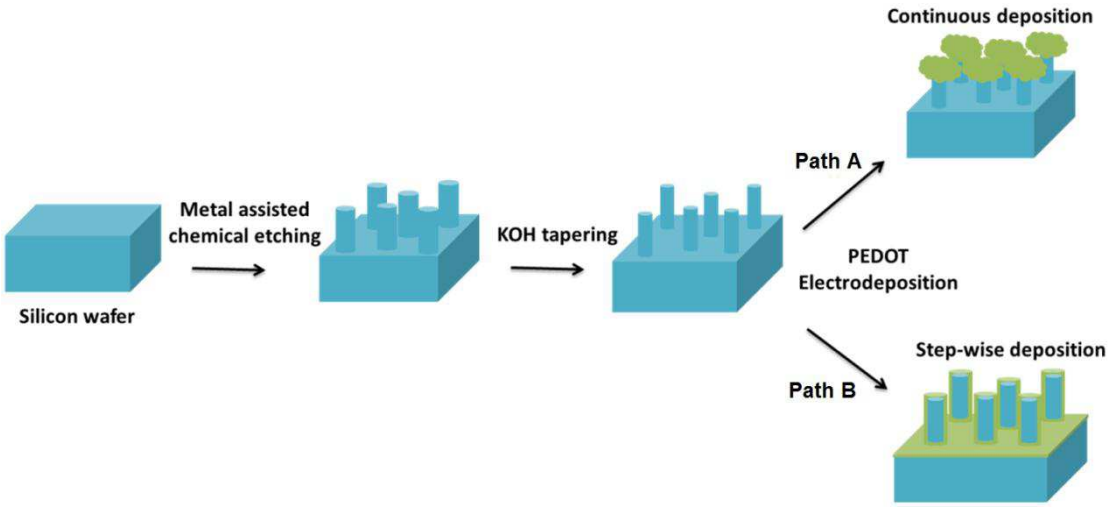


Figure 3-12 Schematic illustration of the processes towards PEDOT/SiNWs hybrid structure: (a) Continuously electrodeposition leads to mushroom-like morphology of PEDOT (green) on the tips of silicon nanowires (blue), while (b) step-wise deposition helps to get conformal PEDOT layer (green) surrounding single silicon wire (blue).

Path A: Continuous deposition

As we said, CV is a powerful characteristic method in electrochemistry to understand reaction processes by observing the current density change with potential. We use CV characterize PEDOT polymerization processes on vitreous carbon, BSi, and SiNWs. The PEDOT fabrication on vitreous carbon is first measured, and the result CV plot is used as reference to analyze those measured on BSi and SiNWs.

PEDOT polymerization on vitreous carbon

In Figure 3-13, from the blank electrolyte (the curve in black), only a slight oxidation current is performed when the potential reaches 1.8V. This could be due to the oxidation of the small amount of water contained in EDOT (97% mass concentration), or directly to the acetonitrile oxidation itself[99]. The reproducibility of the experiment is good while 2 cycles are almost the one after the other.

The cyclic voltammetry measurement from EDOT containing solution, starting from 0 to 2V, is shown in red in Figure 3-13. When the potential is increased, no current is performed till a

potential value of 1.3V. As the potential scans to a higher value, a first EDOT oxidation peak appears in good agreement with the literature[87], leading to a rapid synthesis of PEDOT. The next increase in current around 1.9V can be due to the acetonitrile or the water containing oxidation already mentioned above.

When the potential is reversed, a cross over between the forward and the backward current is observed between 1.3V and 1.1V, drawing a loop. It comes because it is easier to deposit PEDOT on PEDOT during the reverse scan, than PEDOT on vitreous carbon (during the forward scan). This loop is called a nucleation loop and implies that PEDOT film completely covers the initial vitreous carbon surface. When the potential decreases below 0.5V, a small reduction current is performed on the backward scan that shows that the polymer can be put on its reduced state[90]. During the second scan, the oxidation of EDOT begins at a lower potential (1.1V), and no nucleation loop is performed, because the vitreous carbon substrate is completely covered by the PEDOT film during the first cycle. Note that, at the end of experiment, when the electrode is removed from the cell, it is completely covered with a visible blue film.

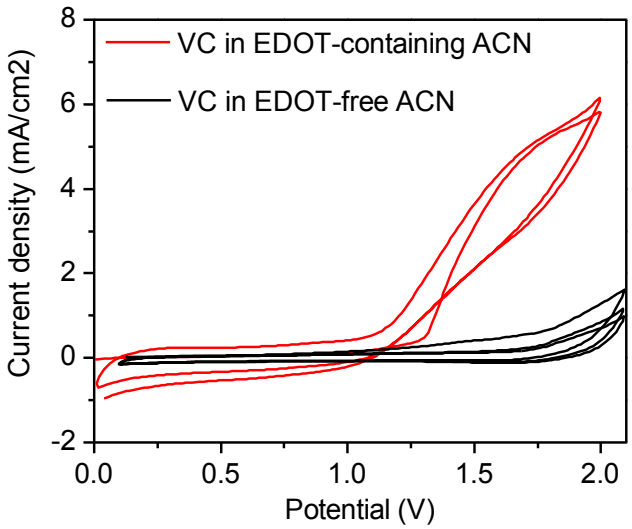


Figure 3-13 CV curves made on vitreous carbon electrode. The EDOT-containing solution is 10mM EDOT + 0.1M $LiClO_4$ in acetonitrile, and the EDOT-free blank solution is 0.1M $LiClO_4$ in acetonitrile. The scan rate is 100mV/s.

PEDOT polymerization on BSi

Figure 3-14 presents the influence of substrates on PEDOT deposition mechanism. Figure 3-14(a) obtained on BSi substrate, shows the similar CV relationship as on vitreous carbon. During the first cycle, no current is performed until the potential reaches a value of 1.3V, followed by a step increase in current due to a rapid EDOT oxidation and PEDOT formation. Notice that the current density performed in this case is smaller than on vitreous carbon,

showing that, despite the light on the Si surface, the substrate is less conductive. Then on the backward scan, the nucleation loop appears, and a reducing current between 0.6 and 0V is due to the reduction state of PEDOT[87]: a PEDOT layer is then also achieved on Bulk Si.

However, some differences appear between vitreous carbon and BSi substrate during the second cycle: a first oxidation peak is here clearly performed between 0.6 and 1V that should correspond to the oxidation of the PEDOT layer[87]; the second oxidation peak between 1.1 and 2V, corresponding to the oxidation of EDOT on PEDOT appears with a weaker current and is followed by a decrease in current. During the third cycle, the current performed in this last potential zone continues to diminish. In this case, the shape of this oxidation peak should not be due to a diffusion control mechanism of EDOT in solution because we do not observe this behavior on vitreous carbon, but rather due to a decrease on Si conductivity during the scans caused by a thickening of a blue PEDOT layer that prevent the light from reaching the Si surface. The lowered amount of photo-generated holes directly causes the decreasing rate of PEDOT synthesis.

PEDOT polymerization on SiNWs

We also compare the SiNWs CV behavior in EDOT-containing acetonitrile solution with that in EDOT-free ACN, as shown in Figure 3-15. Similar to the CV curve on vitreous carbon and on BSi, an inflection point appears at 1.3V. After the inflection potential the current density measured from the EDOT-containing ACN is much higher than that recorded in EDOT-free solution, suggesting that the current density is resulted from PEDOT polymerization.

On SiNWs electrode, the CV curves in Figure 3-14(b) have similar features to bulk silicon in Figure 3-14(a) in the potential region corresponding to PEDOT deposition: a lowering decrease in current density after each cycle, on the second and third cycle the characteristic peaks of the oxidized and reduced state of PEDOT. In addition the peak current density for the first EDOT oxidation on SiNWs is much higher than that on bulk silicon. The cause might be the much rougher surface.

However, during the first oxidation cycle, a large oxidation current is performed between 0.2 and 1.3V, which disappears for the second and the third cycle. To have a better insight on this phenomenon, voltammograms are performed on SiNWs in EDOT free solution and compare to the EDOT containing solution on the same substrate (Figure 3-16). The similarity of the CV curves between SiNWs in EDOT solution and in EDOT-free solution supports the idea that the high first oxidation current density is due to silicon, showing that the nanowires are less stable than the corresponding bulk Si. The supposed silica layer could nevertheless also have a bad an effect of causing a high series resistance in hybrid solar cell of silicon/PEDOT.

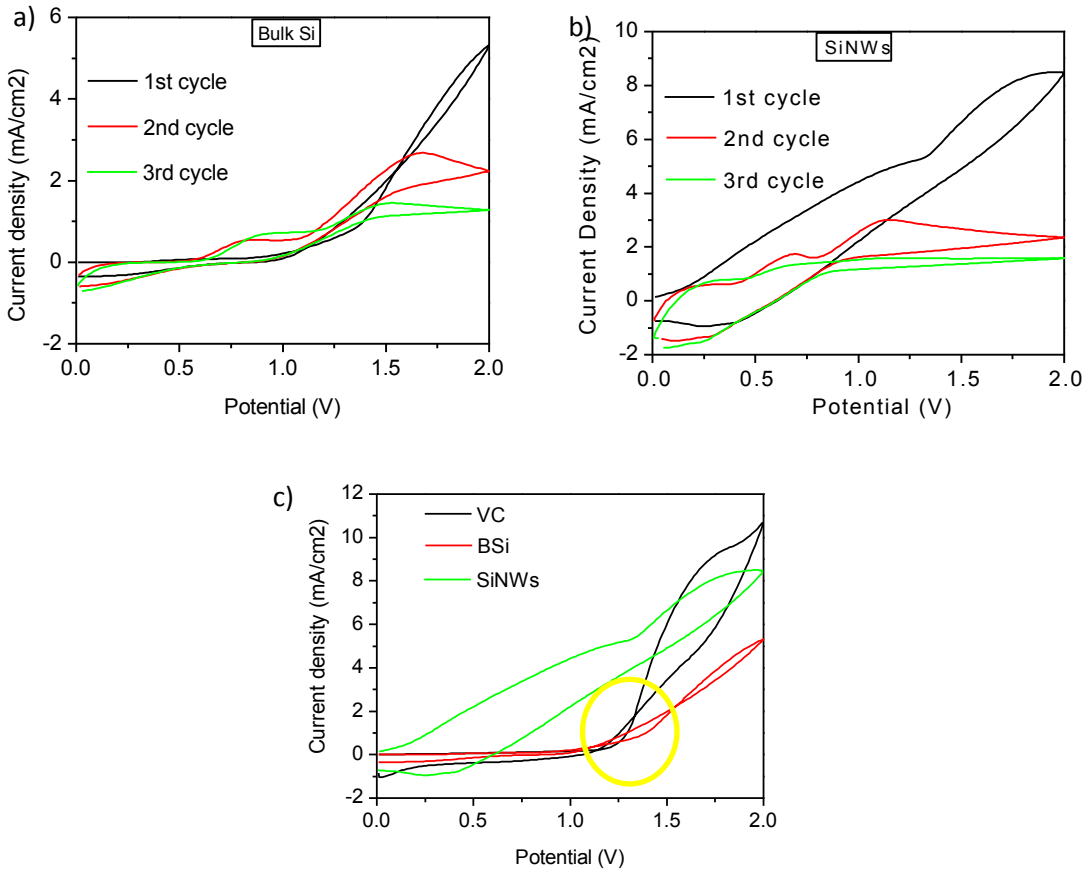


Figure 3-14 Cyclic voltammetric grams of PEDOT fabrication on three different electrodes: (a) bulk silicon, (b) silicon nanowires array. Panel (c) combines the first cycles of three electrodes. The CV measurements with electrodes BSi and SiNWs are made under 100% illumination. The solution is 10mM EDOT with 0.1M $LiClO_4$ in ACN, and the scanning rate is 100mV/s for all the three CV measurements. The yellow ring highlighted the current loops that are characteristic for conductive polymer deposited on electrode. The SiNWs are fabricated first by the electroplating process in 4mM $AgNO_3$ 4.8M HF aqueous solution for 1 minute, and then by the etching process in 0.3M H_2O_2 4.8M HF aqueous solution for 2 minutes. The SiNWs are not treated with KOH tapering.

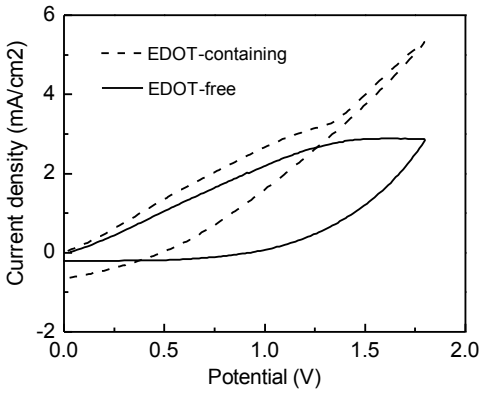


Figure 3-15 Comparison of SiNWs voltammogram from EDOT-containing ACN with that from EDOT-free ACN . The CV measurements are made under 100% illumination. The SiNWs are fabricated first by the electroplating process in 4mM $AgNO_3$ 4.8M HF aqueous solution for 1 minute, and then by the etching process in 0.3M H_2O_2 4.8M HF aqueous solution for 2 minutes. The SiNWs are not treated with KOH tapering.

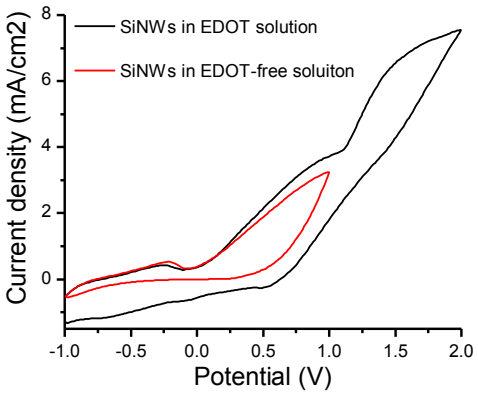


Figure 3-16 Comparison cyclic voltammetry graph of SiNWs in EDOT solution with that in EDOT-free solution. The scanning rates are 100mV/s for both measurements. The CV measurements are made under 100% illumination. The SiNWs are fabricated first by the electroplating process in 4mM $AgNO_3$ 4.8M HF aqueous solution for 1 minute, and then by the etching process in 0.3M H_2O_2 4.8M HF aqueous solution for 2 minutes. The SiNWs are not treated with KOH tapering.

Evidence for illumination significance

The illumination is necessary for PEDOT polymerization with silicon nanowires as electrode. Figure 3-17 shows the CV curves performed under ambient, 70%, and 100% illumination on n SiNWs in an EDOT-containing solution. The comparison clearly shows the need to work under illumination: under ambient light the current density is almost zero, while under illumination the CV curve shows two increases in anodic current around 0.5V and 1.1V. The second oxidation peak corresponds to the EDOT oxidation. The current density in the forward sweep at 100% power is much larger than that at 70% power. The principle of illumination working on PEDOT polymerization on semiconductor has been given in the introduction section. As described in Figure 3-6, the illuminating light generates electron-hole pairs which are separated in the built-in electric field of space charging area in n silicon. The photogenerated holes are swept to EDOT solution across the interface, oxidizing EDOT monomer to trigger the subsequent polymerization step.

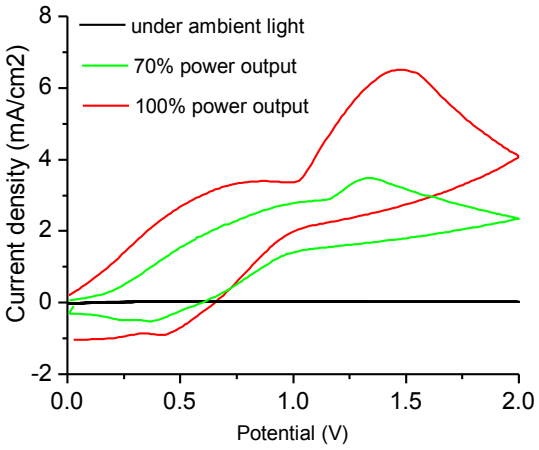


Figure 3-17 Comparison of PEDOT electrodeposition on SiNWs under ambient light (black), under 70% (green), and under 100% (red) lamp light . The SiNWs are fabricated first by the electroplating process in 4mM $AgNO_3$ 4.8M HF aqueous solution for 1 minute, and then by the etching process in 0.3M H_2O_2 4.8M HF aqueous solution for 2 minutes. The SiNWs are not treated with KOH tapering.

PEDOT on SiNWs observations

The SEM and EDX measurements are then performed on a PEDOT deposit on SiNWs substrate (Figure 3-18(a) and Figure 3-18 (b)). The SiNWs are fabricated with EMACE method: first electroplated in 4mM $AgNO_3$/HF for 1min and then etched in 0.3M H_2O_2 /HF bath for 2min. 10 seconds KOH tapering is performed on etched SiNWs. The PEDOT is deposited electrochemically in a potentiostatic manner at fixed 1.5V potential for 5 seconds in 10m EDOT ACN solution with 0.1M $LiClO_4$. The potential 1.5V is selected according to CV measurement on SiNWs in Figure 3-14(b) where 1.5V is larger than the synthesis starting point around 1.2V to make sure PEDOT deposition is conducted at this potential.

The SEM image in Figure 3-18(a) shows a disturbed area by the cutting of the sample. A continuous film is mainly formed on the top of silicon wires. The presence of elements S and C in the EDX analysis of Figure 3-18(b) proves that the film is effectively PEDOT. The bottom space between the Si nanowires seems not to be filled by the polymer. This is caused by the competition between PEDOT polymerization on the tips and EDOT diffusion from solution to deep inner space at the bottom. Because the sharp morphology of the wire tip can produce much more intense electric field, more EDOT cations are produced in the region in proximity to the tip of silicon wires than the bottom part of wire, resulting in an increase in polymer volume at the tip and finally a mushroom-like morphology on top of the sample. The expanded polymer blocks the entry of EDOT diffusion into the deep space, the 2D spread of PEDOT along the wire surface towards the bottom might be prevented due to the lack of EDOT monomer supply.

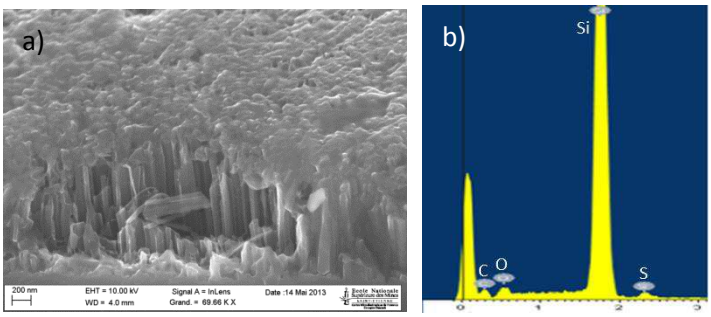


Figure 3-18 SEM and EDX of PEDOT on SiNWs after 5 seconds electrodeposition: (a) SEM tilted view of covering the top of SiNWs array. (b) EDX (Energy-dispersive X-ray) analysis shows the chemical composition of materials, where carbon, oxygen, and sulfur atoms are corresponding to PEDOT. The SiNWs are fabricated first by the electroplating process in 4mM $AgNO_3$ 4.8M HF aqueous solution for 1 minute, and then by the etching process in 0.3M H_2O_2 4.8M HF aqueous solution for 2 minutes. The SiNWs are treated with 10secods KOH tapering. PEDOT are deposited potentiostatically at 1.5V for 5 seconds in 10mM EDOT 0.1M $LiClO_4$ ACN under 100% illumination.

Path B: Step-wise deposition

Step-wise deposition technique

In order to get the conformal deposition, a step-wise deposition is attempted to force the PEDOT formation all around the wire. The scheme as seen Figure 3-19(a) shows that the deposition is composed of several repeated units. In each unit the 1 second pulse in potential at 1.5V is followed by the 10 seconds rest, during which the recording potential corresponds to the open circuit potential (OCP) and is the characteristics of the electrode/electrolyte interface. Any change in this potential can then be correlated to a change in the surface of the substrate due to PEDOT deposition. The unit is made 5 times to get a total deposition pulse period of 5 seconds in order to make comparison with the case of 5 seconds continuous deposition, as seen above.

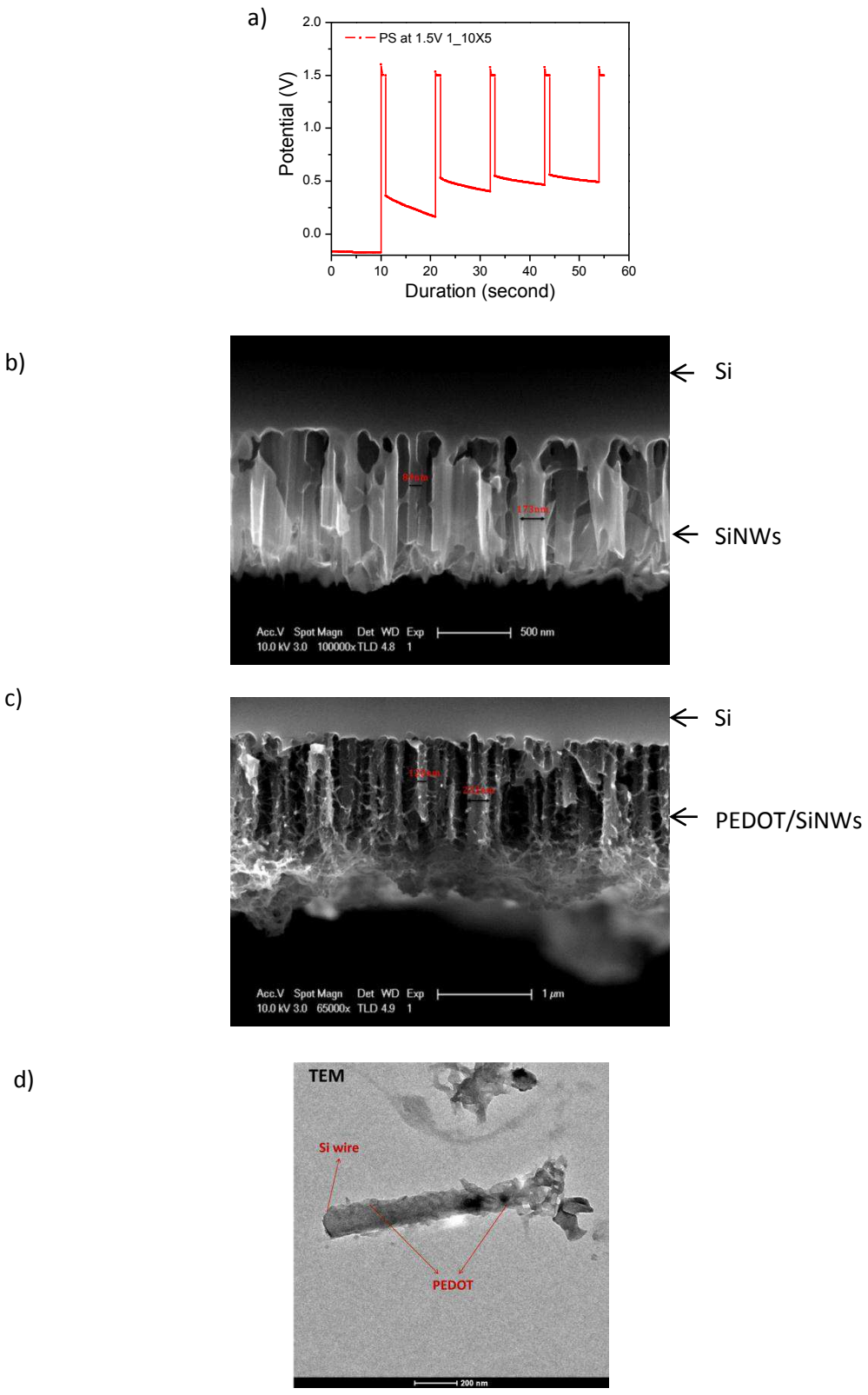


Figure 3-19 Step-wise deposited PEDOT onto SiNWs: (a) Potential – duration characteristics, (b) Cross section view of SEM image of SiNWs without PEDOT. (c) SEM image of cross section of SiNWs array with PEDOT corresponding to the step-wise deposition in (a). (d) TEM of SiNW/PEDOT wire.

As can be seen in Figure 3-19(b) the SiNWs without PEDOT deposition shows sharp edges and concave surfaces along the wire. On the contrary, in Figure 3-19(c) the wire shape is like a column and its wall is covered by a layer and filaments which make sharp edges more rounded. Rather than filling the space between wires, the layer wraps each wire to get a good conformal configuration which is just what's desired for a core-shell structure. The dimension of the wire on average is also increased from 131nm in Figure 3-19(b) to 176nm in Figure 3-19(c). Quite different Figure 3-19 (b) in which the bottom of wire is not covered by polymer, in Figure 3-19(c), we can see the polymer reaches the root of each wire. This should be attributed to the rest time introduced between separated deposition pulses, which allows monomer to diffuse into the deep interspace between wires, and therefore results in the PEDOT formation at the root of wire. In the TEM image in Figure 3-19(d), we can see that the Si wire is wrapping in a polymer.

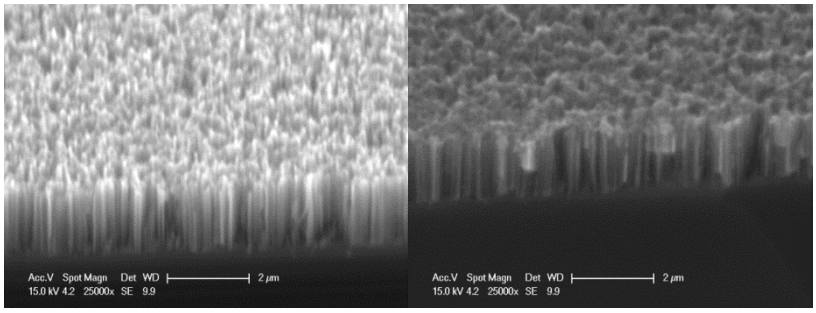
Diffusion effect on PEDOT morphology

In order to investigate the diffusion effect on the morphology of deposited PEDOT onto SiNWs, We change the interspace volume between wires by tuning KOH+IPA tapering duration of 0, 10, 30, and 50 seconds, whose effectiveness can be seen in Figure 3-20 and has been discussed in the previous chapter. All the PEDOT depositions on them are conducted with the same step-wise method under the same condition - see Figure 3-21 where the potential-duration relationships are plotted.

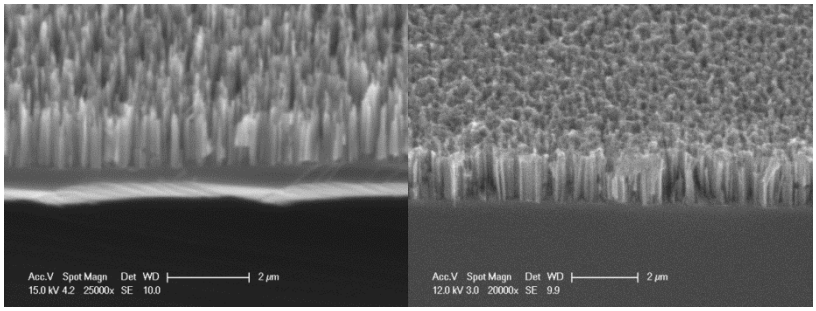
Figure 3-20 gives the comparison of the SiNWs with (on the right) and without PEDOT (on the left, already seen in the previous chapter, added here as reference). The SiNWs are treated without KOH tapering and with 10 seconds, 30 seconds and 50 seconds tapering in (a), (b), (c) and (d), respectively. In Figure 3-20(a) and Figure 3-20 (b), the PEDOT on packed SiNWs is concentrated on the top, while the bottom has less PEDOT. In Figure 3-20(c) and Figure 3-20 (d), the spaced wires are wrapped with PEDOT. SiNWs with 50 seconds tapering treatment are obviously covered by thicker PEDOT than those with 30 seconds. The volume of PEDOT in deep space between wires increases with tapering duration. Since the PEDOT is synthesized under the same condition, and the only difference is the lowered areal density of wires or larger space between wires as seen from the images of without PEDOT in Figure 3-20, we can make the conclusion safely that the enlarged inter-wire space leads to more conformal PEDOT covering layer by permitting monomer diffusion.

Without PEDOT **With PEDOT**

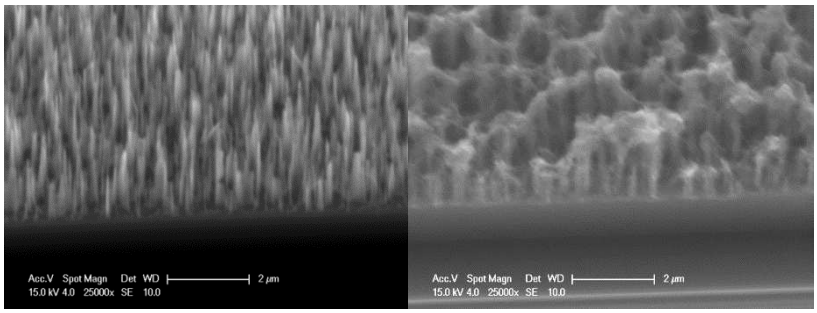
a) without KOH tapering



b) 10 seconds tapering



c) 30 seconds tapering



d) 50 seconds tapering

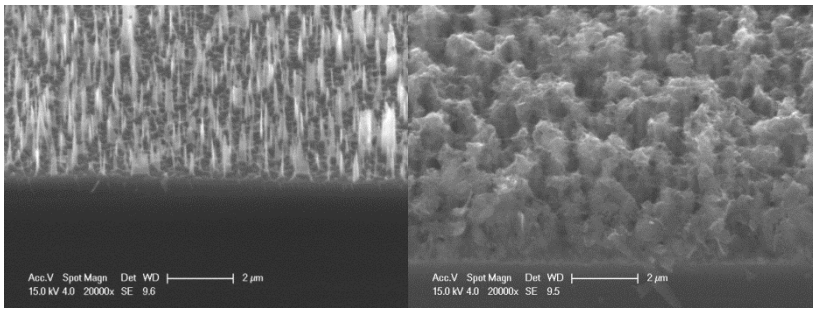


Figure 3-20 SEM observations of cross section of SiNWs samples: without PEDOT on the left and with deposited PEDOT on the right; (a) without KOH treatment, (b) 10s tapering,(c) 30s tapering, and (d) 50s tapering.

OCP changes during step-wise PEDOT deposition

An interesting phenomenon is the OCP changes during the rest time in each unit of deposition, which may be related to wire/PEDOT interface variation. Since OCP is determined by the property of electrode/electrolyte interface[100], its value will be changed as the interface changes. With the process of PEDOT deposition, the interface experiences different stages from the initial SiNW/electrolyte before the start of PEDOT Polymerization, to SiNW&PEDOT/electrolyte as PEDOT partially covers the silicon wire surface, and to the final PEDOT/electrolyte when the entire wire surface is covered by PEDOT. So the OCP must experience the same stages.

Figure 3-21 shows the change in potential during step-wise experiments performed on the different SiNWs treated with KOH process for 0, 10, 30 and 50 seconds, respectively. On the same figure, a PEDOT deposit attempt on the bulk Si (light blue) is also added. For all the SiNWs and BSi substrate, the initial potential is around -0.2V, corresponding then to the potential of Si in this solution. On bulk silicon (see the light blue curve in Figure 3-21.), after the first pulse in potential, the OCP increases to 0.5V. During the following steps, the OCP keeps almost the same value. This suggests that immediately after the first 1 second pulse deposition, the interface of bulk silicon electrode might be entirely covered by the PEDOT, and during the next pulse periods the interface doesn't change any more.

For 50 seconds tapered SiNWs, the electrode has the lowest density of wires, and thus its morphology is close to that of Bulk silicon. The corresponding curve (dark blue curve in Figure 3-21) shows first the OCP rises to 0.45V, a little lower than the OCP of bulk silicon after the first pulse. In the following steps the OCP maintains the stable value as bulk silicon electrode. The PEDOT deposition might cover partially the surface of the substrate after the first pulse, leading to a fractional value of OCP. After two pulses the wires are entirely covered and therefore the subsequent OCPs keep stable.

For SiNWs with 30 seconds tapering (green curve in Figure 3-21), 2 steps are required to get the stable OCP. 10 seconds treatment requires 4 pulses depositing stages to get a stable OCP value (red curve in Figure 3-21), while SiNWs without KOH tapering (black curve in Figure 3-21) need almost 5 steps to reach the ultimate stable OCP. The shorter the KOH tapering is operated, the more the pulses of deposition is needed to reach a stable OCP value.

It is clear that the quantity of steps to stable OCP is dependent on tapering duration. This dependence can be explained as follows:

As we described earlier, the tapering duration determines the wires areal density on substrate, and thus determines the extent of difficulty to which EDOT monomer diffuses into the deep space. If the diffusion is fast in long tapered SiNWs, for example of 50 seconds, the

monomer supply in the deep space is fast to be provided, and therefore more PEDOT can be produced in this region. As a consequence the entire wire surface of 50s tapered SiNWs can be soon covered by PEDOT as the planar BSi. On the contrary, if SiNWs is short tapered, the supply of monomer in deep interspace is difficult. What makes it even more difficult is the PEDOT growth on tips which narrows the pipeline of monomer diffusion. Therefore it takes a longer period, or more pulse stages, to completely cover the full length of wire in the SiNWs with short tapering durations of 10 or 30 seconds. Before the completion is achieved, the partial covering on wire surface may lead the OCP to an intermediate value between the beginning state of Si/solution and the end state of Si/PEDOT.

So the number of steps to a stable OCP reflects the difficulty of monomer diffusion to the interspace between wires that is determined by the tapering duration.

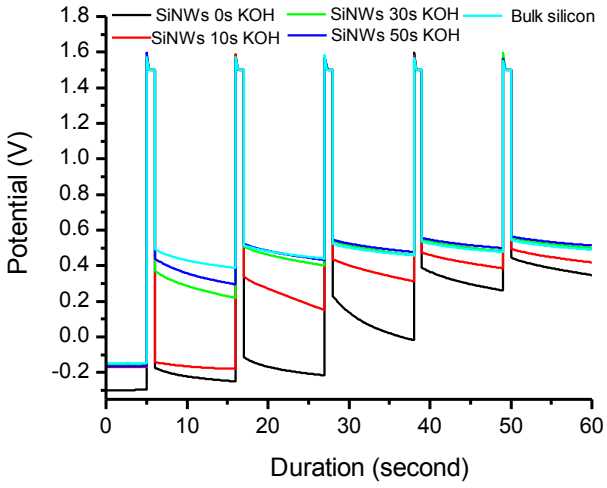


Figure 3-21 Potential-duration relationships in PEDOT step-wise deposition onto SiNWs with various tapering duration: the black curve represents 0 second, red 10 seconds, green 30 seconds, and dark blue 50 seconds, respectively. The light blue curve depicts the deposition with BSi as electrode. The SiNWs are fabricated first by the electroplating process in 4mM $AgNO_3$ 4.8M HF aqueous solution for 1 minute, and then by the etching process in 0.3M H_2O_2 4.8M HF aqueous solution for 2 minutes. All the deposition is conducted under 100% illumination.

OCP relevance to PEDOT covering fraction on wire

In order to verify the speculation that the gradual increase of OCP after steps is caused by the PEDOT partial covering silicon wire surface, another set of experiments are performed with various cycles of PEDOT deposition on SiNWs with 10 seconds tapering. In the step-wise deposition, the unit of one cycle corresponds to a 1s pulse of polarization at 1.5V + 10 seconds rest time.

Figure 3-22 shows the variation of cycles: One cycle in purple, 2 cycles in light blue, 3 cycles in dark blue, 4 cycles in green and 5 cycles in black. Before the first polarization the OCP value corresponding to the SiNWs substrate is around -0.2V. After one cycle the OCP is slightly increased to 0V. After 2 cycles, it reaches a value of 0.2V, and goes on to increase to 0.4V after 3 cycles. The stabilization in potential is reached after 4 cycles. If this speculation is true, the increase of the covered area with the cycles could be put on evidence with SEM observation.

In Figure 3-23 the SEM images of SiNWs with deposited PEDOT corresponding to 1, 2, 3, and 5 cycles are presented. From the top view on the left, the volume of PEDOT on top of SiNWs increases with the cycle's number. Form the tilted view, PEDOT is hard to be distinguished on the cross section with 1 cycle deposition. When the deposition increases to 2 cycles, it becomes easier to see PEDOT in Figure 3-23(b). The deposition of 3 cycles makes thicker PEDOT among wires than that of 2 cycles. However, the difference of PEDOT volume between wires with 5 cycles is hard to say to be pronounced from that of 3 cycles. (The magnification is not high enough). This observation corresponds to the measurement of potential-duration relationship in Figure 3-22. The OCP, determined by the covered fraction of wire surface, increases with deposition cycles from 1 to 3 and ceases to increase after 3 cycles.

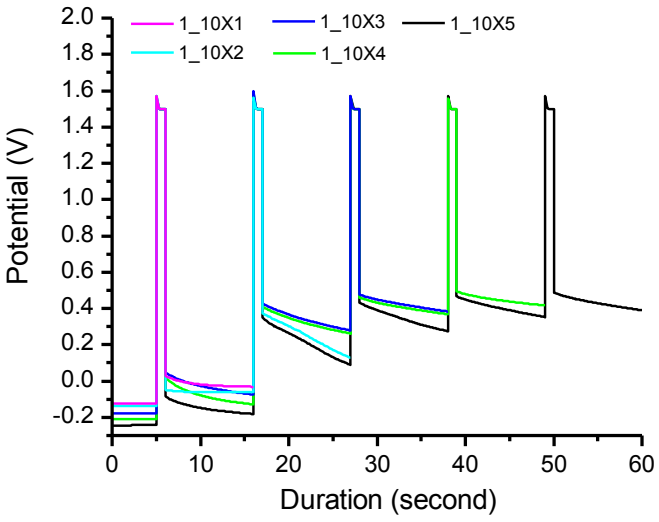


Figure 3-22 Potential-duration relationships in various repetitions of PEDOT step-wise deposition. Each unit of deposition comprises two stages: 1 second pulse and 10 seconds rest time. The curve's color represents the number of unit repetition: purple for 1 cycle, light blue for 2 cycles, dark blue for 3 cycles, green for 4 cycles and black for 5 cycles, respectively. The SiNWs are fabricated first by the electroplating process in 4mM $AgNO_3$ 4.8M HF aqueous solution for 1 minute, and then by the etching process in 0.3M H_2O_2 4.8M HF aqueous solution for 2 minutes. The SiNWs are treated with 10 seconds KOH+IPA tapering. All the deposition is conducted under 100% illumination.

Top view **Tilted view**

a) 1 cycle

b) 2 cycles

c) 3 cycles

d) 5 cycles

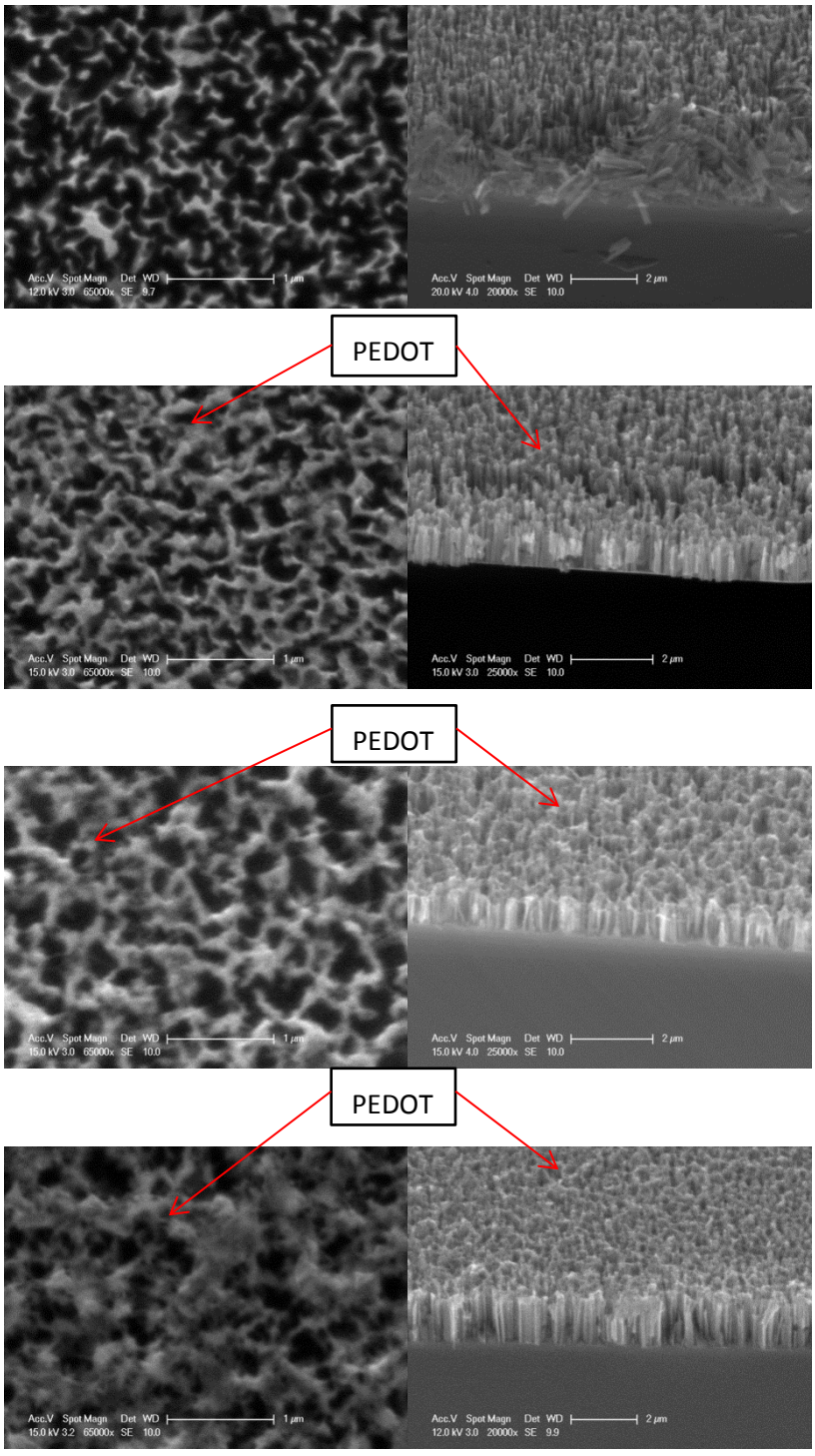


Figure 3-23 SEM images of PEDOT deposited for (a) 1 cycle, (b) 2 cycles, (c) 3 cycles, and (d) 5 cycles on SiNWs. SiNWs are tapered for 10 seconds in KOH+IPA aqueous solution. On the left are the top view images, and on the right are tilted viewed.

3.2.3. PEDOT redox characterization

One of the advantages of PEDOT is that it can be easily doped in EDOT-free solution, and the doping process can be characterized in CV measurement, as presented in the introduction section. In the same way as used to study PEDOT fabrication, we first characterize PEDOT on vitreous carbon, and then we use this result as reference to compare those obtained on SiNWs.

PEDOT characterization on vitreous carbon

PEDOT has been deposited on vitreous carbon with 3 cycles of voltammetry in the potential range of 0-2V at 100mV/s in 10mM EDOT ACN solution containing 0.1M LiClO4. Then the sample (PEDOT on vitreous carbon) is characterized at 20mV/s scanning rate in EDOT-free solution. The low scanning rate allows the different oxidation processes to be distinguished more easily than at 100mV/s that is the usual scan speed.

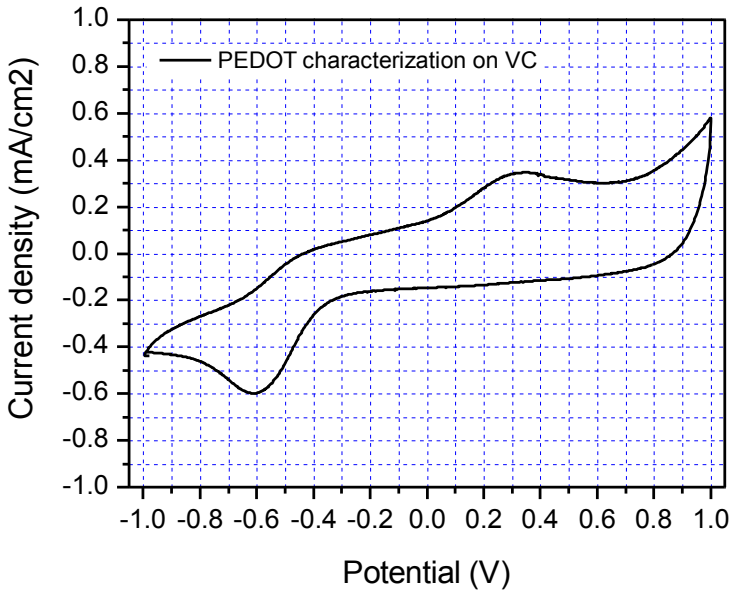


Figure 3-24 Voltammetric characterization of PEDOT deposited on vitreous carbon electrode at 20mV/s scanning rate in EDOT-free 0.1M $LiClO_4$ ACN solution. PEDOT has been deposited with 3 cycles of voltammetry in the potential range of 0-2V at 100mV/s in 10mM EDOT ACN solution containing 0.1M $LiClO_4$.

The voltammogram in Figure 3-24 shows three inflection points in the forward sweep towards positive potential. PEDOT oxidation starts at -0.65V, and reaches the first prepeak at -0.45V. This corresponds to the appearance and accumulation of polaron states in the bandgap of PEDOT. The second oxidation begins at 0.05 with a peak at 0.3V. This oxidation

process is related to the states of bipolaron formed in bandgap. The third oxidation gets started at 0.7V. The process is unknown.

In the reverse sweep to negative potential PEDOT on vitreous carbon shows only one reduction current peak at -0.6V. The two reduction processes of polaron and bipolaron states may merge together and exhibit themselves as one characteristic peak.

PEDOT characterization on SiNWs

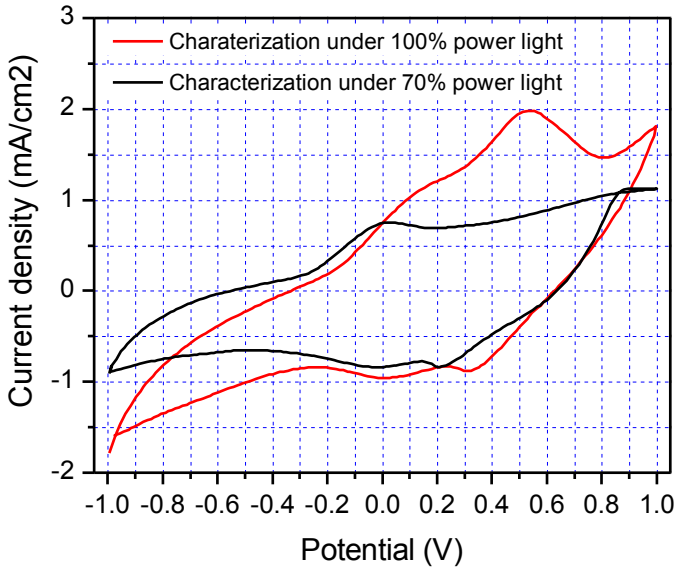


Figure 3-25 Voltammetric characterization of PEDOT deposited on SiNWs electrode at 100mV/s scanning rate in EDOT-free 0.1M $LiClO_4$ ACN solution. Red curve represents voltammetric characterization conducted under 100% working light power, the black one is under 70% light power. The SiNWs are fabricated first by the electroplating process in 4mM $AgNO_3$ 4.8M HF aqueous solution for 1 minute, and then by the etching process in 0.3M H_2O_2 4.8M HF aqueous solution for 2 minutes. The SiNWs are not treated with KOH tapering. PEDOT has been deposited with the same method for the two measurements: 3 cycles of voltammetry in the potential range of 0-2V at 100mV/s in 10mM EDOT ACN solution containing 0.1M LiClO4 under 70% illumination.

The SiNWs show similarity as vitreous carbon in PEDOT characterization. The PEDOT is first deposited on the SiNWs with 3 cycles of voltammetry in the potential range of 0-2V at 100mV/s in 10mM EDOT ACN solution containing 0.1M $LiClO_4$ under 70% illumination. Then the PEDOT on SiNWs is characterized in EDOT-free 0.1M $LiClO_4$ solution under different light power, as seen in Figure 3-25 where the red curve corresponds to 100% power while the black to 70% power. In Figure 3-25 three processes of oxidation are also shown at 100% power (red curves in Figure 3-25), similar to the process obtained on vitreous carbon related to formation of polaron and bipolaron. In the forward scan to positive potential, the first

oxidation starts up from -0.2V with a prepeak at 0.1V. The second oxidation initiates at 0.3V and gives a peak at 0.52V. The third oxidation begins at 0.8V.

Different from the curve on vitreous carbon, the PEDOT on SiNWs shows two characteristic peaks in the cathodic reverse sweep, which corresponds to the reduction of polaron and bipolaron states respectively.

The illumination at 70% power, compared to 100% illuminating power, results in lower current density both in forward and backward sweeps, suggesting that PEDOT is easier to be oxidized under higher intensity of illumination. This again emphasizes significance of illumination in PEDOT doping.

Conclusions

PEDOT layer can be successfully polymerized and deposited on SiNWs array as electrode with the electrochemical method.

The CV measurements in PEDOT deposition show that SiNWs and BSi as electrodes are different from conductive electrode of vitreous carbon. Illumination is the key to understand the difference. Illumination is not only necessary for PEDOT polymerization and also affects the doping level of PEDOT. Illumination provides photogenerated holes that make SiNWs more conductive for oxidation in PEDOT polymerization and in PEDOT doping.

By using the step-wise deposition, a conformal PEDOT layer can be obtained to wrap each single silicon wire. Competition between PEDOT polymerization on wire tips and EDOT monomer diffusion is the mechanism that determines the morphology of PEDOT on SiNWs. The diffusion effect on the morphology of PEDOT is identified by tuning the interspace between wires. The OCP during PEDOT step-wise deposition can be an indicator to know PEDOT covering percentage of single silicon wire surface.

The silica layer appearing during PEDOT fabrication on SiNWs surface should be avoided or reduced by removing water in ACN solution. Bis-EDOT might be an alternative for EDOT to fabricate PEDOT since it has relatively low oxidation potential[101].

PEDOT doping level is a key parameter that determines PEDOT/SiNWs cell performance. It could be improved further by using more powerful illuminating laser.

Chapter 4. Characterization of SiNW/PEDOT solar cell

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Glossary

AAO	Anodic Aluminum Oxide
ACN	Acetonitrile
Ag	Silver
AgNO3	Silver Nitrite
ALD	Atomic Layer Deposition
BSi	Bulk Silicon
CV	Cyclic Voltammetry
CVD	Chemical Vapor Deposition
EDOT	3,4-ethylenedioxythiophene
EDX	Energy-Dispersive X-ray
EMACE	Electroless Metal-Assisted Chemical Etching
HF	Hydrogen Fluoride
H_2O_2	Hydrogen Peroxide
H_2SO_4	Sulfuric Acid
GaAs	Gallium Arsenide
GaIn	Gallium–Indium eutectic
J-V	Current density - Voltage
M-S	Mott-Schottky
MIS	Metal Insulator Semiconductor
PEDOT	Poly(3,4-ethylenedioxythiophene)
PF^{6-}	Hexafluorophosphate
PS	Potentiostatic
Ref	Reference
SEM	Scanning Electron Microscope
SHE	Standard Hydrogen Electrode
Si	Silicon
SiNWs	Silicon Nanowires
ZnO	Zinc Oxide

List of symbols

Symbol	Description	Unit
A^{**}	Richardson's constant	$A/cm^2\text{-}K^2$
A_{eff}	Effective area	cm^2
E_c	Conduction band	eV
E_{fm}	Fermi level of metal	eV
E_{fs}	Fermi level of semiconductor;	eV
E_g	Band gap of semiconductor	eV
E_s	Interface state position in Si bandgap	eV
E_v	Valence band	eV
FF	Fill factor	-
J	Current density	mA/cm^2
J_{lk}	Leakage current density	$\mu A/cm^2$
J_p	Photocurrent density	mA/cm^2
J_s	Saturation current density	mA/cm^2
J_{sc}	Short circuit current density	mA/cm^2
k_B	Boltzmann's constant	J/K
n	Ideality factor	-
N_s	Interface state density	$eV^{-1}\ m^{-2}$
q	Electronic charge	C
Q_{in}	Charge quantities in insulator	C/cm^2
Q_{sc}	Charge quantities in depletion layer	C/cm^2
Q_s	Charge quantities in interface states	C/cm^2
R_{lk}	Leakage resistance	$k\Omega\ cm^2$
R_s	Series resistance	$\Omega\ cm^2$
T	Absolute temperature	K
V	Applied voltage on solar cell	V
V_D	Applied voltage across the diode	V
V_i	Voltage drop across the interfacial insulator	V
V_{oc}	Open circuit Voltage	V
η	Energy conversion efficiency	-
δ	Insulator thickness	nm
φ_s	Potential difference between semiconductor surface and body	V
Φ_B	Schottky barrier height	V
Φ_m	Work function of metal	V
Φ_0	Neutral level of the interface states	V
χ	Electron affinity of the semiconductor	V

4.1. Fabrication

The scheme in Figure 4-1 presents the normal procedure to make SiNWs/PEDOT hybrid solar cell, including the first process of metal-assisted electroless chemical etching, then the process of PEDOT deposition using either a step-wise way or a continuous way, and the following back contact and the last process of silver grids evaporation. The processes of chemical etching and PEDOT deposition have been described in their previous corresponding sections. Here all the SiNWs are fabricated with EMACE method: first electroplated in 4mM $AgNO_3$ for 1 minute, and then etched in 0.3M H_2O_2 for 2 minutes. All PEDOT in this chapter is electrodeposited in 10mM EDOT 0.1M $LiClO_4$ ACN solution. The photograph of a complete solar cell is shown as Figure 4-2.

The backside of SiNWs is spotted with GaIn and placed on a copper substrate to form the back contact. Because of its liquid property, it is easy to spread GaIn over the silicon substrate and therefore accelerate the cell's fabrication. But from the band diagram in Figure 4-3 the work function of GaIn is a little higher than E_c of silicon. In order to improve the cell's performance, it is better to make Al back contact in the further study.

PEDOT work function or Fermi level in our cell had not been determined due to lack of electrochemistry knowledge of SiNWs as electrode. The work function of PEDOT is from the literature[51].

The front contact on the side of PEDOT is silver grids that are evaporated with electron beam evaporation. From the band diagram in Figure 4-3 silver is selected because its work function is higher than that of PEDOT, allowing charge holes to be collected.

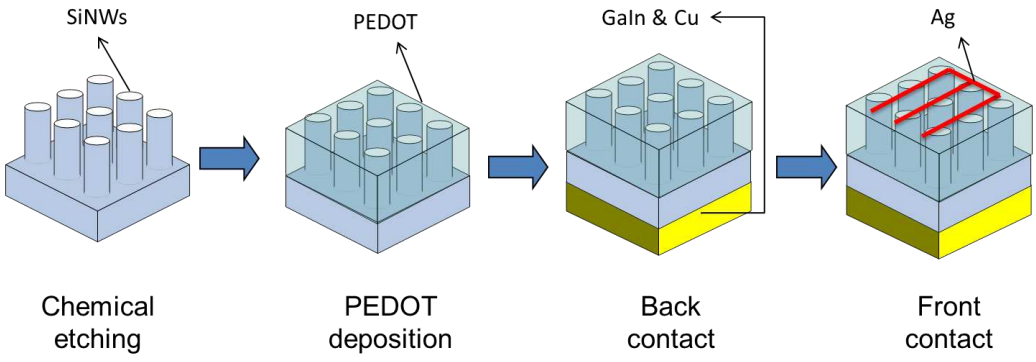

Figure 4-1 Schematic illustration of the processes towards PEDOT/SiNWs hybrid structure

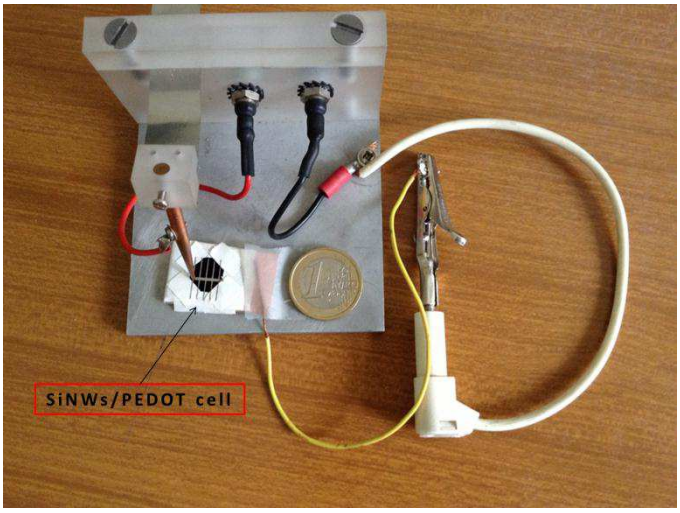

Figure 4-2 Photograph of the hybrid cell on the working station in comparison with 1-Euro coin

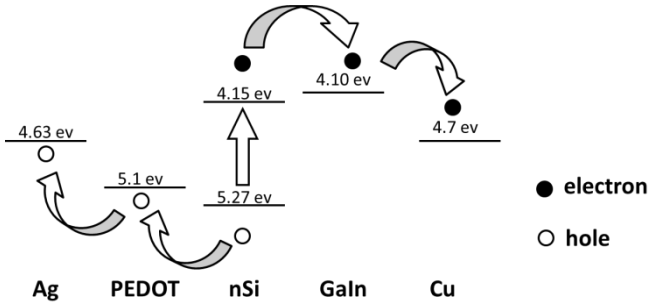

Figure 4-3 Band diagram of PEDOT/n-SiNWs hybrid cell with Ag as front contact and with GaIn&Cu as back contact. PEDOT work function is from the literature[51]

4.2. Analysis on *J-V* curves

4.1.1. *J-V* characteristic parameters

SiNWs/PEDOT structure can be viewed as a Schottky diode[60,102–104], and PEDOT can be simplified as a conducting material like metal with Fermi level in equilibrium with n type silicon. We have measured the Current-Voltage IV characteristics of SiNWs/PEDOT Schottky diode both in dark and under illumination. The current density is obtained by dividing the measured current by the projected area of the cell. For instance the cell in Figure 4-2 its projected area is about 0.5 cm^2. PEDOT are electrodeposited onto the SiNWs for 3 voltammetry cycles from -1V to 2V. The dark *J-V* curve shown in Figure 4-4 in semi-logarithmic plot presents an obvious rectifying behavior. So we try to first interpret the SiNWs/PEDOT diode based on the classic thermionic emission theory.

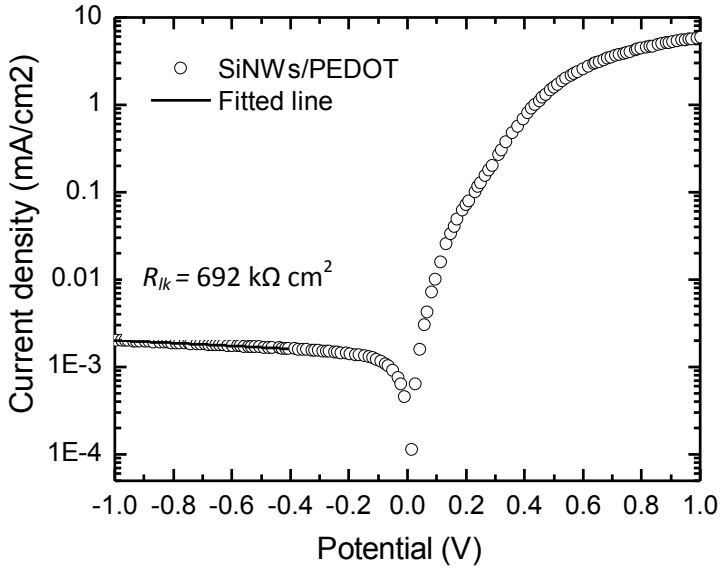

Figure 4-4 Dark current–voltage semi-logarithmic plot of SiNWs/PEDOT hybrid cell. The fitting line denotes the leakage resistance R_{lk}= 692 kΩ cm². The SiNWs are fabricated first by the electroplating process in 4mM $AgNO_3$ 4.8M HF aqueous solution for 1 minute, and then by the etching process in 0.3M H_2O_2 4.8M HF aqueous solution for 2 minutes. The SiNWs are not treated with KOH tapering. PEDOT are electrodeposited onto the SiNWs for 3 voltammetry cycles from -1V to 2V in 10mM EDOT 0.1M $LiClO_4$ ACN under 100% illumination.

According to the thermionic emission model for a Schottky diode, the current density *J* flows through the diode is given by

$$J = J_s \, exp\left(\frac{-qV_D}{nk_BT}\right) \qquad 4\text{-}1$$

Where q is the electronic charge, k_B is the Boltzmann's constant, T is the absolute temperature, and V_D is the applied potential across the diode. n is the ideality factor, a dimensionless parameter involved in the *J-V* characteristics to take into account the non-ideal behavior.[27] The J_s is saturation current density and can be expressed by[105]

$$J_s = A^{**}T^2\, exp(\frac{-q\Phi_B}{k_B T}) \qquad 4\text{-}2$$

Where Φ_B is the Schottky barrier height which can be seen in Figure 4-5, where E_c, E_v, E_g are the conduction band, the valence band, and the band gap of semiconductor, respectively. E_{fm} E_{fs} are the Fermi levels of metal and semiconductor. A^{**} is the Richardson's constant 112 A/cm^{2}K^2 for n type silicon[105].

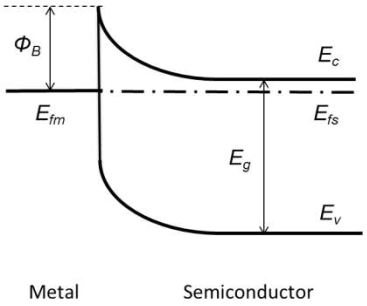

Figure 4-5 Band diagram of metal-semiconductor contacts [27].

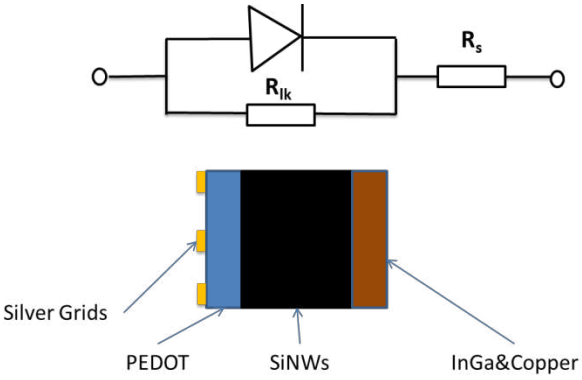

Figure 4-6 Schematic of simplified equivalent circuit and device configuration for electronic characterization

The equivalent circuit of SiNWs/PEDOT hybrid cell is presented in Figure 4-6 which includes the leakage resistance R_{lk} and the series resistance R_s. The leakage resistance R_{lk} represents alternative paths for charge bypassing the Si/PEDOT heterojunction region that might be caused by the direct touching between front grids and back contact. These alternative paths for charge transport may also be composed of chains of defects in the hybrid junction[106]. The R_s may be the sum of the resistances of silicon, PEDOT, wire, front grids, back contact and especially caused by the oxidative interface layer between silicon and PEDOT.

Taking into account leakage resistance R_{lk} and series resistance R_s, the *J-V* characteristic Equation 4-1 can be rewritten by

$$J = J_s\left\{exp\left[\frac{q(V - JR_s)}{nk_BT}\right] - 1\right\} - \frac{V - JR_s}{R_{lk}} \qquad 4\text{-}3$$

where *V* is the applied potential on the entire device. The term *V* - JR_s replaces V_D in Equation 4-3 because of the potential-partition effect of series resistor.

We use Cheung-Cheung's method[107] to extract series resistance R_s and ideality factor *n* from the dark *J-V* curves measured on our hybrid cells. For our cell the series resistance R_s is so large that its extraction is usually very hard directly from the semilog plot of dark *J-V* curve. Cheung-Cheung's method is selected because of its accuracy[108], and its derivation can be seen in Appendix A.

For example, the series resistance R_s and ideality factor *n* are extracted from the fitted regime of *J-V* curve from 0.37V to 0.57V in Figure 4-7. Higher bias regime gives rise to inaccuracy in ideality factor calculation. The series resistance is R_s = 41.6 Ω cm^2 which is highly suspected as a result of interfacial oxidative layer.

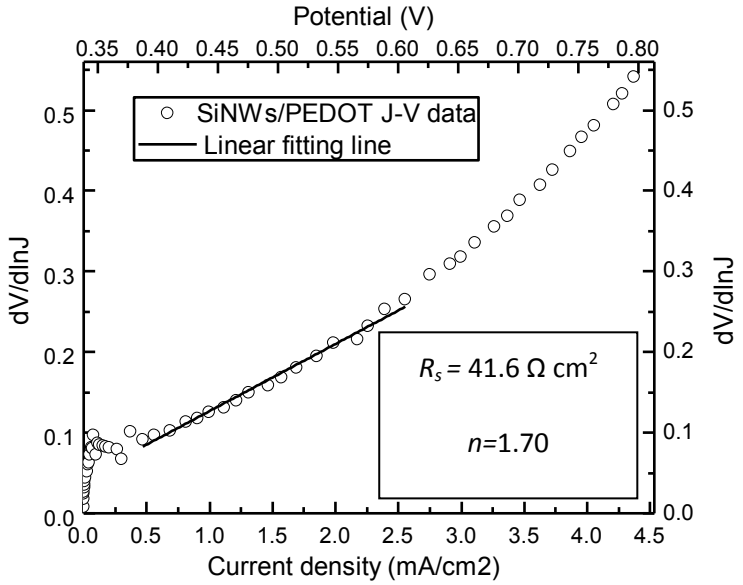

Figure 4-7 dV/dln$J$ vs current plot. The fitting line gives the value of R_s = 41.6 Ω cm^2 from slope and ideality factor n = 1.70 from y axis intercept. The data comes from *J-V* curve in Figure 4-4.

The leakage resistance R_{lk} can be directly calculated from the slope of the *J-V* curve in the reversion bias region[108]. See Figure 4-4, the calculated region is selected from -0.4V to -1V, the fitting line coincides quite well with the raw data curve.

Usually shunt resistance of a solar cell is calculated from its light *J-V* curve. But in our case, the leakage resistance is measured from dark *J-V* curve in the reverse bias range from -1 to -0.4V. Compared with shunt resistance, the leakage resistance is directly related to the interface defects condition that is of a great interest for us. So we choose leakage resistance R_{lk} rather than shunt resistance to characterize our cell.

The leakage current density J_{lk} is picked at reverse bias of -1V for all the dark *J-V* curves. The same reason for its selection as leakage resistance is that it reflects the alternative current, associated with interface traps between PEDOT and silicon. The saturation current density is extracted from the forward *J-V* curve, while leakage current density is viewed from the reverse dark *J-V* curve. Although in the diode equation as in Equation 4-3, the two terms, the saturation current density and the leakage current density, should be the same at a large reverse bias; they are usually different for a real Schottky diode. In fact, the saturation current density reflects the barrier height of a Schottky diode, as seen in Equation 4-2, while the leakage current represents a resistance parallel connected with a diode which is a transport pathway composed by surface states[106]. When the parallel leakage resistance is rather small, the two terms can be deviated from each other largely. As far as the characterization for passivation effect is concerned, the leakage current or leakage resistance would be more appropriate than saturation current.

The photocurrent density J_p is measured at reverse bias -1V from the light *J-V* curves. Because of the large series resistance in our cell, the short current density J_{sc} alone may not present light absorption in our cell. Fortunately the photocurrent density J_p gives an alternatively way to help illustrating on how absorption is affected by PEDOT deposition.

Next we will show how the fabrication parameters influencing the hybrid diode performance, such as illumination, potential, and duration in the continuous deposition.

4.1.2. Illumination during PEDOT fabrication

As we discussed previously about the importance of illumination in PEDOT fabrication and doping, here we continue to analyze the influence of illumination during PEDOT fabrication on PEDOT/SiNWs hybrid cell performance.

In Figure 4-8 PEDOT for the measured *J-V* curves is fabricated with potentiostatic electrodeposition at 1.5V for 10 seconds under illumination of 70% and 100% lamp power outputs. In Figure 4-8(a) the plot of current density vs. duration shows little difference between the curves of two intensities at 100% and at 70% output. So we would say that the volume of PEDOT deposited on SiNWs is almost the same.

The 100% power output in Figure 4-8(b) makes the cell more like an ideal diode with higher forward current density and lower reverse current density than 70% power output does. Indeed, from Table 4-1 where we summarize the characteristic parameters for the two cells, the ideality factor n = 1.55 for 70% output made cell is larger than that for 100% output made cell n = 1.49. In addition the cell made at 100% output almost shows its advantages over that made at 70% in almost all of the diode parameters except V_{oc}, including series resistance, leakage current, leakage resistance, short circuit current density, and so on. Besides, the cell with PEDOT at 70% power output shows "S"-shaped illuminating *J-V* curve the dashed line in Figure 4-8(c), that is, the current density is deviating from ideal rectification shape at forward potential larger than 0.1V, which could be attributed to charge accumulation in the heterojunction[109],[110]. After a photon has been absorbed by hybrid cell, a pair of electron and hole is produced and separated by build-in field when they diffuse into the heterojunction. Then the charge electron goes to the cathode via n type silicon body, while the charge hole travels through PEDOT to be collected by anode. Due to the lower conductivity of PEDOT compared with n silicon, the holes are not effectively collected by the contact and get accumulated in PEDOT. This charge accumulation causes high recombination at forward bias which leads to a decrease in current density. The "S" shaped *J-V* curve suggests the low PEDOT conductance. Or more precisely, it suggests the mismatch between Si and PEDOT in conductance[109],[110].

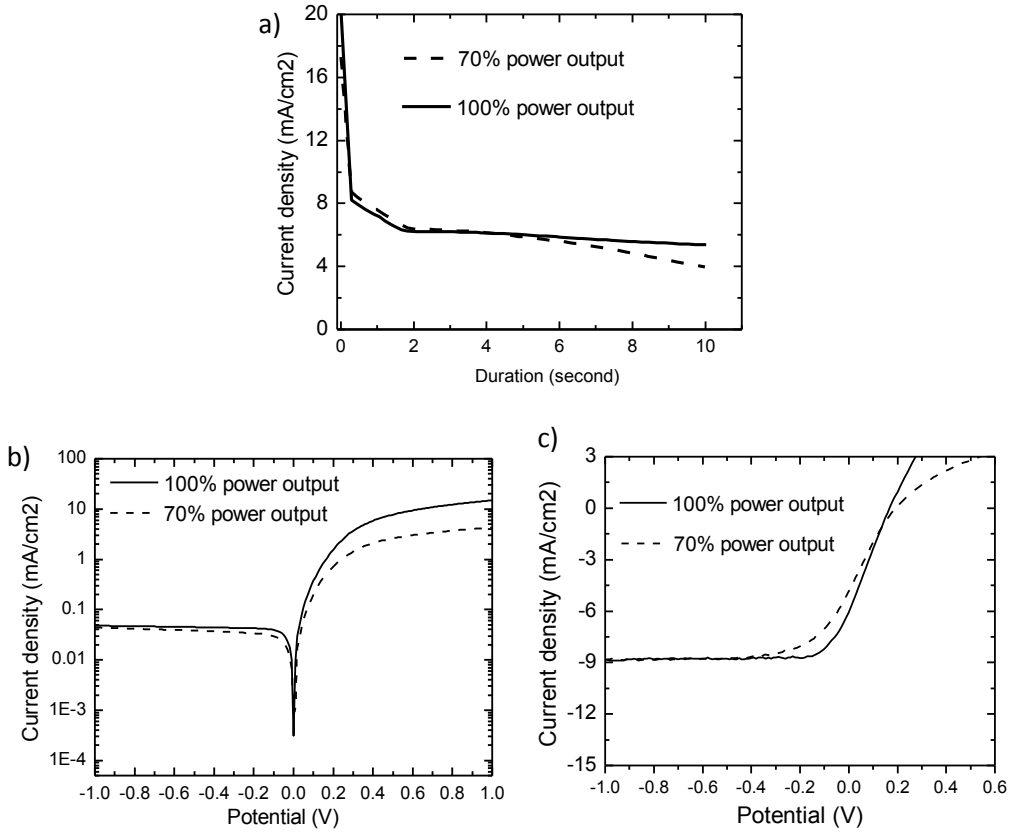

Figure 4-8 Comparison of PEDOT continuously deposited under illumination at 100% and at 70% output: (a) Current density-potential curves of PEDOT PS deposited at 100% (solid line) and 70% (dashed line) output; (b) dark J-V curves with PEDOT fabricated at 100% (solid line) and 70% (dashed line) output; (c) illumination J-V curves with PEDOT at 100% (dashed line) and 70% (dashed line) output. The SiNWs are fabricated first by the electroplating process in 4mM $AgNO_3$ 4.8M HF aqueous solution for 1 minute, and then by the etching process in 0.3M H_2O_2 4.8M HF aqueous solution for 2 minutes. The SiNWs are not treated with KOH tapering.

Table 4-1 Performance of the cells with PEDOT made under illumination at 100% and 70% output

Parameters		R_s	R_{lk}	n	J_{lk}	V_{oc}	J_{sc}	η	J_p
unit		Ω cm^2	kΩ cm^2	-	μA/cm^2	V	mA/cm^2	-	mA/cm^2
Output	70%	100	44	1.55	43.88	0.20	4.9	0.21%	8.83
	100%	39	81	1.49	47.93	0.17	6.1	0.25%	8.84

Since the volumes of PEDOT at the two lamp power are comparable as can be seen in Figure 4-8 (a), we may rule out the thickness influence on the cell's performance. The difference in

the two cells' performance may be originated from the conductivity of PEDOT layer. Let's look back at Figure 3-25, the PEDOT under 100% illuminating intensity presents higher anodic current than that under 70% power, which means more dopants of anion (ClO_4^-) are involved in the polymer PEDOT[88], and therefore higher conductivity can be achieved at higher illumination intensity.

We may speculate that the influence of illumination on *J-V* performance might be resulted from the conductivity of PEDOT that is related to light intensity. But how light intensity affects PEDOT conductivity is still unknown.

4.1.3. Duration of PEDOT deposition

We also estimate the effect of depositing duration on the hybrid cell from *J-V* measurement. Figure 4-9 (a) presents the curves of current density VS duration of each PEDOT polymerized at 1.5V under illumination of 70% power output for 5 seconds, 10 seconds, and 30 seconds. The curves almost overlap each other, suggesting good reproducibility of the deposition process. Obviously in Figure 4-9(c) the J_{sc} increases as the deposition duration decreases, it is also the same for the photocurrent density J_p in Table 4-2. The reason might be light-prevention effect due to PEDOT thickness. PEDOT layer thickness is proportional to the fabrication duration. As PEDOT layer gets thicker with fabrication duration, more photons are prevented from reaching the silicon part. So the short current density J_{sc} and the photocurrent density J_p decrease. The same light prevention effect can also be seen in PEDOT fabrication process, like in Figure 3-14 (b), where the new born PEDOT layer causes reduction in the number of photons access to the interface, leading to the decreasing current density after each scanning cycle.

Although the light *J-V* curve in Figure 4-9(c) shows that the photocurrent density J_p of the hybrid cell measured at -1V could be as high as 13 mA/cm^2 in the case of 5 seconds PEDOT, the short circuit current density J_{sc} actually loses its value to 7.32 mA/cm^2 at bias = 0V. The cause might be the large resistance in series connection with the hybrid diode. The calculation with Software Matlab® in Figure 4-10 tells how the light *J-V* is dependent on series resistance. When series resistance R_s is lower than 10 Ω cm^2, it has weak effect on J_{sc} which equals the photocurrent density J_p of 30mA/cm^2, but when R_s is higher than 50 Ω cm^2, the J_{sc} loses its value from 30mA/cm^2 as J_p and decreases with series resistance.

So where does the series resistance come from? One possibility is SiNWs surface oxidation by oxygen and water dissolved in the ACN solution during PEDOT synthesis process. By comparison of the series resistances listed in Table 4-2, it is clear that the series resistance R_s increases with duration. Thus one can suspect that longer time of exposure to oxygen and water in ACN leads to thicker silica layer and therefore higher series resistance, since the

silica layer that covers the interface between silicon and PEDOT works as a barrier against transport of photo-generated carriers across the junction.

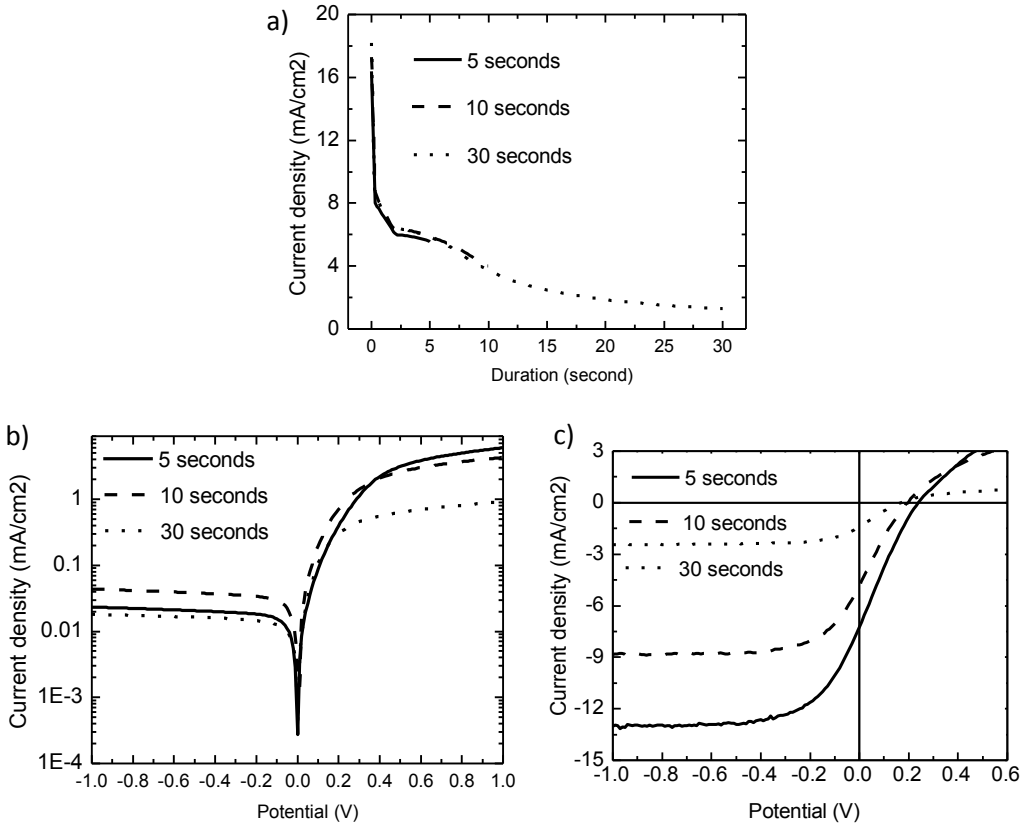

Figure 4-9 Comparison of characterization of PEDOT deposited for various durations: (a) Current density VS potential curves of PEDOT PS deposited for 30 seconds (dotted), 10 seconds (dashed), 5 seconds (solid), respectively. (b) Dark and (c) illuminating J-V curves of SiNWs hybrid solar cells with PEDOT corresponding to (a). The SiNWs are fabricated first by the electroplating process in 4mM $AgNO_3$ 4.8M HF aqueous solution for 1 minute, and then by the etching process in 0.3M H_2O_2 4.8M HF aqueous solution for 2 minutes. The SiNWs are not treated with KOH tapering. PEDOT are electrodeposited onto the SiNWs in 10mM EDOT 0.1M $LiClO_4$ ACN under 100% illumination.

Another evidence, which supports the origin of series resistance is the silicon oxidation during PEDOT deposition, can be found from the CV measurements of PEDOT fabrication in Figure 3-14(c), where the CV curve on SiNWs has a huge current density before EDOT starts to be oxidized and polymerized to PEDOT. This current density might be corresponding to silicon oxidation (The reason has been given in Chapter 3). Because silicon oxidation operates at a much lower potential 0V than EDOT polymerization initial potential at 1.3V, the oxidation of silicon is much easier in thermodynamics than PEDOT synthesis. Even though there are only a few traces of water and oxygen in anhydrous solution, silica layer still forms on the silicon surface in the competition with EDOT oxidation. So in order to

reduce silica layer thickness, one way is to reduce further the water concentration in ACN. Perhaps there's another way to help EDOT win the competition by reducing the initial oxidation potential of EDOT.

But how does the depositing potential influence on the hybrid cell's performance? That will be the content in the next section.

Table 4-2 Performance of the cells with PS depositing durations of 5, 10, and 30s

Parameters		R_s	R_{lk}	n	J_{lk}	V_{oc}	J_{sc}	η	J_p
unit		Ω cm^2	kΩ cm^2	-	μA/cm^2	V	mA/cm^2	-	mA/cm^2
Duration (s)	5	50	89	2.43	23.34	0.24	7.32	0.38%	13.02
	10	100	44	1.55	43.88	0.20	4.90	0.21%	8.83
	30	381	145	0.81	18.09	0.17	1.44	0.05%	2.44

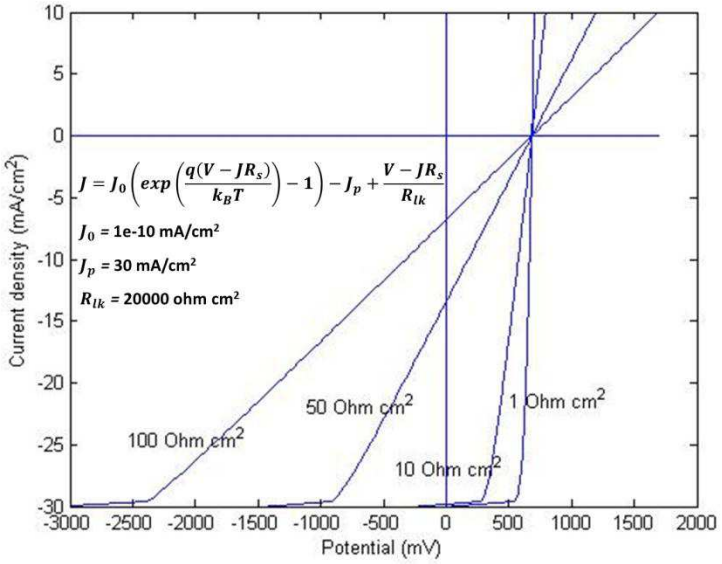

Figure 4-10 Calculated illuminating *J-V* curves with various series resistances: 100 Ω cm², 50 Ω cm², 10 Ω cm² and 1 Ω cm². The function of current density with potential is detailed on the graph, including the parameters' value used in this function: reverse saturation current density J_0, photo-generated current density J_p, and leakage resistance R_{lk}.

4.1.4. Potential during PEDOT fabrication

The potential used for PEDOT polymerization also plays a role on hybrid cell *J-V* characteristic. In Figure 4-11 (a) (b) two cells of PEDOT are fabricated at 1.25V and 1.5V for 10 seconds under 70% power output. Figure 4-11(a) shows that similar current density

curves for two potentials, suggesting that PEDOT thickness difference is not a key factor influencing the *J-V* characteristic. However, the *J-V* curves of the two cells in Figure 4-11(b) show a huge difference. The sample of PEDOT made at 1.5V has obviously better J_{sc} than that at 1.25V. It is the same for the two samples with PEDOT fabricated for 5 seconds in Figure 4-11(c) and (d).

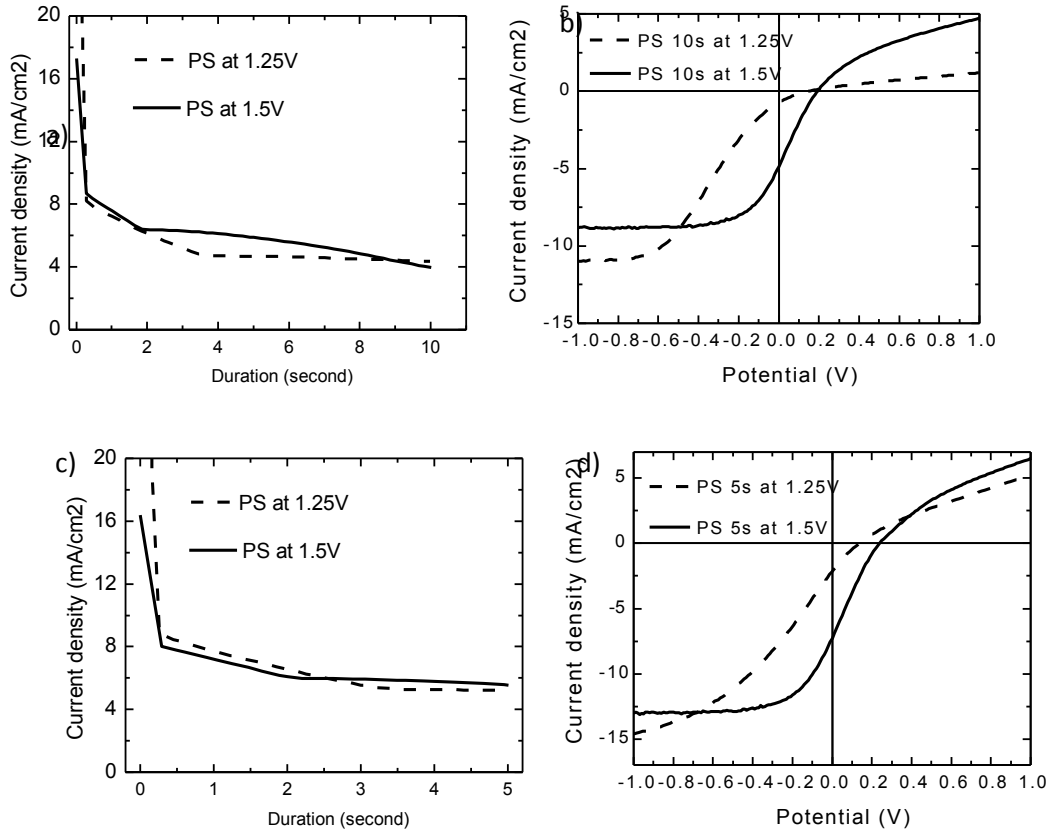

Figure 4-11 Comparison of cells with PEDOT fabricated at 1.25V (dashed line) and 1.5V (solid line) under 70% lamp power output: (a) Current density-potential plots of 10 seconds PS deposition at 1.25V (dashed line) and at 1.5V (solid line); (b) J-V characteristic curves of cells with PEDOT corresponding to (a); (c) Current density-potential relationships of 5 seconds PS deposition at 1.25V (dashed line) and at 1.5V (solid line); (d) J-V characteristics of the cells with PEDOT corresponding to (c). The SiNWs are fabricated first by the electroplating process in 4mM $AgNO_3$ 4.8M HF aqueous solution for 1 minute, and then by the etching process in 0.3M H_2O_2 4.8M HF aqueous solution for 2 minutes. The SiNWs are not treated with KOH tapering.

The J_{sc} difference may be contributed to series resistance. Comparing the series resistance R_s in Table 4-3 extracted from dark *J-V* curves corresponding to the samples in Figure 4-11, the R_s = 100 Ω cm^2 at 1.5V is much lower than R_s = 648 Ω cm^2 at 1.25V. Let us review Figure 3-17. The cyclic voltammetry curve of 70% power shows that PEDOT polymerization just begins at 1.2V (the inflection potential is at 1.2V). The reaction rate at 1.25V for PEDOT deposition is

consequently much slower than the rate at 1.5V. As we described in the last subsection, EDOT oxidation is in fact competing with silicon oxidation during the polymerization. Because of the lower oxidation rate at 1.25V, for the same deposition duration more silicon is oxidized in the case of polymerization at 1.25V than at 1.5V. As a consequence a thicker silica layer is formed at 1.25V, which leads to a higher series resistance on the interface.

Above is the *J-V* analysis for continuously deposited PEDOT/SiNWs cell, and next we will discuss the cells made with step-wise deposited PEDOT.

Table 4-3 Performance of the cells with 10s PS deposited PEDOT at 1.5V and at 1.25V

Parameters		R_s	R_{lk}	n	J_{lk}	V_{oc}	J_{sc}	η	J_p
unit		Ω cm^2	kΩ cm^2	-	μA/cm^2	V	mA/cm^2	-	mA/cm^2
$P_{deposition}$ (V)	1.5	100	44	1.55	43.88	0.20	4.90	0.21%	8.83
	1.25	648	32	0.22	103.21	0.15	0.73	0.02%	10.99

4.1.5. Step-wise deposited PEDOT

The most remarkable feature of our PEDOT/SiNWs hybrid cell is the ultralow leakage current density and the ultrahigh leakage resistance.

All of the leakage resistances of our cells, see Table 4-4, are on the scale of kΩ cm^2. The diode made on BSi has a leakage resistance close to 10 MΩ cm^2. The resistance parallel to diode is very large, suggesting a good passivation effect to remove interfacial states which constitute the pathway across the interface in the junction[106],[111].

In the work of Samgmoo Jeong et al[58], PEDOT is spin coated on a silicon nanocones array to form a hybrid cell. Although the cell has the efficiency as high as 12%, the leakage current at -0.4V is a little larger than 0.1mA/cm^2. One can speculate that the J_{lk} would be even higher at -1V, because of the linear dependence of J_{lk} on reverse bias.

On the contrary, our cell either made with continuously or step-wise deposition has much lower leakage current density. As seen in Table 4-4, the leakage current densities J_{lk} measured at -1V from dark IV curve are on the scale of μA/cm^2, and the cell made in step-wise manner has a leakage current J_{lk} = 3.76 μA/cm^2, at least 30 times lower than that of the cell made with spin-coating method in literature[58].

The leakage current density is directly related to the charge trapping states on the interface. For example, in the Tian et al work[112], when the intrinsic silicon layer is added between p type core and n type shell of silicon, the leakage current density is greatly reduced. The reduction in leakage current density is contributed from the elimination of interface states

between core and shell. Baek et al[113] uses ALD technique to passivate SiNWs, and the leakage current density after ALD passivation is reduced to a few μA, comparable to our leakage current density with step-wise deposition. They also believe that the passivation due to ALD is the cause for low leakage current density.

As we have mentioned in the introduction chapter, the surface dangling bond can be passivated by carbon. It is probable that the passivation effect takes place when PEDOT deposition is conducted on SiNWs surface. As can be seen in Table 4-4, the cells made in the step-wise way has lower leakage current density than those made in the continuously way. For example, the J_{lk} of the cell with 5s continuously deposition is 23.34 μA/cm^2, while the 1_10X5 cell has only 3.76 μA/cm^2. As presented in the previous chapter, the continuous deposition leads to partially covering on the upper portion of SiNW (see Figure 3-18), while step wise method can get a conformal layer wrapping the entire lateral wall (see Figure 3-19). This covering difference gives rise to a passivation difference. The better passivated cell made in the step-wise deposition has a relatively low leakage current density.

In addition, the 1_10X5 fabrication has longer breaking time of 10s between pulses than 1_2X5 cell with breaking time of 2s. The longer breaking time allows more EDOT to penetrate into the deep inter-space between wires, and therefore a better covering and passivating layer can be formed. As a consequence, the 1_10X5 cell has the leakage current density 3.76 μA/cm^2 lower than the 1_2X5 cell of J_{lk} 8.44 μA/cm^2.

Besides, the bulk silicon has less surface states than SiNWs, and thus the leakage current density of BSi hybrid cell is much lower than that of SiNWs -see Table 4-4. For BSi cell with 5s deposition the leakage current density is 1.81 μA/cm^2, less than half the leakage current density 3.76 μA/cm^2 of the 1_10X5 cell. This also supports the speculation that surface states are the cause for leakage current density. The deposition of relatively long time 10s increases leakage resistance by about 8 times compared with 5s deposition from 1195 to 9102 kΩ cm^2. This could be explained with the passivation effect: long time deposition leads to more complete passivation.

The passivation effect can also be used to interpret the high leakage current density which occurs on the spin-coated PEDOT/SiNWs cell. Even if a conformal layer could be formed on the surface, the spin-coated PEDOT may not be so adherent to silicon surface. On the contrary, the PEDOT synthesis would preferentially take place and be deposited at those sites where surface defects are located, because these locations usually have higher energy which facilitates nucleation of PEDOT by lowering energy barrier. That's why the electrodeposited PEDOT has the ability to passivate defects on SiNW surface.

Table 4-4 Summary of performance parameters of the hybrid solar cells

	SiNWs (continuously)			SiNWs (step-wise)		Bulk Si (continuously)	
Duration	5s	10s	30s	1_2X5	1_10X5	5s	10s
R_s (Ω cm^2)	50	100	381	52	87	23	22
R_{lk} (kΩ cm^2)	89	44	146	480	1010	1195	9102
n	2.43	1.55	0.81	3.01	2.97	2.88	2.84
J_{lk} (μA/cm^2)	23.34	43.88	18.09	8.44	3.76	1.81	0.81
V_{oc} (V)	0.24	0.2	0.17	0.21	0.22	0.17	0.17
J_{sc} (mA/cm^2)	7.32	4.9	1.44	2.77	2.61	0.97	0.78
η	0.38%	0.21%	0.05%	0.12%	0.12%	0.02%	0.02%
FF	0.22	0.21	0.21	0.21	0.21	0.14	0.13
J_p (mA/cm^2)	13.02	8.83	2.44	5.5	4.52	9.41	6.92

The leakage current could be improved further by reducing the interfacial surface states that are maintained by silica interfacial layer. Sun Baoquan group demonstrates the passivation effect of mythyl/allyl on quality improvement of SiNWs diode[114]. The estimated saturation current density is as low as 44.6nA/cm^2. Although the leakage current density J_{lk} is not provided from their report, this saturation current could be viewed as the lowest limit for the leakage current density.

For our cell, the leakage current density J_{lk} = 3.76 μA/cm^2 is about 85 times higher than the saturation current density 44.6 nA/cm^2 tested by Sun et al. Perhaps this is due to the existence of silica interfacial layer, because silica layer is believed to cause the charge trapping states on the interface[27]. In the Table 4-4, the series resistance increases with duration, for example it grows from 52 to 87 Ω cm^2 when breaking time increases from 2 seconds to 10 seconds in unit period. The prolonged breaking time, and thus longer exposure to water and oxygen dissolved in ACN, would cause more silicon oxidation occurrence, leading to a higher series resistance. The trapping interfacial states between silica layer and silicon wire thus may not be passivated by PEDOT, resulting in the remaining leakage current density larger than the saturation current density.

As stated in Chapter 1 of introduction to the basics of solar cells, the V_{oc} of a solar cell can be limited by a low shunt resistance because it provides an alternative way for charge transport

and weakens the photovoltaic effect. But in our case, the resistance parallel to the diode is ultra large, so the low V_{oc} about 0.2V in our cell should not be attributed to the shunt resistance. If the passivation effect could be confirmed further, the Fermi level pinning effect due to the interfacial trapping states could also be ruled out as a reason for the low V_{oc}. Therefore, the cause for the low V_{oc} might be the poor doping in the PEDOT. In fact, the electrodeposited PEDOT is dark blue and not as transparent as expected, suggesting the PEDOT is not on its highly oxidized states, because the light blue color and highly transparency in visible spectrum is always coming along with high conductivity, see the introduction in Chapter 3. We tried to measure the conductance of PEDOT with 4-point probe measurement, but the rough surface on SiNWs makes it difficult to conduct this operation.

In order to know the density of interfacial surface states, we use several other techniques to estimate its quantity in silicon bandgap.

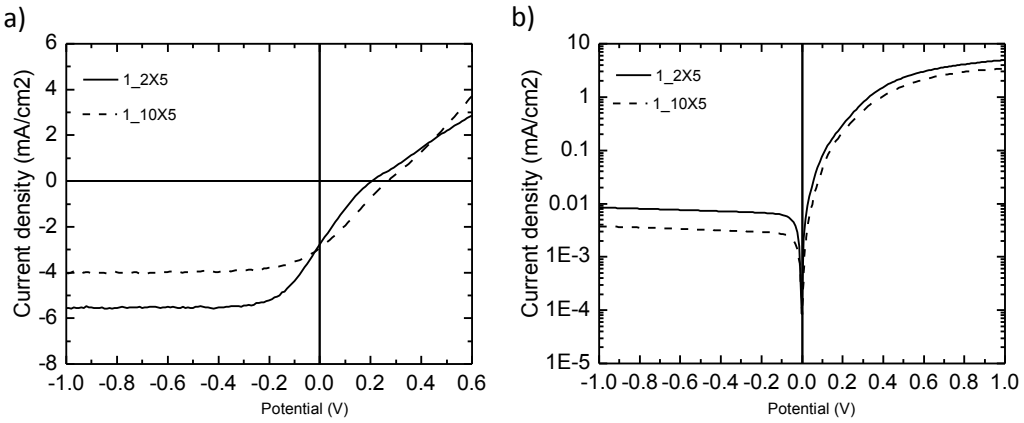

Figure 4-12 a) light and b) dark *J-V* curves of the samples made with step-wise deposition. The 1_2X5 (solid line), 1_10X5 (dashed line) denote that depositing pulse of 1 second is followed by breaking time of 2 seconds and 10 seconds, respectively. The unit of process of pulse and break is repeated 5 times to make the two samples. The SiNWs are fabricated first by the electroplating process in 4mM $AgNO_3$ 4.8M HF aqueous solution for 1 minute, and then by the etching process in 0.3M H_2O_2 4.8M HF aqueous solution for 2 minutes. The SiNWs are treated with KOH + IPA tapering for 10 seconds. PEDOT are electrodeposited onto the SiNWs at a fixed potential 1.5V during the pulse stages in 10mM EDOT 0.1M $LiClO_4$ ACN under 100% illumination.

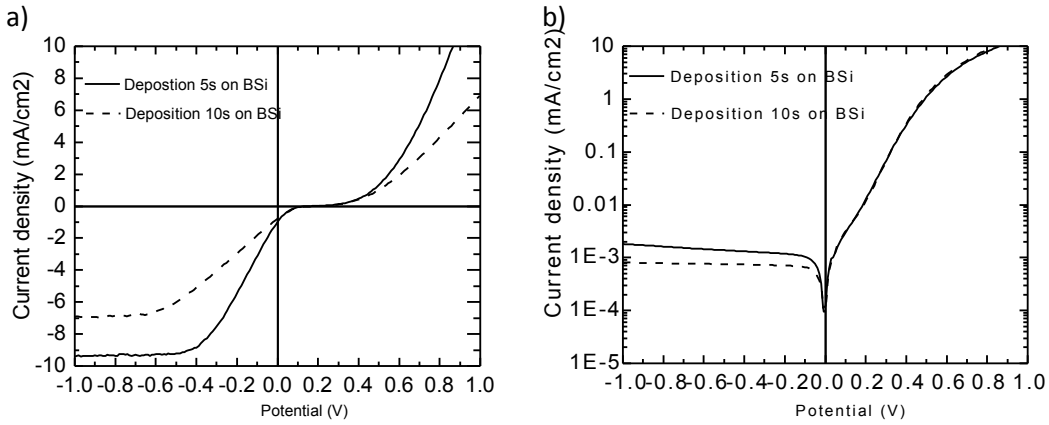

Figure 4-13 a) light and b) dark J-V curves of the cells made on BSi with 5 and 10 seconds PEDOT deposition at a fixed potential 1.5V in 10mM EDOT 0.1M $LiClO_4$ ACN under 100% illumination.

4.3. Capacitance measurement

Because the silica layer actually cannot be avoided, the real structure is more like a Metal-Insulator-Semiconductor (MIS). The band diagram of MIS Schottky diode under bias voltage is shown in Figure 4-14, where Φ_m is the work function of metal, χ the electron affinity of the semiconductor, V_i the voltage drop across the interfacial insulator, Φ_0 the neutral level of the interface states measured from the top of the valence band. E_c, E_v, E_g are the conduction band, the valence band, and the band gap of semiconductor, respectively. E_{fm} E_{fs} are the Fermi levels of metal and semiconductor; the difference between them is caused by an applied voltage V. The insulator thickness is δ. φ_s is the potential difference of semiconductor surface and deep body, which indicates band bending.

If the thickness of oxide layer is large enough (δ > 2nm), the communication between interface states and metal can be neglected.[115] The interface states are in equilibrium with semiconductor. Charge occupation in these states is determined by Fermi function. So the interface state between the neutral level of the interface states Φ_0 and semiconductor Fermi level E_{fs} can be taken as an acceptor that is probably occupied. When semiconductor Fermi level varies with the applied voltage V, the interface states a few k_BT/q around Fermi level experience electron trapping from and electron emitting into semiconductor. Therefore the semiconductor and interface states can be viewed as two parallel connected capacitors because of their charge communication with each other. In terms of the insulator of oxide silicon, because it serves as voltage divider, it should be arranged in series with semiconductor and interface states. The simplified equivalent circuit is shown in Figure 4-14. The mathematical deduction of the equivalent circuit can be seen in literature[116].

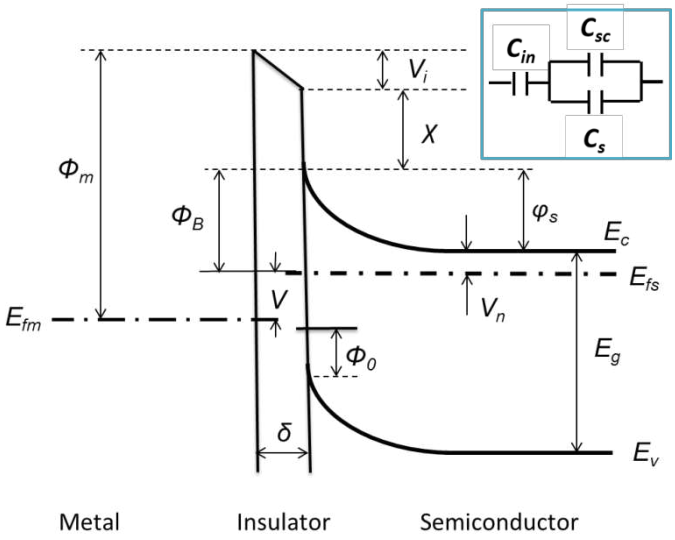

Figure 4-14 Band diagram for Metal/Insulator/Semiconductor MIS structure under non-equilibrium conditions. The inset of equivalent circuit of capacitors simplifies and reveals the relationship between insulator and silicon in charge storing. Adapted from the literature [27]**.**

As a result of the involvement of interface states and insulator between metal and semiconductor, the Mott-Schottky relationship in Equation 4-4 can be affected. In Figure 4-15 the M-S relationship is dependent on the frequency used for measurement. Linearity is shown for the frequency 65 kHz, while for 65Hz the linearity is disturbed. The influence of frequency is believed to be related to the interface states, which would not respond to a single high frequency, but contribute to the measured capacitance at low frequency. The higher the frequency is used, the fewer interface states take part into the measurement.[117]

According to Equation 4-4 4-5, the barrier height can be extracted from x axis intercept. The extracted barrier height is about 0.78eV for SiNWs/PEDOT diode.

$$C^{-2} = \frac{2}{q\varepsilon_{sc}N_D}\left(V + \frac{k_BT}{q} - \left(\Phi_B + \frac{k_BT}{q}\,ln\left(\frac{N_D}{N_{CB}}\right)\right)\right) \qquad 4\text{-}4$$

$$\Phi_B = V_{x0} + \frac{k_BT}{q} - \frac{k_BT}{q}\ln\left(\frac{N_D}{N_{CB}}\right) \qquad 4\text{-}5$$

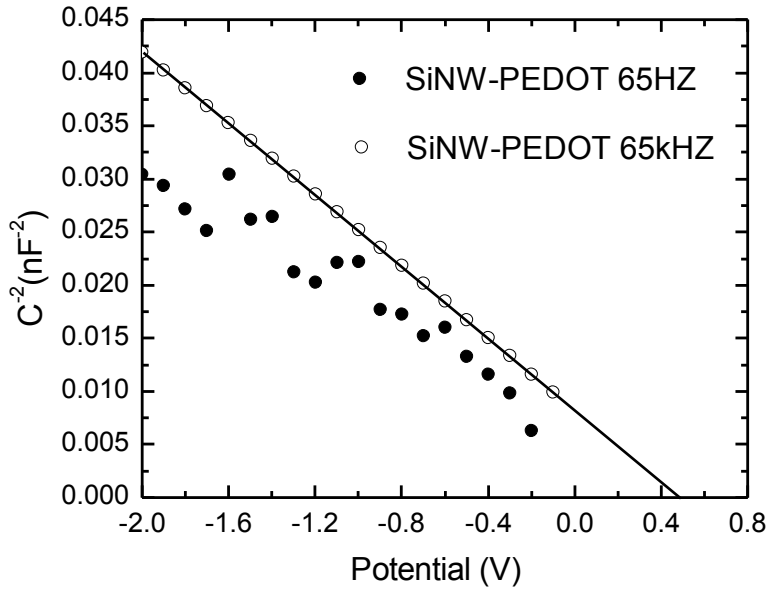

Figure 4-15 Mott-Schottky (M-S) relationship of SiNWs/PEDOT hybrid cell . The empty circles denote M-S relationship at 65kHz, while the full circles on are corresponding to that at 65Hz. The fitted solid line for 65kHz M-S relationship has the intercept on the bias axis showing the flat band potential of 0.496V. The SiNWs are fabricated first by the electroplating process in 4mM $AgNO_3$ 4.8M HF aqueous solution for 1 minute, and then by the etching process in 0.3M H_2O_2 4.8M HF aqueous solution for 2 minutes. The SiNWs are not treated with KOH tapering. PEDOT are electrodeposited onto the SiNWs for 3 voltammetry cycles from -1V to 2V in 10mM EDOT 0.1M $LiClO_4$ ACN under 100% illumination.

4.4. Interface states density

By using *J-V* curve and barrier height extracted from M-S relationship, the interface states density can be estimated and its position in bandgap can also be plotted as in Figure 4-16. The method is presented in Appendix B.

In Figure 4-16, the SiNWs are fabricated with EMACE method: first electroplated in 4mM $AgNO_3$ for 1 minute, and then etched in 0.3M H_2O_2 for 2 minutes. PEDOT is electrodeposited onto the SiNWs for 3 voltammetry cycles from -1V to 2V in 10mM EDOT 0.1M $LiClO_4$ ACN solution.

The interface states density of SiNWs in Figure 4-16 is about one order of magnitude higher than silicon wafer[117]. The high density of silicon nanowires is believable, because during the etching process there must be a lot of defects on the silicon lateral surface. Furthermore, as we have stated, the continuously depositing PEDOT fabrication cannot achieve a conformal layer covering the entire silicon nanowire lateral surface. In addition the SiNWs are not

treated with KOH tapering. So the continuous CV method of deposition and the narrow interspace between SiNWs may cause PEDOT growth just on the top of SiNWs array, leading to the lower part of the SiNWs not passivated by PEDOT. The lack of passivation layer on the surface also leads to high density of interface states.

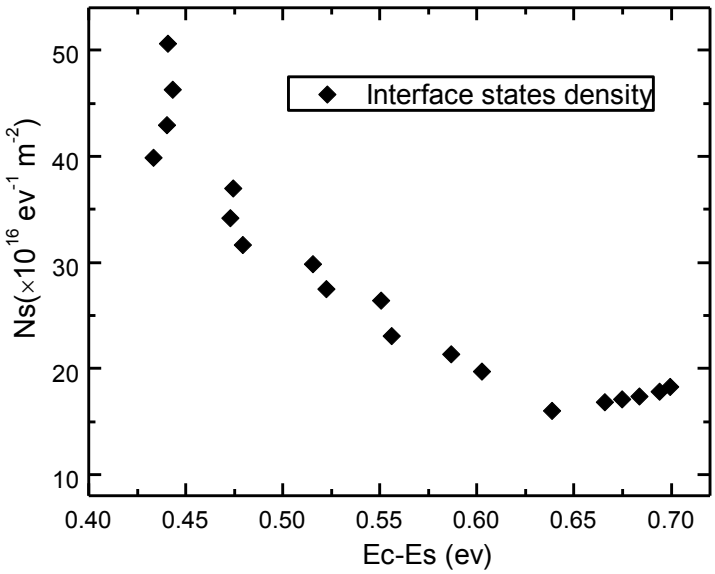

Figure 4-16 Plot of interface states density N_s vs. its position E_s in band gap of silicon with respect to conduction band edge E_c. The SiNWs are fabricated first by the electroplating process in 4mM $AgNO_3$ 4.8M HF aqueous solution for 1 minute, and then by the etching process in 0.3M H_2O_2 4.8M HF aqueous solution for 2 minutes. The SiNWs are not treated with KOH tapering. PEDOT are electrodeposited onto the SiNWs for 3 voltammetry cycles from -1V to 2V in 10mM EDOT 0.1M $LiClO_4$ ACN under 100% illumination.

4.5. EQE measurement

The EQE spectra of SiNWs/PEDOT and BSi/PEDOT are presented in Figure 4-17. Compared with bulk Si, SiNWs make the cell more efficient in light converstion in the visible range and near infrared range. The reason might be the strong light trapping effect in SiNWs array. However, the overall quantum efficiency is rather for both SiNWs and bulk Si cell, the maximum is approximately 15%. One possible reason might be the high series resistance which becomes a high energy barrier against charge collection. Another possible reason is that the low transparency of PEDOT in the visible range, and most absorption takes place in PEDOT rather than in SiNWs. The absorption loss in PEDOT leads to low EQE.

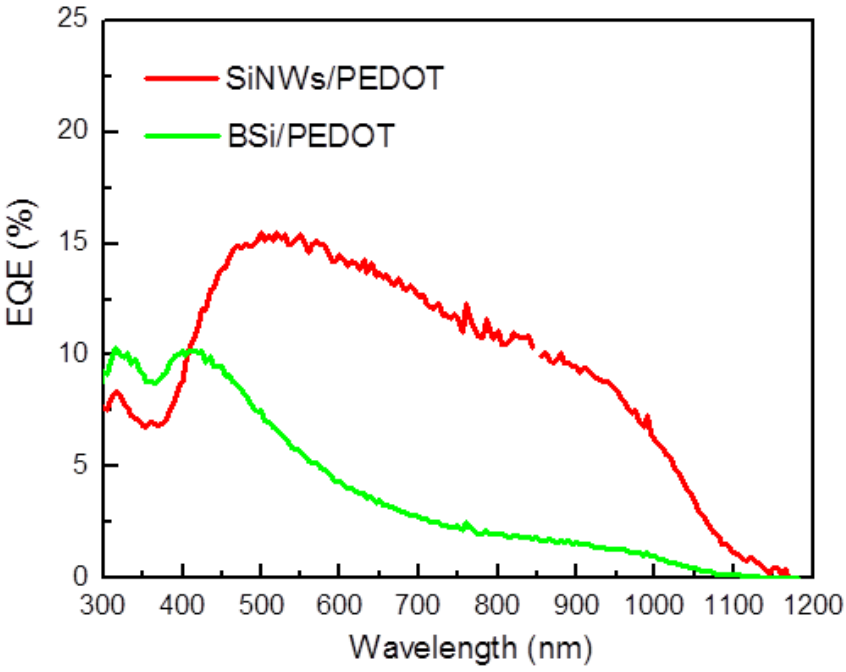

Figure 4-17 EQE measurements on SiNWs/PEDOT and BSi/PEDOT hybrid cells. SiNWs were fabricated with Ag plating in 4mM $AgNO_3$ for 1 minute and then with etching in 0.3M H_2O_2 for 2 minutes. PEDOT was polymerized with step wise deposition 1_10X5 in 10mM EDOT ACN of 0.1M $LiClO_4$ under 100% illumination.

Conclusions

Strong illumination intensity during PEDOT synthesis favors a better diode. Illumination is significant because it provides charge carriers of holes that may be the key for both PEDOT synthesis and doping.

Long duration of PEDOT deposition results in thicker PEDOT layer which attenuates the absorption of light. This effect exists both in PEDOT fabrication and light *J-V* curve measurement.

Higher potential during PEDOT fabrication supports to fabricate better diode perhaps because it offers higher energy to dope PEDOT.

The step-wise manner of deposition achieves a conformal layer that passivates the interface states and thus leads to a dramatic decrease in leaky current density.

The limiting factor to improve SiNW/PEDOT hybrid cell might be the series resistance caused by silicon oxidation during electrodeposition. Silicon oxidation could be reduced by using EDOT dimer (bis-EDOT) for PEDOT polymerization due to its much lower oxidation potential than EDOT monomer[101].

In order to identify and improve conductivity of PEDOT, the working principle of electrodeposition should be understand for SiNWs electrode. The performance of SiNWs electrode is quite different from its bulk counterpart in PEDOT synthesis and in its doping as we observed. This might be related with the enhanced light absorption in SiNWs array as well as a large number of surface defects. More research is needed to improve the conductivity of electrodeposited PEDOT.

The impedance spectrum might provide the way to know the PEDOT electronic property[118]. Also impedance spectrum is a power tool to know the property of SiNWs as electrode in electrolyte[119]. Besides capacitance got from impedance measurement gives the Mott-Schottky relationship that could provide the information of PEDOT Fermi level as well as the surface states on silicon nanowires[60].

Conclusions and Perspectives

We now try to summarize the main results that we can draw from this study, and also offer work opportunities.

- Antireflection property of SiNWs

  By utilizing EMACE method, the 13-16mM $AgNO_3$ range has been found to lead to low reflection. At 13mM $AgNO_3$ the reflection can be as low as 1% in the wavelength range of 500nm to 800nm. The relationship between $AgNO_3$ concentration and SiNWs reflection is studied.

- SiNWs morphology modified with tapering process

  KOH tapering process helps to enlarge the inter-room between wires by reducing the areal density of wires. More significantly, the strong light trapping effect is still maintained in SiNWs if the tapering is shorter than 30 seconds.

- PEDOT polymerization on SiNWs electrode

  We also demonstrated that the PEDOT layer can be successfully polymerized and deposited on SiNWs array as electrode with the electrochemical method. The CV measurements in PEDOT deposition show that SiNWs and BSi as electrode are different from the conductive electrode of vitreous carbon. Illumination is not only necessary for PEDOT polyermization, also affects the doping level of PEDOT. Illumination provides photogenerated holes that make SiNWs more conductive both in PEDOT polymerization and in PEDOT doping.

- Core-shell SiNW/PEDOT structure by using step-wise deposition

  By using the step-wise deposition, the conformal PEDOT layer can be obtained to wrap each single silicon wire. Competition between PEDOT polymerization on wire tips and EDOT monomer diffusion is the mechanism that determines the morphology of PEDOT on SiNWs. The EDOT diffusion effect on the morphology of PEDOT is confirmed by tuning the interspace between wires. The OCP during PEDOT step-wise deposition can be an indicator to know PEDOT covering percentage of single silicon wire surface.

- Ultrahigh leakage resistance and ultralow leakage current density in SiNWs/PEDOT cell

  The SiNWs/PEDOT cell made with the step-wise deposition has a leakage current J_{lk} = 3.76μA/cm^2 at least 30 times lower than the cell made with spin-coating method in literature[58]. The leakage resistance parallel to diode can be larger than 1MΩ cm^2,

suggesting a good passivation effect to remove interfacial states which constitutes the pathway for charge transport at reverse bias. The reason might be that PEDOT preferentially deposits at those sites where surface defects are located.

Next is the methods that would work to understand and further improve the SiNWs/PEDOT cell's performance

- ✧ The limiting factor to improve SiNWs/PEDOT hybrid cell might be the series resistance. The series resistance might be either caused by silicon oxidation during electrodeposition, or due to the low doping level of PEDOT. The combination of high resolution TEM and focused ion beam would work to investigate the interface properties and confirm the thickness of silica layer between Si crystal and PEDOT.

- ✧ The interfacial silica layer could be avoided or reduced by removing water in ACN solution. Bis-EDOT might be an alternative for EDOT to fabricate PEDOT since it has relatively low oxidation potential[101].

- ✧ PEDOT doping level is a key parameter that determines PEDOT/SiNWs cell performance. More research is needed to improve the conductivity of electrodeposited PEDOT. It could be improved further by using more powerful illuminating lamp.

- ✧ The high leakage resistance suggests a passivation effect of PEDOT to eliminate surface states. The impedance spectrum might provide the way to know the PEDOT interfacial states property[118]. Some other methods might also helpful to know the interface such as XPS[120], transient voltage measurement[121].

Through this study, we demonstrated the feasibility of the hybrid solar cells, combining silicon nanowires and PEDOT polymer. The different steps of this realization have been shown in the corresponding chapters. The main advantage of such a structure is the simplicity to both the structure of silicon and deposit PEDOT, using efficient and low-cost methods such as chemical etching method and electrochemical deposition. These two processes have never been used before at the same time for the production of solar cells.

Despite this innovative approach, the results of our cells are not satisfactory, and more work is needed to improve their efficiencies. However, this study allows us to imagine the production of hybrid solar cells with reasonable performance at a low cost.

Appendix A. Cheung-Cheung's method

Cheung and Cheung developed a method to evaluate series resistance and ideality factor of a practical Schottky diode by only using the forward *I-V* characteristic curve. According to the thermionic emission model for a Schottky diode, the current *I* flows through the diode is given by

$$I = I_s \, exp\left(\frac{-qV_D}{nk_BT}\right) \quad \text{A-1}$$

Where q is the electronic charge, k_B is the Boltzmann's constant, T is the absolute temperature, and V_D is the applied potential across the diode. n is the ideality factor, a dimensionless parameter involved in the *I-V* characteristics to take into account the non-ideal behavior.[27] The I_s is saturation current and can be expressed by[105]

$$I_s = A_{eff}A^{**}T^2 \, exp(\frac{-q\Phi_B}{k_BT}) \quad \text{A-2}$$

where Φ_B is the Schottky barrier height; A^{**} is the Richardson's constant 112 A/cm^{2}K^2 for n type silicon[105], A_{eff} is the effective diode area.

$$I = I_s\left\{exp\left[\frac{q(V - IR_s)}{nk_BT}\right] - 1\right\} - \frac{V - IR_s}{R_{lk}} \quad \text{A-3}$$

Because the large value of leakage resistance compared with the forward bias within 2V, the last term of Equation A-3 can be neglected and Equation A-3 can be reduced to

$$I = I_s\left\{exp\left[\frac{q(V - IR_s)}{nk_BT}\right] - 1\right\} \quad \text{A-4}$$

When the bias across diode $V - IR_s > 3k_BT/q$ the equation becomes

$$I = I_s \, exp\left[\frac{q(V - IR_s)}{nk_BT}\right] \quad \text{A-5}$$

Using Equation A-2 about I_s, Equation A-5 can be rewritten by

$$V = IR_s + n\Phi_B + \frac{n}{\beta}\ln(\frac{I}{A_{eff}A^{**}T^2}) \quad \text{A-6}$$

Where

$$\beta = \frac{q}{k_BT} \quad \text{A-7}$$

Differentiating Equation A-6 with respect to *I* and rearranging terms, we obtain

$$\frac{\mathrm{d}V}{\mathrm{d}\ln I} = IR_s + \frac{n}{\beta} \quad \text{A-8}$$

Thus, a plot of dV/dln$I$ vs I will give resistance R_s as the slope and n/β as the y-axis intercept. One advantage of Cheung-Cheung's method for SiNWs/PEDOT diode is no need to consider the real diode area A_{eff}, which is neglected during the differentiating operation and has no effect on the resulted resistance and ideality factor.

Werner[108] confirmed the accuracy of Cheung-Cheung's method and he also points out the method should be operated in the intermediate bias regime of forward J-V curve. When the forward bias is in the lower regime, the curve is mainly dominated by leakage current, while in the larger regime the series resistance can be changed by conductivity modulation. In the intermediate voltage regime the potential drops at series resistance and at diode are comparable.

Appendix B. Interface states density extraction method

The band diagram of MIS diode is shown in Figure B-1 which is the same as Figure 4-14. Φ_m is the work function of metal, χ the electron affinity of the semiconductor, V_i the voltage drop across the interfacial insulator, Φ_0 the neutral level of the interface states measured from the top of the valence band. E_c, E_v, E_g are the conduction band, the valence band, and the band gap of semiconductor, respectively. E_{fm} E_{fs} are the Fermi levels of metal and semiconductor; the difference between them is caused by an applied voltage V. The insulator thickness is δ. φ_s is the potential difference of semiconductor surface and deep body, which indicates band bending.

When a forward bias V is applied to the diode this bias is burdened partly on insulator capacitance by ΔV_i and partly semiconductor capacitance $\Delta\varphi_s$. Since the surface potential φ_s and V_i are taken as positive, at the forward bias V, ΔV_i and $\Delta\varphi_s$ are negative.

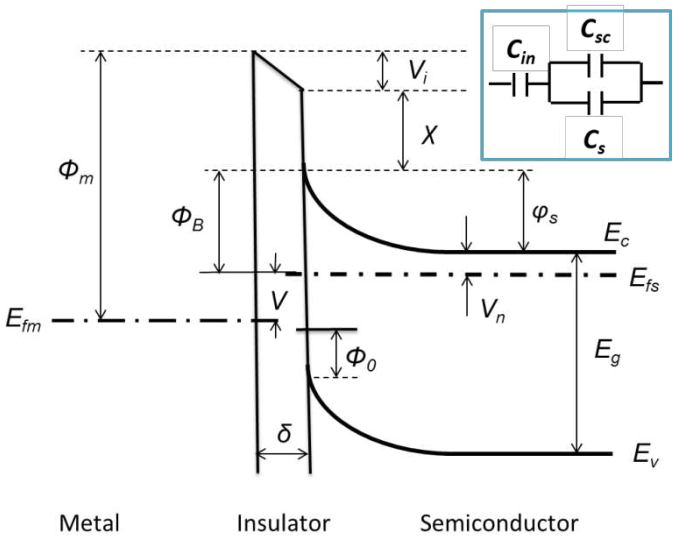

Figure B-1 Band diagram for Metal/Insulator/Semiconductor MIS structure under non-equilibrium conditions. The inset of equivalent circuit of capacitors simplifies and reveals the relationship between insulator and silicon in charge storing. Adapted from the literature [27]**.**

So the relationship between applied potential and its partitions on insulator and semiconductor is

$$V = (-\Delta V_i) + (-\Delta\varphi_s) \qquad \text{B-1}$$

We define the fraction of potential drop on semiconductor and interface states as f

$$f \equiv \frac{-\Delta\varphi_s}{V} \qquad \text{B-2}$$

$$f = \frac{-\mathrm{d}\varphi_s}{\mathrm{d}V} \quad \text{B-3}$$

Then, the partition of voltage drop on insulator is given by

$$\frac{-\mathrm{d}V_i}{\mathrm{d}V} = 1 - f \quad \text{B-4}$$

Considering the insulator as a simple plate capacitor, the voltage drop across the insulator is obtained as

$$-\mathrm{d}V_i = \frac{\mathrm{d}Q_{in}}{\varepsilon_{in}/\delta} \quad \text{B-5}$$

Charge conversion in these capacitances gives

$$Q_{in} + Q_{sc} + Q_s = 0 \quad \text{B-6}$$

Where Q_{in}, Q_{sc}, and Q_s are charge quantities stored in insulator, semiconductor depletion layer and interface states, respectively.

The net charge quantity stored in interface states at voltage V can be calculated by the following equation

$$Q_s(V) = -q\int_{\Phi_0}^{E_g - q\varphi_s(V) - qV_n} N_s(E)\mathrm{d}E \quad \text{B-7}$$

Where N_s is the density of interface states in bandgap of silicon, and for a constant N_s, the net charge quantity is

$$Q_s(V) = -qN_s[E_g - q\varphi_s(V) - qV_n - q\Phi_0] \quad \text{B-8}$$

$$\frac{\mathrm{d}Q_s}{\mathrm{d}\varphi_s} = q^2 N_s \quad \text{B-9}$$

The charge in depletion layer of semiconductor is[27]

$$Q_{sc}(\mathrm{V}) = -[2q\varepsilon_{sc}N_d\varphi_s(V)]^{\frac{1}{2}} \quad \text{B-10}$$

$$\frac{\mathrm{d}Q_{sc}}{\mathrm{d}\varphi_s} = \frac{\varepsilon_{sc}}{W} \quad \text{B-11}$$

$$W = \left[\frac{2\varepsilon_{sc}}{qN_d}\varphi_s(V)\right]^{\frac{1}{2}} \quad \text{B-12}$$

Where W is the depletion layer of semiconductor, which is usually several dozens of nanometers.

Using Equation B-3, B-4, B-9, B-11we get

$$\frac{\mathrm{d}V_i}{\mathrm{d}V} = \frac{\delta}{\varepsilon_{in}}\frac{\mathrm{d}(-Q_{sc} - Q_s)}{\mathrm{d}V} = -\frac{\delta}{\varepsilon_{in}}\left(\frac{\mathrm{d}Q_{sc}}{\mathrm{d}\varphi_s}\frac{\mathrm{d}\varphi_s}{\mathrm{d}V} + \frac{\mathrm{d}Q_s}{\mathrm{d}\varphi_s}\frac{\mathrm{d}\varphi_s}{\mathrm{d}V}\right) \quad \text{B-13}$$

$$\frac{1-f}{f} = \frac{\delta}{\varepsilon_{in}}\left(\frac{\mathrm{d}Q_{sc}}{\mathrm{d}\varphi_s} + \frac{\mathrm{d}Q_s}{\mathrm{d}\varphi_s}\right) \quad \text{B-14}$$

$$\frac{1}{f} = 1 + \frac{\delta}{\varepsilon_{in}}\left(\frac{\varepsilon_{sc}}{W} + q^2 N_s\right) \quad \text{B-15}$$

Compared with depletion layer in semiconductor that is usually several dozen nanometers, the oxide insulator layer is one order of magnitude thinner. So the depletion layer contribution to ideality factor in Equation B-15 can be neglected, and Equation B-15 becomes

$$\frac{1}{f} = 1 + \frac{\delta}{\varepsilon_i} q^2 N_s \quad \text{B-16}$$

Taken into account the tunneling effect through the insulator of oxide layer, the Schottky diode equation can be corrected by[117],[115]

$$I = A_{eff} A^{**} T^2 exp(-\Phi^{1/2}\delta)\ exp\left\{\frac{-q[\varphi_{s0} + \Delta\varphi_s + V_n]}{k_B T}\right\} \quad \text{B-17}$$

Where Φ is the mean barrier height presented by the thin interfacial layer, φ_{s0} the band bending potential at zero bias. The term exp$(-\Phi^{1/2}\delta)$ is known as the transmission coefficient across the thin insulator layer.

Φ_B is the barrier height of Schottky diode, see in Figure 4-14.

$$\Phi_B = \varphi_{s0} + V_n \quad \text{B-18}$$

Using Equation B-2 and Equation B-18, we can rewrite the corrected diode equation to be

$$I = A_{eff} A^{**} T^2 exp(-\Phi^{1/2}\delta)\ exp(\frac{-q\Phi_B}{k_B T}) exp\left\{\frac{qfV}{k_B T}\right\} \quad \text{B-19}$$

The current Equation B-19 can be simplified further

$$I = I_s\ exp\left\{\frac{fqV}{k_B T}\right\} \quad \text{B-20}$$

Where

$$I_s = A_{eff} A^{**} T^2 exp(-\Phi^{1/2}\delta)\ exp(\frac{-q\Phi_B}{k_B T}) \quad \text{B-21}$$

By replacing the term *f* with Equation B-16, the diode *J-V* relationship becomes:

$$I = I_s\ exp\left[\frac{qV}{(1 + \frac{\delta}{\varepsilon_i} q^2 N_s) k_B T}\right] \quad \text{B-22}$$

Equation B-22 provides the possibility to estimate interface states density and their distribution in bandgap of silicon based on measured *J-V* curve. The method can be found in literature[117]. After differentiation operation of applied voltage *V* with respect to ln*I* as in the Cheung-Cheung's method, Equation B-22 can be transformed to be

$$N_s(V) = \frac{\varepsilon_i}{q^2 \delta}\left(\frac{k_B T}{q}\frac{\mathrm{d}V}{\mathrm{d}\ln I} - 1\right) \quad \text{B-23}$$

We have extracted the ideality factor n = 1.70. According to the relationship between silica layer's thickness and the Schottky diode ideality factor, see Figure B-2, it is estimated that the thickness δ of oxide layer between silicon and PEDOT is 2.88nm.

The position of interface states in band gap is defined with respect to conduction band edge of silicon as E_c-E_s=$q\Phi_B$-(q/n) V.[117]

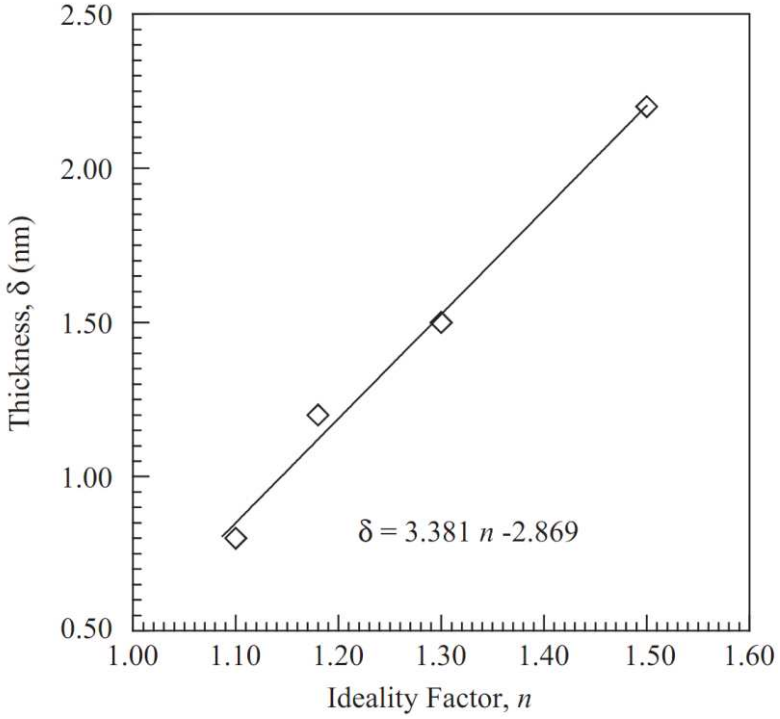

Figure B-2 Relationship of thickness δ of oxide layer on silicon with ideality factor n [122]

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Summary: Today human beings are suffering energy crisis. One possible solution is to get solar power directly from the sun by creating highly efficient solar cells at a low cost. Through this study, we demonstrated the feasibility of the hybrid solar cells, combining silicon nanowires and PEDOT polymer. The main advantage of such a structure is the simplicity to both the structure of silicon and the deposition of PEDOT, using efficient and low-cost methods of metal-assisted chemical etching (EMACE) and electrochemical deposition. The silicon nanowires (SiNWs) array becomes an active research subject nowadays in photovoltaic application mainly due to its good light trapping effect. The etched SiNWs obtained can reach a reflection lower than 3% in the whole visible range. The areal density of SiNWs in array can be tuned by KOH tapering process. Besides core-shell junction in Si nanowire is effective in photogenerated carriers' collection. It is first time, to our knowledge, that the polymer PEDOT is electrochemically polymerized with etched SiNWs as electrode, and a real core-shell junction wrapping individual silicon nanowire can be realized. The core-shell morphology is dependent on the competition between EDOT diffusion to wire bottom space and PEDOT growth on wire tips. The fabricating parameters of illumination intensity, potential, and duration are investigated about their influence on the I(V) characterization of PEDOT/SiNWs cells. The most remarkable feature of our PEDOT/SiNWs hybrid cell is its ultralow leakage current density and ultrahigh leakage resistance, suggesting a good passivation effect to remove interfacial states which constitutes the pathway for charge transport at reverse bias.

Key Words: photovoltaic, hybrid solar cells, silicon nanowires, PEDOT, light trapping, chemical etching, electrodeposition.

Résumé : Le contexte énergétique actuel est un enjeu sociétal. L'utilisation de l'énergie solaire au travers de cellules solaires photovoltaïques à bas-coût et à haut rendement, est une des voies envisagées pour répondre aux besoins énergétiques. Ce travail de thèse a permis de démontrer la faisabilité de cellules solaires hybrides, basées sur une jonction de type « cœur/coquille » entre des nanofils de silicium obtenus par gravure chimique et du PEDOT polymérisé par voie électrochimique. Les principaux avantages d'une telle structure sont à la fois la simplicité et le faible coût des méthodes utilisées pour la réalisation de la cellule. Les nanofils de silicium, grâce à leur capacité à piéger la lumière, conduisent à des propriétés d'anti-reflet très intéressantes avec notamment des valeurs de réflexion inférieures à 3% sur toute la gamme spectrale du visible. La réalisation de telles jonctions a fait l'objet d'une étude poussée sur les différentes caractéristiques de dépôt du polymère, tels que l'intensité lumineuse, le potentiel appliqué et la durée du procédé. L'influence de ces paramètres sur la mesure I(V) de la cellule solaire hybride complète a également été étudiée. On peut noter en particulier que l'on obtient ainsi une densité de courant de fuite très faible et une résistance de fuite très élevée, permettant d'émettre l'hypothèse d'une bonne passivation des états de surface. Ceci constitue une voie prometteuse pour obtenir un bon transport de charges en polarisation inverse.

Mots Clefs : photovoltaïque, cellules solaires hybrides, nanofils de silicium, PEDOT, piégeage de la lumière, gravure chimique, électrodépôt.