Characterization of Normal Propagation Delay for Delay Degradation Model (DDM)*

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Abstract. In previous papers we have presented a very accurate model that handles the generation and propagation of glitches, which makes an important headway in logic timing simulation. This model is called *Delay Degradation Model* (DDM). Characterizing DDM completely also implies the characterization of the *normal propagation delay.* In this paper, we propose a simple heuristic model that includes its dependence on the *output load* and the *input transition time.* We have tested this model and found a mean deviation lower than 4%. Also, we present a characterization process for this model that is fully integrated into AUTODDM without affecting the total simulation time needed to characterize a standard cell.

1 Introduction

In the field of logic simulation of digital CMOS circuits, delay models exist that take into account most issues affecting accuracy [1–4]: low voltage, submicron and deep submicron devices, transition waveform, etc. There are also dynamic effects, the most important being the so-called *input collisions* [5], which happens when two or more input signals change almost simultaneously. The type of input collision that more notably affects the behaviour of digital circuits are the *glitch collisions,* or those that may cause narrow pulses or glitches. In previous papers [6–8] we have presented a very accurate model that handles the generation and propagation of glitches, which makes an important headway in logic-timing simulation. This model is called *Delay Degradation Model* (DDM).

One important point in any delay model (including the DDM) is the definition of the model parameters and the set up of a useful characterization process

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that describes how the model parameter values are obtained. This information is necessary to be able to reproduce simulation results by others and also to check the viability of the approach: a model that is very hard or expensive to characterize may be useless. In previous papers [8, 9] we have described the characterization process of the degradation parameters of DDM and we have presented a tool that automates the process, called AUTODDM.

The mentioned DDM is compatible with any model for the *normal propagation delay*, where "normal" means the conventional delay considered by most logic-timing simulators when degradation effect is not taken into account. In the specialized literature there are different papers [1, 2] where authors present accurate normal delay models and it would be possible to select one of these models to provide a normal propagation delay model for the DDM, though, since they are models focused on the geometric level, they are not suited to our aims.

At this time, the DDM focuses on circuits described at the gate-level, and is being implemented in a logic-timing simulator based on standard cells, called HALOTIS [10]. From this perspective, an appropriate normal propagation delay model that complements the DDM should be described at the same level. It should be simple enough to be fast and easy to implement without significant loss of accuracy, and must be also easy to characterize, possibly using the same data extracted from the DDM characterization.

In this work, we have obtained such a model for the normal propagation delay, suited for the DDM, that includes its dependence on the *output load* and the *input transition time* at the gate-level. We have also developed a characterization process and included it in the previously developed tool AUTODDM [9]. The analysis is carried out in a 0.35 μm CMOS technology using the standard cell library provided by The Foundry.

The organization of the paper is as follows: in Sect. 2 the characterization process of the degradation parameters is presented; in Sect. 3 we present the results of the normal propagation delay evaluation and we propose a simple model that fits the real behaviour very well; Sect. 4 presents the characterization process for the proposed model; finally we will finish with the main conclusions of this work.

2 Characterization Process of the Degradation Parameters

The equation to evaluate the propagation delay according to the DDM is:

$$t_p = t_{p0}\left[1 - \exp\left(-\frac{T - T_0}{\tau}\right)\right] \tag{1}$$

where T is the time elapsed since the last output transition, t_{p0} is the normal propagation delay and T_0 and τ are the degradation parameters.

For each gate, τ and T_o depend on the output load (C_L), the supply voltage (V_{DD}), the input transition time (τ_{in}) and the position of the input that is

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changing state (i). It has been obtained [8] that this dependence can be expressed as:

$$\tau_x V_{DD} = A_{xi} + B_{xi} C_L \tag{2}$$

$$T_{0x} = \left(\frac{1}{2} - \frac{C_{xi}}{V_{DD}} \right) \tau_{in} \tag{3}$$

where x stands for r or f depending on the sense of the output transition (rise or fall respectively).

A CMOS gate is fully characterized with respect to the degradation effect when the set $\{A_{xi}, B_{xi}, C_{xi}\}$ is obtained for each gate input. So, the objective of the characterization process is to obtain the values of the set of degradation parameters of (2) and (3) for a particular gate, i.e.:

$$\{A_{xi}, B_{xi}, C_{xi}\} \qquad x = r, f \qquad i = 1...n \tag{4}$$

The characterization process is composed of three main tasks [9]: (a) obtain t_p vs. T curves corresponding to (1); (b) obtain τ vs. C_L curves corresponding to (2); and (c) obtain T_0 vs. τ_{in} curves corresponding to (3).

The main idea in this process is to establish the adequate variation ranges of C_L and τ_{in} in order to obtain accurate values of A, B, and C. With respect to the variation of C_L, the range depends on the gate's input capacitance (C_{in}) varying between $2C_{in}$ and $10C_{in}$, while the range of τ_{in} is calculated as a function of the normal propagation delay when the input transition time is zero (this parameter is called t_{ps}). So, an adequate range for τ_{in} varies between $0.1t_{ps}$ (corresponding to sufficiently fast transitions) and $10t_{ps}$ (corresponding to sufficiently slow transitions).

3 Normal Propagation Delay Analysis and Modeling for DDM

Actually, characterizing the DDM completely also implies the characterization of the normal propagation delay (t_{p0}), and the value of t_{p0} depends on both C_L and τ_{in} [1, 4]. Our main objective is to analyse the behaviour of t_{p0} in order to implement it, as part of DDM, in a logic timing simulator (HALOTIS) focused on the simulation of circuits based on standard cell libraries. The model for t_{p0} should be simple and fast in terms of computation time, though it must be accurate enough inside the C_L and τ_{in} variation ranges exposed in the previous section. This model should also be developed at the same level than the DDM (at the gate-level) providing a set of characteristic gate parameters.

We have studied the value of t_{p0} with respect to C_L and τ_{in} for three different gates: an inverter (INV), a two-inputs NAND gate (NAND2), and a two-inputs NOR gate (NOR2). For these gates we have measured the delay from each input to the output of the gate for both falling and raising output transitions. We will note each case as GATE i-R/F, where GATE is INV (inverter), NAND2 (two-inputs NAND gate), or NOR2 (two-inputs NOR gate); i is the number of

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the input changing; R means a rising output transition; and F means a falling one.

Figure 1.a presents the three-dimensional representation of t_{p0} with respect to C_L and τ_{in} obtained by electric simulation with HSPICE [11] (in subsequent paragraphs, we will refer to these data as a *HSPICE-grid*) for the case of INV 1-R (inverter, input 1 changing with raising output). As we can observe, the grid surface conforms practically to a plane. Figures 1.b and 1.c show the corresponding grid obtained for the cases of NAND2 2-R and NOR2 1-F respectively. In these last two figures it can be seen the same behaviour as in the first one.

Due to these results, we propose the next simple heuristic model in order to fit the normal propagation delay:

$$t_{p0} = D_{xi}C_L + E_{xi}\tau_{in} + F_{xi} \tag{5}$$

where D_{xi}, E_{xi}, and F_{xi} are the model parameters. An individual parameter value is obtained for each type of output transition (r or f, noted by x) and each input of the gate (noted by i).

This model relies on the mentioned set of parameters $\{D_{xi}, E_{xi}, F_{xi}\}$ which have to be characterized for each gate and transition type. In order to verify that this simple model correctly adjusts the gates behaviour, we have fitted these parameters using multiple linear regression over the HSPICE-grid. Figure 2 shows the same representations of Fig. 1's but, in this case, t_{p0} is calculated applying (5). It is clear that the behaviour of this simple model correctly adjusts the HSPICE-grid.

The mentioned result has been obtained for the whole set of studied cases. In table 1 we can see, for each case: the value of the parameters (D, E, and F), the mean absolute error ($\overline{err}$) in ps, and the mean deviation ($\overline{dev}$) expressed into percentages. This error measures are calculated contrasting the value of t_{p0} in the HSPICE-grid with the value obtained from the proposed model (5). It shows clearly that the approximation is adequate, since the mean deviation is always lower than 4%.

4 Characterization Process of Normal Propagation Delay

Once we have established a linear model for the value of t_{p0}, we have to develop a characterization process to be included in AUTODDM. Our intention is also to reduce the impact on the total characterization time as much as possible.

Actually, it is possible to perform an adequate characterization of the D, E, and F parameters using the same data reported by AUTODDM. This tool performs two groups of simulations: one for a set of C_L values and a fixed typical τ_{in} and the other for a set of τ_{in} values and a fixed typical C_L. So, data reported by AUTODDM provide two lines in the HSPICE-grid (Fig. 3).

Figure 4 shows the approximation obtained starting from AUTODDM data. As we can see, these values are practically the ones obtained for Fig. 2. In table 2 we present the characterization data obtained from AUTODDM results for the

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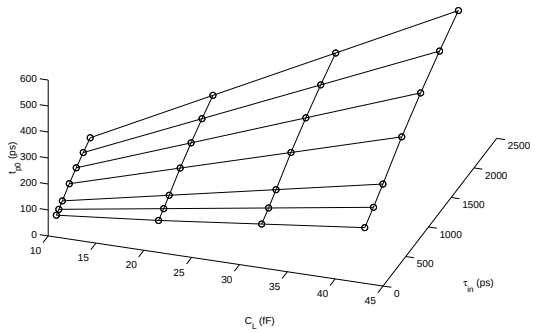
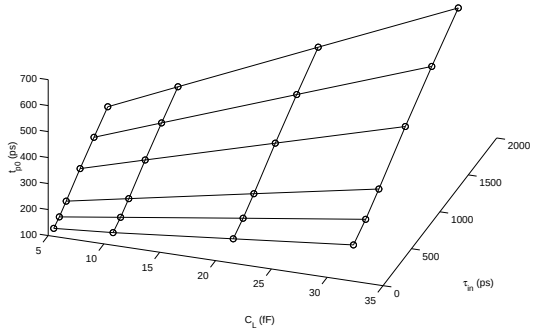


(a)



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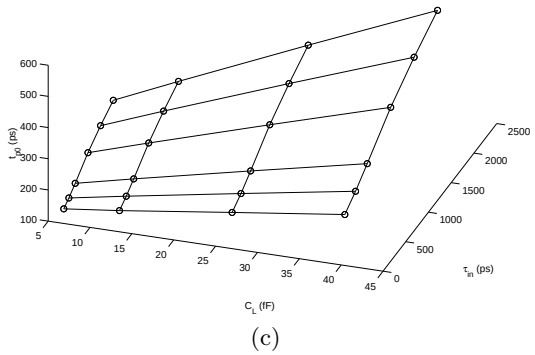

(c)

Fig. 1. HSPICE-grids for: (a) INV 1-R, (b) NAND2 2-R, and (c) NOR2 1-F

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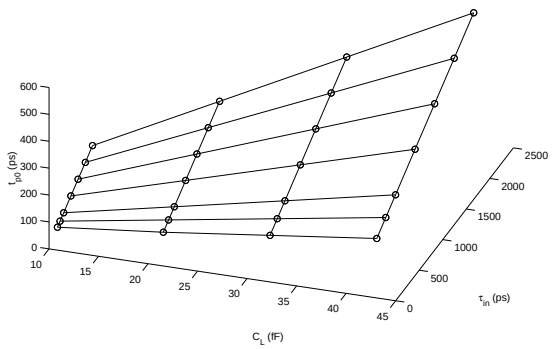
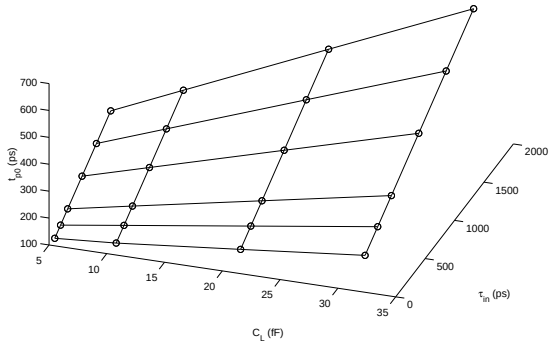


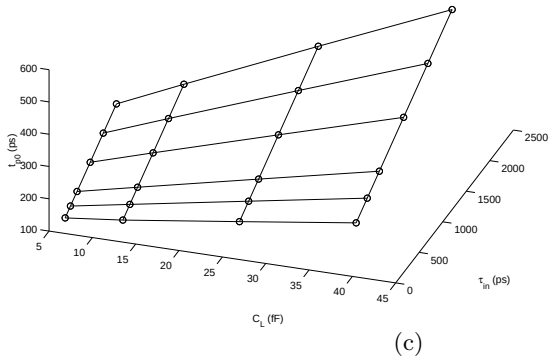
$D = 4.27$
$E = 0.180$
$F = 30.0$

(a)



$D = 4.16$
$E = 0.213$
$F = 93.1$

(b)



$D = 3.61$
$E = 0.135$
$F = 114.9$

(c)

Fig. 2. Grids obtained with (5) applying multiple linear regression to HSPICE data for: (a) INV 1-R, (b) NAND2 2-R, and (c) NOR2 1-F

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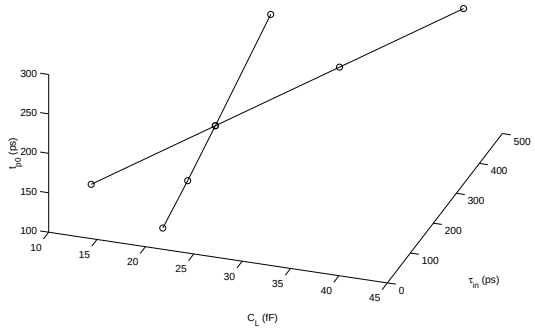
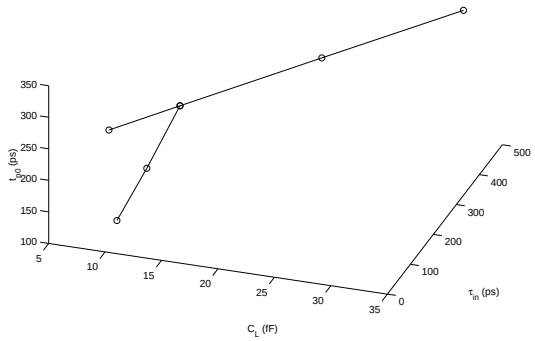


(a)



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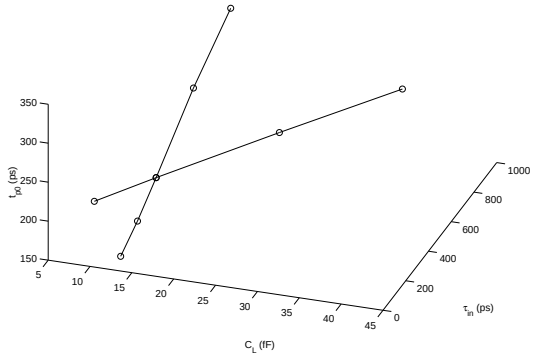

(c)

Fig. 3. Points obtained with AUTODDM for: (a) INV 1-R, (b) NAND2 2-R, and (c) NOR2 1-F

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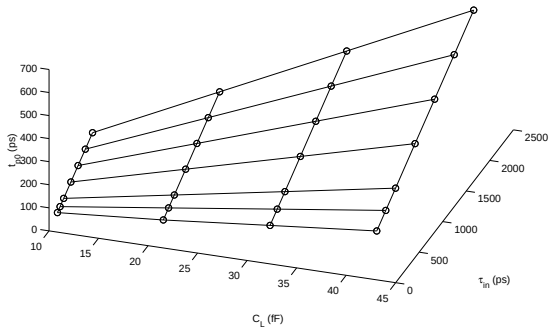
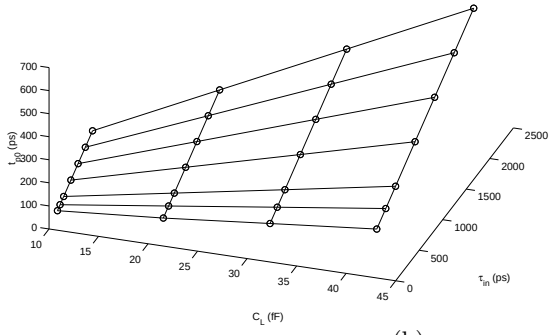


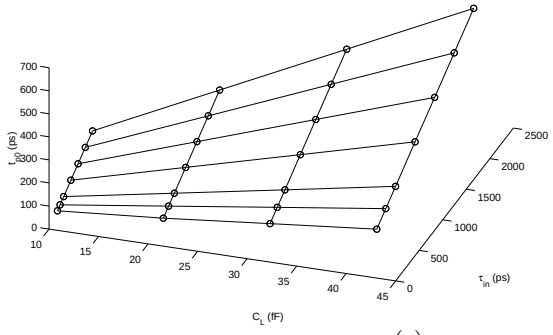
$D = 4.03$
$E = 0.200$
$F = 30.9$

(a)



$D = 4.25$
$E = 0.193$
$F = 95.0$

(b)



$D = 3.51$
$E = 0.144$
$F = 113.6$

(c)

Fig. 4. Grids obtained with (5) applying multiple linear regression to AUTODDM data for: (a) INV 1-R, (b) NAND2 2-R, and (c) NOR2 1-F

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Table 1. Characterization of normal propagation delay parameters using HSPICE data

Gate	Case	D (ps/fF)	E	F (ps)	$\overline{err}$ (ps)	$\overline{dev}$ (%)
INV	1-R	4.27	0.180	30.0	4.6	1.74
INV	1-F	3.57	0.100	31.5	6.8	3.75
NAND2	1-R	4.21	0.202	55.4	2.2	1.03
NAND2	2-R	4.16	0.213	93.1	3.0	1.20
NAND2	1-F	2.77	0.083	42.4	3.9	3.27
NAND2	2-F	2.75	0.019	61.1	3.8	3.34
NOR2	1-R	4.07	0.087	99.7	3.8	1.63
NOR2	2-R	3.95	0.160	43.9	2.6	1.24
NOR2	1-F	3.61	0.135	114.9	4.8	1.58
NOR2	2-F	3.47	0.125	59.7	4.6	2.29

same cases contemplated in table 1. The error values shown in this second table have been calculated in reference to the HSPICE-grid.

So, on the one hand, the use of this simple heuristic model allows us to include the whole calculus into AUTODDM without affecting the total simulation time needed to characterize a standard cell. On the other hand, these data allow us to obtain practically the same values for the parameters D, E, and F, and to keep the mean deviation under 4%.

Table 2. Characterization of normal propagation parameters using AUTODDM data

Gate	Case	D (ps/fF)	E	F (ps)	$\overline{err}$ (ps)	$\overline{dev}$ (%)
INV	1-R	4.03	0.200	30.9	8.0	2.47
INV	1-F	3.53	0.109	31.3	7.4	3.89
NAND2	1-R	4.22	0.188	57.0	5.2	1.90
NAND2	2-R	4.25	0.193	95.0	9.8	2.72
NAND2	1-F	2.88	0.078	42.7	4.1	3.57
NAND2	2-F	2.86	0.014	62.1	3.9	3.47
NOR2	1-R	3.97	0.103	99.1	7.8	2.87
NOR2	2-R	3.89	0.167	43.6	2.7	1.15
NOR2	1-F	3.51	0.144	113.6	5.2	1.60
NOR2	2-F	3.53	0.120	61.1	4.9	2.59

5 Conclusions

Characterizing the DDM completely also implies the characterization of the normal propagation delay (t_{p0}), and the value of t_{p0} depends on both C_L and τ_{in}. This paper presents the analysis we have carried out about the value of t_{p0} in a 0.35 μm CMOS technology. In this way, we have proposed a simple heuristic

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model for t_{p0} that includes its dependence on the output load (C_L) and the input transition time (τ_{in}). Despite its simplicity, the model is accurate enough in the range of interest. Also, we have presented a characterization process for this model that is fully integrated into AUTODDM without affecting the total simulation time needed to characterize a standard cell. Finally, we have tested this model and found that its mean deviation is, for all cases, lower than 4%.

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