KEY FRONT-END CIRCUITS IN MILLIMETER-WAVE SILICON-BASED WIRELESS TRANSMITTERS FOR PHASED-ARRAY APPLICATIONS

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[To the students of the Georgia Institute of Technology]

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I want to thank my advisor, Dr. Hua Wang, for providing feedback and brainstorm throughout my works in my Ph.D. career. It is also my pleasure to join one of the best labs in the RF/millimeter-wave integrated circuit field in the world, including cutting-edge equipment and intelligent people. I truly appreciate my family for their unlimited support; I cannot obtain my Ph.D. degree without them.

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SUMMARY

Millimeter-wave (mm-Wave) phased arrays have been widely used in numerous wireless systems to perform beam forming and spatial filtering that can enhance the equivalent isotropically radiated power (EIRP) for the transmitter (TX). As well as it can minimize the interferences and further increase signal-to-noise ratio (SNR) for the receiver (RX). Regarding the existing phased-array architectures, an mm-Wave transmitter includes several building blocks to perform the desired delivered power and phases for wireless communication.

Power amplifier (PA) is the most important building block. It needs to offer several advantages, e.g., high efficiency, broadband operation and high linearity. With the recent escalation of interest in 5G wireless communication technologies, mm-Wave transceivers at the 5G frequency bands (e.g., 28 GHz, 37 GHz, 39 GHz, and 60 GHz) have become an important topic in both academia and industry. Thus, PA design is a critical obstacle due to the challenges associated with implementing wideband, highly efficient and highly linear PAs at mm-Wave frequencies. However, there exists several fundamental challenges for mm-Wave PA in silicon due to the lower transistor cut-off frequency (f_{max}) compared to compound III-V processes, lower breakdown voltage and lossy silicon substrate, which causes high design complexity and difficulty. In this dissertation, we present several PA design innovations to address the aforementioned challenges.

Additionally, phase shifter (PS) also plays a key role in a phased-array system, since it governs the beam forming quality and steering capabilities. A high-performance phase

shifter should achieve a low insertion loss, a wide phase shifting range, dense phase shift angles, and good input/output matching.

For PA design, first, an mm-Wave continuous-mode harmonically-tuned PA is proposed to provide an instantaneously broadband operation, high PA efficiency and an ultra-compact size at 28.5GHz. Based on the harmonically-tuned technique, a continuous-mode Class-F^{-1} PA can be realized and present a power-added efficiency and saturated power (P_{sat}). Moreover, we combine both continuous-mode Class-F and Class-F^{-1} PA operation to realize a continuous-mode hybrid Class-F/F^{-1} PA to provide a broader operation bandwidth and also maintain high PA efficiency. Importantly, these continuous-mode harmonically-tuned operation delivers output power and drain efficiency equivalent to that of the standard narrow band Class-F and Class-F^{-1} PA operations.

Secondly, an mm-Wave PA with a power combiner-type N-/P-MOS amplitude-to-phase (AM-PM) distortion cancellation scheme is proposed to provide a <1° AM-PM distortion and maintain high PAE at V-band range. Although multiple AM-PM distortion cancellation schemes have been reported, they usually require additional elements or circuits. However, elements or circuits induce extra losses to downgrade the PA performance even they maintain high PA linearity. Our proposed technique not only improve PA linearity but provide high PAE.

For phase shifter design, we present an mm-Wave fully differential transformer-based passive reflection-type phase shifter (RTPS) capable of performing full span 360° continuous phase shift from 58 to 64 GHz. It consists of two transformer-based 90° couplers and two transformer-based multi-resonance reflective loads to provide 360° phase

shift with low loss and ultra-compact chip size. Our proof-of-concept design is implemented in a standard 130-nm BiCMOS process with a core area of 480μm×340μm. It achieves a wide phase shifting range of 367° and a low insertion loss IL (3.7dB<|IL|<10.2dB) at62 GHz and maintains a full span 360° phase shifting range from58 to 64 GHz. Moreover, it supports360° phase shifting with a constant IL, i.e., |IL|=10, 11, 12 dB, at an IL variation of less than 0.74 dB at 62 GHz. To the best of our knowledge, this design achieves a first-ever full span 360° phase shifting (up to 367°),the lowest IL, the smallest IL variation, and the best figure-of-merit of 37.1°/dB among reported 60 GHz fully integrated RTPS in silicon.

CHAPTER 1. INTRODUCTION

With the rapid growth of the fifth generation (5G) communication, multiple non-contiguous millimeter-wave (mm-Wave) frequency bands (e.g., 24, 28, 37 and 39 GHz) are being allocated in different countries and regions. For example, the 5G frequency spectrums are allocated as, 27.5-28.35 GHz and 37-40 GHz (USA), 24.25-27.5 GHz and 31.8-33.4 GHz (Europe), and 24.25-27.5 GHz and 37-42.5 GHz (China). The frequency bands will extend to V-band (40-75 GHz) or even higher in the future. An ultra-broadband mm-Wave TX that can cover all these potential 5G bands will enable frequency diversity and international roaming as well as supporting wideband Multiple-Input-Multiple-Output (MIMO) wireless technology with ultra-compact elements by eliminating the need for assembling several single-band TXs. Thus, regarding future commercial the 5G products, it can release design difficulty and save manufacture cost significantly for targeting multiple frequency bands.

PA plays a crucial role in TX for mobile devices since it consumes a majority of the DC power, shortening usage/standby times and transmitting ranges. Thus, the efficiency of a mm-Wave PA is the key metric to perform. Additionally, 5G mm-Wave systems are expected to support wideband spectrum-efficient complex modulation schemes (e.g., 64- and 256-QAM) to achieve Gb/s link throughput revolution. These complex modulation schemes, however, often come with high-density constellations that demand stringent linearity to provide higher spectral efficiency, i.e. large-signal AM-AM and AM-PM distortion, on the PAs. Thus, the 5G communication system can support large and fragmented spectrum, dynamic spectrum access, and short packet transmissions with

loose synchronization requirements. Therefore, in order to support future wideband MIMOs, desired mm-Wave silicon-based PA solutions should offer wide carrier bandwidth for multiple the future 5G frequency bands, high efficiency for longer usage/standby times, high linearity for complex modulation schemes, sufficient output power for required transmitting ranges, and compact size for cost reduction simultaneously [1]-[25].

Figure 1.1 shows continuous-wave (CW) performance comparisons with reported mm-Wave PAs in SiGe and CMOS process from 20 GHz to 50 GHz. According to [26], both SiGe and CMOS PAs exhibit upper performance envelopes for peak PAE vs. P_{sat}, showing "device limited regime" in the low/medium P_{sat} region determined by the intrinsic power device efficiency and "circuit/combiner limited regime" in the medium/high P_{sat} region governed by the combiner efficiency. Thus, these upper performance envelopes are big challenges for PA designers.

Figure 1.2 shows the plot of average PAE (PAE_{avg}) vs average output power (P_{avg}) for SiGe and CMOS PA in modulation with 64QAM from 20 GHz to 50 GHz. There are two major groups of P_{avg}, e.g., P_{avg}=5-7dBm with PAE_{avg}=~10% and P_{avg}=9-11dBm PAE_{avg}=~10-20% respectively. Note that this plot does not distinguish modulation speeds (i.e., data-rate or symbol-rate) of the reported PA designs. For future 5G wireless communication, the proposed data-rate is at least 0.8 Gb/s at mm-Wave frequency bands.

Basic linear PAs, e.g., Class-A and Class-AB PAs, offer design simplicity and good linearity [27]-[31]. However, their simple "all-short" output harmonic terminations fundamentally limit the peak efficiency. On other hand, mm-Wave time-domain switching

PAs, e.g., Class-E PAs, show high peak efficiency but limited linearity [27][28][32]-[34]. They cannot support complex modulations without major digital pre-distortion (DPD) computation, while DPD at Gb/s usually requires substantial power and complexity for future 5G communication. To solve this classic efficiency-linearity challenge, there are multiple reported advanced PA architectures, such as Doherty PAs [7][31] and Outphasing PAs [2][27]. They can boost the back-off efficiency and maintain high linearity for mm-Wave 5G applications. However, the former often requires large area, while the latter also demand extensive DPD to increase design and implementation complexity.

According to the reported PA design recently, a promising alternative solution is the overdriven linear PAs with harmonically-tuned impedance terminations to address the classic efficiency-linearity challenge. Multiple recent designs show that Class-AB, Class-J, Class-F and inverse Class-F (Class-F^{-1}) harmonically-tuned terminations on linear PAs can boost their peak efficiency and still preserve high linearity. The reported harmonically-tuned terminations usually consist manifold L-C resonant tanks to provide the desired harmonic impedances. However, these designs either have limited bandwidth due to narrowband harmonic terminations, require area-consuming passive networks, constraining their use in broadband MIMO systems, or increase design and implementation complexity [35]-[39]. To address these PA issues, we present continuous-mode harmonically-tuned PA to achieve wide bandwidth, high efficiency and compact form-factor together, offering future 5G PA solutions. Moreover, we proposed a V-band PA employing our NMOS/PMOS AM-PM distortion cancellation technique to further improve the linearity. Also, this PA design includes a series-parallel distributed-active transformer (DAT), performing low loss and proving the PA optimal load.

The applications of mm-Wave phased array systems include ultra-high data-rate transmission, emerging 5G communication, and radar and imaging systems [127]-[141]. Phase shifters (PS) play a key role in a phased array system, since it governs the beam forming quality and steering capabilities. A high-performance phase shifter should achieve a low insertion loss (IL), a wide phase shifting range, dense phase shift angles, and good input/output matching. We present a millimeter-wave fully differential transformer-based passive reflection-type phase shifter (RTPS) capable of performing full span 360° continuous phase shift from 58GHz to 64GHz.

Taking full advantages of the increasing transistor speed, my Ph.D. research focuses on exploring new silicon-based PA topologies and circuit techniques to achieve state-of-the-art performance for various emerging applications at mm-Wave. Through my Ph.D. career at Georgia Tech GEMS Lab, I did research on the design challenges in mm-Wave PA, and devoted my research efforts in implementing energy efficient, broadband and high linearity using advanced silicon technologies. The major contributions of my dissertation are listed below.

1. We propose a mm-Wave silicon-based harmonically-tuned PA designs by using continuous-mode Class-F^{-1} and continuous-mode hybrid Class-F/F^{-1} PA operations at 5G bands.

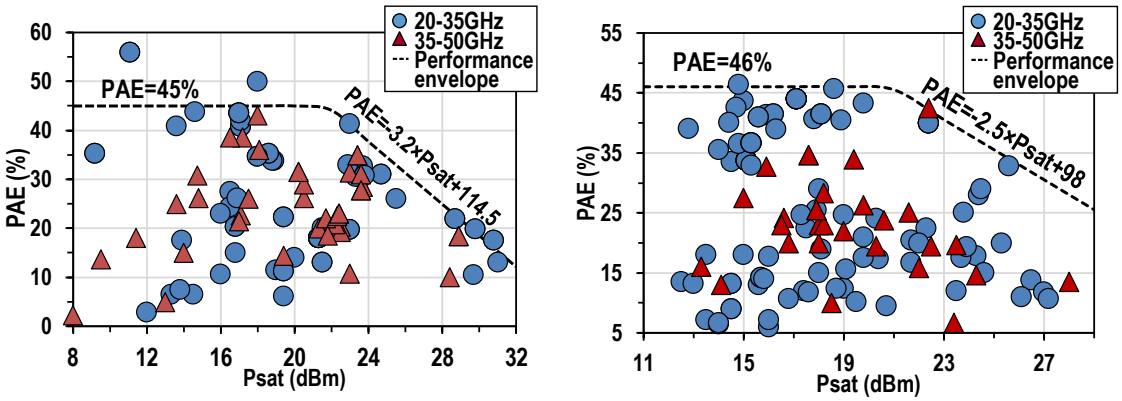
2. We propose a mm-Wave silicon-based V-band PA with the proposed N-/P-MOS AM-PM distortion cancellation scheme to achieve <1º AM-PM distortion and PAE of 35%.

3. We propose a millimeter-wave fully differential transformer-based passive

reflection-type phase shifter which performs full span 360° continuous phase shift from 58GHz to 64GHz with low insertion loss or constant insertion loss.

The remainder of this dissertation is organized as follows.

In this dissertation, the design details of the mm-Wave silicon-based harmonically-tuned Continuous-mode PA designs are discussed in Chapter 2. The proposed power-combining-based NMOS/PMOS AM-PM distortion cancellation scheme are demonstrated in Chapter 3. Later, Chapter 4 shows the design and implementation of the proposed RTPS. Finally, Chapter 5 summarizes this dissertation.



(a) **(b)**

Figure 1.1 – PAE comparison with state-of-the-art mm-Wave silicon-based PAs in (a) SiGe and (b) CMOS process (20-50 GHz) [26].

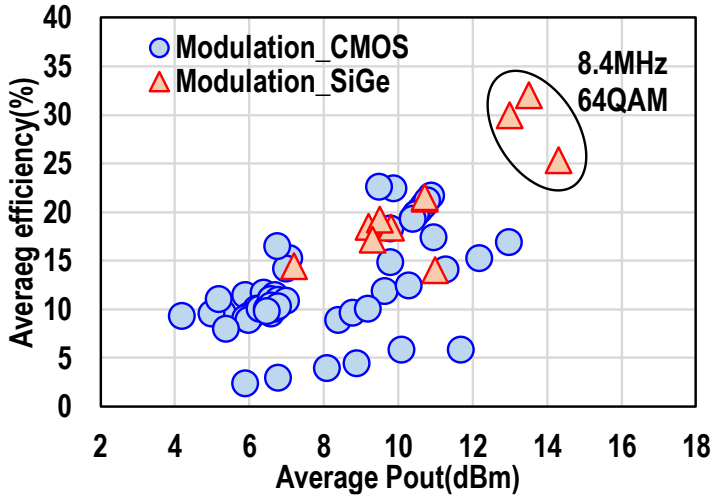


Figure 1.2 – Average Efficiency vs Average Output Power for SiGe and CMOS PAs in modulation with 64QAM (20-50 GHz) [26].

CHAPTER 2. HARMONICALLY-TUNED PA OPERATION

The basic continuous-mode PA operation and our proposed continuous-mode harmonically-tuned are discussed in this chapter. The implementation and measurement results are also presented.

2.1. Introduction

The device output voltage and current waveforms are essential for optimizing the device-level PA performance, e.g., output power, efficiency, or linearity. A harmonically-tuned PA with finite harmonic terminations (e.g., only the fundamental, 2nd-, and 3rd-order harmonics) is designed to achieve high efficiency by loading the proper terminations at its fundamental and harmonic frequencies. In the time domain, proper harmonic terminations shape the voltage and current waveforms on the power transistor drain/collector terminal to minimize the overlap between the current and voltage, boosting the efficiency. In practice, higher order harmonics (>3rd-order) provide limited contributions and are difficult to generate and terminate [40]-[46].

2.1.1. Conventional Class-F PA operation

The conventional Class-F PA output network provides high impedance terminations at odd harmonics and low impedance terminations at even harmonics [40]. Thus, the voltage waveform v_F on drain/collector terminal behaves as a square waveform and can be expressed (including DC-/1st-/3rd-term) as

$$v_F(\theta) = V_{DC} - v_{F1}\cos\theta + v_{F3}\cos 3\theta, \tag{2-1}$$

$$v_{F1}/V_{DC} = 2/\sqrt{3}, v_{F3}/V_{DC} = 1/3\sqrt{3},$$

where V_{DC} represents the dc supply voltage, and $V_{F,1}$ and $V_{F,3}$ are the voltage swing at fundamental and 3rd-harmonic frequencies respectively. Furthermore, the device current behaves as a half-sine waveform (including DC/1st/2nd term) as

$$i_F(\theta) = I_{DC} + i_{F,1}\cos\theta + i_{F,2}\cos 2\theta, \tag{2-2}$$

$$i_{F,1}/I_{DC} = \pi/2, i_{F,2}/I_{DC} = 2/3,$$

where I_{DC} is the DC current, and $I_{F,1}$ and $I_{F,2}$ are the current swing at fundamental and 2nd-harmonic frequencies, respectively. The normalized time-domain current and voltage waveforms are shown in Figure 2.1 (i.e., the blue solid line represents the voltage and the red solid line represents current).

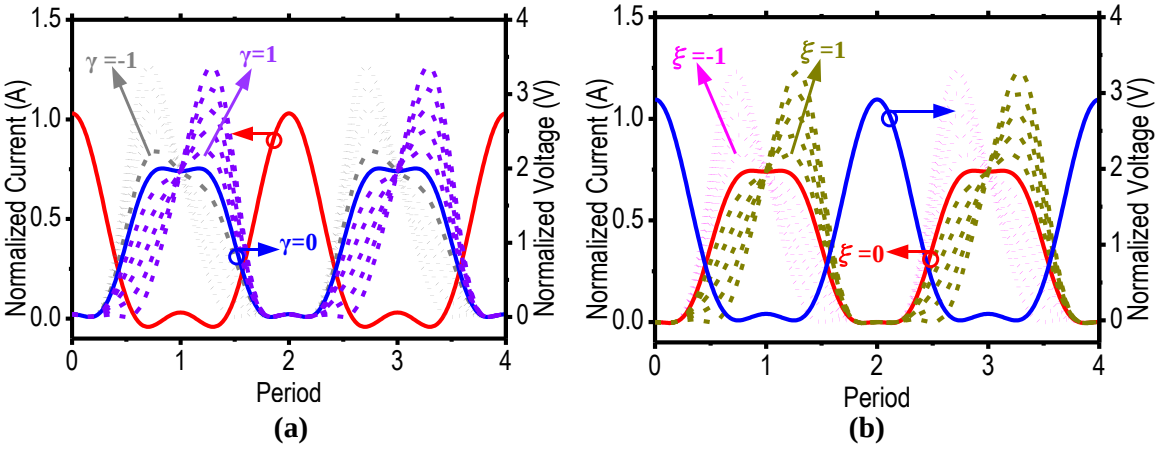


Figure 2.1 – Theoretical current and voltage waveforms composed of the fundamental, 2nd- and 3rd-harmonics for (a) conventional/continuous-mode Class-F and (b) conventional/continuous-mode Class-F^{-1} operations.

2.1.2. Conventional Class-F^{-1} PA operation

The conventional Class-F^{-1} PA is a dual of the Class-F PA by exchanging the current and voltage waveforms. Namely, the conventional Class-F^{-1} PA generates a half-sinusoidal voltage waveform and a square current waveform with high impedance for even order harmonic output impedance and low impedance for odd order harmonic output impedance. The voltage waveform v_{IF} can be written as

$$v_{IF}(\theta) = V_{DC} + v_{IF,1}\cos\theta + v_{IF,2}\cos 2\theta, \tag{2-3}$$

$$v_{IF,1}/V_{DC} = \sqrt{2}, v_{IF,2}/V_{DC} = 1/2,$$

where $V_{IF,1}$ and $V_{IF,2}$ are the voltage swing at fundamental and 3rd-order harmonic frequencies, respectively. Thus, the current on a transistor behaves as a square waveform and it can be expressed as

$$i_{IF}(\theta) = I_{DC} - i_{IF,1}\cos\theta + i_{IF,3}\cos 3\theta \tag{2-4}$$

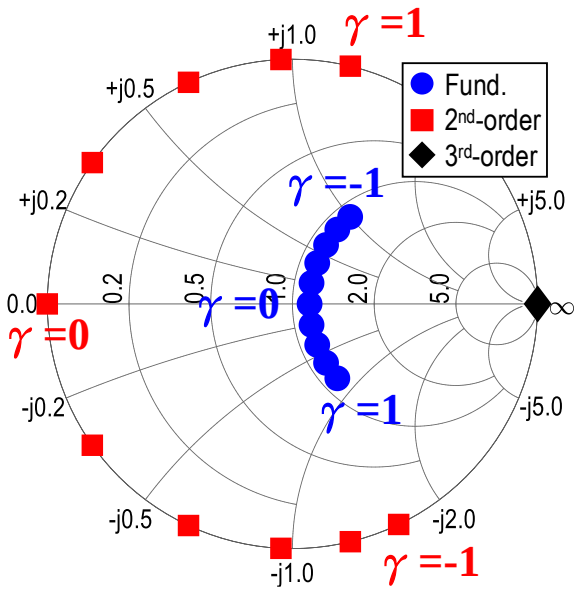
$$i_{IF,1}/I_{DC} = 1.162, i_{IF,3}/I_{DC} = 0.162,$$

where $I_{IF,1}$ and $I_{IF,3}$ are the current swing at fundamental and 3rd-order harmonic frequencies, respectively [44]. The normalized time-domain current and voltage waveforms are shown in Figure 2.1(b) (i.e., the blue solid line represents voltage and the red solid line represents current respectively).

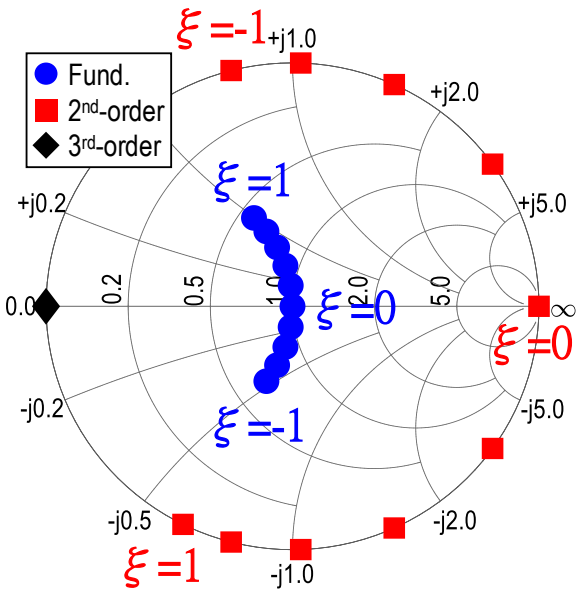
Moreover, the PA efficiency η, (i.e., drain efficiency for MOSFET and collector for Bipolar) can be expressed as,

$$\eta = \frac{P_{delivery}}{P_{DC}} = \frac{1}{2}\left(\frac{v_{F,1} \text{ or } v_{IF,1}}{V_{DD}}\right)\left(\frac{i_{F,1} \text{or } i_{IF,1}}{I_{DC}}\right) = \eta_{\max}\left(1 - \frac{V_k}{V_{DC}}\right), \quad (2\text{-}5)$$

where $\eta_{\max}$ represents the maximum PA efficiency, V_k is the knee voltage which represents a minimum limit on the swing across the transistor. An ideal Class-F PA with fundamental, 2nd-and 3rd- harmonics can achieve an $\eta_{\max}$ of 90.6 % while a Class F^{-1} PA can achieve an $\eta_{\max}$ of 81.6 %, respectively [27]. To maintain high PA efficiency, conventional Class-F and Class-F^{-1} PA output networks need to provide multiple accurate harmonic impedance terminations, resulting in narrow carrier bandwidths [27][37][38].



(a)



(b)

Figure 2.2 – Fundamental, 2nd- and 3rd-harmonic load impedances for (a) continuous-mode Class-F and (b) continuous-mode Class-F^{-1} PA operations.

2.1.3. Continuous-mode Class-F and Class-F^{-1} PA

Continuous-mode harmonically tuned PAs generalize the optimum harmonic termination conditions and thus substantially expand the carrier frequency range. In reference [41], the author introduces a continuous-mode PA, alleviating the precise harmonic requirements of the conventional ones by offering multiple impedance terminations that can be dynamically distributed over the desired operation bandwidth, while preserving the desired output power and efficiency. Given by [41], for the continuous-mode Class-F PA operation, the voltage waveform in (2-1) is extended by multiplying an additional defining term, shown as

$$v_{CF}(\theta) = (V_{DC} - v_{F1}\cos\theta + v_{F3}\cos 3\theta) \times (1 - \gamma \sin\theta). \tag{2-6}$$

The first bracket of (2-6) is the voltage waveform formulation for the conventional Class-F as expressed in (2-1) with γ=0. The last bracket in (6) is a defining term ($1-\gamma\sin\theta$) that performs a new design space. Thus, the parameter γ varies between -1 and 1 (i.e., $-1 \leqq \gamma \leqq 1$), forming a family of voltage waveforms that provide multiple solutions Figure 2.2(a), gray dot lines for γ<0 and purple dash lines for γ>0) to maintain constant power and efficiency. As result, each value of corresponding to the particular PA output fundamental, 2nd- and 3rd-order harmonic impedances can be expressed as [44],

$$Z_{CF,1} = R_{opt}\frac{2}{\sqrt{3}} + j\gamma R_{opt}, Z_{CF,2} = jR_{opt}\frac{7\sqrt{3}\pi}{24}\gamma, Z_{CF,3} = \infty, \tag{2-7}$$

where R_{opt} is the optimum impedance of the standard Class-B operation with all harmonics short-circuited. The impedance trajectories can be presented on the Smith chart (Figure 2.2a).

On other hand, for the continuous-mode Class-F^{-1} PA operation, the current waveform in (2-2) can be also extended by multiplying an additional defining term, expressed as

$$i_{CIF}(\theta) = \left(I_{DC} - i_{IF,1}\cos\theta + i_{IF,3}\cos 3\theta\right) \times \left(1 - \xi \sin\theta\right). \tag{8}$$

The first bracket of (2-8) is the conventional voltage waveform formulation for the conventional Class-F^{-1} operation as expressed in (2-2) with ξ=0. The last bracket of (2-8) is also a defining term ($1-\xi\sin\theta$), offering a new design space. The parameter ξ varies between -1 and 1 (i.e., $-1 \leqq \xi \leqq 1$), forming a family of current waveforms that provide multiple solutions Figure 2.2(b), magenta dot lines for $\xi<0$ and dark-yellow dash lines for $\xi>0$) to maintain constant delivery power and efficiency. Each value of corresponding to the continuous-mode PA output fundamental, 2nd-order and 3rd-order harmonic impedances can be expressed as the following [44],

$$Y_{CIF,1} = G_{opt}\sqrt{2}i_{IF,1} + jG_{opt}\sqrt{2}i_{DC}\xi, \tag{9}$$

$$Y_{CIF,2} = jG_{opt}2\left(i_{IF,1} + i_{IF,3}\right)\xi,\ Y_{CIF,3} = \infty,$$

where G_{opt} (=$1/R_{opt}$) is as the optimum admittance. The impedance trajectories can be shown on the Smith chart (Figure 2.2b). These continuous-mode PA operations can be realized over the desired operation bandwidth by applying the required harmonic

impedances for the different γ or ξ values. Additionally, these continuous-mode PAs can deliver output power and efficiency almost equivalent to that of the conventional PAs [41]-[44].

The PA load impeance (e.g., Z_L) behaviours for different PA operation are summarized in Table II. It is obvious that the coninuoious-mode PA operaion (i.e., $\gamma \neq 0$ and $\xi \neq 0$.) causes fundamental impedance (e.g., Capacitive/Inductive or Inductive/Capacitive) and 2nd-harmonic impedance (e.g., Inductive/Capacitive or Capacitive/Inductive) out of phase. The 3rd-harmonic impedances stay high or low.

Table 2.1 – PA Load Impedance Behaviors for Different Operations

Operation		Fundamental Impedance		2nd harmonic Impedance		3rd harmonic Impedance	
		$\|Z_L\|$	Z_L	$\|Z_L\|$	Z_L	$\|Z_L\|$	Z_L
Class-F	$\gamma=0$	$R_{opt,F}$	0	Low	0	High	0
Class-F^{-1}	$\xi=0$	$R_{opt,IF}$	0	High	0	Low	0
Continuous-Class-F	$\gamma>0$	$R_{opt,F}$	Capacitive	Low	Inductive	High	either
	$\gamma<0$	$R_{opt,F}$	Inductive	Low	Capacitive		
Continuous-Class-F^{-1}	$\xi>0$	$R_{opt,IF}$	Inductive	High	Capacitive	Low	either
	$\xi<0$	$R_{opt,IF}$	Capacitive	High	Inductive		

2.1.4. Proposed Continuous-mode PA Output Network

Most existing continuous-mode and harmonically-tuned PA output networks require multiple passive components and transmission lines for multi-resonance tuning, inevitably increasing the network complexity, losses, and size. Our PA output network exploits and uses parasitic elements in one on-chip transformer to achieve continuous-mode harmonic tuning at both differentials- and common-mode with substantial network simplification and area-saving (Figure 2.3).

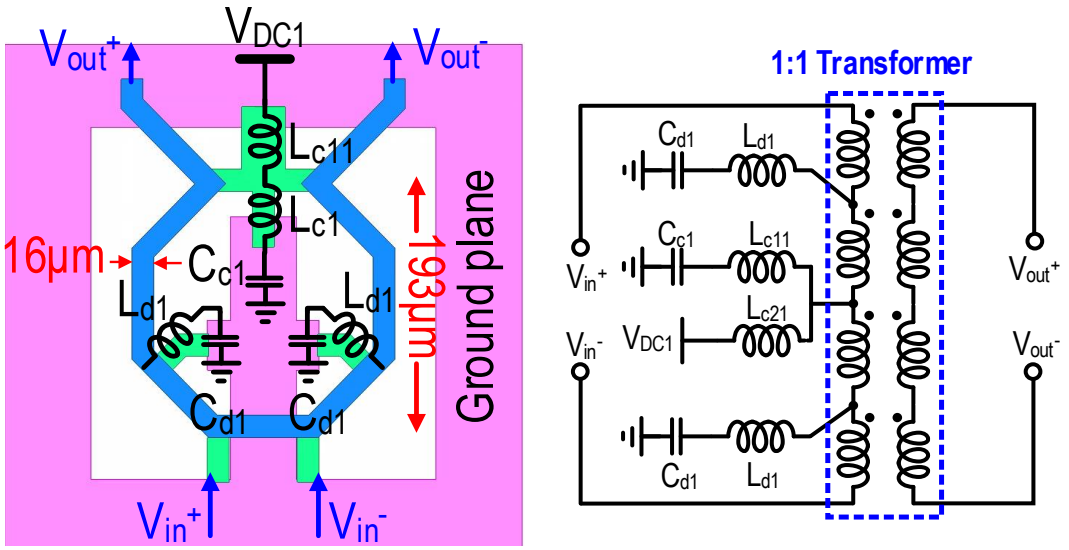
2.2.1. Continuous-Mode Class-F^{-1} PA Output Network

The proposed differential continuous-mode Class-F^{-1} PA output network is as shown in Figure 2.3(a). It consists of one 1:1 transformer and three harmonic tuning capacitors ($2\times C_{d1}$ and C_{c1}). This structure utilizes two symmetrically embedded branches L_{d1} inside the transformer for the 3rd-order harmonic impedance tuning in differential-mode, and two extended branches L_{c1} and L_{c11} for the 2nd-order harmonic impedance tuning in common-mode respectively. Figure 2.4 shows the simplified differential and common-mode half-circuits at the fundamental, 2nd- and 3rd-order harmonic frequencies respectively. L_{dm1}/L_{cm1} and L_{dm2}/L_{cm2} are the differential/common-mode half-circuit inductances of the transformer, and the output leads are absorbed into the transformer secondary coil (Figure 2.4a-b). Moreover, L_{m1} and L_{k1} are the magnetizing and leakage inductances of the transformer in the differential-mode half-circuit (Figure 2.4d).

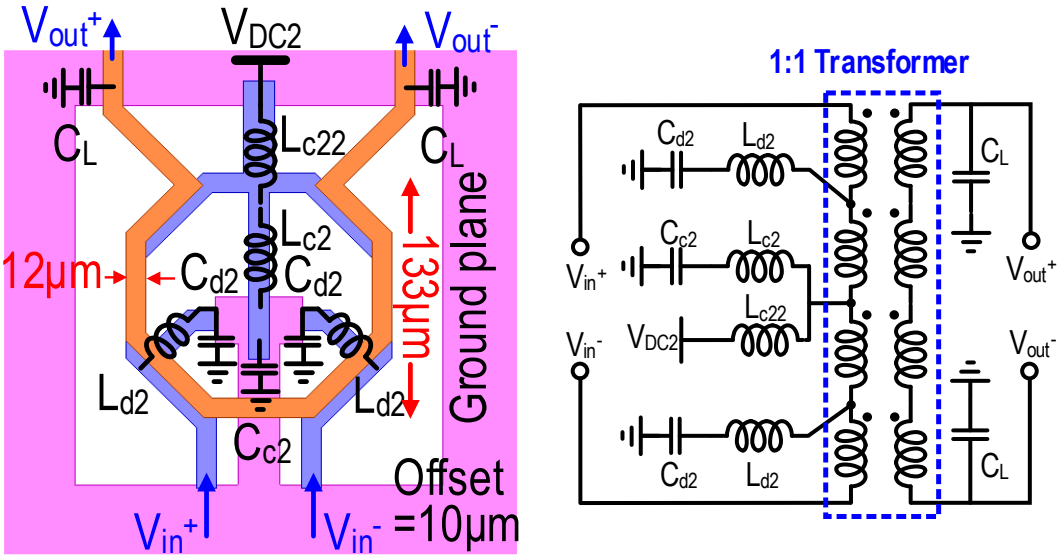
In the differential mode, the center-tap of the transformer is virtual ground, so L_{c1}/L_{c11} and C_{c1} do not affect the fundamental and 3rd-order harmonic impedances. C_{d1}-L_{d1}-L_{dm2}

form a multi-resonance tank Z_1 with high-frequency resonance. At the fundamental frequency, the series network C_{d1}-L_{d1} behaves like a small capacitor, resulting in a high impedance to the transformer. Thus, the transformer performs matching with the PA output capacitance C_{out} and provides the desired fundamental load impedance to the PA (Figure 2.4c). At the 3rd-order harmonic frequency, C_{d1}-L_{d1} is slightly below its series resonance, which shorts out L_{dm2} and forms a series resonance of C_{d1}-L_{d1}-L_{m1}-L_{k1} to provide a desired low impedance. In the common-mode half-circuit, the network of $C_{c1}/2$, $2\times L_{c1}$, and $2\times L_{c11}$ forms a multi-resonance tank Z_2 (Figure 2.4b). At the 2nd-order harmonic frequency, Z_2 provides a high impedance, resulting in the remaining series tank of C_{d1}-L_{d1} as a capacitor. Thus, the 2nd-order harmonic impedance is dominated by C_{out}, L_{cm1} and the effective capacitance due to series C_{d1}-L_{d1}, which achieve desired 2nd-order harmonic impedance (Figure 2.4e).

The trajectories of half-circuit load impedance at fundamental, 2nd- and 3rd-order harmonics with the PA output capacitance C_{out} are shown on the Smith Chart in Figure 2.5. The fundamental load impedance is mostly inductive for lower frequency ($0\leq\xi\leq1$) and capacitive for higher frequency ($-1\leq\xi\leq0$), and vice versa for the 2nd-order harmonic impedance. The fundamental and the 2nd-order harmonic impedances of the upper operation bandwidth follow the constant conductance circles, while the 3rd-order-harmonic impedance is kept low. These aspects verify that the PA achieves continuous-mode Class-F^{-1} harmonic terminations for its fundamental, 2nd-, and 3rd-order impedances [41]-[44].



(a)



(b)

Figure 2.3 – EM and schematic of (a) continuous-mode Class-F^{-1} PA and (b) continuous-mode hybrid Class-F/-F^{-1} PA.

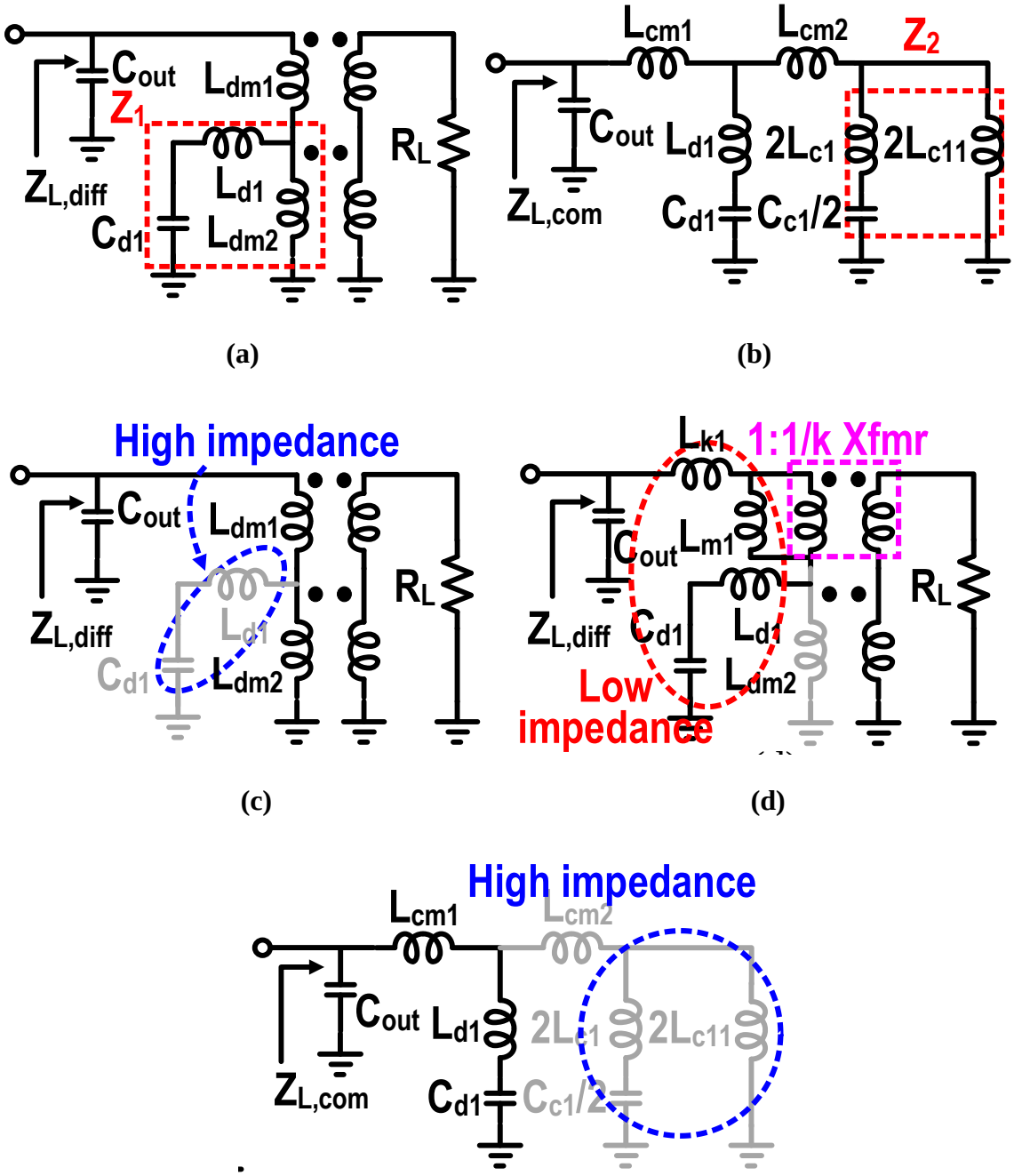


Figure 2.4 – Simplified of (a) differential-mode and (b) common-mode half circuits of the continuous-mode Class-F^{-1} PA output network at (c) the fundamental frequency (d) the 3rd-harmonic of lower band, and (e) the 2nd-harmonic frequencies, respectively.

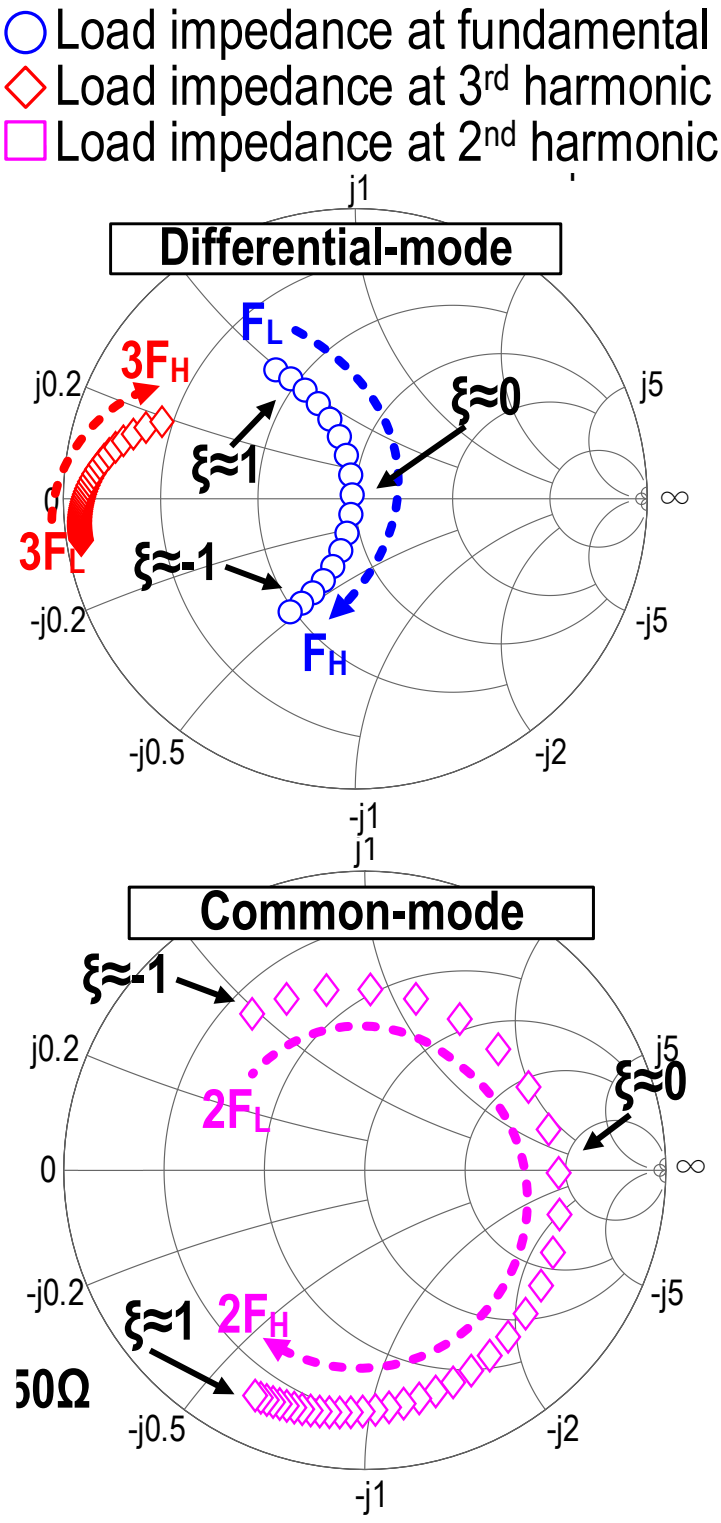


Figure 2.5 – Trajectories of the half-circuit load impedance at fundamental, 2nd- and 3rd-order harmonic frequencies (characteristic impedance Z_0 =50Ω).

2.2.2. *Continuous-mode Hybrid Class-F/F^{-1} PA Output Network*

This continuous-mode hybrid Class-F/F^{-1} PA output network combines continuous-mode hybrid Class-F and F^{-1} PA operations together to further extend the bandwidth. Compared to the continuous-mode Class-F^{-1} PA output network, the two matching capacitors (i.e., $2\times C_L$) can facilitate the fundamental operation bandwidth extension, and the longer branches L_{c2} can provide a larger inductance for 2nd-order harmonic impedance, as shown in Figure 2.3(b). It also consists of one 1:1 transformer, three harmonic tuning capacitors (i.e., $2\times C_{d2}$ and C_{c2}), and two matching capacitors (i.e., $2\times C_L$) to realize hybrid Class-F and Class-F^{-1} operations at the lower (ω_L) and higher frequency (ω_H) bands, respectively, as shown in Figure 2.3(b). The PA output harmonic termination network is explained in Figure 2.6(a)-(h). Here, L_{dm3}/L_{cm3} and L_{dm4}/L_{cm4} represent the differential-/common-mode half-circuit inductances of the transformer, and the output leads are absorbed into the secondary coil. C_{d2}-L_{d2}-L_{dm4} forms a multi-resonance tank Z_3 (Figure 2.6a). In the common-mode half-circuit, the network of C_{c2} /2, $2\times L_{c2}$, and $2\times L_{c22}$ forms a multi-resonance tank Z_4 (Figure 2.6b).

At fundamental operation frequencies ($\omega_L \leq \omega \leq \omega_H$), the series network C_{d2}-L_{d2} behaves as a small capacitor (Figure 2.6c) to provide a high impedance. So, this high impedance branch can be ignored. Thus, $Z_{L,diff}$ can be converted to a simplified model as shown in Figure 2.6(d). $k^2\times L_p$ and $(1-k^2)\times L_p$ are the magnetization and leakage inductances respectively of the transformer in the half-circuit differential-mode (Figure 2.6d). The equivalent inductance L_p is roughly equal to L_{dm3} and L_{dm4}. Thus, Figure 2.6(d) forms the

matching network with the PA output capacitance C_{out} and provides PA the desired fundamental load impedance.

At the 3rd-order harmonic of the higher band ($\omega=3\omega_H$), the series network C_{d2}-L_{d2} impedance is slightly below its series resonance, which shorts out L_{dm4} and forms a series resonance of C_{d2}-L_{d2}-L_{m3}-L_{k2} to offer a low load impedance (Figure 2.6e). In this case, L_{m2} and L_{k2} represent the magnetization and leakage inductances of coil L_{dm3} of the transformer in the half-circuit differential-mode. Also, at the 3rd-order harmonic of the lower band ($\omega=3\omega_L$), $Z_{L,diff}$ sees a high impedance by L_{dm3} and Z_3 in parallel with C_{out}. At the 2nd-order harmonic of the higher band ($\omega=2\omega_H$), Z_4 provides a high impedance, while the remaining C_{d2}-L_{d2} series tank behaves as a capacitor (Figure 2.6g). Therefore, the 2nd-order harmonic impedance $Z_{L,com}$ is dominated by C_{out}, L_{cm3} and the effective capacitance due to series C_{d2}-L_{d2} branch, achieving the desired continuous-mode 2nd-order harmonic impedance.

Additionally, at the 2nd-order harmonic of the lower band ($\omega=2\omega_L$), Z_2 becomes inductive. Moreover, the series network C_{d2}-L_{d2} remains capacitive. Therefore, $Z_{L,com}$ can present a low overall impedance. The trajectories of the half-circuit load impedance at fundamental, 2nd- and 3rd-order harmonics with the absorbed PA output capacitance C_{out} are shown on the Smith Chart in Figure 2.7(a).

The fundamental load impedance ($\omega_L\leq\omega\leq\omega_H$) is inductive, while the 2nd-order harmonic load impedances ($\omega=2\omega_L$ or $\omega=2\omega_H$) are capacitive and provide $-1\leq\gamma<0$ for continuous-mode class-F PA operation and $-1\leq\xi<0$ for continuous-mode Class-F^{-1} PA operation, respectively. Compared with the fundamental, the 3rd-oder harmonic load impedance is low for lower band ($\omega=3\omega_L$) while it is high for higher band ($\omega=3\omega_H$). The

load impedance trajectories demonstrate the continuous-mode hybrid Class-F/F^{-1} PA. The impedance responses of each harmonic over frequency are shown in Figure 2.7(b).

The design procedure of the PA output network is starting from building a 4^{th}-order matching network using passive lumped elements (e.g., inductors and capacitors) at fundamental frequency, like Figure 2.6(d). The designed values of the passive lumped elements are depended on the load-pull simulation. For the harmonic-thing, the importance is that the required lumped inductors and capacitors are necessary arranged properly in the differential and common modes to realize the 2^{nd}- and 3^{rd}-order harmonic impedance terminations for the continuous-mode operation, respectively. Here, the values of the inductors and capacitors are determined by the continuous-mode design equations, as discussed in Section II. Then, a transformer with the routing traces and pads (i.e., GSGSG pads) is to replace the lumped elements. As a result, the transformer needs to be well optimized and simulated to determine the inductances and capacitances (e.g., C_{c1}, C_{c2}, C_{d1}, C_{d2}, L_{d1}, L_{d2} and so on).

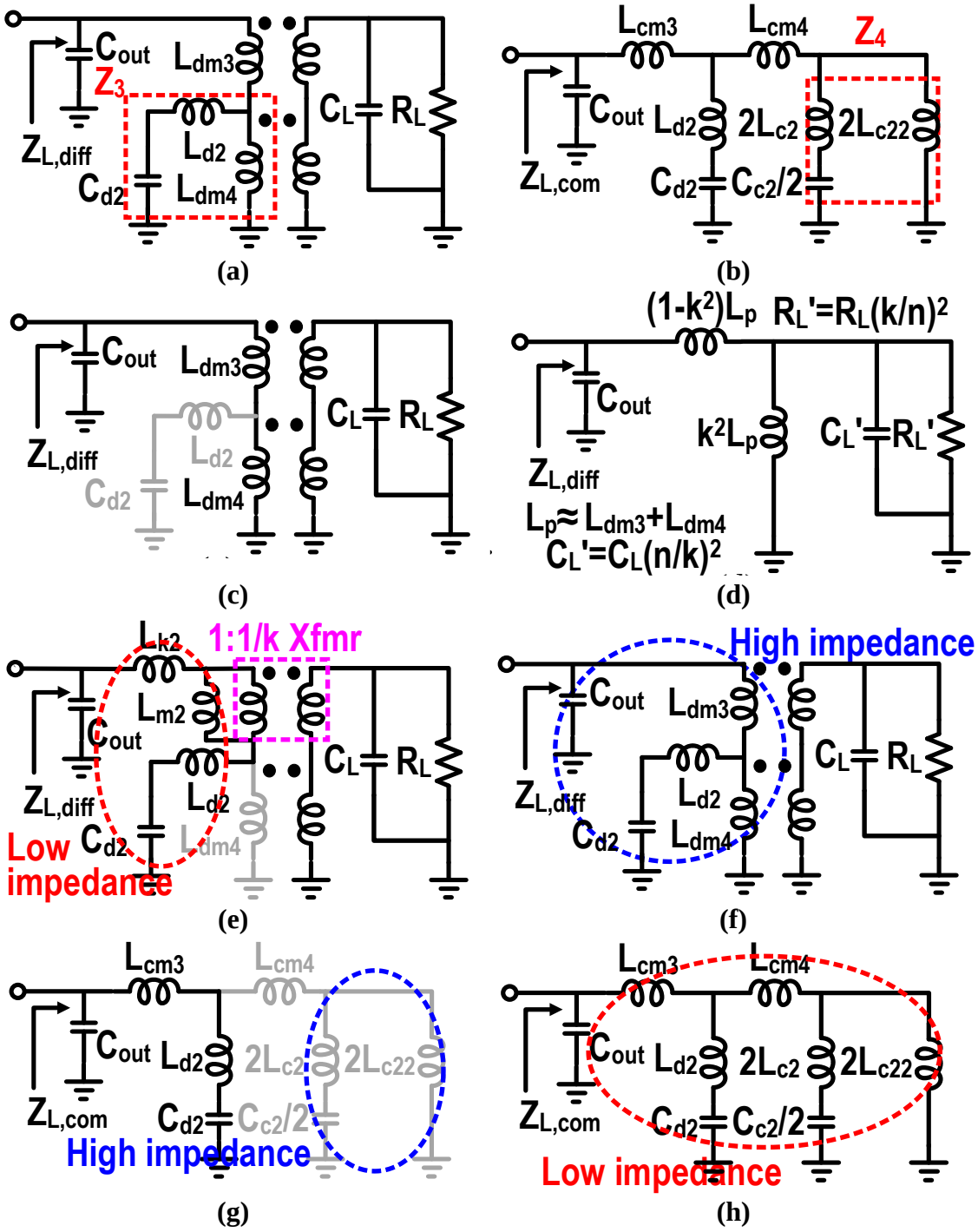
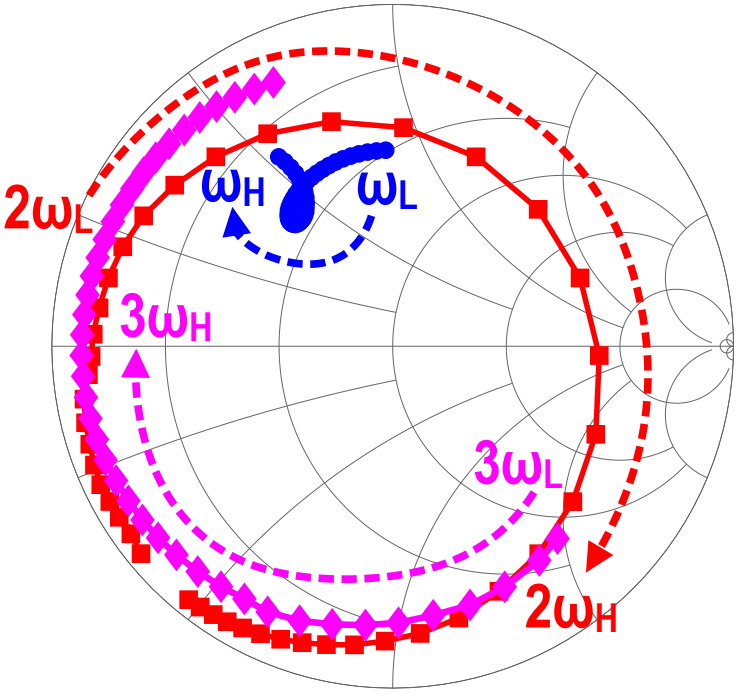
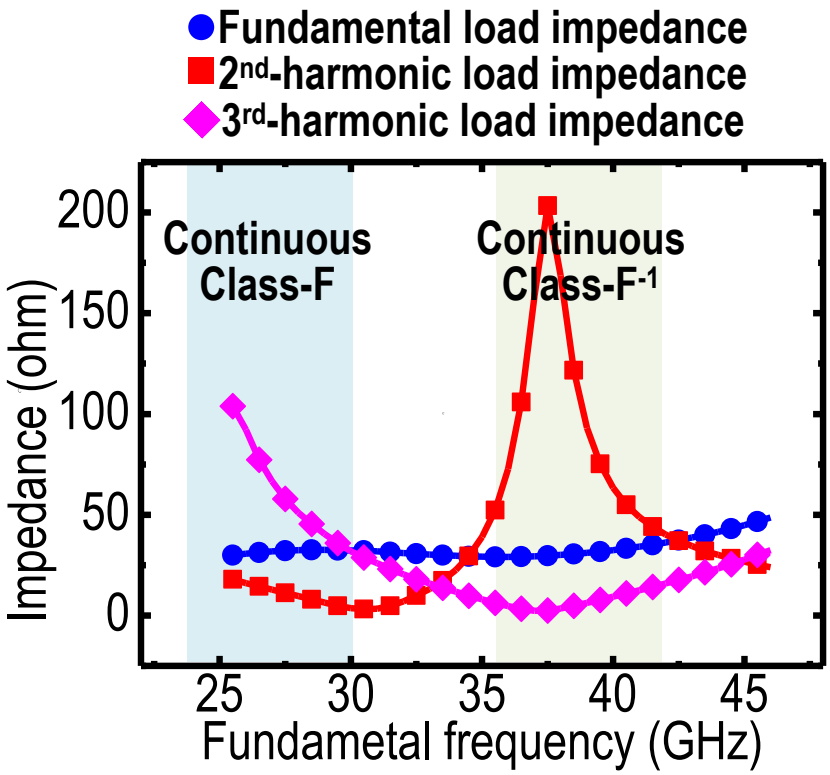


Figure 2.6 – Simplified half circuits of the (a) differential-mode, (b) common-mode of the continuous-mode hybrid Class-F/F^{-1} PA output network at (c) the fundamental frequency ($\omega_L \leqq \omega \leqq \omega_H$) and (d) the fundamental equivalent circuit, (e) the 3rd-order harmonic of lower band ($\omega=3\omega_L$), (f) the 3rd-order harmonic of higher band ($\omega=3\omega_H$), (g) the 2nd-order harmonic of lower band ($\omega=2\omega_L$), and (h) the 2nd-order harmonic of higher band ($\omega=2\omega_H$).



(a)



(b)

Figure 2.7 – (a) Trajectories of half-circuit load impedance at fundamental, 2nd-and 3rd-order harmonic frequencies (Z_0 =50Ω), and (b) impedance response.

2.1.5. Continuous-Mode Harmonically-Tuned PA Implementation

2.3.1. Design 1: A Two-Stage Continuous-mode Class-F^{-1} PA

Figure 2.8(a) shows the schematic of the two-stage continuous-mode Class-F^{-1} PA design. It is composed of a driver (DR) stage and a PA stage followed by the proposed differential transformer-based harmonically-tuned PA output network, implemented in GlobalFoundries 0.13 μm SiGe BiCMOS process. The transformer-based harmonically-tuned PA output network has been fully analyzed in the previous section. The transistor size of DR (i.e., Q_1 and Q_2) is 21 μm/120 nm and the transistor size of PA (i.e., Q_3 and Q_4) is 32 μm/120 nm, respectively. Two series input resistors R_b are 10 Ω for both DR and PA stages to improve stability. Both PA and DR stages utilize neutralization capacitors (C_{N_DR}=30 fF and C_{N_PA}=40 fF) to improve power gain, reverse isolation and stability. The input and inter-stage matching networks are realized by two 1-to-1 transformers respectively, and two input capacitors (C_{in1}=128 fF) and two inter-stage capacitors (C_{int}=55 fF). The DR stage is biased (V_{B_DR}) at 0.84 V and DC supply voltage (V_{CC_DR}) is 0.9 V, and the PA stage is biased (V_{B_PA}) at 0.83 V and DC supply voltage (V_{CC_PA}) is 1.9 V, respectively. To enhance PA linearity, a harmonic trap network (i.e., R_{s1}=R_{s11}=25 Ω and C_{s1}=C_{s11}=200 fF) is added at the PA input to provide a low 2^{nd}-order harmonic source impedance. The DC and peak current of the PA stage are 16 mA and 48 mA, respectively.

2.3.2. Design 2: A One-Stage Continuous-mode Class-F/F^{-1} PA

Figure 2.8(b) shows the schematic of the one-stage differential hybrid continuous-mode Class-F/F^{-1} PA design. It is composed of only the PA stage followed by the proposed differential transformer-based PA output network, implemented in a Globalfoundries 45nm

CMOS SOI process. The PA is realized using a cascode topology with identical sizes (W/L=6×30 μm/40 nm) for M_1, M_2, M_3, and M_4 that are biased at V_G=0.3 V, V_{cas}=1.3 V, and V_{DD}=2 V. The capacitive neutralization scheme (C_n=55 fF) is used for the bottom transistor pair (M_1/M_2). The input matching network is composed of a 1:1 transformer with parallel capacitors C_{in}=160 fF and a parallel resistor R_g=170 Ω. The DC and peak current of the PA stage is 24 mA and 65/70/68 mA at 28/37/39 GHz, respectively.

2.3.3. Design 3: A Two-Stage Continuous-mode Class-F/F^{-1} PA

Figure 2.8(c) shows the schematic of the two-stage differential hybrid continuous-mode Class-F/F^{-1} PA design, consisting of a DR stage and a PA stage. This design is an extended version of the one-stage differential hybrid continuous-mode Class-F/F^{-1} PA. Thus, both designs cooperate the identical continuous-mode hybrid Class-F/F^{-1} PA output networks. The DR stage is realized using a CS topology with identical sizes (W/L=6×30 μm/40 nm) for M_5 and M_6. It is biased at V_{G_DR}=0.32 V, and V_{DD_DR}=0.8 V. In addition, the PA stage is also realized using a cascode topology with identical sizes (W/L=6×30 μm/40 nm) for M_7, M_8, M_9, and M_{10} that are biased at V_{G_PA}=0.32 V, V_{cas_PA}=1.4 V, and V_{DD_PA}=2 V. The neutralization capacitors (C_{n_DR}) for DR stage are 55 fF and the neutralization capacitors (C_{n_PA}) for PA stage are 55 fF, respectively. The input and inter-stage matching networks of this two-stage PA design are also realized by two 1:1 transformer, and two input capacitors (C_{in2}=140 fF). The DC and peak current of the PA stage is 25 mA and 70/80/87 mA at 28/37/39 GHz, respectively.

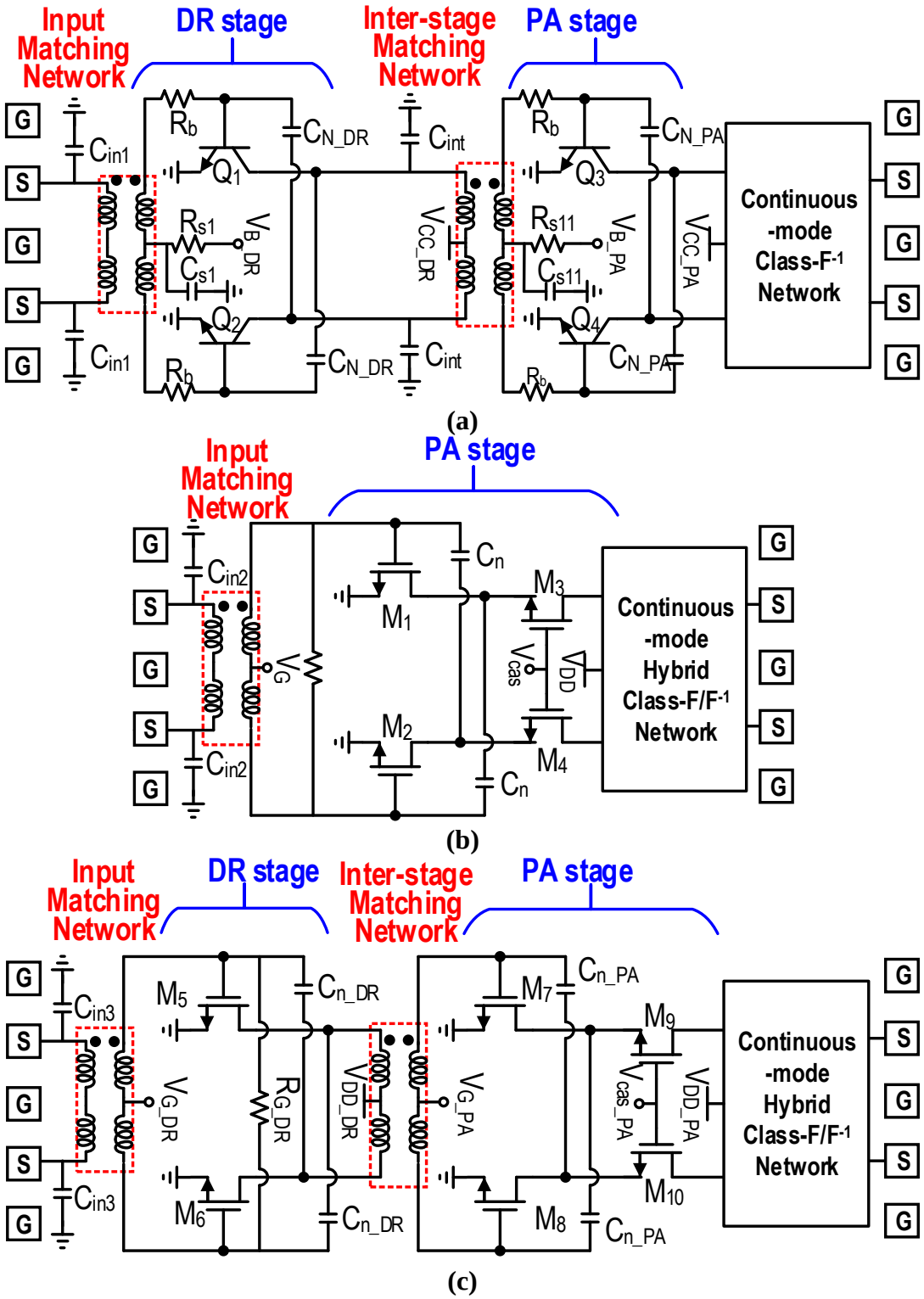


Figure 2.8 – Schematic of (a) two-stage continuous-mode Class-F^{-1} PA, (b) one- and (c) two-stage continuous-mode hybrid Class-F/F^{-1} PAs.

2.1.6. Measurement Results

2.4.1. Design 1: A Two-Stage Continuous-Mode Class-F^{-1} PA

The first PA design occupies a 0.91×0.32 mm^2 core area excluding pads (Figure 2.9a). All designs are measured by direct probing. The CW large-signal and small-signal S-parameter measurements are shown in Figure 2.10. At 28.5 GHz, this PA achieves P_{sat} of 17 dBm and P_{1dB} of 15.2 dBm, the power gain (G_p) of 20 dB and peak PAE (PAE_{max}) of 43.5 % (Figure 2.10a). Figure 2.10(c) shows 20.3 dB of peak S_{21} for the measured small-signal S-parament. The measured P_{sat} is from 16.4 to 17.4 dBm from 19 to 29.5 GHz, achieving a 43.3 % P_{sat} 1-dB (BW_{1dB}) bandwidth (Figure 2.10b). The measured PAE includes the loss of the DR stage, PA stage and the output network. This PA is first measured using 64-QAM signals at 1.5 GSym/s (9 Gb/s) and 3 GSym/s (18 Gb/s) at the carrier frequency ($f_{carrier}$) of 28.5 GHz (Figure 2.11a). Without DPD, the measured EVM is below <-25 dB for all data rates. At 3 GSym/s, the EVM is -25 dB with average output power (P_{avg}) of 9.8 dBm and average PAE (PAE_{avg}) of 18.4 %. Next, this PA is measured using 256-QAM signals at 0.8 GSym/s (6.4 Gb/s) and 1GSym/s (8 Gb/s) at $f_{carrier}$ of 28.5 GHz (Figure 2.11b). The EVM is kept below -30 dB for all data rates. At 1 GSym/s, the EVM is -30 dB with P_{avg} of 8.7 dBm and PAE_{avg} of 16.3 %. Noted that the roll-off factor (α) of the raised-cosine shaped filter is 0.35, the same setting as the following modulation measurements.

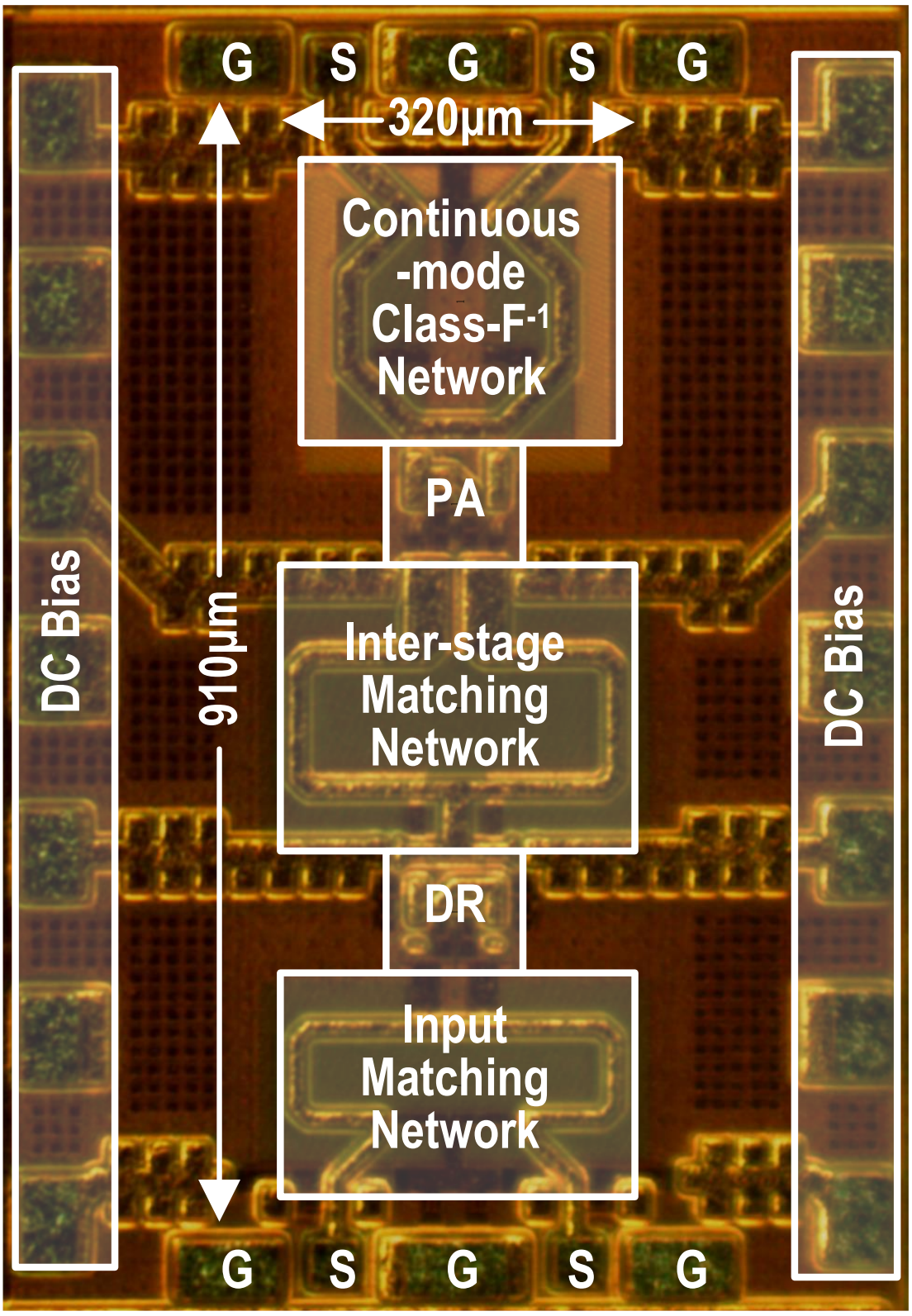


Figure 2.9 – Chip microphotograph of two-stage continuous-mode Class-F^{-1} PA

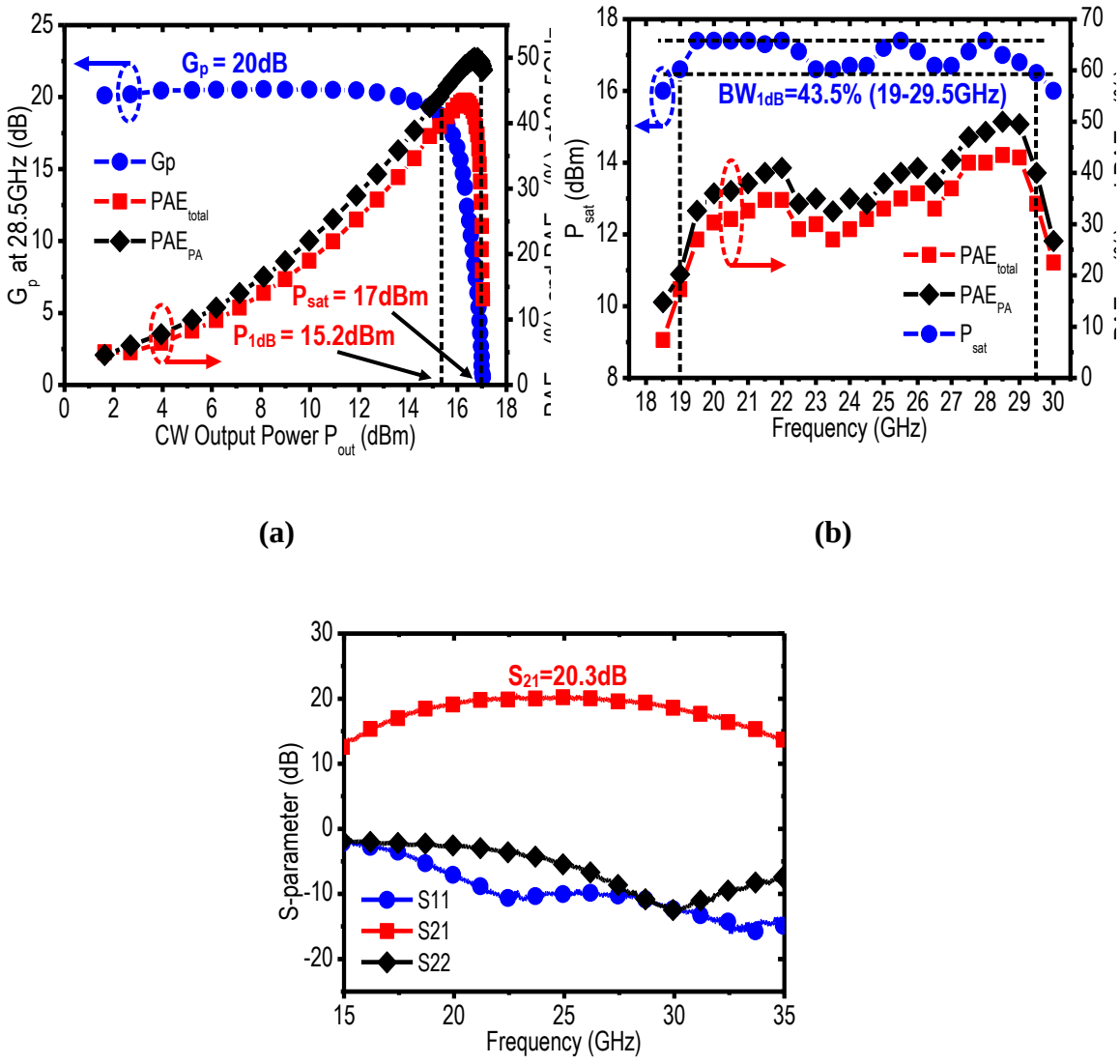


Figure 2.10 – (a) measured CW large-signal performance at 28.5 GHz, (b) measured CW large-signal performance vs. frequency and (c) measured small-signal S-parameter of two-stage continuous-mode Class-F^{-1} PA.

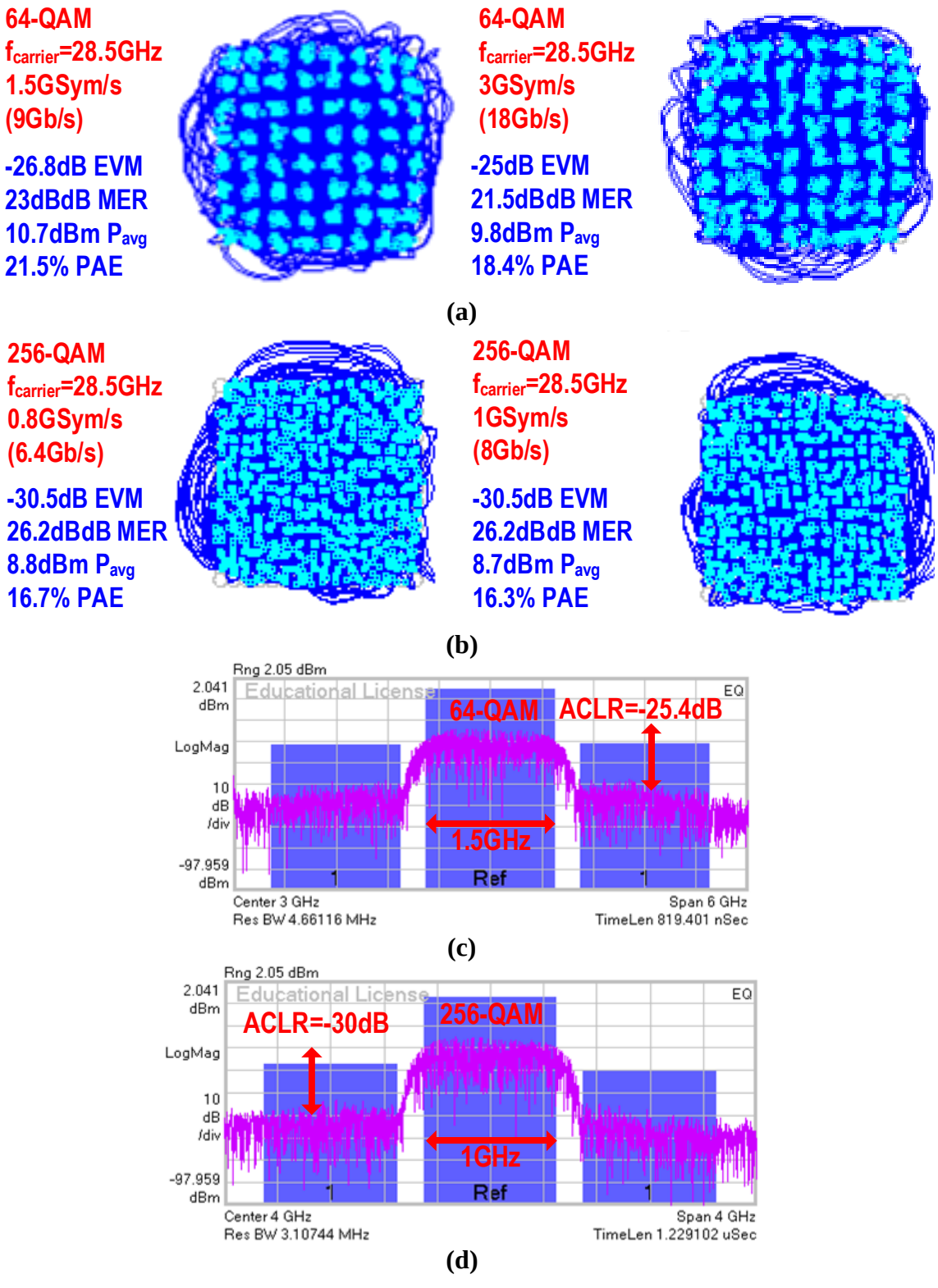


Figure 2.11 – (a) 64-QAM constellation, (b) 256-QAM constellation, (c) 64-QAM spectrum and (d) 256-QAM spectrum at $f_{carrier}$ of 28.5 GHz of Design 3.

2.4.2. Design 2: A One-Stage Continuous-mode Class-F/F^{-1} PA

The second PA design occupies a 0.55×0.25 mm^2 core area, as shown in Figure 2.12. Figure 2.13 shows the measured CW large-signal performance at 28, 37 and 39 GHz respectively. At 28 GHz, this proposed PA design achieves P_{sat} of 18.6 dBm, PAE_{max} of 45.7 % and G_p of 11.4 dB. At 37 GHz, the PA demonstrates P_{sat} of 18.6 dBm, PAE_{max} of 40.2 % and G_p of 10.7 dB. At 39 GHz, the PA achieves P_{sat} of 18.5 dBm, PAE_{max} of 41.2 % and G_p of 10.5 dB. This PA achieves high efficiency (i.e., $PAE_{max}\geq$40 %) and delivers almost constant P_{sat} at all the potential 5G bands (28/37/39 GHz). The P_{sat} 1-dB bandwidth is 54.3 % from 23.5 GHz to 41 GHz and the peak PAE is 46 % at 29 GHz, as shown in Figure 2.13(c). Also, it maintains over 30 % PAE from 25.5 GHz to 41 GHz (46.6 %). Figure 2.13(d) also demonstrates that the Class-F mode operates around 28 GHz, while Class-F^{-1} mode operates around 38 GHz. A mode transition is clearly shown around 35 GHz, which matches our analysis in Section III. In Figure 2.13(e), the measured small-signal S-parameter shows that 3-dB bandwidth is 51 % (25.9-43.7 GHz.)

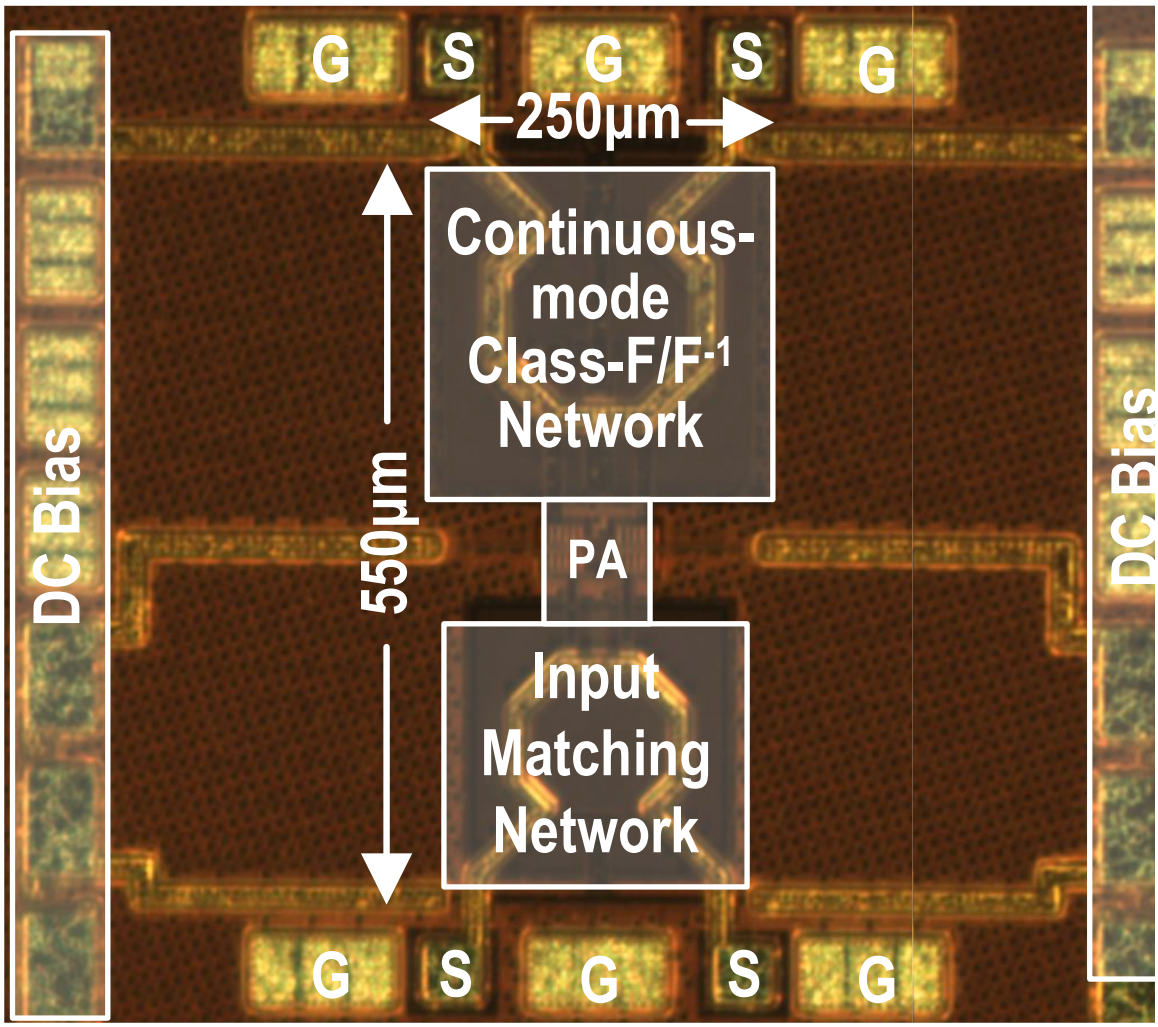


Figure 2.12 – Chip microphotograph of one-stage continuous-mode hybrid Class-F/F^{-1} PA.

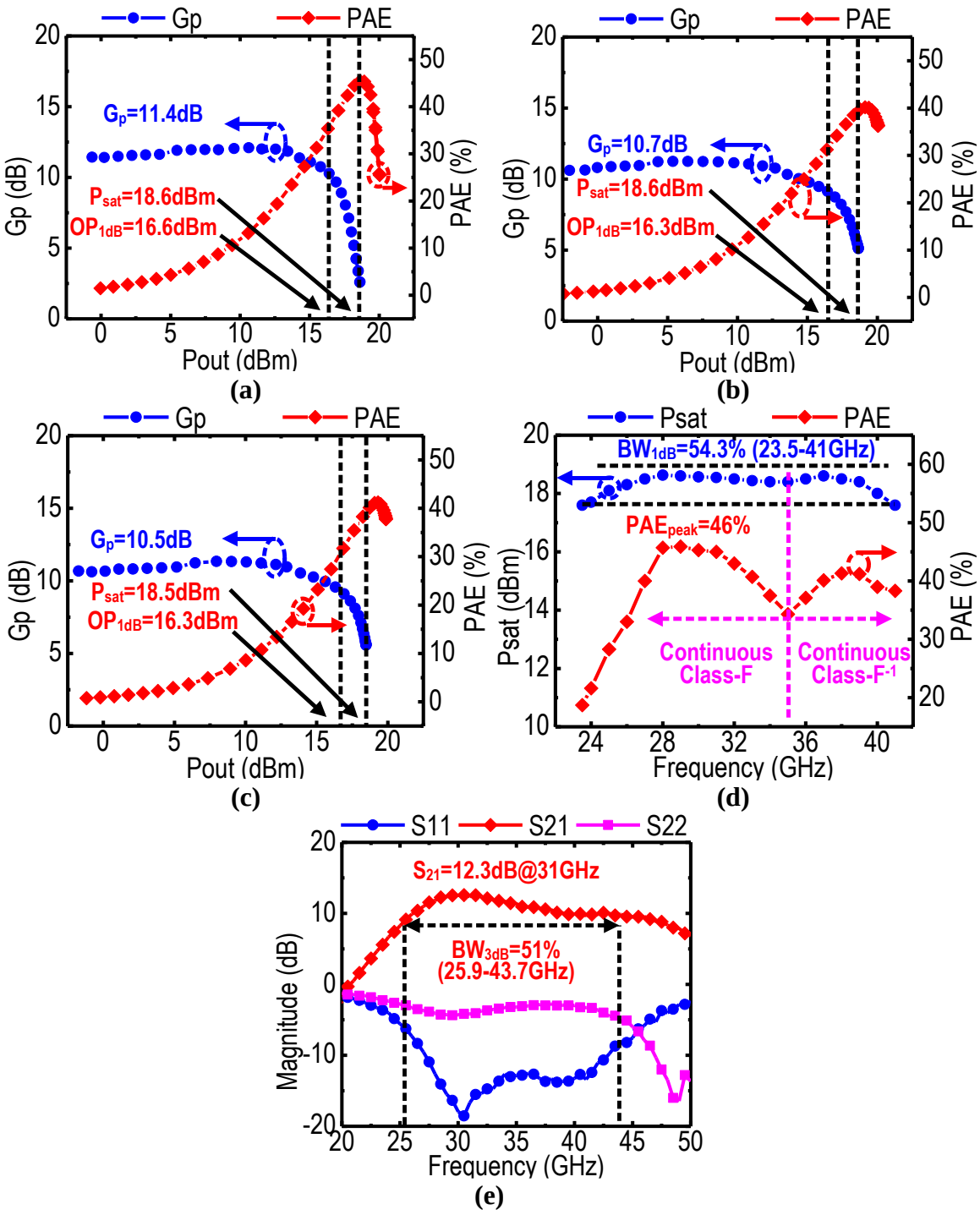


Figure 2.13 – One-stage continuous-mode hybrid Class-F/F^{-1} PA CW large-signal measurement at (a) 28 GHz, (b) 37 GHz and (c) 39 GHz, (d) Psat/PAE vs. frequency, and (e) small-signal S-parameter.

2.4.3. Design 3: A Two-Stage Continuous-mode Class-F/-F^{-1} PA

The third PA design occupies a 0.82×0.25 mm^2 core area, as shown in Figure 2.14. Figure 2.15 shows the measured CW large-signal performance at 28, 37 and 39 GHz. At 28 GHz, this PA achieves P_{sat} of 18.9 dBm, PAE_{max} of 43.2 % and G_p of 18.7 dB. At 37 GHz, the PA demonstrates P_{sat} of 18.9dBm, PAE_{max} of 37 % and Gp of 18 dB. At 39 GHz, the PA achieves P_{sat} of 18.9 dBm, PAE_{max} of 36 % and G_p of 15.6 dB. The measured CW large-signal performance vs. frequency is shown in Figure 2.15(d). The P_{sat} 1-dB bandwidth is 55.1 % from 23 GHz to 40.5 GHz. This design maintains over 30 % PAE from 24 GHz to 40 GHz (50 %). A mode transition is clearly shown around 33 GHz. The measured small-signal S-parameter shows 3-dB bandwidth is 49.4 % from 23.8 GHz to 39.4 GHz (Figure 2.15d). This PA is measured using 64-QAM signals at 0.5 GSym/s (3 Gb/s) at $f_{carrier}$ of 24 GHz, 28 GHz, 37 GHz and 39 GHz respectively (Figure 2.16). Without DPD, the measured EVM is below <-25 dB. At $f_{carrier}$ of 24 GHz, P_{avg} of 9.8 dBm and PAE of 9 %. At $f_{carrier}$ of 28 GHz, P_{avg} is 10.3 dBm and PAE_{avg} is 13.1 %. At $f_{carrier}$ of 37 GHz, P_{avg} is 11.7 dBm and PAE_{avg} is 11.9 %. At $f_{carrier}$ of 39 GHz, P_{avg} is 11 dBm and PAE_{avg} is 10.2 %. This PA design satisfies the stringent linearity requirement for future 5G bands (28/37/39 GHz). The large-signal and modulation comparisons with other PAs are listed in Table 2-1 and Table 2-2, respectively.

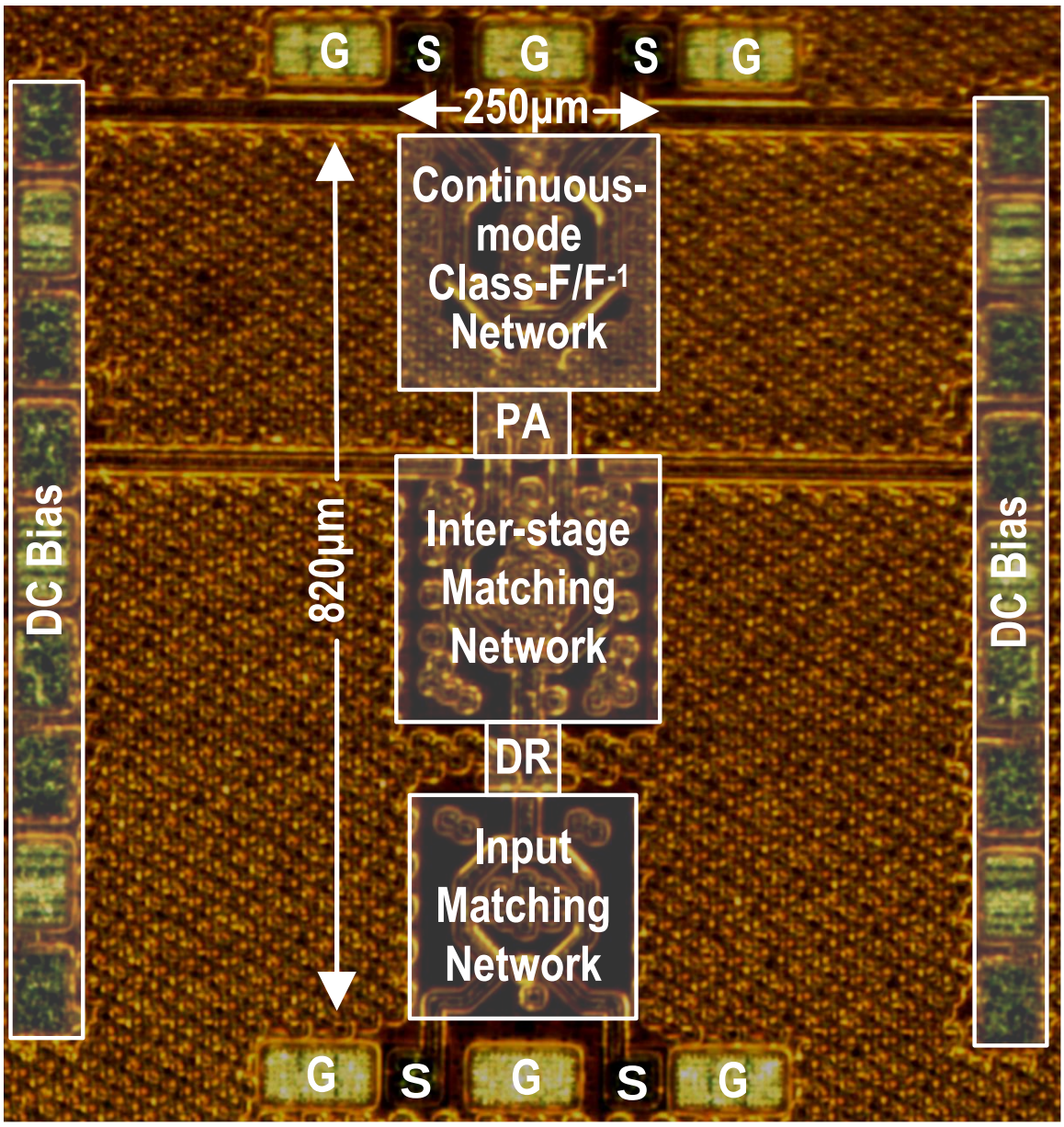


Figure 2.14 – Chip microphotograph of two-stage continuous-mode hybrid Class-F/F^{-1} PA.

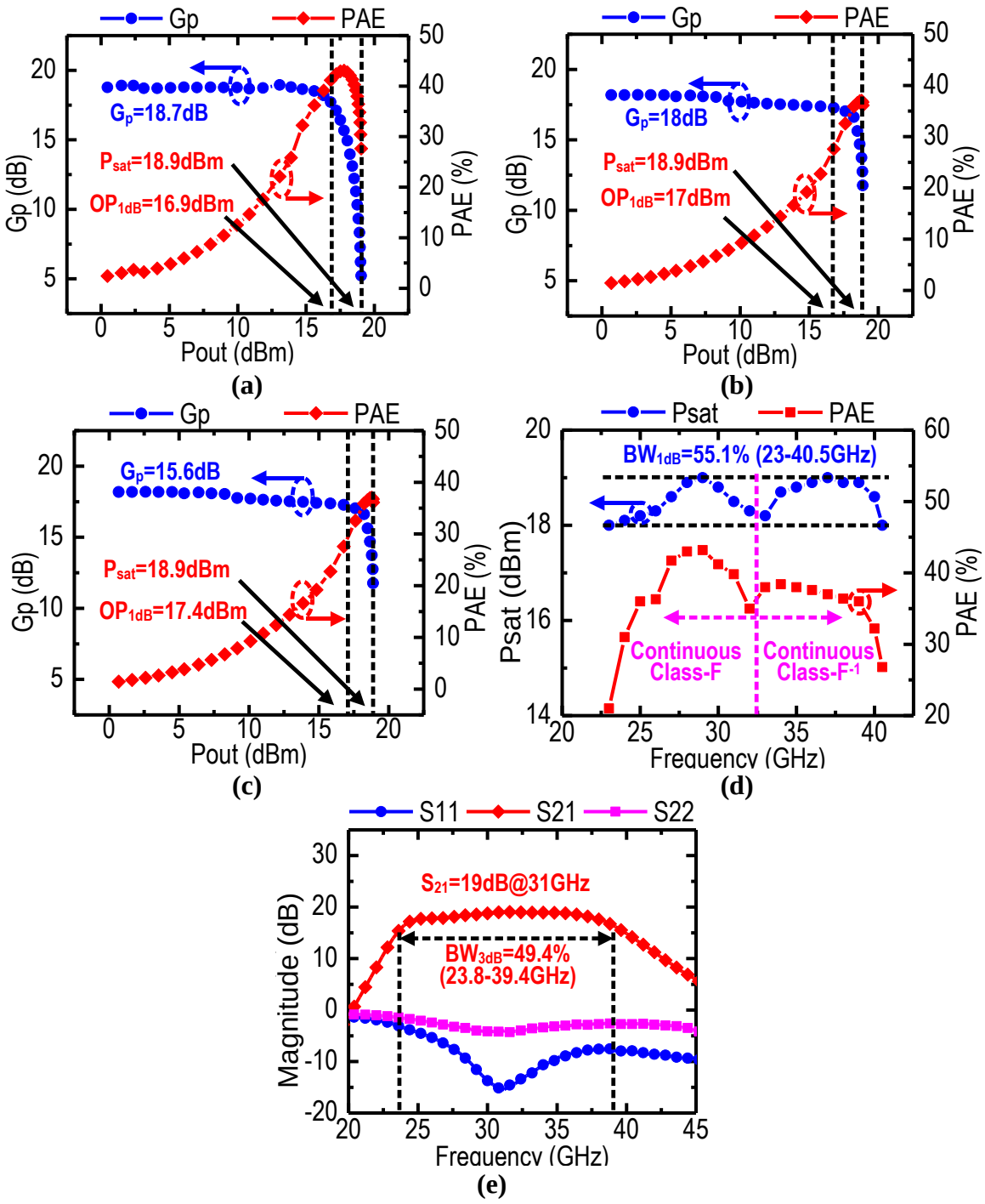


Figure 2.15 – Two-stage continuous-mode hybrid Class-F/F^{-1} PA CW large-signal measurement at (a) 28 GHz, (b) 37 GHz and (c) 39 GHz, (d) Psat/PAE vs. frequency, and (e) small-signal S-parameter.

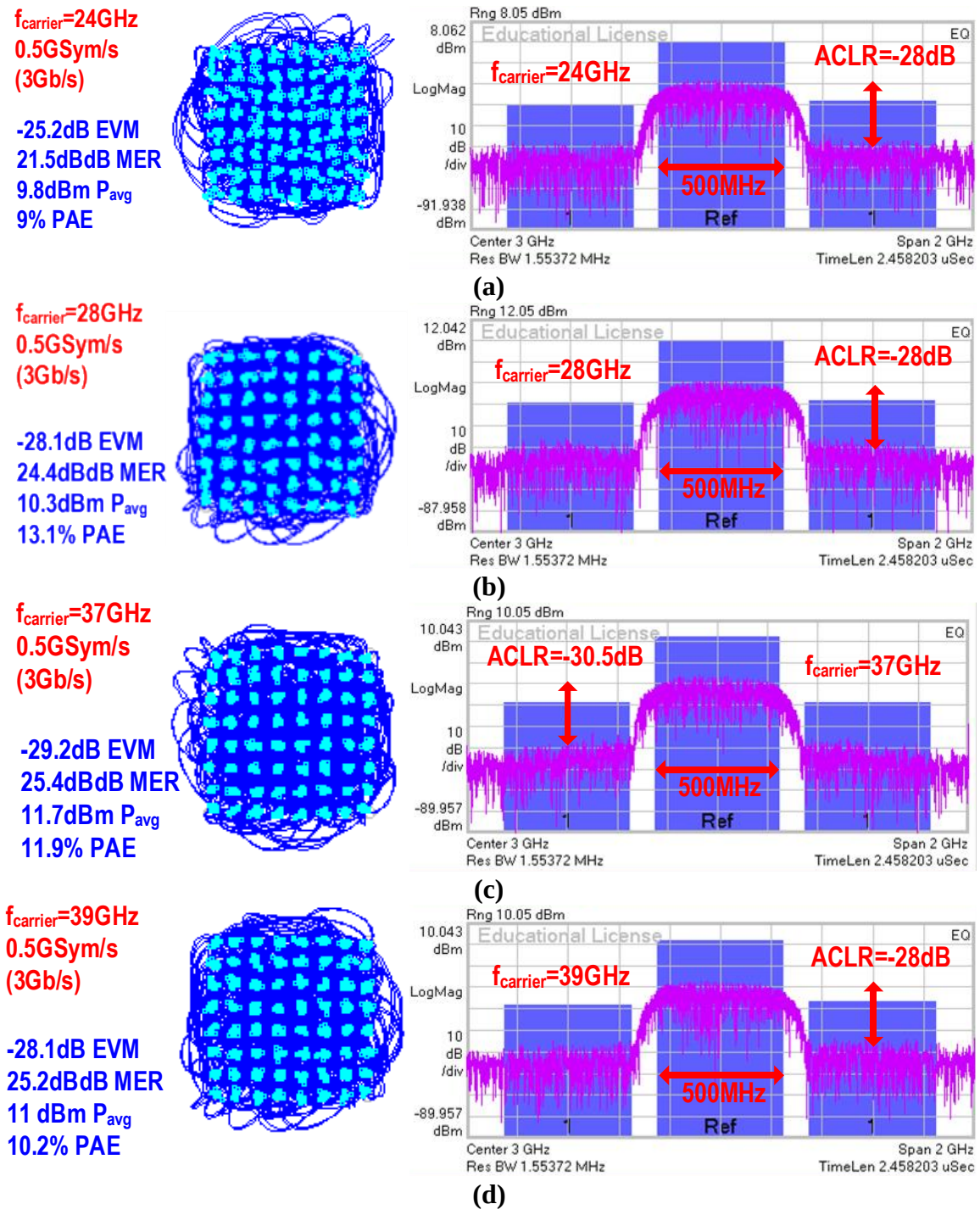


Figure 2.16 – Two-stage continuous-mode hybrid Class-F/F^{-1} PA modulation measurement results (0.5 GSym/s) at (a) 24 GHz, (b) 28 GHz, (c) 37 GHz, (d) 39 GHz respectively.

Table 2.2 – CW Performance Comparison with State-of-the art Silicon-based Mm-Wave Power Amplifier at Related Frequency

	P_{sat} 1-dB Freq. (GHz)	P_{sat} 1dB BW (%)	Operation Freq. (GHz)	P_{sat} (dBm)	PAE_{max} (%)	Gain (dB)	OP1dB (dBm)	VDD (V)	Process	Topology	Size (mm^2)
Design 1	19-29.5	43.3	28.5	17	43.5	20	15.2	1.9	130nm SiGe	2-stg. Continuous Class-F^{-1}	0.29
Design 2	23.5-41	54.3	28 37 39	18.6 18.6 18.5	45.7 40.2 41.2	11.4 10.7 10.5	16.6 16.3 16.3	2	45nm SOI CMOS	1-stg. Continuous Hybrid Class-F/ F^{-1}	0.14
Design 3	23-40.5	55.1	28 37 39	18.9 18.9 18.9	43.2 37 36	18.7 18 15.6	16.9 17 17.4	2	45nm SOI CMOS	2-stg. Continuous Hybrid Class-F/ F^{-1}	0.21
[7] Hu	28-42	40	28 37 39	16.8 17.1 17	20.3 22.6 21.4	18.2 17.1 16.6	15.2 15.5 15.4	1.5	130nm SiGe	2-stg. Doherty	1.76
[35] Sarkar	27-39	7.1	28	18.6	35.3	15.3	15.5	3.6	130nm SiGe	1-stg. Continuous Class-AB	0.27
[20] Ali	26-34	26.7	29	14.75	46.4	10	13.2	1.1	65nm CMOS	1-stg. Continuous Class-F	0.12
[22] Ali	27-30*	10.5*	28	15.6	41	15.8	14	1.1	65nm CMOS	2-stg Continuous Class-F w/ Xfmr AM/PM correction	0.24
[15] Vigilante	25-48***	63*	43	16.6	24.2	20.8	13.4	0.9	28nm CMOS	Class-AB w/ power combiner	0.16
[18] Zhang	26-29*	10.9	27	18.1	41.5	20.5	16.8	1	40nm CMOS	2-Way 2-stg. CS w/ Inductive degeneration	0.36
[8] Indirayanti	28-33*	22.2*	32	19.8	21	22	16	1	28nm CMOS	2-Way Xfmr-based Doherty	0.59
[37] Mortazavi	24-31	25.5	27	17.1	40	10.3	15	2.2	130nm SiGe	1-stg. Hybrid Class- F^{-1}/F	0.27
[38] Mortazavi	36-39.5*	9.3*	38	16.5	38.5	16	15	2.4	130nm SiGe	2-stg. Class- F^{-1}	0.5
[16] Shakib	27-31*	13.8	30	15.3	36.6	16.3	14.3	1.15	28nm CMOS	2-stg. CS w/ Inductive degeneration	0.16
[17] Shakib	26-33*	23.3*	27	15.1	33.7	22.4	13.7	1.1	40nm CMOS	3-stg. w/ dual-resonance Xfmr	0.23
[19] Park	26-28.5*	9.2*	28	19.8	28.5	13.6	18.6	2.2	28nm CMOS	1-stg. 2-stacked Class-AB	0.28
[21] Huang	22-30*	30.7	28	26	34.1	16.3	23.2	2.4	90nm CMOS	2-Way 1-stg. Cascode w/ Xfmr combiner	0.4**
[1] Rabet	-	-	28	23	41.4	-	-	4	130nm SiGe	Outphasing w/ Triaxial Balun	0.56**
[32] Datta	39-43*	4*	41	23.4	34.9	12.5	-	4.5	130nm SiGe	2-stacked Class-E	1
[10] Chappidi	30-55	58.8	40	23.7	28.5	23.4	-	4	130nm SiGe	Dual-Freq. PBO reconfigurable	0.96

*Graphically estimated from reported figures, **Pads included, ***Small-signal -3dB BW.

Table 2.3 – Modulation Performance Comparison With State-of-the art Silicon-based Mm-Wave Power Amplifier at Related Frequency

	Carrier Frequency (GHz)	Modulation Scheme	Data Rate (Gb/s)	EVM (dB)	P_{out}@EVM (dBm)	PAE@EVM (%)
Design 1	28.5	64-QAM 1-CC 256-QAM 1-CC	9/18 6.4/8	-26.8★/-25★ -30.5★/-30.5★	10.7/9.8 8.8/8.7	21.5/18.4 16.7/16.3
Design 3	24/28/37/39	64-QAM 1-CC	3	25.2★/-28.1★/-29.2★ /-28.1★	9.8/10.3/11.7/11	9/13.1/11.9/10.2
[7] Hu	28/3739	64-QAM	6/3/3	-26.6★/-30.3★/-28.7★	7.2/9.5/9.3	14.4&/19.2&/17.2&
[20] Ali	28	64-QAM 256-QAM	2 0.4	-25.6★ -31.7★	10.4 9.4	19.3 16.3
[21] Huang	28	256-QAM	0.8	-32★	20	-
[18] Zhang	27	64-QAM	6	-25#	8.4	8.8
[35] Sarkar	28	16-QAM OFDM	3.2	-22★	12.6*	11.5
[38] Mortazavi	38	64-QAM/128-QAM	0.049/0.049	-26★	13.5/13.5	20*/20*
[15] Vigilante	34	64-QAM	6	-25#	5.9	2.3
[8] Indirayanti	32	64-QAM	15	-25★	11.7	5.75
[16] Shakib	30	64-QAM OFDM 1-CC	1.5	-25#	5.3	9.6
[17] Shakib	27	64-QAM OFDM 8-CC	4.8	-25#	6.7	11
[1] Rabet	28	64-QAM OFDM	0.48+	-30.5#	14.3	25.3
[10] Chappidi	30/50	16-QAM	4	-18.2★/19.2★	16.4/16.9	19.9&/24.6&

#Normalized w.r.t average power, ★Normalized w.r.t peak power, +Memoryless DPD, &Collector efficiency, *Graphical estimation.

2.1.7. Chapter Summary

In this chapter, we present three differential fully integrated continuous-mode PAs, implemented in 130 μm SiGe (design 1) and 45 nm CMOS SOI (design 2 and 3) processes. These PAs utilize our proposed transformer-based continuous-mode harmonically-tuned PA output networks to provide the required fundamental, 2nd- and 3rd-order harmonic load impedance terminations respectively. All designs achieve high PAE and ultra-wide P_{sat} 1dB bandwidth. Importantly, our continuous-mode PA output network only occupies one single transformer footprint and does not require any additional tunable elements or switches, providing an ultra-compact design for massive MIMO applications. Additionally, the modulation measurements meet the stringent 5G linearity requirement.

CHAPTER 3. A POWER AMPLIFIER WITH NMOS/PMOS NONLINEAITY CANCELLATION SCHEME

3.1. Introduction

The next-generation millimeter-wave (mm-Wave) wireless communication systems are required to support spectrum-efficient modulation schemes (e.g., 64-QAM, 256-QAM or 5G NR) with Gb/s link throughput. Also, these modulations accompany single and/or multiple component-carriers (CCs), i.e., orthogonal frequency-division multiplexing (OFDM) with multiple CCs [53]-[56]. These high-order modulation schemes entail complex constellations and pose a highly stringent demand on the linearity of the mm-wave front-end circuits, especially power amplifiers (PAs), i.e., large-signal amplitude-to-amplitude (AM-AM) and amplitude-to-phase (AM-PM) distortions, as well as the PA energy efficiency [53]-[82]. Therefore, the future mm-Wave PA solutions need to offer high linearity, high efficiency, required output power, simple design and compact size simultaneously for phased array and/or massive MIMO applications [83]-[86].

To boost the PA efficiency, the mm-Wave PAs usually are biased in deep Class-AB toward Class-B regions, instead of Class-A region. By this means, the PA efficiency is enhanced effectively but it sacrifices the PA linearity, resulting PAs with poor error-vector-magnitude (EVM) and adjacent channel power ratio (ACPR) performances. Those metrics are the major performance indexes of the next generation wireless communication systems. In other words, those high-efficiency-oriented mm-Wave PAs cannot accommodate the stringent linearity requirements for future spectrum-efficient modulation schemes.

Practically, the major PA AM-PM distortion comes from the nonlinear capacitors, such as drain-to-source C_{gs} and gate-to-drain C_{gd} capacitors in MOSFET devices. Mm-Wave PAs often utilize neutralization capacitors C_n to improve the power gain G_p and stability. However, fixed C_n capacitors cannot completely cancel the varying C_{gd} values as well as its varying Miller input capacitances due to device gain compression. Moreover, the C_{gs} also vary substantially versus input voltage amplitudes and lead to AM-PM distortions. Therefore, several RF/mm-Wave PA linearity improvement techniques without DPD are reported, such as input PMOS capacitance cancellation [87], multi-gated transistors (MGTRs) [88][89], adaptive biasing, harmonic trapping [90], PMOS neutralization capacitors [91] and push-pull NMOS/PMOS transistor compensation [92][93]. Those PA linearity improvement techniques can minimize the nonlinearity, but they usually require additional biasing circuitries/routings, complicate devices arrangements, sophisticated PA output matching network designs/layouts and extra resonators including multiple inductors and capacitors. Even though PA linearity can be improved by those techniques, they inevitably induce extra loss to further degrade the PA overall performance, especially at mm-Wave frequency ranges. Thus, this is a challenge to improve the mm-Wave PA linearity and maintain performance simultaneously.

To avoid the aforementioned drawbacks, the NMOS/PMOS transistor compensation technique is an excellent candidate [92]-[94]. Reference [92] combines NMOS and PMOS devices since they exhibit the opposite nonlinear behaviors for C_{gs}. However, this push-pull NMOS/PMOS compensation enables cancellation of multiple device-level nonlinearities (capacitors, transconductance, and output conductance), the existing designs arrange NMOS/PMOS in an inverter-like configuration with less-than the

supply voltage (V_{DD}) output voltage swings and undesired bias interactions, limiting their use in scaled CMOS technologies for high efficiency mm-Wave PAs. The similar topology is reported in ref. [92]. Although, in the AC perspective, NMOS and PMOS transistors are not physically connected since the primary coil of the PA output transform is inserted between PMOS and NMOS, in the DC perspective, this topology is still an inverter-like one, still limiting the PA performance at mm-Wave frequencies.

To address this challenge, we present a doubly hybrid NMOS/PMOS V-band PA topology with a transformer-based 4-way series-parallel distributed-active-transformer (DAT) output matching network. This topology preserves the cancellation of multiple device nonlinearities but allows large output voltage swings close-to two times of supply voltage (i.e., $2\times V_{DD}$) to avoid compromising output power or efficiency due to device knee voltages (V_{knee}) and limited voltage headroom. Moreover, it decouples the DC gate and drain biasing of the NMOS/PMOS devices, and different biasing points and duty-cycles can be applied on the NMOS and PMOS PA devices to collectively optimize the AM-PM and AM-AM linearity, saturated power (P_{sat}), output 1-dB compression point (OP_{1dB}), and maximum/power-backoff (PBO) PAE, etc. Further, NMOS and PMOS power devices have been mixed at the PA, driver (DR), and pre-driver (PDR) stages to achieve doubly-hybrid NMOS/PMOS nonlinearity cancellation. Also, the 4-way series-parallel DAT output matching network provides low loss power combining and desired PA optimum loads. Our PA design covers 50.4 GHz-58.6 GHz with 35.4 % peak PAE, 16.3dBm Psat, and only 0.4° AM-PM distortion at 55 GHz. The AM-PM distortion is below 2° over 50-57GHz. It supports 64-QAM modulation with 15.6 % PAE_{avg} and 9.5 dBm P_{avg} at 0.5 GSym/s as well as 14.5 % PAE_{avg} and 10.8 dBm of P_{avg} for 5G NR CP-OFDM 64-QAM 1-CC 400 MHz

modulation. This design not only supports single CC but also multiple CCs, showing the capacity of accommodate advanced complex modulations.

3.2. MOSFET AM-AM and AM-PM Distortion Analysis

Figure 3.1 shows a differential PA with the input and output matching networks (e.g., L_{in} and L_{out}), and its simplified small-signal single-ended half-circuit. Here, C_{gs}, C_{gd}, C_{ds}, g_m, g_{ds}, R_s and R_L represent the small-signal parasitic drain-to-source, gate-to-drain, drain-to-source capacitors, transconductance, gate-to-source conductance, source and load resistors, respectively. The output gate-to-source resistor is reverse to g_{ds}, i.e., $R_{ds} = 1/g_{ds}$. For delivering maximum output power, we assume R_L has been converted to the optimum load R_{opt} which is determined by the breakdown voltage, V_{knee}, and maximum output current by the output matching network. Also, most mm-Wave PAs utilize the neutralization capacitor C_n pairs to improve the power gain G_p and stability.

The input and output referred C_{gd} capacitors due to Miller's effect with C_n can be expressed respectively as

$$C_{gd}' = \left(1 + g_m R_{opt} \| R_{ds}\right)\left(C_{gd} - C_n\right), \tag{3-1}$$

and

$$C_{gd}'' = \left(1 + 1/g_m R_{opt} \| R_{ds}\right)\left(C_{gd} - C_n\right). \tag{3-2}$$

Thus, the effective input capacitor C_{in} and output capacitor C_{out} can be represented as $C_{in}=C_{gs}+C_{gd}'$ and $C_{out}=C_{ds}+C_{gd}''$ respectively. Figure 3.2(a) shows the various extracted small-signal parasitics parameters (i.e., 45nm SOI process) of a NMOS transistor

versus the gate-to-source voltage V_{gs}. Again, to boost PA efficiency, the PA is biased in deep Class-AB toward Class-B regions. So, when a PA is fed by an input signal with a small voltage amplitude, the input voltage swing crosses the saturation region and cutoff region, (e.g., the red waveform in Figure 3.2a). The conduction angle α is defined as the proportion of the input voltage swing in the saturation region to the cutoff region per cycle. Likely, when a PA is fed by an input signal with a large voltage amplitude (e.g., the blue waveform in Figure 3.2b), the duration angle β is defined as the proportion of the input voltage swing in triode region to saturation region per cycle. For example, $\beta = 0$ means the transistor works in the saturation ($\alpha=2\pi$) or saturation-and-cutoff ($\alpha<2\pi$) regions and $\beta >$ 0 means the transistor works in triode region partially per cycle and the PA starts to be compressed, depended on the input voltage swings. Thus, considering α and β, the effective input capacitor can be re-written as

$$\begin{aligned} C_{in}(\alpha,\beta) = &\left(1-\frac{\beta}{2\pi}\right)\left(\frac{\alpha}{2\pi}\right)C_{gs}^{sat.} + \left(1-\frac{\alpha}{2\pi}\right)C_{gs}^{cutoff} \\ &+\left(\frac{\beta}{2\pi}\right)C_{gs}^{triode} + \left[1+g_m(\alpha,\beta)R_L \| R_{ds}(\alpha,\beta)\right] \\ &\times\left[\left(1-\frac{\beta}{2\pi}\right)\left(\frac{\alpha}{2\pi}\right)C_{gd}^{sat.} + \left(\frac{\beta}{2\pi}\right)\left(1-\frac{\alpha}{2\pi}\right)C_{gd}^{triode} - C_n\right], \end{aligned} \tag{3-3}$$

where the $C_{gs}^{sat.}$ and C_{gs}^{cutoff} are the values of C_{gs} when the PA works in the saturation and cutoff regions respectively. Similarly, the $C_{gd}^{sat.}$ and $C_{gd}^{triode.}$ are the values of C_{gd} when the PA works in the saturation and triode region respectively. Thus, the effective input capacitor can be re-expressed as

$$C_{out}(\alpha,\beta)=\left(1-\frac{\beta}{2\pi}\right)\left(\frac{\alpha}{2\pi}\right)C_{ds}^{sat.}+\left(1-\frac{\alpha}{2\pi}\right)C_{ds}^{cutoff}$$
$$+\left(\frac{\beta}{2\pi}\right)C_{ds}^{triode}+\left[1+\frac{1}{g_m(\alpha,\beta)R_L\|R_{ds}(\alpha,\beta)}\right] \quad (3\text{-}4)$$
$$\times\left[\left(1-\frac{\beta}{2\pi}\right)\left(\frac{\alpha}{2\pi}\right)C_{gd}^{sat.}+\left(\frac{\beta}{2\pi}\right)\left(1-\frac{\alpha}{2\pi}\right)C_{gd}^{triode}-C_n\right].$$

It can be observed that The effective input and output capacitors are time-average and considerably modulated by α and β with respect to the input voltage amplitude, generating undesired AM-PM distortion. Additionally, the drain current and g_m of the device shows an exponential behavior for applying a low V_{gs}, leading the device to a quadratic region with a dramatic change. Since those nonlinear transconductance $g_m(\alpha,\beta)$ and parasitic drain-to-source resistor $R_{ds}(\alpha,\beta)$ generate higher-order components and also are also associated to the α and β, they achieve gain peaking or/and compression on AM-AM distortion [94]-[97]. The capacitance value of the neutralization capacitor C_n is chosen to maximize the PA stability and keep the PA unconditionally stable, so it can be determined as $C_n=C_{gs}^{sat.}$. Although C_n seems to delete C_{gs} and cancel out the drain-to-gate feedback, practically it contributes $2\times C_n$ from the drain terminal to the gate terminal at the second harmonic frequency, which remixes with the fundamental components to generate unwanted third-order nonlinearity. Figure 3.2(a) also shows that C_{gd} exhibits a constant value cross the saturation and triode regions, i.e., $C_{ds}^{sat.}\approx C_{ds}^{triode}$, as well as C_{gd} also shows a flat variation over the all operating regions, i.e., $C_{dg}^{sat.}\approx C_{dg}^{triode}\approx C_{dg}^{cutoff}$. Therefore, the effective input and output capacitors can be simplified respectively as

$$C_{in}(\alpha,\beta)=\left(1-\frac{\beta}{2\pi}\right)\left(\frac{\alpha}{2\pi}\right)C_{gs}^{sat.}+\left(1-\frac{\alpha}{2\pi}\right)C_{gs}^{cutoff}+\left(\frac{\beta}{2\pi}\right)C_{gs}^{triode}, \quad (3\text{-}5)$$

$$C_{out}(\alpha,\beta)=\left(1-\frac{\beta}{2\pi}\right)\left(\frac{\alpha}{2\pi}\right)C_{ds}^{sat.}+\left(1-\frac{\alpha}{2\pi}\right)C_{ds}^{cutoff}+\left(\frac{\beta}{2\pi}\right)C_{ds}^{triode}. \tag{3-6}$$

Moreover, the output voltage V_L cross R_L can be written as

$$V_L(j\omega)=g_m I_{in}\frac{R_{ds}R_{opt}}{R_S}\frac{1+j\omega C_{in}R_S-\omega^2 L_{in}C_{in}}{1+j\omega C_{out}(R_{ds}+R_L)-\omega^2 L_{out}C_{out}}. \tag{3-7}$$

Then, the phase of a NMOS PA at certain operating frequency ω_0 can be presented as

$$\angle V_L(j\omega_0)\big|_{NMOS}=\tan^{-1}\left(\frac{\omega_0 C_{in}R_S}{1-\omega_0^2 L_{in}C_{in}}\right)-\tan^{-1}\left[\frac{\omega_0 C_{out}(R_{ds}+R_L)}{1-\omega_0^2 L_{out}C_{out}}\right], \tag{3-8}$$

To achieve the desired PA performance, the inductors L_{in} and L_{out} of the input and output networks are designed to resonate out the C_{in} and C_{out} at P_{1dB} point separately. So, their values can be determined as

$$L_{in}=\frac{1}{\omega_0^2 C_{in}(\alpha=\alpha_{P1dB},\beta=0)}=\frac{1}{\omega_0^2\left[\left(\frac{\alpha_{P1dB}}{2\pi}\right)C_{gs}^{sat.}+\left(1-\frac{\alpha_{P1dB}}{2\pi}\right)C_{gs}^{cutoff}\right]}, \tag{3-9}$$

as well as

$$L_{out}=\frac{1}{\omega_0^2 C_{out}(\alpha=\alpha_{P1dB},\beta=0)}=\frac{1}{\omega_0^2\left[\left(\frac{\alpha_{P1dB}}{2\pi}\right)C_{ds}^{sat.}+\left(1-\frac{\alpha_{P1dB}}{2\pi}\right)C_{ds}^{cutoff}\right]}, \tag{3-10}$$

P_{1dB} point. However, due to the fixed inductors L_{in} and L_{out}, the effective input and output capacitors C_{in} and C_{out} cannot be perfectly tuned out in all operating regions. Thus, the AM-PM distortion of a NMOS PA can be expressed in (3-11), where α_{ss} represent the conduction angle when an NMOS PA operates in the small-signal region. It is obvious that

the AM-PM distortion with a given transistor size is associate to α_{ss}, α_{P1dB}, R_L. In other words, we can set the PA with an appropriate bias voltage and the optimum load to reach very low AM-PM distortion but this PA cannot approach the desired power and efficiency, which is a well-known and troublesome trade-off in PA design.

$$\left|\angle V_L'(j\omega_0)\right|_{NMOS}$$

$$= \left| \tan^{-1}\left\{ \frac{\omega_0\left[\left(\frac{\alpha_{ss}}{2\pi}\right)C_{gs}^{sat.}\Big|_{NMOS}+\left(1-\frac{\alpha_{ss}}{2\pi}\right)C_{gs}^{cutoff}\Big|_{NMOS}\right]R_S'}{1-\frac{\left(\frac{\alpha_{ss}}{2\pi}\right)C_{gs}^{sat.}\Big|_{NMOS}+\left(1-\frac{\alpha_{ss}}{2\pi}\right)C_{gs}^{cutoff}\Big|_{NMOS}}{\left(\frac{\alpha_{P1dB}}{2\pi}\right)C_{gs}^{sat.}\Big|_{NMOS}+\left(1-\frac{\alpha_{P1dB}}{2\pi}\right)C_{gs}^{cutoff}\Big|_{NMOS}}} \right\} - \tan^{-1}\left\{ \frac{\omega_0\left[\left(\frac{\alpha_{ss}}{2\pi}\right)C_{ds}^{sat.}\Big|_{NMOS}+\left(1-\frac{\alpha_{ss}}{2\pi}\right)C_{ds}^{cutoff}\Big|_{NMOS}\right]\times\left[R_{ds}(\alpha,\beta)+R_{opt}\right]}{1-\frac{\left(\frac{\alpha_{ss}}{2\pi}\right)C_{ds}^{sat.}\Big|_{NMOS}+\left(1-\frac{\alpha_{ss}}{2\pi}\right)C_{ds}^{cutoff}\Big|_{NMOS}}{\left(\frac{\alpha_{P1dB}}{2\pi}\right)C_{ds}^{sat.}\Big|_{NMOS}+\left(1-\frac{\alpha_{P1dB}}{2\pi}\right)C_{ds}^{cutoff}\Big|_{NMOS}}} \right\} \right|, \quad (3\text{-}11)$$

Figure 3.2(b) exhibits the various extracted small-signal parameters of a PMOS transistor versus the gate-to-source voltage V_{gs}. So, the AM-PM distortion of a PMOS PA can be expressed in (3-12). The corresponding AM-PM behaviors of NMOS and PMOS PAs are shown in Figure 3.3, caused by the time-average effective C_{in} and C_{out} [98]. The NMOS PA presents a negative AM-PM distortion at P_{1dB}, on the contrary, the PMOS PA presents a positive AM-PM distortion at P_{1dB}. Our idea is to utilize this opposite behavior to generate a flat AM-PM distortion at P_{1dB} or even beyond.

$$\left|\angle V_L'(j\omega_0)\right|_{PMOS}$$

$$= \left| \tan^{-1}\left\{ \frac{\omega_0\left[\left(\frac{\alpha_{ss}}{2\pi}\right)C_{gs}^{sat.}\Big|_{PMOS}+\left(1-\frac{\alpha_{ss}}{2\pi}\right)C_{gs}^{cutoff}\Big|_{PMOS}\right]R_S'}{1-\frac{\left(\frac{\alpha_{ss}}{2\pi}\right)C_{gs}^{sat.}\Big|_{PMOS}+\left(1-\frac{\alpha_{ss}}{2\pi}\right)C_{gs}^{cutoff}\Big|_{PMOS}}{\left(\frac{\alpha_{P1dB}}{2\pi}\right)C_{gs}^{sat.}\Big|_{PMOS}+\left(1-\frac{\alpha_{P1dB}}{2\pi}\right)C_{gs}^{cutoff}\Big|_{PMOS}}} \right\} \right.$$

$$\left. - \tan^{-1}\left\{ \frac{\omega_0\left[\left(\frac{\alpha_{ss}}{2\pi}\right)C_{ds}^{sat.}\Big|_{PMOS}+\left(1-\frac{\alpha_{ss}}{2\pi}\right)C_{ds}^{cutoff}\Big|_{PMOS}\right]\times\left[R_{ds}(\alpha,\beta)+R_{opt}\right]}{1-\frac{\left(\frac{\alpha_{ss}}{2\pi}\right)C_{ds}^{sat.}\Big|_{PMOS}+\left(1-\frac{\alpha_{ss}}{2\pi}\right)C_{ds}^{cutoff}\Big|_{PMOS}}{\left(\frac{\alpha_{P1dB}}{2\pi}\right)C_{ds}^{sat.}\Big|_{PMOS}+\left(1-\frac{\alpha_{P1dB}}{2\pi}\right)C_{ds}^{cutoff}\Big|_{PMOS}}} \right\} \right| \quad (3\text{-}12)$$

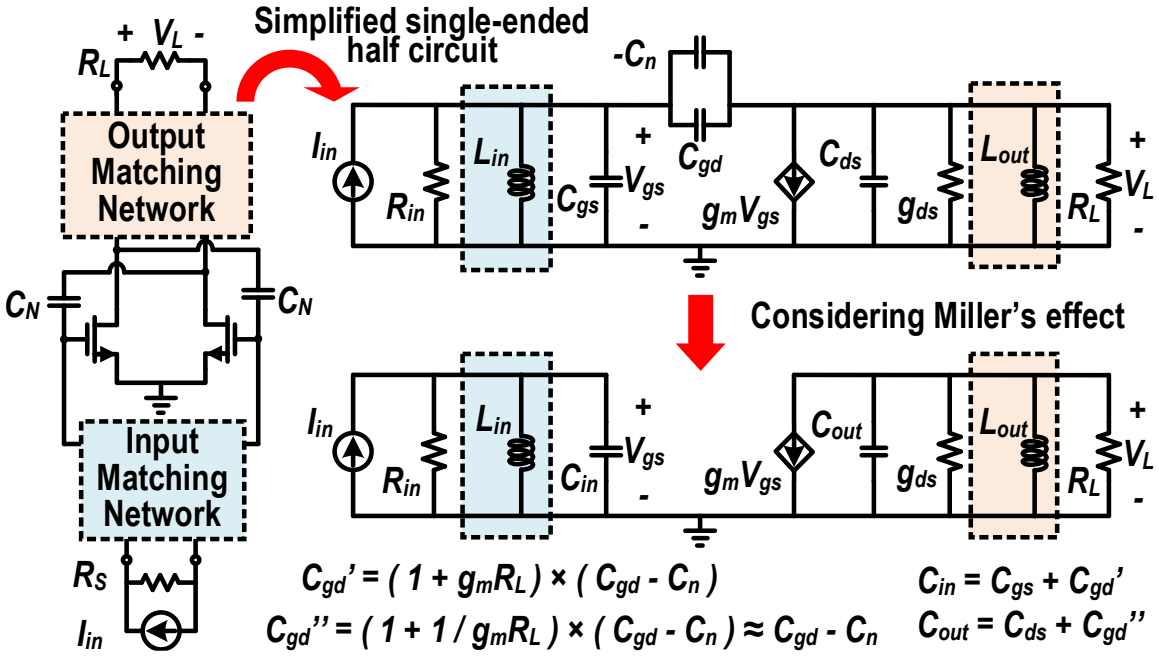


Figure 3.1 – A neutralized PA and its simplified single-ended half circuit.

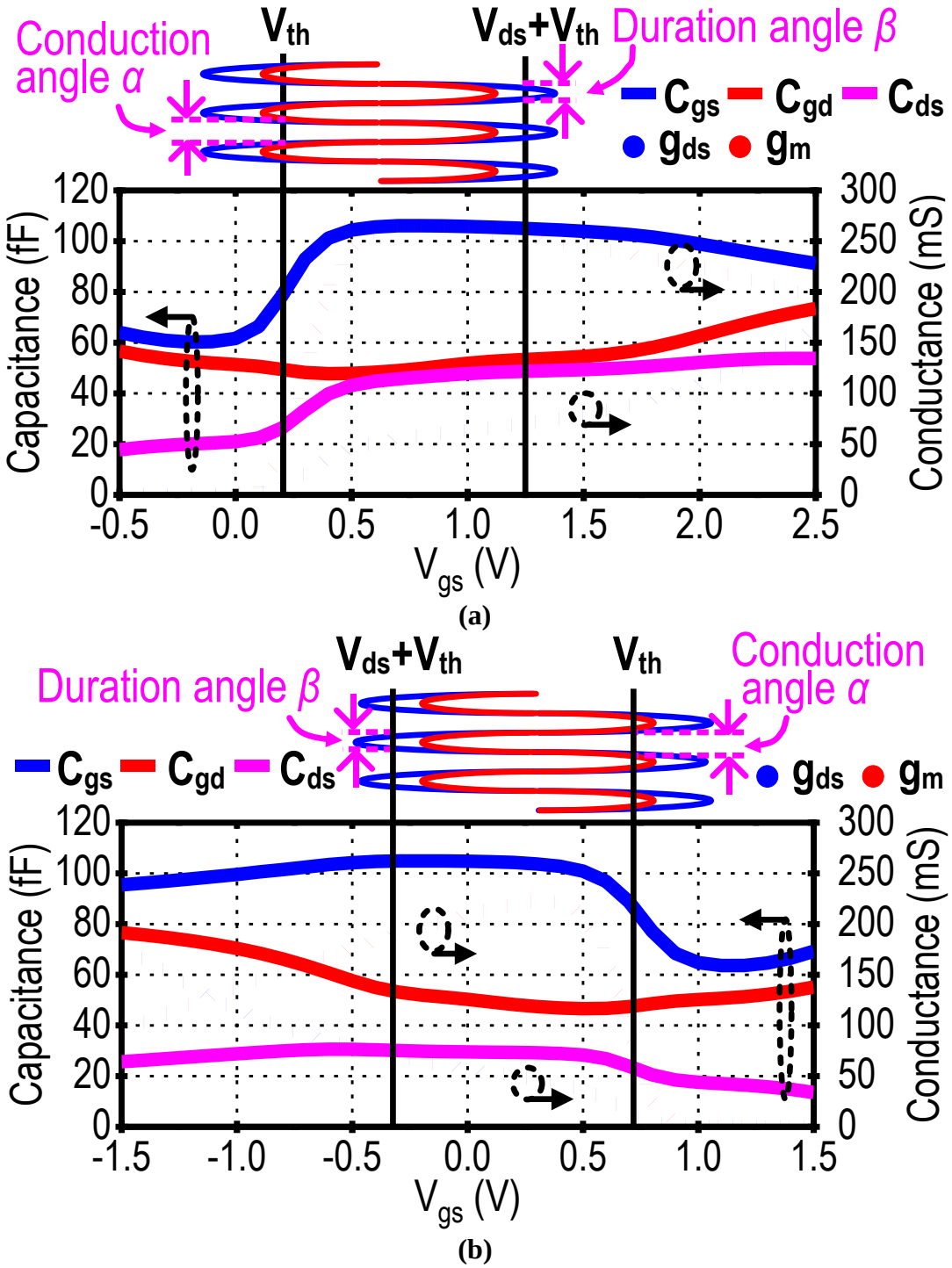


Figure 3.2 – The extracted gate-to-source C_{gs}, gate-to-drain C_{gd} and drain-to-source C_{ds}, and transconductance g_m and drain-to-source conductance g_{ds} in (a) NMOS and (b) PMOS transistor.

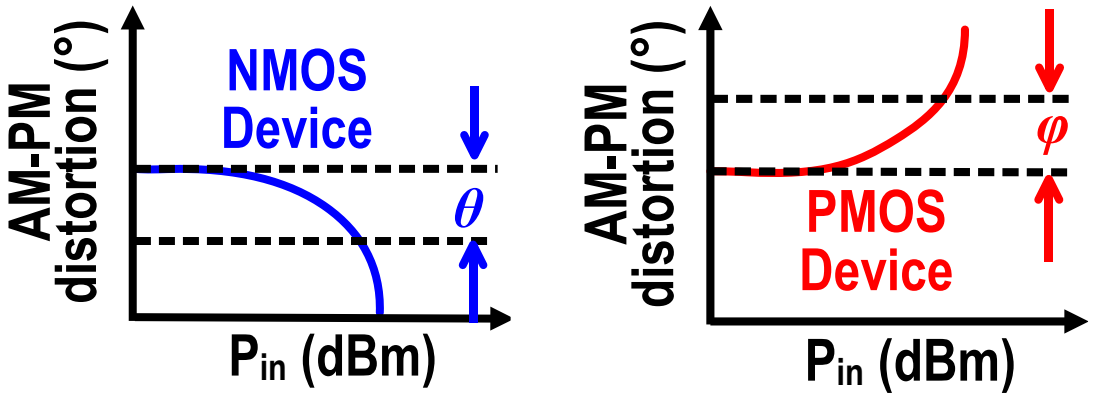


Figure 3.3 – The AM-PM behaviors of NMOS and PMOS PAs.

3.3. Proposed NMOS/PMOS AM-PM Nonlinearity Cancellation Scheme

3.3.1. Concept of doubly NMOS/PMOS nonlinearity cancellation scheme

Figure 3.4 shows the design concept and diagram of our proposed doubly NMPS/PMOS nonlinearity cancellation scheme. According to Equation (11) and (12), the NMOS PA shows a static negative phase shift (i.e., $\angle$-θ) and contrarily the PMOS PA shows a static positive phase shift (i.e., $\angle\varphi$) at P_{1dB}, as also shown in Figure 3.3.Thus, the PDR stage and DR stage provide negative and positive AM-PM distortions $\angle$-θ_{PDR} and $\angle\varphi_{DR}$, respectively. The first hybrid nonlinearity cancellation scheme cascade PDR and DR stages to achieve the overall AM-PM distortion $\angle(-\theta_{PDR} + \varphi_{DR})$ at the output of DR stage. So, we can minimize $\angle(-\theta_{PDR} + \varphi_{DR})$ by optimizing proper bias voltage settings for PDR and DR stages, which provides a high-quality signal to feed the PA stage. Similarly, the NMOS PA and PMOS PA provide negative and positive AM-PM distortion $\angle$-θ_{PA} and $\angle$-θ_{PA}, respectively. So, the second hybrid nonlinearity cancellation scheme combines NMOS PA and PMOS PA at PA stage to achieve the total AM-PM distortion of $\angle(-\theta_{PDR} + \varphi_{DR} + \varphi_{PA} - \theta_{PA})$ at the load R_L. Also, the total AM-PM distortion can be

optimized by adopting appropriate bias voltage settings for NMOS PA and PMOS PA at PA stage. Namely, we mix the PRD-DR and hybrid NMOS/PMOS PA nonlinearity cancellation to offer a doubly nonlinearity cancellation for the superior linearity performance. Besides, AM-AM peaking, caused by the nonlinear transconductance g_m (α, β), can be suppressed by our doubly NMPS/PMOS nonlinearity cancellation technique with appropriate biasing settings, allowing an overall AM-AM cancellation.

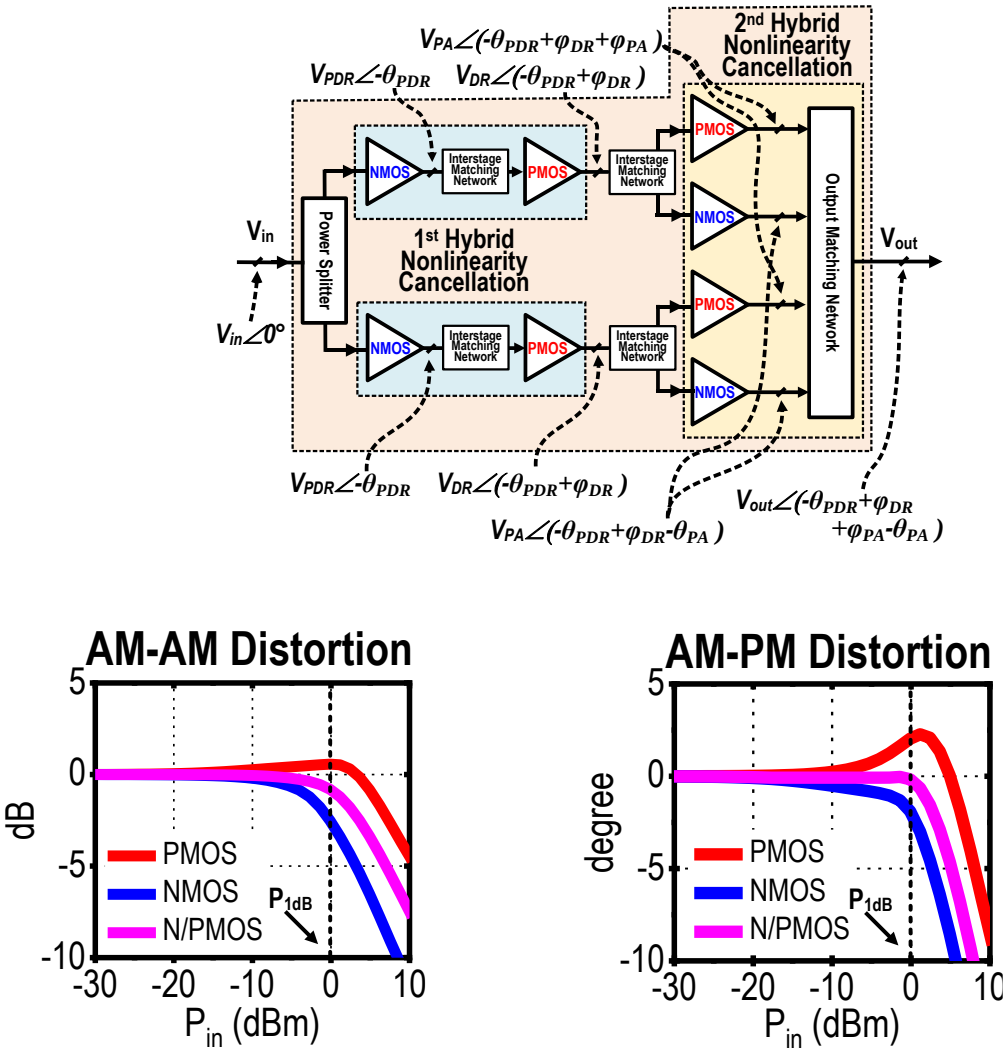


Figure 3.4 − The concept of the proposed doubly nonlinearity cancellation scheme.

3.3.2. PA output network NMOS/PMOS Linearity Improvement Scheme

Our proposed PA leverages these device nonlinearity properties by combining the output drain currents of NMOS and PMOS PAs through a DAT power combiner for nonlinearity cancellation (Figure 3.5). The differential input signals V_{inn}^{+}/V_{inn}^{-} and V_{inp}^{+}/V_{inp}^{-} drive the NMOS and PMOS PAs, and the resulting NMOS/PMOS PA drain currents are I_n and I_p, respectively. The drain currents In and Ip further induces I_n' and I_p' and combines as $I_{n/p}$ at the secondary coil of the combiner, where they cancel the opposite AM-AM/AM-PM behaviors caused by the nonlinear capacitors and transconductances g_m. The AM-AM and AM-PM distortion curves for NMOS/PMOS-only PAs and the proposed hybrid PA are shown in Figure 3.4. The combined current $I_{n/p}$ presents complementary amplitude/phase behaviors and minimizes the AM-AM and AM-PM distortions at P1dB for superior linearity performance. Moreover, since NMOS and PMOS PAs are both loaded by transformers, both can achieve full voltage swings and avoid headroom issues due to V_{knee} and limited V_{DD} without losing power and efficiency.

3.3.3. Series-Parallel DAT Output Power Combiner

This series-parallel DAT-based power combiner consists of a differential transformer network with eight single-ended (i.e., four differential) primary inputs and a differential secondary output connected to the load (R_L). The eight single-ended inputs driven by the differential outputs of total four NMOS/PMOS PAs. Additionally, two pairs of NMOS and PMOS PAs are placed oppositely for simple DAT routing and V_{DD}/GND arrangement (Figure 3.6).

A DAT-based power combiner is realized by a slab type transformer to achieve both higher quality factor and series power combining for the two NMOS PAs or two PMOS PAs, while the parallel combining is used to combine the NMOS/PMOS PA outputs for nonlinearity cancellation [99]. The outer diameter of the series-parallel DAT is 130 μm. The coil width is 8μm, and coil-coil spacing is 3 μm. The primary coils use one 3.9μm copper layer (OB layer) for the signal traces and the DC paths to NMOS PA V_{DD} with another 3.9 μm copper layer (OA layer) as the DC underpasses to PMOS PA GND, while the secondary coil uses the top 4.1μm aluminum (LD layer). Importantly, the two primary coils are not connected while the correct DC voltages DAT operation are provided. The simulated passive efficiency of the proposed output network is over 80% from 40 to 70 GHz (Figure 3.7).

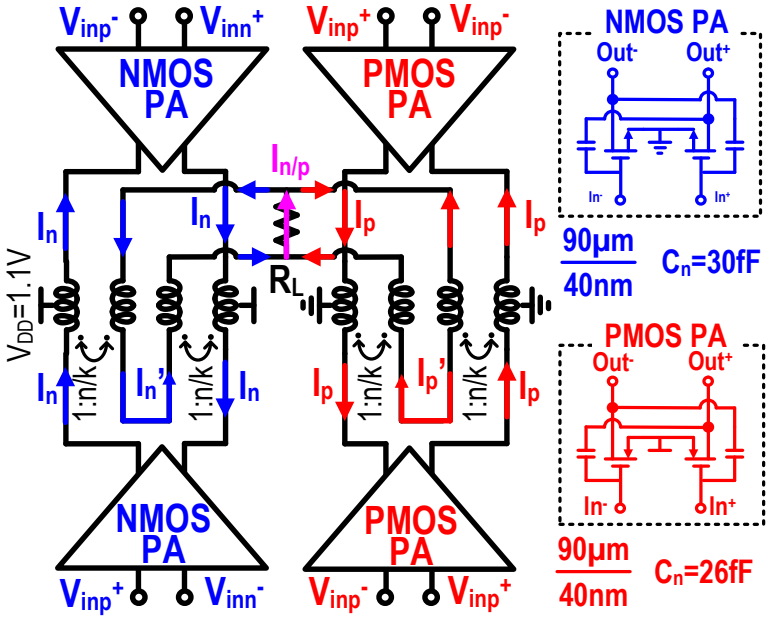


Figure 3.5 − The schematic of the hybrid NMOS/PMOS nonlinearity cancellation scheme.

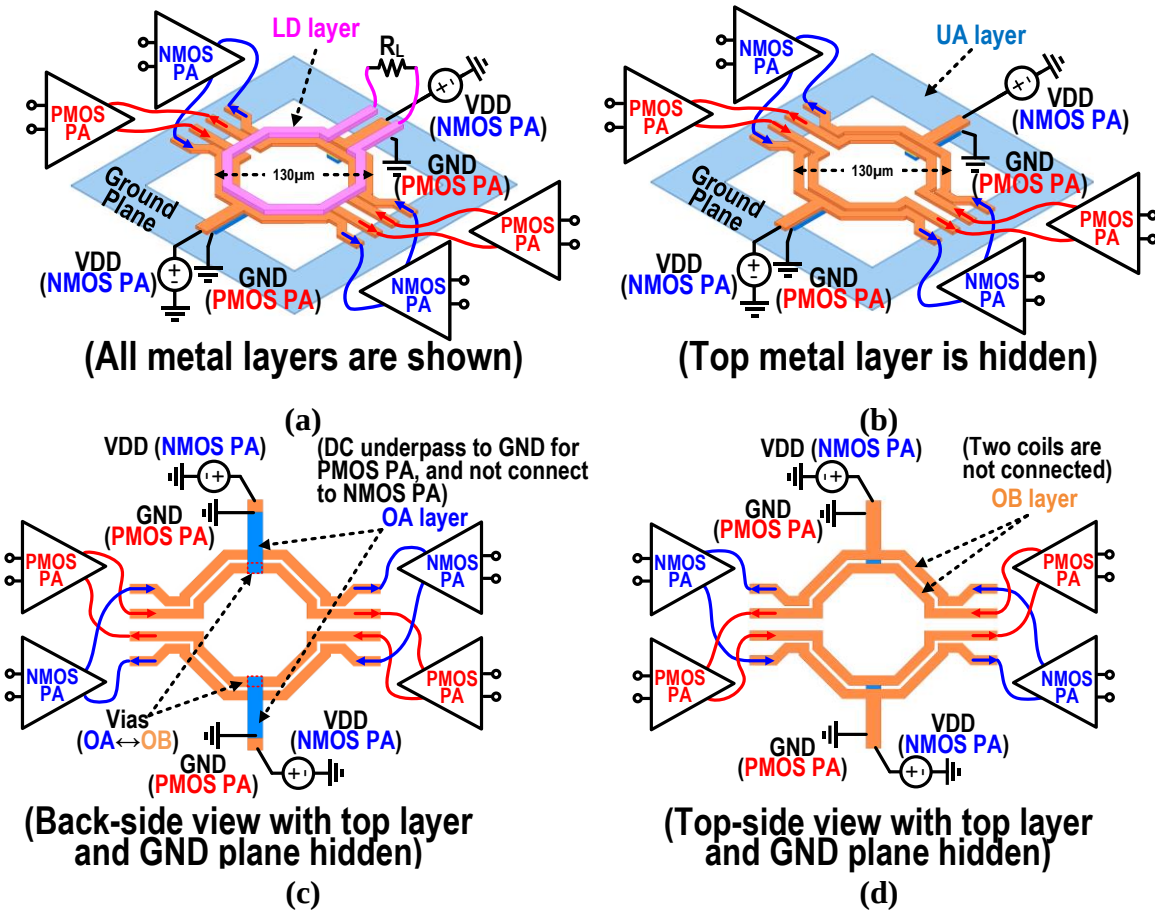


Figure 3.6 – The 3D EM model of the hybrid NMOS/PMOS nonlinearity cancellation PA with 4-way series-parallel DAT.

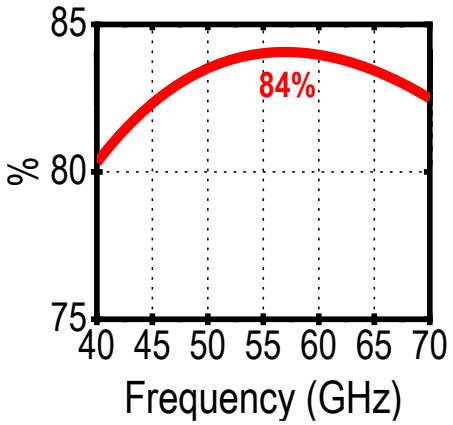


Figure 3.7 – The simulated passive efficiency of the proposed series-parallel DAT.

3.4. PA Implementation

Figure 3.8 shows the schematic of the proposed doubly hybrid NMOS/PMOS nonlinearity cancellation PA. This PA is implemented in GlobalFoundries 45nm CMOS SOI process. To provide desired gain and output power, this PA employs two PA branches, each branch includes three stages, such as PA, DR, and PDR. All three stages adopt common-source topology with neutralization capacitors to improve power gain, reverse isolation and stability. Moreover, each PA consists of both NMOS and PMOS devices, while the DRs and the PDRs adopt PMOS and NMOS devices respectively. Such a double-hybrid configuration achieves further PA nonlinearity cancellations as discussed in the previous section. The V_{DD} for the PA, DR and PDR stages are 1.1V, 0.9V and 0.8V, respectively. Moreover, the neutralization capacitors for each stage (e.g., C_{n_nmos}, C_{n_pmos}, C_{n_DR} and C_{n_PDR}) are 30 fF, 37 fF, 26 fF and 12 fF, respectively. The size ratio between PA, DR and PDR is 3(×2):3:1, and the practical PA size is marked in Fig. 3.9. The inter-stage transformer matching network between the PA and DR stages also serves as a 1:2 power splitter to feed both PMOS and NMOS PAs. Proceeding each PDR, a transformer balun transfers the single-ended input signal to the differential signal. For acquiring a better matching between each branch, a single-ended signal is directly split by two equal length transmission lines, instead of using a differential signal. Thus, the input matching network ties the balun of each path by the transmission lines (180 μm, Z0=66 Ω) and employs two parallel 30 fF capacitors and one series capacitor 35 fF at the pad for input matching. Figure 3.9 shows the chip microphotographic of our proposed PA, it occupies a 0.66×0.27 mm^2 core area excluding pads. This PA is measured by direct probing.

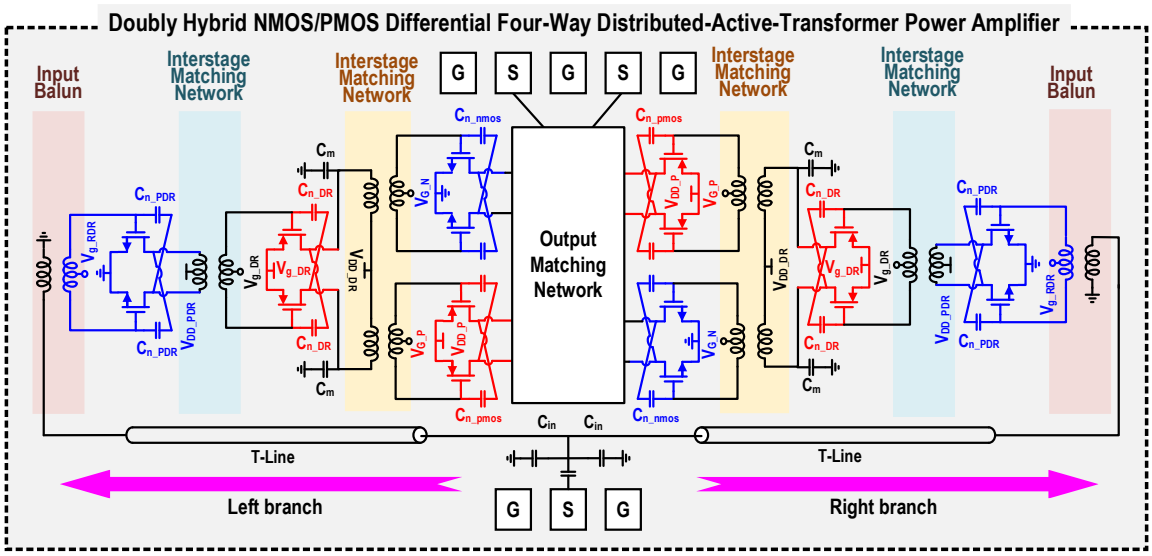


Figure 3.8 – The schematic of the proposed PA.

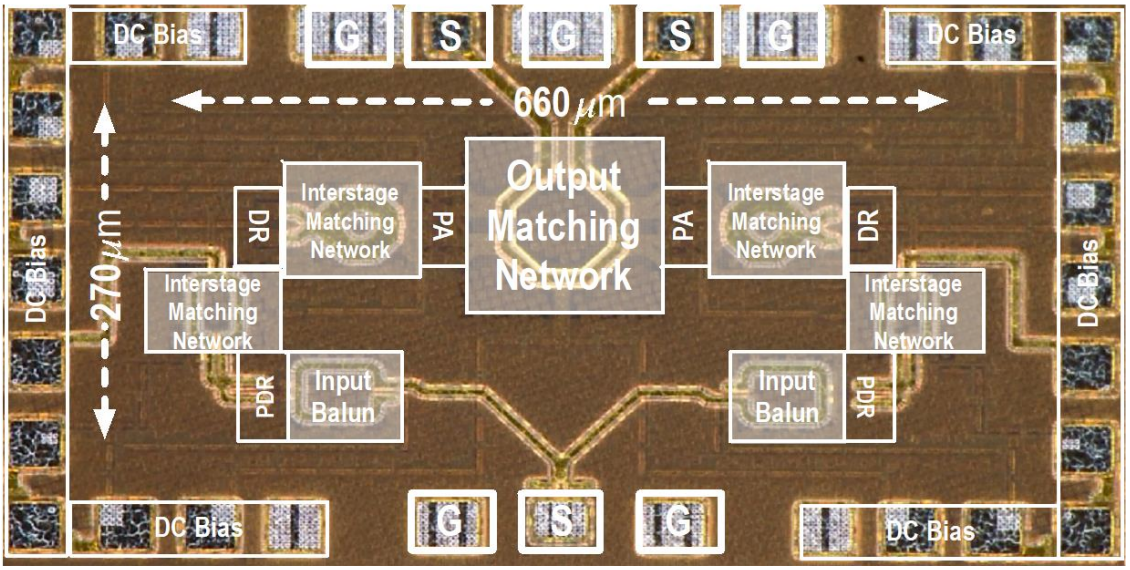


Figure 3.9 – The chip microphotographic.

3.5. Measurement Results

A giant benefit of our proposed PA is that the bias voltages (e.g., V_{Gnmos} and V_{Gpmos}) for the NMOS and PMOS PAs can be set independently. Unlike ref. [109], for this inverter-like NMOS/PMOS topology, the NMOS and PMOS transistors are physically connected, which cannot arbitrarily set gate voltage bias for NMOS and PMOS PA respectively, since their bias points are associated substantially, the same as the similar topology in ref. [109]. Thus, our hybrid NMOS/PMOS PA topology can provide contour plots (Figure 3.10) with different NMOS and PMOS gate voltage bias settings of the measured (a)AM-AM distortion, (b) AM-PM distortion, (c) P_{sat}, (d) OP_{1dB} (e) G_p, (f) PAE_{max}, (g) PAE_{P1dB}, and (h) PAE at 6dB PBO (PAE_{6dB_PBO}) at 55 GHz, respectively. In those contours, the V_{Gnmos} is varied from 0.2 V to 0.4 V, while V_{Gpmos} is varied from 0.7 V to 0.9 V, and the voltage step is 0.02V for each one.

Those contours show that the PA can be optimized for one or multiple performance specifications. A high-linearity mode (HLM) and a high-efficiency mode (HEM) are selected with different bias settings. HLM is set as (V_{Gnmos}, V_{Gpmos}) = (0.26 V, 0.82 V) and HLM is set as (V_{Gnmos}, V_{Gpmos}) = (0.22 V, 0.86 V), respectively. The detailed PA performance for each mode are shown in the following section. Figure 3.11 shows the CW large-signal measurements for HLM and HEM respectively at 55 GHz, highlighted as yellow and magenta stars. HLM achieves 16.3 dBm P_{sat}, 13.5 dBm OP_{1dB}, 18.8dB G_p, 35.4% PAE_{max}, 28.9% PAE at P_{1dB} (PAE_{P1dB}) and 16.9 % PAE_{6dB_PBO}. On other hand, HEM achieves 16.1 dBm P_{sat}, 15 dBm OP_{1dB}, 16.4 dB G_p, 36% PAE_{max}, 35.2 % PAE_{P1dB} and 18.6 % PAE_{6dB_PBO} at 55 GHz. Additionally, at 55 GHz and P_{1dB}, HLM achieves almost no AM-AM peaking and 0.4 ° AM-PM distortion, and HEM also achieves almost no AM-

AM peaking and 3.5 ° AM-PM distortion. The measured large-signal performance and small-signal S-parameters are summarized over frequency. The peak S_{21} is 18.8 dB with 3-dB bandwidth of 52.7-57.2 GHz. Table 3.1 summarizes a comparison table to show the CW performance with other state-of-the-art PA designs at the related frequencies.

Figure 3.12 shows the single-carrier 64-QAM modulation measurements without digital predistortion (DPD). At 55 GHz, our PA achieves 15.6/12.1 % PAEavg, 9.5/9.4 dBm Pavg, -25.2/-25.4 dB rms EVM (EVM_{rms}), and 30.3/31 dBc Adjacent Channel Power Ratio (ACPR) for 0.5/1 GSym/s 64-QAM, respectively. In addition, at 2/3 GSym/s, it achieves 10.5/9.1 % PAEavg, 8.7/8.1 dBm Pavg and -25.2/-24.5 dB EVMrms. The PA achieves the single-carrier 64-QAM highest modulation rate of 3 GSym/s (18 Gb/s) among the reported V-band silicon PAs. Note that due to the limited equipment bandwidth, the ACPR values cannot be accurately measured at 1 GSym/s and 3 GSym/s.

From Figure 3.13 to Figure 3.16, it shows the 5G NR CP-OFDM FR2 64-QAM modulation measurements at fcarrier of 55 GHz without DPD for various CC and modulation bandwidth. For 1-CC/2-CC FR2 400 MHz (total 400/800 MHz), our PA achieves 14.5/9.5 % PAE_{avg}, 10.8/8.67 dBm P_{avg}, -23.5/-23.1 dB EVM_{rms}, and -25.8/-26.4 dBc ACPR. Additionally, For 4-CC, our PA is measured with FR2 100 MHz and 200 MHz (total 400 MHz and 800 MHz) respectively, it achieves 12.3/8.1 % PAE_{avg}, 10/8.9 dBm P_{avg}, -23.1/-23.3 dB EVM_{rms}, and -24.5/-24.6 dBc ACPR. The PA performance comparisons with other state-of-the-art mm-Wave PA designs at the related frequencies are exhibited in Table 1. The PA achieves the single-carrier 64-QAM highest modulation rate of 3 GSym/s (18 Gb/s) among the reported V-band silicon PAs.

Figure 3.17 shows the 5G NR CP-OFDM 64-QAM 1-CC FR2 400 MHz modulation measurements at $f_{carrier}$ of 55 GHz with respect to the different supply voltages V_{DD}., e.g., (a) P_{avg}, (b) PAE_{avg} and (c) ACPR. When the V_{DD} increases, the P_{avg} increases accordingly at the EVM ≤ -24 dB. On other hand, for PAE_{avg}, at lower EVM values, for example EVM ≥ -23 dB, the PAE_{avg} for each V_{DD} value is close. However, the PA supplied with lower V_{DD} cannot maintain enough linearity for the low EVM requirement (i.e., EVM ≤ -24 dB). Figure 13(c) shows ACPR values are very similar when the proposed PA is supplied with the given V_{DD} values. Table 3.2 also summarizes a comparison table to show the modulation measurements with other state-of-the-art PA designs at the related frequencies.

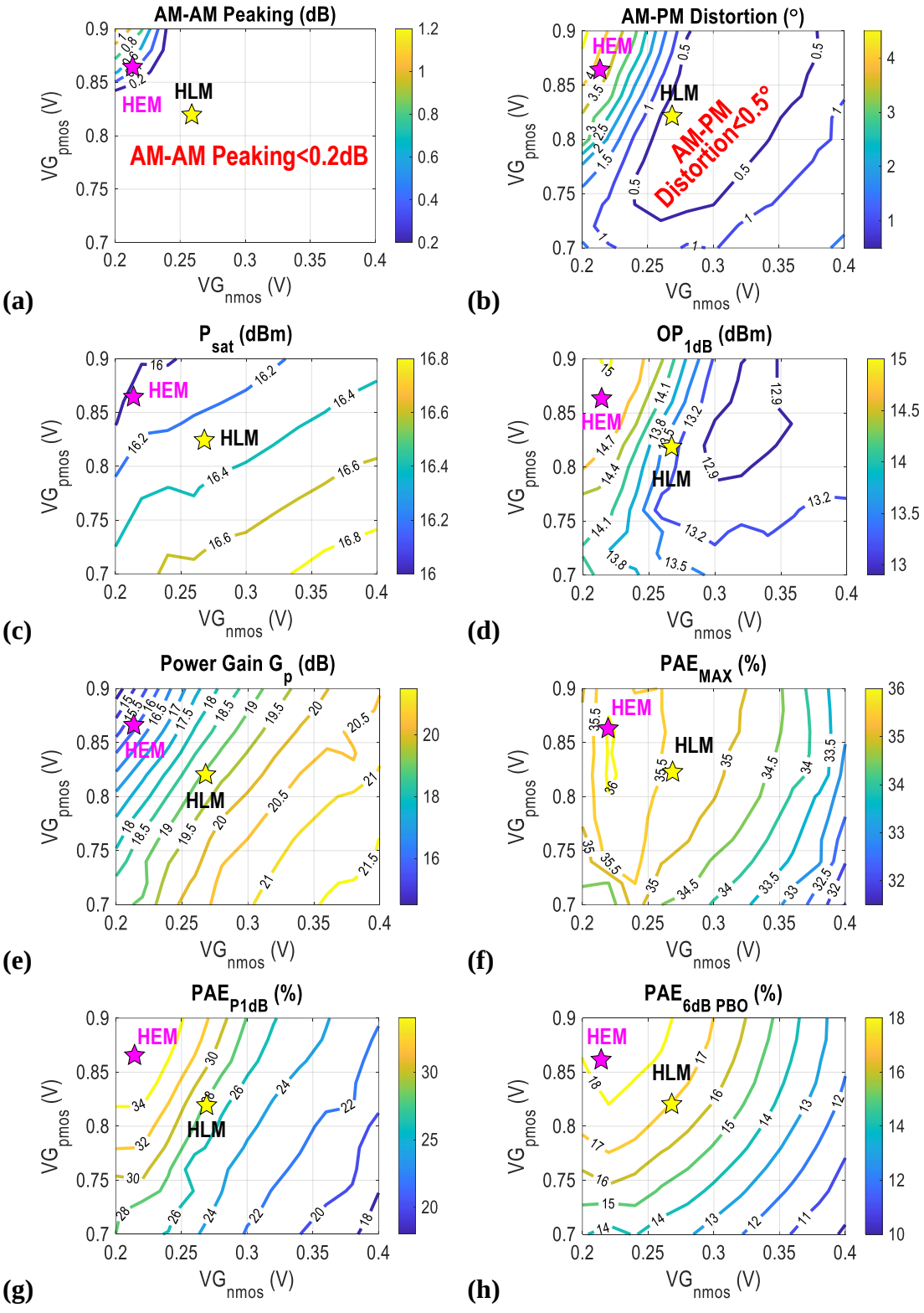


Figure 3.10 − Measured CW performance vs. the gate voltages, e.g., (a)AM-AM distortion, (b) AM-PM distortion, (c) P_{sat}, (d) OP_{1dB} (e) G_p, (f) PAE_{max}, (g) PAE_{P1dB}, and (h) PAE_{6dB_PBO}.

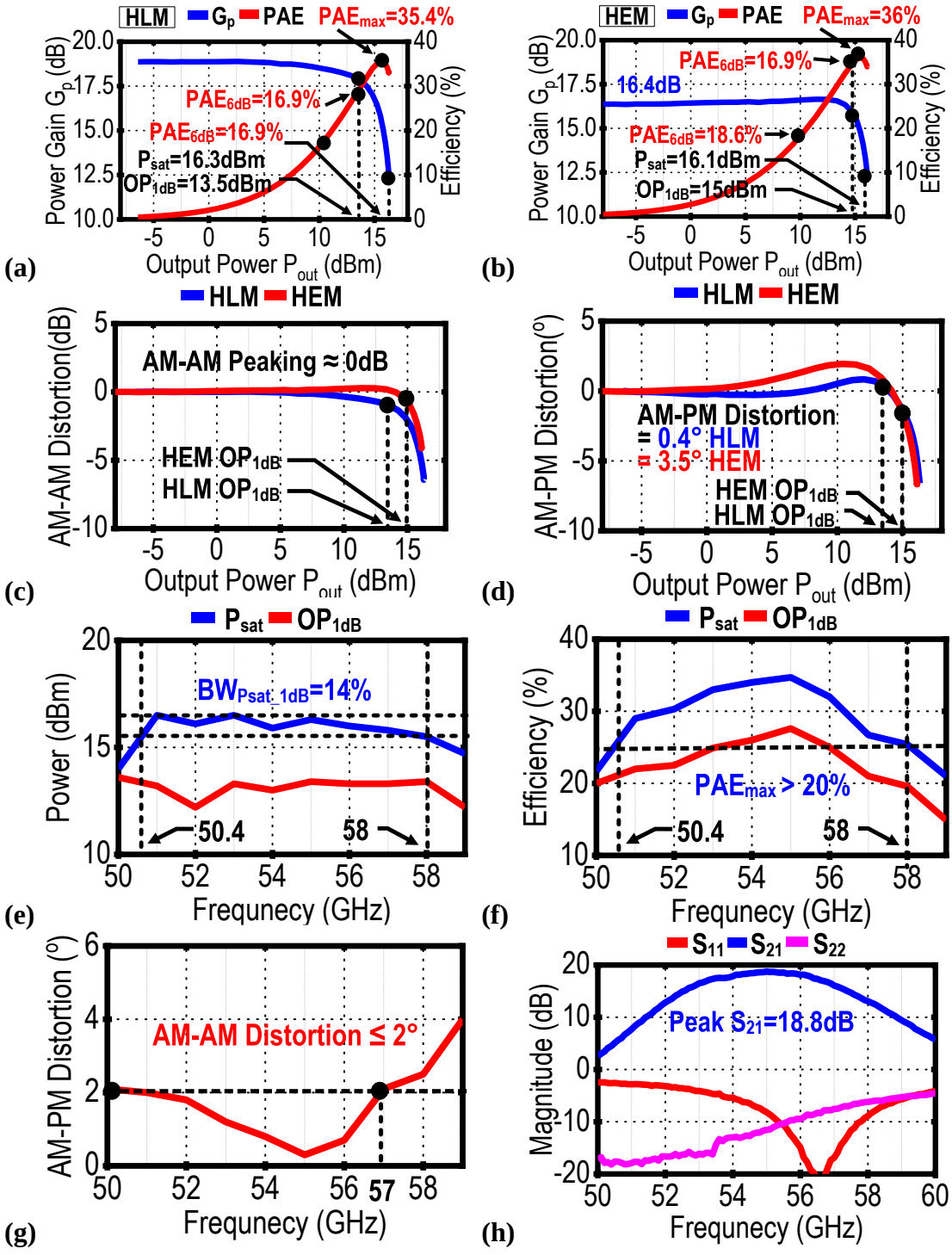


Figure 3.11 – (a) the measured CW large-signal performance at 55GHzfor High-Linearity-Mode (HLM), (b) the measured CW large-signal performance at 55GHz for High-Efficiency-Mode (HEM), (c) the AM-AM distortion, (d) the AM-PM distortion, (f) the delivery power, (g) the efficiency and (h) The S-parameters.

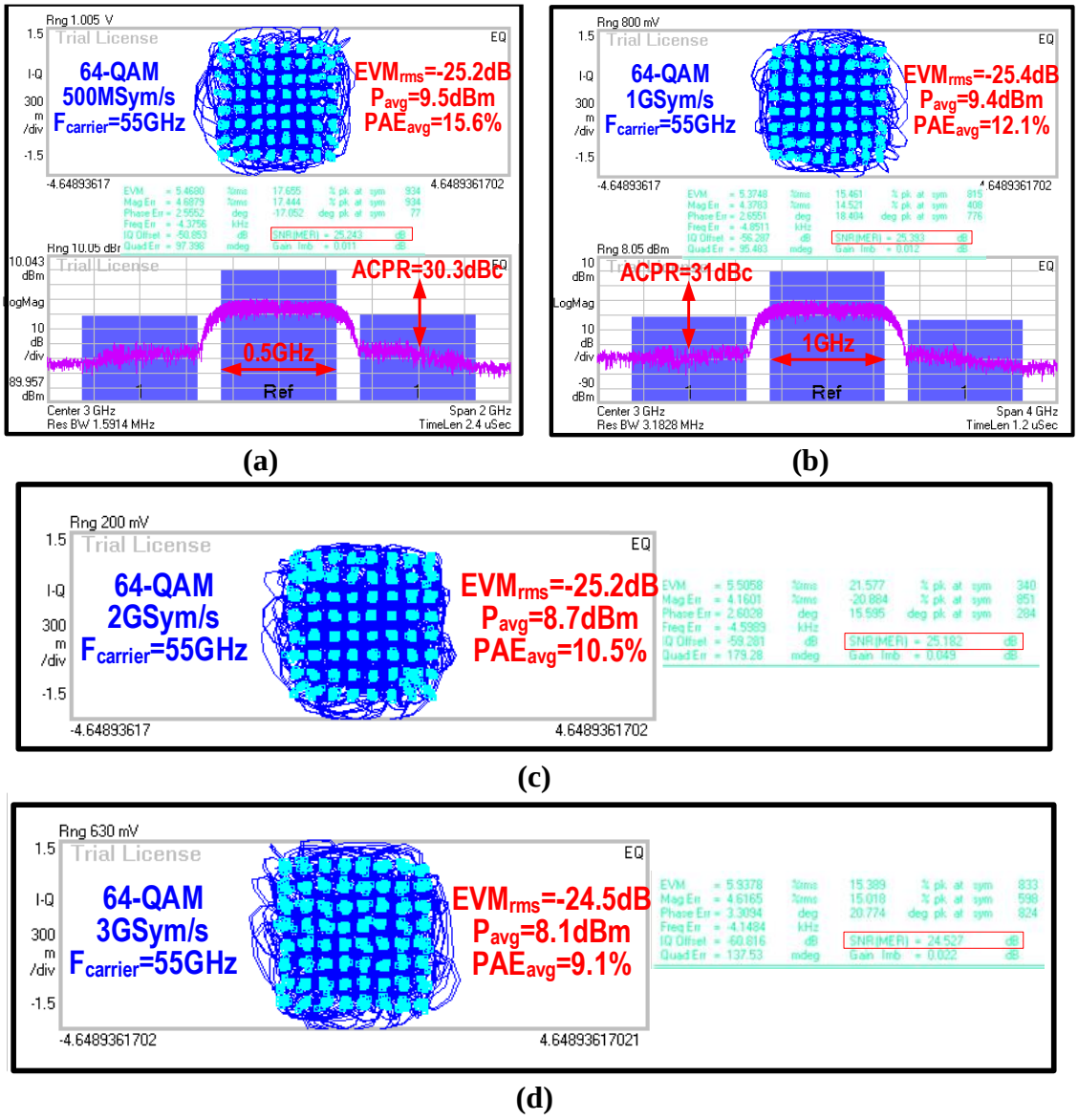


Figure 3.12 − The single-carrier 64-QAM modulation results at (a) 0.5 GSym/s, (b) 1 GSym/s, (c) 2 GSym/s and (d) 3 GSym/s. For 1 GSym/s and 3 GSym/s, due to the limited equipment bandwidth, their ACPR values cannot be accurately measured.

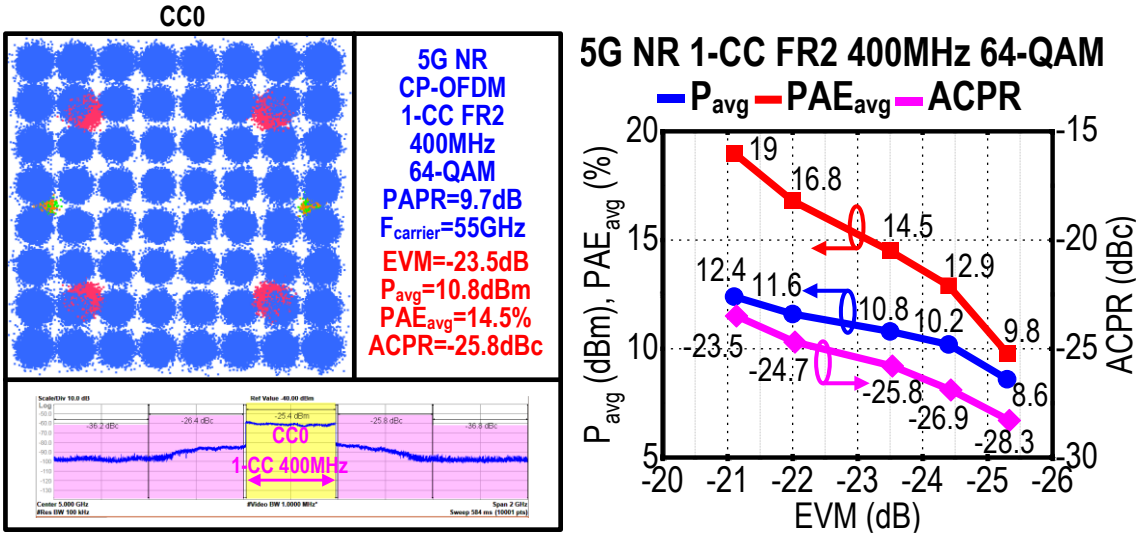


Figure 3.13 − The 5G NR 64-QAM CP-OFDM modulation results with 1-CC FR2 400MHz.

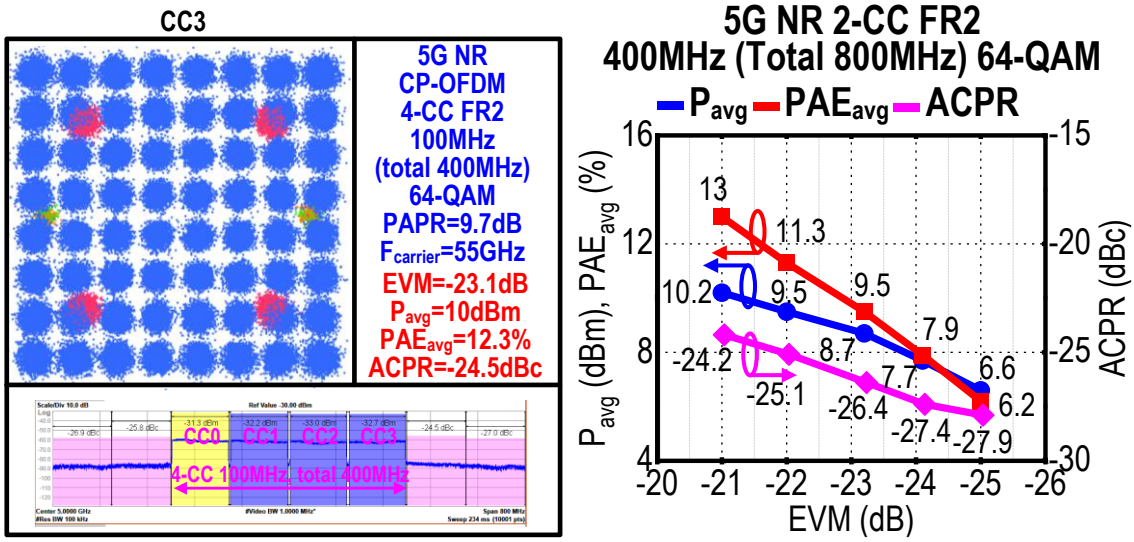


Figure 3.14 − The 5G NR 64-QAM CP-OFDM modulation results with 2-CC FR2 400MHz.

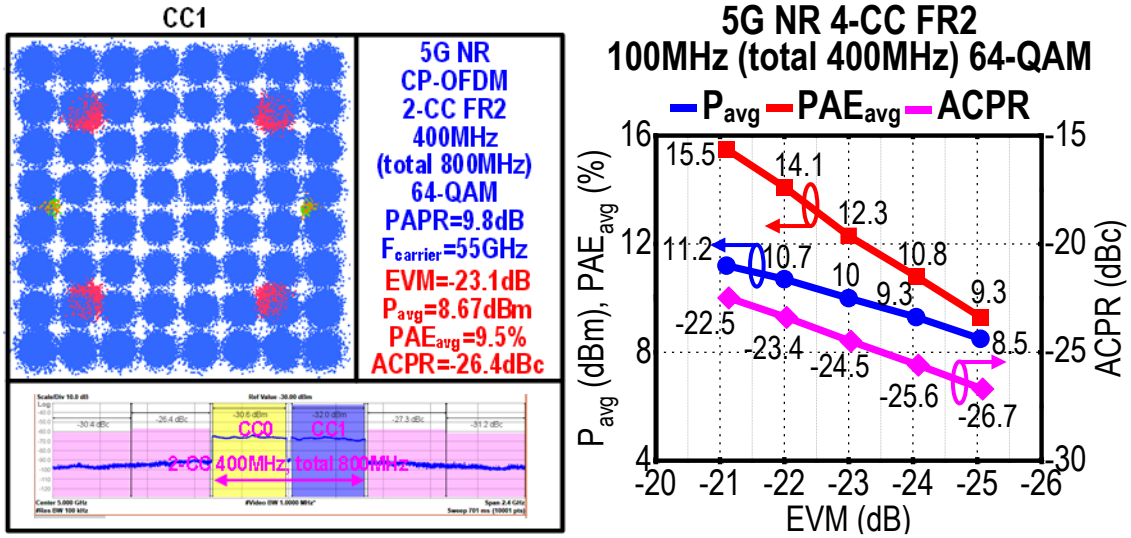


Figure 3.15 − The 5G NR 64-QAM CP-OFDM modulation results with 4-CC FR2 100MHz.

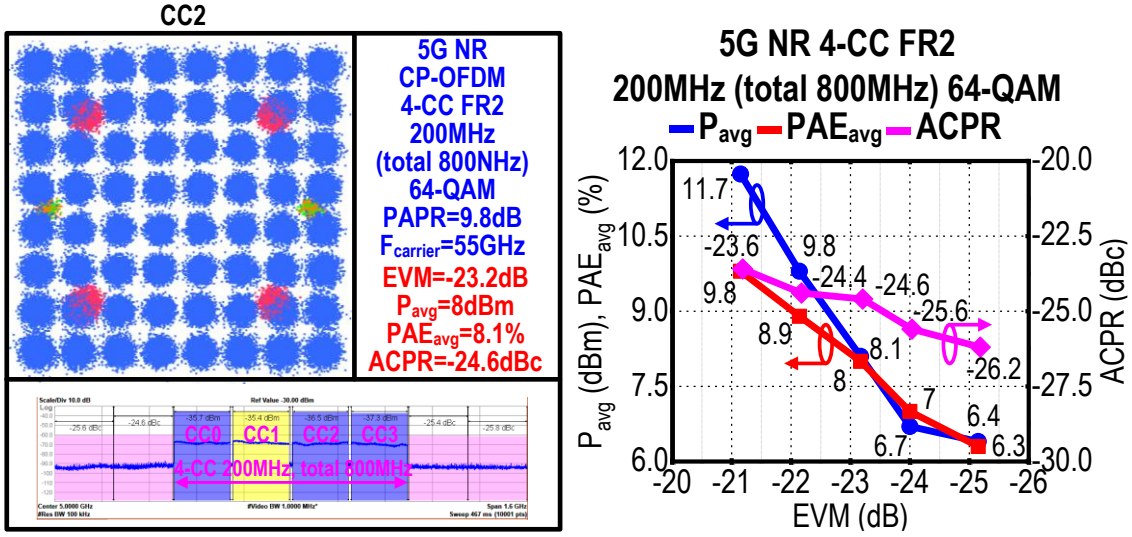
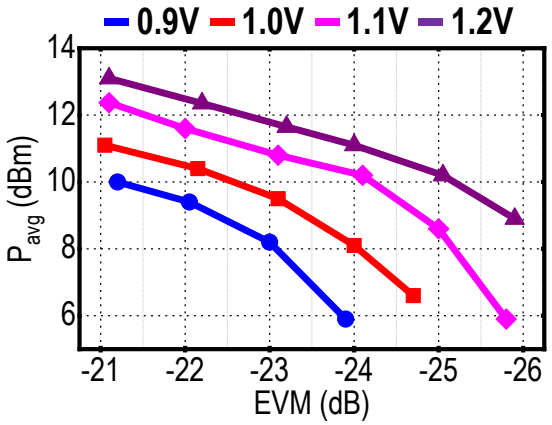
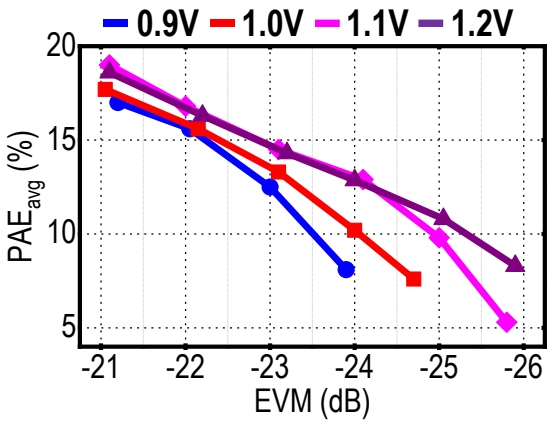


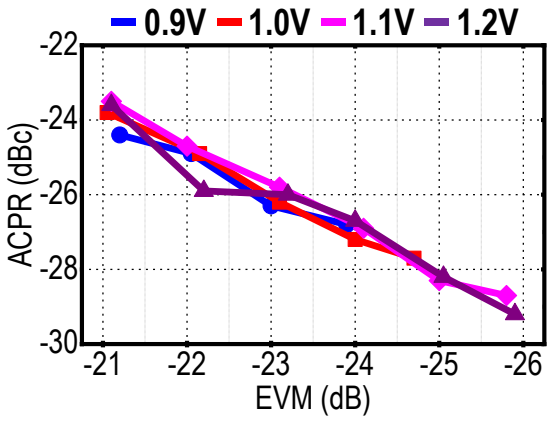
Figure 3.16 − The 5G NR 64-QAM CP-OFDM modulation results with 4-CC FR2 200MHz.



(a)



(b)



(c)

Figure 3.17 − The measured 5G NR 64-QAM CP-OFDM 1-CC FR2 400MHz modulation results, e.g., (a) P_{avg}, (b) PAE_{avg} and (c) ACPR with various V_{DD} values (V_{DD} = 0.9, 1.1, 1.1 and 1.2 V).

Table 3.1 – CW Performance Comparison with The State-Of-The-Art Silicon-Based Mm-Wav E PA at Related Frequency

	V_{DD} (V)	Freq. (GHz)	Gain (dB)	P_{sat} (dBm)	OP_{1dB} (dBm)	PAE_{max} (%)	PAE_{P1dB} (%)	PAE_{6dB_PBO} (%)	Tech.	Topology	Core area (mm^2)
HLM	1.1	55	18.8	16.3	13.5	35.4	28.9	16.9	45nm CMOS SOI	Doubly Hybrid NMOS/PMOS compensation w/ 4-way series-parallel DAT	0.18
HEM			16.4	16.1	15	36	35.2	18.6			
Zhao JSSC 13'	1	60	17	17	13.9	30.3	21.7	8.4*	40nm CMOS	Diff. 2-way Class-AB	0.07
Kulkarni *TMTT 16'*	1.8	60	22.4	16.4	13.9	23	18.9	8	40nm CMOS	N/PMOS push-pull	0.08
Chappidi *ISSCC 16'*	4	55	18.8	23.6	19.9	27.7	15.7	11*	130nm SiGe	Asymmetric 2-way combiner	1.02
Chou TMTT 16'	1.2	60	20.1	20.6	17.6	20.3	8*	3*	90nm CMOS	Class-AB w/ radial combiner	0.43
Chen ISSCC 11'	1	60	20.3	18.6	15	15.1	6.8	2	65nm CMOS	3-stg. Class-AB	0.28
Jen	1.8	60	26.1	14.5	10.5	10.2	-	-	90nm CMOS	3-stg. w/ DAT combiner	0.64
TMTT 09'	3		26.6	18	14.5	12.2	-	-			
Varonen *JSSC 08'*	1.2	60	12.8	7	1.5	4*	-	-	65nm CMOS	3-stg. Sigle-ended Class-AB	0.61
Bassi *JSSC 15'*	1	53	13	13.3	12	16	-	-	28nm CMOS	2-stg. Diff. Class-AB	0.334#
Nguyen *RFIC 19'*	2	60	12.9	20.1	19.3	26.5	25.9	16.6 (7dB PBO)	45nm CMOS SOI	Coupler-Based Differential Doherty	0.76
Sun IMS 19'	2.4	58	19.6	22.2	19.7	17.8	-	-	90nm CMOS	2-stacked & 2-way Combiner	0.264
Chang TMTT 19'		60	29.7	23.7	19.9	22.1	11.1	-	65nm CMOS	3-stg. w/ 4-way combiner	0.653
Chu RFIC 20'	0.95	65	21.4	17.9	13.5	26.5	15	18	16nm FinFET CMOS	2/4-way Non-uniform combiner	0.14
Gong IMS 20'	2	60	17.3	24.4	23.9	14.2	-	-	90nm SiGe	Balanced PA w/ asymmetric coupled lines	1.22
Nguyen *ISSCC 18'*	1.9	65	-	19.4	19.2	28.3	27.5	20.1	45nm CMOS SOI	Multi-feed antenna-based Doherty	-

*Graphically estimated from reported figures, #The area including pads.

Table 3.2 – Modulation Comparison with The State-Of-The-Art Silicon-Based Mm-Wave PA at Related Frequency

	Carrier Freq. (GHz)	Modulation Scheme	Data Rate (Gb/s)	EVM (dB)	P_{avg} (dBm)	PAE_{avg} (%)
This design	55	Single Carrier 64-QAM	3	-25.2	9.5	15.6
			6	-25.4	9.4	12.1
			12	-25.2	8.7	10.5
			18	-24.5	8.1	9.1
		5G NR CP-OFDM 64-QAM	2.4 (1-CC FR2 400MHz, total 400MHz)	-23.5	10.8	8
			3.2 (2-CC FR2 400MHz, total 800MHz)	-23.1	10	12.3
			2.4 (4-CC FR2 100MHz, total 400MHz)	-23.1	8.7	9.5
			4.8 (4-CC FR2 200MHz, total 800MHz)	-23.2	8	8.1
Chappidi *ISSCC 16'*	55	Single Carrier 64-QAM	3	25**	12.8	-
Kulkarni *TMTT 16'*	60	Single Carrier 64-QAM	3	-25.2	7	-
Chu RFIC 20'	65	Single Carrier 64-QAM	6	-21.6	11.2	9.4
Nguyen *RFIC 19'*	60	Single Carrier 64-QAM	3	-23.1	13.8	15.7
Nguyen *ISSCC 18'*	65	Single Carrier 64-QAM	6	-26.7*	14.2	20.2

*EVM is normalized to peak, **No information about EVM normalization

3.6. Chapter Summary

We present a V-band doubly hybrid NMOS/PMOS differential four-way DAT-based power amplifier, implemented in 45-nm CMOS SOI process. The proposed doubly hybrid NMOS/PMOS nonlinearity cancellation can substantially improve the PA linearity. Additionally, the independent gate bias scheme can perform various contours of the measured PA performance metrics to optimize the PA performance in different operation modes, e.g., high-linearity mode (HLM) and high-efficiency mode (HEM) in this design. Also, the DAT-based transformer can combine both NMOS and PMOS PAs and show a low loss, compact and simple PA output network design. Thus, this PA design address the PA linearity-efficiency tradeoff. It provides a high linearity and efficiency simultaneously, achieving superior measured CW and modulation performance at V-band.

CHAPTER 4. A MILLIMETER-WAVE FULLY INTEGRATED PASSIVE REFLECTION-TYPE PHASE SHIFTER WITH TRANSFORMER-BASED MULTI-RESONANCE LOADS FOR 360° PHASE SHIFTING

4.1. Introduction

Passive phase shifters provide multiple benefits over active vector-modulator phase shifters [142]-[148], such as zero DC power consumption and superior linearity, which are essential in large-scaled and power-constrained phased array systems. Commonly used passive phase shifter topologies include switched-line [145], [146], travelling-wave [146], [148], loaded-line [147], switched-filter [149], [150], and reflection-type [151]-[172]. Switched-line and travelling-wave topologies both require one or multiple transmission lines, leading to excessive chip areas even at mm-Wave frequencies. Switched-filter topology replaces the transmission lines by high-/low-pass filters for size reduction, but it cannot provide continuous or dense phase shift. Loaded-line topology also experiences these similar issues.

4.2. Reported RTPS Topologies

Reflection-type phase shifter (RTPS) exhibits several unique advantages over the other passive phase shifter topologies, including continuous and dense phase shift, moderate size, and cascadable operation [151]-[172]. Therefore, RTPS is an excellent candidate to meet the stringent requirements in high performance phased array systems.

A single-ended RTPS typically consists of a 90° coupler and two identical tunable passive reflective loads, as shown in Figure 4.1. Popular tunable reflective load topologies include tunable capacitors, series L-C resonators, parallel L-C resonators, and C-L-C π-networks, and the impedance of the reflective load is tuned to achieve the desired phase shifting angle and range [151]-[172]. The design and limitation of these passive reflective load networks will be comprehensively analyzed in this paper. The phase shifting range of an RTPS is solely governed by the load reactance tuning range [151]-[172]. However, the passive loss substantially limits the reactance tuning range of the reflective loads and also the phase shifting range of the RTPS. In practice, the phase shifting range of one mm-Wave RTPS is usually around or below 180°[159]-[164]. Based on the reported RTPS, a high-order reflective load can extend the reactance tuning range and increase the phase shifting range. However, a high-order reflective load typically requires complicated passive designs and exhibits higher passive loss. Although some fully integrated low-GHz RTPS with high-order reflective loads achieve a 360° phase shifting range, they suffer from severe IL even at those low GHz frequencies [155]. Other low-loss 360° RTPS designs are discrete designs with high-quality passive loads at low GHz frequencies [151]-[154], and these 360° designs are unsuitable for mm-Wave fully integrated RTPS applications. Another practical approach is to cascade multiple mm-Wave RTPS designs to realize a wide phase shifting range [159]. Although this approach may achieve 360° phase shift, it often exhibits exceedingly high IL. For example, a reported 180° mm-Wave RTPS consists of two π-network loads with IL of 7.5dB [159], and cascading two of such RTPS designs for 360° phase shift will result in a total IL of 15dB. Thus, there exists a major challenge to realize a mm-Wave RTPS which can achieve full span 360° phase shift and low IL simultaneously.

4.3. RTPS Design Challenge

To address this challenge, we propose a fully integrated differential mm-Wave RTPS that employs two transformer-based 90° couplers and two transformer-based multi-resonance reflective loads to simultaneously achieve a full span 360° phase shift, low IL, and an ultra-compact chip area [171]. Other non-silicon technologies, such as MEMS RTPS or hybrid integration of MEMS and CMOS RTPS, can achieve higher FoM [152], [153]. However, using phase shifters of non-silicon technologies with silicon-based transceiver circuits will require heterogeneous integration or careful packaging, which will increase the cost, integration complexity, and possible performance degradation for mm-Wave operations in practice. Our proof-of-concept design is fully integrated in commercially available standard 130nm BiCMOS process. It covers a full span 360° phase shifting range from 58GHz to 64GHz, and demonstrates the lowest IL, the smallest IL variation, and the best RTPS figure-of-merit (FoM) of 37.1°/dB compared with other reported 60GHz RTPS designs [159]-[161], [164].

4.4. Reflective Load Designs in RTPS

In this section, we will present several reported reflective load topologies and their load impedance tuning range. The phase shift limit of each reflective load will also be discussed. We will also present our proposed transformer-based multi- resonance load and its achievable 360° phase shifting range.

Figure 4.1 demonstrates a generic RTPS design with its signal path and the input/output phase shift. First, the input signal is split to two paths with 90° phase difference by the 90° coupler. Next, the resulting two split signals are reflected from the

two reflective loads at the through and couple ports. Assume that these two reflective loads are identical, the two reflected signals will be combined in-phase at the RTPS output (the isolation port) to generate the desired output phase shift. At the same time, the two reflected signals will cancel each other at the input port and result in the desired input matching. Assume that the two reflective loads and the 90° coupler are lossless, the total phase shift can be obtained as

$$\theta = -90° - 2\tan^{-1}\left(\frac{X_L}{Z_0}\right) = -90° - \angle\Gamma, \tag{4-1}$$

where X_L is the reflective load impedance; Z_0 is the characteristic impedance of the 90° coupler; Γ is the reflection coefficient of X_L normalized by Z_0 [159], [163], [168]. Therefore, the output phase shift of an RTPS is now equivalently expressed as the phase of the load reflection coefficient $\angle\Gamma$. This relationship will be used to facilitate the RTPS load design and analysis in this paper. Note that Γ is on the unit circle of the Smith chart for lossless reflective loads. To synthesize the desired phase shift, X_L is varied from $X_L^{\min}$ to $X_L^{\max}$, and the phase shifting range $\Delta\theta$ is thus found as

$$\Delta\theta = \theta_{\max} - \theta_{\min} = 2\left[\tan^{-1}\left(\frac{X_L^{\max}}{Z_0}\right) - \tan^{-1}\left(\frac{X_L^{\min}}{Z_0}\right)\right] = \angle\Gamma\left(X_L^{\min}\right) - \angle\Gamma\left(X_L^{\max}\right). \tag{4-2}$$

From equation (4-2), the phase difference of the two reflection coefficients, i.e., $\Gamma(X_L^{\max})$ and $\Gamma(X_L^{\min})$, should be maximized to achieve a wide phase shifting range $\Delta\theta$. Next, we will present several reported reflective load configurations and our proposed transformer-based multi-resonance load. Their load impedance tuning limits and the achievable phase shifting ranges are also analyzed. For simplicity, the following analyses

assume that the passive reflective loads and the 90° coupler are both lossless.

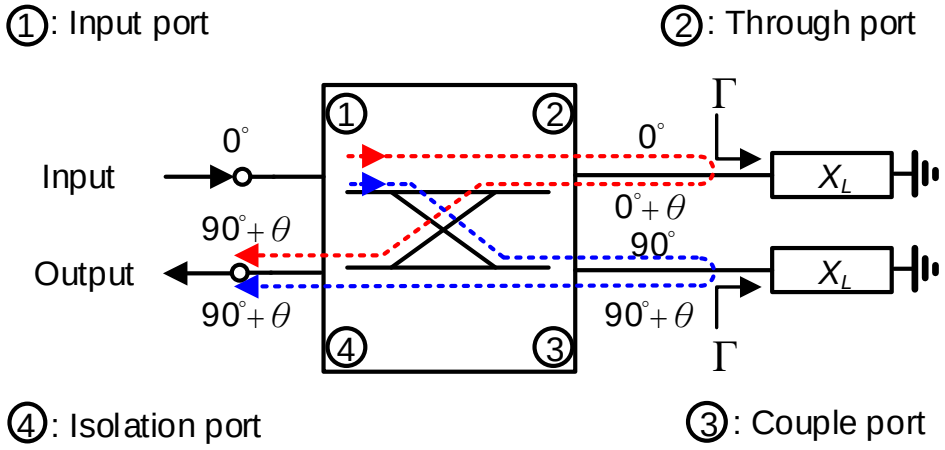


Figure 4.1 – A single-ended reflection-type phase shifter (RTPS).

4.4.1. Capacitive load (CL)

The simplest reflective load in an RTPS is a capacitive load (CL) [155]-[158], e.g., a varactor or a switch-controlled capacitor bank. Figure 4.2(a) shows the CL topology and its load impedance tuning trajectory along the unit circle on the Smith chart at a fixed operating frequency. The load impedance Z_L of the capacitance C is located at the half side of the Smith chart, and C is varied from C^{min} to C^{max}, e.g., the achievable minimum and maximum capacitance. Thus, the phase shift of CL is the phase difference of the load reflection coefficients by C^{min} and C^{max}. In practice, CL only provides a marginal phase shifting range due to its limited impedance tuning range. For a CL RTPS, the $\Delta\theta$, i.e., equation (4-2), can be expressed as

$$\begin{aligned}\Delta\theta &= 2\tan^{-1}\left(\frac{1}{Z_0\omega_0 C^{\min}}\right) - 2\tan^{-1}\left(\frac{1}{Z_0\omega_0 C^{\max}}\right) \\ &= 2\tan^{-1}\left(\frac{1}{Z_0\omega_0 C^{\min}}\right) - 2\tan^{-1}\left(\frac{1}{Z_0\omega_0 \alpha C^{\min}}\right).\end{aligned} \tag{4-3}$$

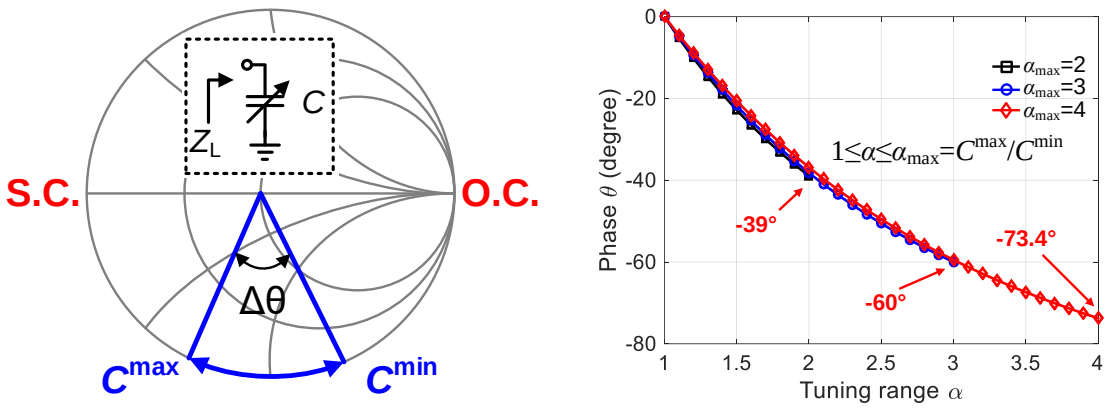
Assume α is the tuning range of the load capacitor and $\alpha_{\max}$ is its maximum value, i.e., $1 \le \alpha \le \alpha_{\max} = C^{\max}/C^{\min}$, and ω_0 is the operating frequency. Further, the $\Delta\theta$ of CL can be simplified as

$$\Delta\theta = 2\tan^{-1}\left[\frac{Z_0\omega_0 C^{\min}(\alpha - 1)}{\alpha\left(Z_0\omega_0 C^{\min}\right)^2 + 1}\right]. \tag{4-4}$$

For a given maximum capacitor tuning range $\alpha_{\max}$, the $\Delta\theta$ of CL can be maximized by choosing $C^{\min} = 1/\left(\sqrt{\alpha_{\max}} Z_0\omega_0\right)$, and the resulting maximum phase shifting range $\Delta\theta_{\max}$ of CL is

$$\Delta\theta_{\max} = 2\tan^{-1}\left(\frac{\alpha_{\max} - 1}{2\sqrt{\alpha_{\max}}}\right). \tag{4-5}$$

Figure 4.2(b) summarizes the $\Delta\theta$ versus $\alpha_{\max}$. For $\alpha_{\max}$=3, i.e., a typical tuning range for a varactor in silicon process, the $|\Delta\theta_{\max}|$ is only 60° (Figure 4.2b), matching the results in [156]. For $\alpha_{\max}$=4, the $|\Delta\theta_{\max}|$ only increases by 13.4°. In reality, the varactors or switch-controlled capacitor banks present passive loss, and the $|\Delta\theta_{\max}|$ is considerably reduced from the theoretical value. Thus, a CL RTPS only achieves limited phase shift in practice [156].



(a) **(b)**

Figure 4.2 – (a) The load impedance tuning range for a lossless capacitive load (CL) by tuning C, and (b) the simulated phase shifting range as the capacitor load tuning range α varies from 1 to its maximum value for different α_{max} (e.g., α_{max}=2, 3, or 4). Assume that the optimum C^{min} value, i.e., $C^{min} = 1/\left(\sqrt{\alpha_{max}} Z_0 \omega_0\right)$ is used in this CL RTPS design.

4.4.2. Series L-C resonant load (SLC)

To further extend the phase shifting range, series L-C resonant loads (SLC) are used in RTPS [155]-[158]. Assuming all the passive components are lossless, an SLC load generates a series resonance as a short circuit (S.C.) for the load impedance Z_L (Figure 4.3a). Increasing capacitance C_s makes Z_L inductive and then moves Z_L to approach Z_1; Z_1 is defined as the SLC load impedance Z_L at the maximum C_s as C_s^{max}. On the other hand, decreasing C_s makes Z_L capacitive and pushes Z_L to reach Z_2, which is the SLC load impedance Z_L at the minimum C_s as C_s^{min}. The phase shift of SLC load is realized by the phase difference between the reflection coefficients of Z_1 and Z_2. However, due to the limited tuning range of C_s in practice, an SLC RTPS cannot achieve a full span 360° phase shift [155]-[158].

The phase shifting range $\Delta\theta$ of an SLC RTPS can be expressed below, assuming C_s is varied from C_s^{min} to C_s^{max},

$$\Delta\theta = 2\tan^{-1}\left(\frac{\omega_0^2 L_s C_s^{max} - 1}{Z_0\omega_0 C_s^{max}}\right) - 2\tan^{-1}\left(\frac{\omega_0^2 L_s C_s^{min} - 1}{Z_0\omega_0 C_s^{min}}\right), \tag{4-6}$$

which can be further simplified as

$$\Delta\theta = 2\tan^{-1}\left\{\frac{Z_0\omega_0 C_s^{min}(\alpha - 1)}{1 - \omega_0^2 C_s^{min}\left[(\alpha+1)L_s + \alpha C_s^{min}\left(\omega_0^2 L_s + Z_0^2\right)\right]}\right\}, \tag{4-7}$$

where α stands for the load capacitor tuning range and αmax is its maximum value, i.e., $1 \le \alpha \le \alpha_{max} = C_s^{max}/C_s^{min}$.

The optimum series inductance value L_s can be found as $L_s = (\alpha_{max} + 1)/\left(2\alpha_{max}\omega_0^2 C_s^{min}\right)$ by differentiating equation (4-7) with respect to L_s. By choosing C_s^{min} as $C_s^{min} = 1/\left(\sqrt{\alpha_{max}} Z_0\omega_0\right)$, the maximum phase shifting range $\Delta\theta_{max}$ of an SLC RTPS can be obtained in equation (4-8), aligning well with the results in [156],

$$\Delta\theta_{max} = 4\tan^{-1}\left(\frac{\alpha_{max} - 1}{2\sqrt{\alpha_{max}}}\right). \tag{4-8}$$

The $\Delta\theta$ of an SLC RTPS for different α_{max} is plotted in Figure 4.3. It shows that, for α_{max}=3, the $|\Delta\theta_{max}|$ of an SLC RTPS is only 120°, and the $|\Delta\theta|$ is only increased by 27.5° for α_{max}=4, agreeing well with the results in [156]. Thus, an SLC RTPS cannot achieve 360° phase shift with a practical capacitor tuning range α. The passive losses limit the $\Delta\theta_{max}$ [155]-[158].

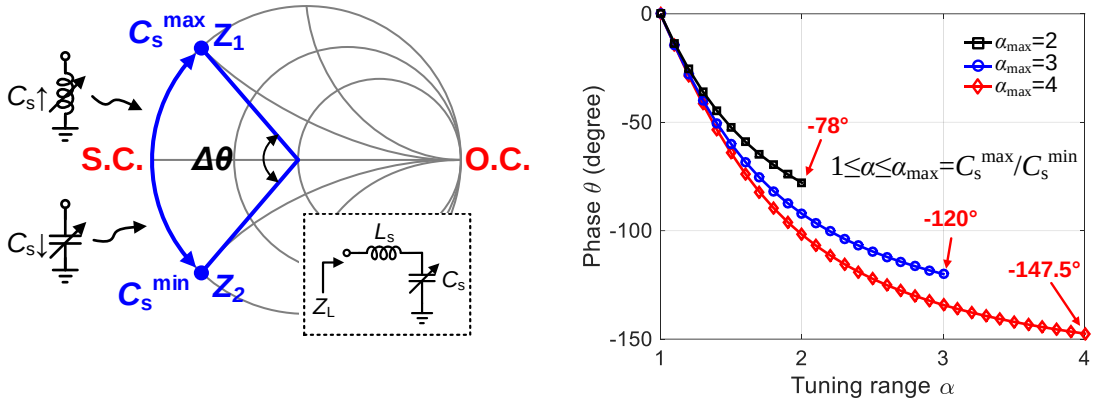


Figure 4.3 – (a) The load impedance trajectory for a lossless parallel L-C load (PLC) by tuning C_p, and (b) the simulated phase shifting range for different maximum capacitor tuning range $\alpha_{max}=C_p^{max}/C_p^{min}$, e.g., α_{max}=2, 3, or 4. Assume the optimum C_p^{min} and L_p values are used in this PLC RTPS design.

4.4.3. Parallel L-C Resonant Load (PLC)

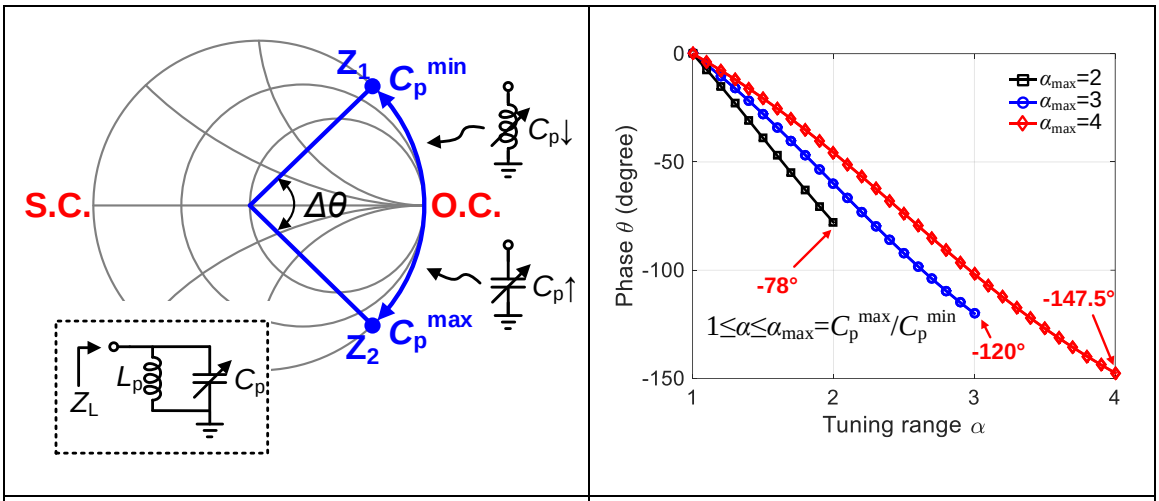
As the dual implementation of the SLC load, parallel L-C resonant load (PLC) can also be used for RTPS designs [163]. The PLC load impedance trajectory along the unit circle of the Smith chart is shown in Figure 4.4(a), indicating that PLC generates a parallel resonance as an open circuit (O.C.) for the load. In practice, a PLC load also cannot offer a full span 360° phase shifting range, due to the limited tuning range of C_p [163]. Different from an SLC load, decreasing capacitance C_p makes the PLC load impedance Z_L inductive and approaching Z_1, which is the load impedance Z_L at the minimum C_p as C_p^{min}. On the other hand, increasing C_p makes the PLC load impedance capacitive and pushes Z_L to reach Z_2, which is the load impedance Z_L at the maximum C_p of C_p^{max}. Similar to an SLC RTPS, the $\Delta\theta$ of PLC RTPS is determined by the phase difference of the reflection coefficients of Z_1 and Z_2, and it can be expressed in equation (9).

$$\begin{aligned}\Delta\theta &= 2\tan^{-1}\left[\frac{\omega_0 L_p}{Z_0\left(1-\omega_0^2 L_p C_p^{\max}\right)}\right]-2\tan^{-1}\left[\frac{\omega_0 L_p}{Z_0\left(1-\omega_0^2 L_p C_p^{\min}\right)}\right]\\ &= 2\tan^{-1}\left[\frac{Z_0\omega_0^3 L_p^2 C_p^{\min}\left(\alpha-1\right)}{Z_0^2-\left(\alpha+1\right)Z_0^2\omega_0^2 L_p C_p^{\min}+\alpha Z_0^2\left(\omega_0^2 L_p C_p^{\min}\right)^2+\left(\omega_0 L_p\right)^2}\right].\end{aligned} \tag{4-9}$$

The optimum parallel inductance L_p value can be found as $L_p = 2/\left[(\alpha_{max}+1)\omega_0^2 C_p^{min}\right]$ by differentiating equation (4-9) with respect to L_p for achieving the maximum phase shift. Moreover, choosing $C_p^{min} = 1/\left(\sqrt{\alpha_{max}} Z_0 \omega_0\right)$, the $\Delta\theta_{max}$ is obtained as

$$\Delta\theta_{max} = 2\tan^{-1}\left[\frac{4\sqrt{\alpha_{max}}\left(\alpha_{max}-1\right)}{\left(\alpha_{max}-1\right)^2-4\alpha_{max}}\right]. \tag{4-10}$$

The $\Delta\theta_{max}$ of a PLC RTPS for different α_{max} is plotted in Figure 4.4(b). From Figure 4.3(b) and Figure 4.4(b), it can be summarized that a 2nd-order L-C resonator (e.g. SLC and PLC) only covers one resonance point on the Smith chart, i.e., S.C. or O.C.; it performs a larger phase shifting range than a CL RTPS, but it still cannot achieve 360° full-range phase shift [163]. Increasing the α_{max} can only marginally improve the phase shifting range (Figure 4.3b and Figure 4.4b), and cascading multiple stages directly suffers from passive loss penalty. However, the analysis above indicates that employing high-order reflective loads with multi-resonance will expand the load trajectory on the Smith chart, cover multiple S.C. or O. C. resonance points, and thus increase the RTPS phase shifting range [158]-[160].



(a) (b)

Figure 4.4 – (a) The load impedance trajectory for a lossless parallel L-C load (PLC) by tuning C_p, and (b) the simulated phase shifting range for different maximum capacitor tuning range $\alpha_{max}=C_p^{max}/C_p^{min}$, e.g., α_{max}=2, 3, or 4. Assume the optimum C_p^{min} and L_p values are used in this PLC RTPS design.

4.4.4. CLC π-resonator load with one tunable capacitor

The CLC π-resonator load with one tunable capacitor (CLC-1) is widely adopted in RTPS to realize a high-order reflective load [155], [158]-[159]. The load reflection coefficient behavior is demonstrated in Figure 4.5. CLC-1 can cover two resonance points, i.e., an O.C. and an S.C., which extend the phase shifting range significantly. When L_1 and C_2 form a series resonance as an S.C. load, the load impedance Z_L of CLC-1 is zero. When C_2 decreases, the L_1-C_2 series resonator becomes capacitive, making Z_L reach Z_2, which is defined as the load impedance Z_L at the minimum C_2 value as C_2^{min}. On the other hand, when C_2 increases, the L_1-C_2 resonator becomes inductive and can form a parallel resonance with the fixed capacitor C_3 to realize an O.C. load, denoted as Z_1. Moreover, C_2 can be further increased to move Z_L beyond O.C. and reach Z_3, which is defined as Z_L at the maximum C_2 value as C_2^{max}.

The phase shifting range is thus more than 180°. The CLC-1 load impedance Z_L is expressed as

$$Z_L = \frac{1-\omega_0^2 L_1 C_2}{j\omega_0\left(C_3 + C_2 - \omega_0^2 L_1 C_2 C_3\right)}. \tag{4-11}$$

The phase difference can be written as

$$\Delta\theta = 2\tan^{-1}\left[\frac{1-\omega_0^2 L_1 C_2^{\max}}{Z_0\omega_0\left(C_3 + C_2^{\max} - \omega_0^2 L_1 C_2^{\max} C_3\right)}\right] - 2\tan^{-1}\left[\frac{1-\omega_0^2 L_1 C_2^{\min}}{Z_0\omega_0\left(C_3 + C_2^{\min} - \omega_0^2 L_1 C_2^{\min} C_3\right)}\right]. \tag{4-12}$$

Further, since C_2 varies from $C_2^{\min}$ to $C_2^{\max}$, the total phase shifting range can be derived using equation (4-12). Assume the same capacitor equation $C_2^{\min} = 1/\left(\sqrt{\alpha_{\max}} Z_0 \omega_0\right)$ is used as the CL, SLC, and PLC loads. Let $C_3 = \beta C_2^{\min}$ with β as the ratio of C_3 over $C_2^{\min}$. The optimum inductance value L_1 can be found as $L_1 = \left[(\alpha_{\max}+\beta)^2 + \alpha_{\max}\left(1+\beta^2\right)\right] / \left[2\alpha_{\max}\omega_0^2 C_2^{\min}\left(\alpha_{\max}+\beta^2\right)\right]$ that achieves the maximum phase shift for given $\alpha_{\max}$, β, and $C_2^{\min}$. Finally, the $\Delta\theta_{\max}$ of a CLC-1 RTPS is derived in equation (4-13).

$$\Delta\theta_{\max} = 2\tan^{-1}\left[\frac{4\alpha_{\max}\left(-\alpha_{\max}^3 - 2\alpha_{\max}^2\beta^2 + \alpha_{\max}^2 - \alpha_{\max}\beta^4 + 2\alpha_{\max}\beta^2 + \beta^4\right)\sqrt{\alpha_{\max}}}{\begin{array}{c}-\alpha_{\max}^5 + \alpha_{\max}^4\left(6-3\beta^2\right) + \alpha_{\max}^3\left(10\beta^2 - 3\beta^4 - 1\right) \\ +\alpha_{\max}^2\beta^2\left(6\beta^2 - 3 - \beta^4\right) + \alpha_{\max}\beta^4\left(2\beta^2 - 3\right) - \beta^6\end{array}}\right]. \tag{4-13}$$

Figure 6a depicts the $\Delta\theta$ of a CLC-1 RTPS versus the capacitor tuning range α of C_2 ($1 \le \alpha \le 3 = \alpha_{\max}$) and capacitor ratio β ($0 \le \beta \le 3$). It shows that if α and β equal 3, the $|\Delta\theta_{\max}|$ is 266.3°. Note that when β equals 0, CLC-1 is reduced to SLC, and therefore the $|\Delta\theta_{\max}|$ is

120°, matching well with the results for SLC RTPS (Figure 4.3). Compared with CL, SLC and PLC designs, CLC-1 demonstrates that a high-order resonator load indeed improves the phase shifting range for the same α_{max}. Figure 4.6 shows that the total phase shift of a CLC-1 RTPS versus α and large values of β (up to 20). It can be found that the $|\Delta\theta_{max}|$ can reach 360° (e.g., $|\Delta\theta_{max}|$=357° for α=α_{max}=3 and β=20) however with drastic phase shift changes at large β values. This drastic phase shift change is not desired in practice. In reality, the $|\Delta\theta_{max}|$ of a CLC-1 RTPS is generally smaller than 360° with practical capacitive tuning and inevitable passive loss. For example, the phase shifting range of a CLC-1 RTPS in [155] and [158] is only 85° at 10.5GHz and only 147° in [159] at 60GHz.

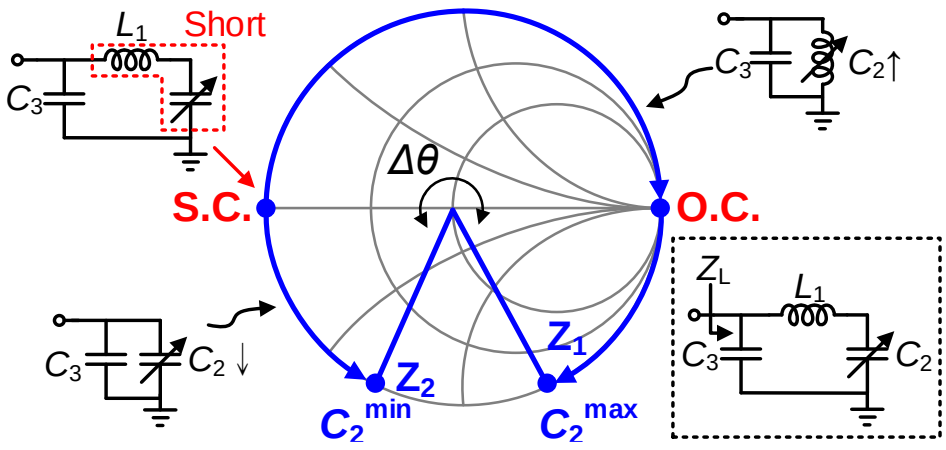


Figure 4.5 – The load impedance tuning range for a lossless CLC π-resonator load with one tunable capacitor (CLC-1).

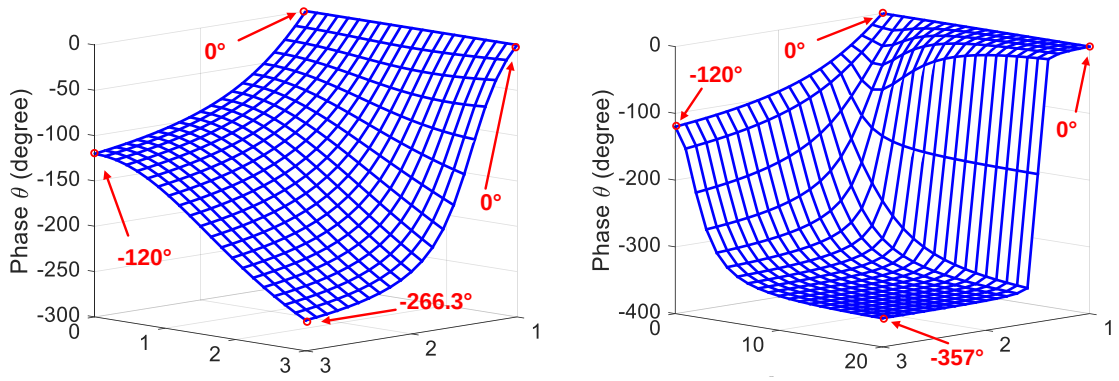


Figure 4.6 – The simulated CLC-1 phase shifting range versus the capacitor tuning α and capacitor ratio β (i.e., $\beta=C_3/C_2^{min}$) for a lossless CLC-1 RTPS load. The phase shifting range is referenced to zero for α =1, i.e., no capacitive tuning. It covers (a) 0≤ β≤3 and (b) 0≤β≤ 20.

4.4.5. CLC π-resonator load with two tunable capacitors

A CLC π-resonator load with two tunable capacitors (CLC-2) is also employed in RTPS designs. Different from CLC-1, CLC-2 allows both C_2 and C_3 to be tunable (Figure 4.7) [158], [160]. This tunable C_3 provides an additional degree of freedom to extend the RTPS phase shift. Like CLC-1, CLC-2 also covers two resonance points with one S.C. and one O.C. The load impedance trajectory of the CLC-2 load is shown in Figure 4.7. When L_1 and C_2 resonate and form an S.C. load, the load impedance Z_L is zero, similar to the CLC-1 load. When the L_1-C_2 resonator becomes capacitive, the tunable capacitance C_3 can further extend the load trajectory toward O.C. by reducing the C_3 value, achieving a wider phase shift than CLC-1. The location of Z_3 on the Smith chart depends on the tuning ratio of C_3 and the relative values of C_2 and C_3. Similarly, when the CLC-2 load forms an O.C.

load as the CLC-1 load, increasing the C_3 value will move the load impedance further into the capacitive region of the Smith chart, also extending the phase shift. Equation (4-14) expresses the $\Delta\theta$ of a CLC-2 RTPS.

$$\Delta\theta = 2\tan^{-1}\left[\frac{1-\omega_0^2 L_1 C_2^{\max}}{Z_0\omega_0\left(C_3^{\max}+C_2^{\max}-\omega_0^2 L_1 C_2^{\max} C_3^{\max}\right)}\right] -2\tan^{-1}\left[\frac{1-\omega_0^2 L_1 C_2^{\min}}{Z_0\omega_0\left(C_3^{\min}+C_2^{\min}-\omega_0^2 L_1 C_2^{\min} C_3^{\min}\right)}\right]. \quad (4\text{-}14)$$

To investigate the $\Delta\theta_{\max}$ of the CLC-2 RTPS, for simplicity, we assume C_2 and C_3 have the same $\alpha_{\max}$, i.e., $\alpha_2^{\max}=C_2^{\max}/C_2^{\min}=\alpha_{\max}$ and $\alpha_3^{\max}=C_3^{\max}/C_3^{\min}=\alpha_{\max}$, although C_2 and C_3 can vary independently to achieve the target phase shift. Also, we assume $C_3^{\min}=\beta C_2^{\min}$, where β is the capacitor ratio between $C_3^{\min}$ and $C_2^{\min}$. Using the same design capacitor design equation $C_2^{\min}=1/\left(\sqrt{\alpha_{\max}}Z_0\omega_0\right)$ as for the CL, SLC, PLC, and CLC-1 cases, the optimum L_1 can be found in equation **Error! Reference source not found.**. Thus, t he $\Delta\theta_{\max}$ of a CLC-2 RTPS is derived in equation **Error! Reference source not found.** for given $\alpha_{\max}$ and β values.

$$L_1 = \frac{\left(\begin{array}{l}\sqrt{\beta\left(\omega_0 Z_0 C_2^{\min}\right)^2\left\{\beta\left(\alpha_{\max}C_2^{\min}\right)^2\left[Z_0^2\omega_0^2\left(\beta+1\right)^2+1\right]+\beta-2\alpha_{\max}\right\}+1} \\ +\alpha_{\max}\beta\left(1+\beta\right)\omega_0^2 Z_0^2\left(C_2^{\min}\right)^2-1\end{array}\right)}{\alpha_{\max}\left(\alpha_{\max}+1\right)\left(\beta\omega_0^2 Z_0 C_2^{\min}\right)^2 C_2^{\min}}. \quad (4\text{-}15)$$

$$\Delta\theta_{\max} =$$

$$2\tan^{-1}\left\{\frac{\sqrt{\alpha_{\max}}\left[\begin{array}{l}\beta\left(1-\alpha_{\max}\beta\right)-1\\+\sqrt{\beta^2\left(\alpha_{\max}+\dfrac{1}{\alpha_{\max}}\right)+\left(\beta+1\right)^2+\beta^3\left(\beta+2\right)}\end{array}\right]}{\beta\left(\begin{array}{l}\left(2\alpha_{\max}-\beta\right)\beta+\left(1+\beta\right)\\-\sqrt{\beta^2\left(\alpha_{\max}+\dfrac{1}{\alpha_{\max}}\right)+\left(\beta+1\right)^2+\beta^3\left(\beta+2\right)}\end{array}\right)}\right\}$$

$$-2\tan^{-1}\left\{\frac{\left[\begin{array}{l}\left(\alpha_{\max}\beta-\alpha_{\max}-\beta^2\right)\\+\alpha_{\max}\sqrt{\left(\alpha_{\max}+\dfrac{1}{\alpha_{\max}}\right)\beta^2+\left(\beta+1\right)^2+\beta^3\left(\beta+2\right)}\end{array}\right]}{\sqrt{\alpha_{\max}}\left(\begin{array}{l}\left(2\alpha_{\max}-\beta^2\right)\beta\\-\alpha_{\max}\beta\sqrt{\left(\alpha_{\max}+\dfrac{1}{\alpha_{\max}}\right)\beta^2+\left(\beta+1\right)^2+\beta^3\left(\beta+2\right)}\end{array}\right)}\right\}. \quad (4\text{-}16)$$

Figure 4.8 shows the total phase shifting range of a CLC-2 RTPS with independent C_2 and C_3 tuning and different capacitor ratios β (i.e., $\beta=C_3^{\min}/C_2^{\min}$). Assume that the maximum tuning ranges of C_2 and C_3 are the same as $\alpha_{\max}$. When β equals 0, CLC-2 is reduced to SLC, and the $|\Delta\theta_{\max}|$ is 120° (Figure 4.8a), agreeing well with the results in Fig. 3a. Furthermore, when β increases, the total phase shifting range also increase accordingly, as shown in Figure 4.8(b)-(d). If $\alpha_{\max}$ and β both equal 3, the $|\Delta\theta_{\max}|$ is 360° (Figure 4.8c).

Compared with CLC-1, the CLC-2 demonstrates that an additional tunable capacitor C_3 indeed extends the total phase shift. Moreover, if β is sufficiently large (e.g., β=10), the $|\Delta\theta_{\max}|$ of a CLC-2 RTPS is over 360° but also with undesired drastic phase changes (Figure 4.8Figure 4.8d). CLC-2 is a popular reflective load due to its large phase shift and simple design [158], [160]. Again, once the passive loss is considered, the $|\Delta\theta_{\max}|$

is reduced substantially in practice. For example, the $|\Delta\theta|$ of a CLC-2 RTPS in [158] is 340° with 12.6dB loss at 2.4GHz and is only 180° with 7.5dB loss at 60GHz in [159].

Theoretically, a fourth-order (or even higher-order) reflective load can achieve a larger phase shift to the full range 360°. However, increasing the load order by simply adding more passive components will substantially increase the passive loss and area [155], [158]. Our proposed transformer-based multi-resonance load overcomes these issues and achieves a 360° full-span phase shift with low loss and a compact area; its operation is introduced in the next section.

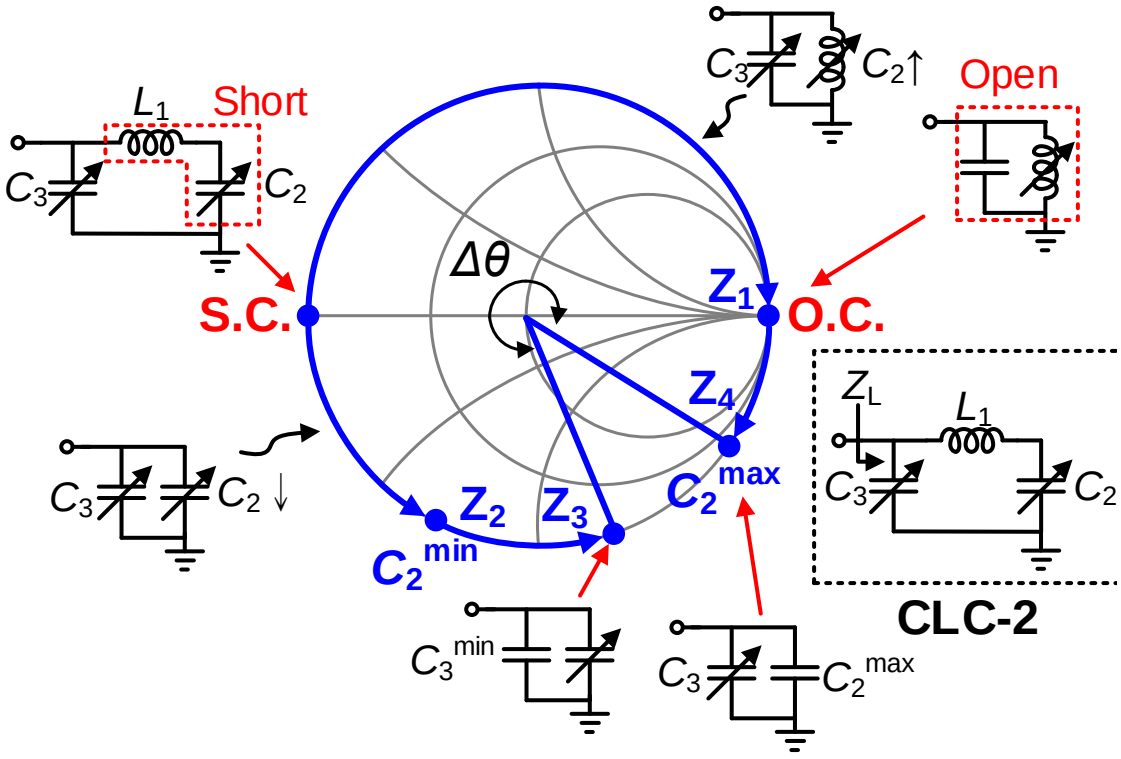


Figure 4.7 – The load impedance tuning range for a lossless CLC π-resonator load with two tunable capacitors (CLC-2).

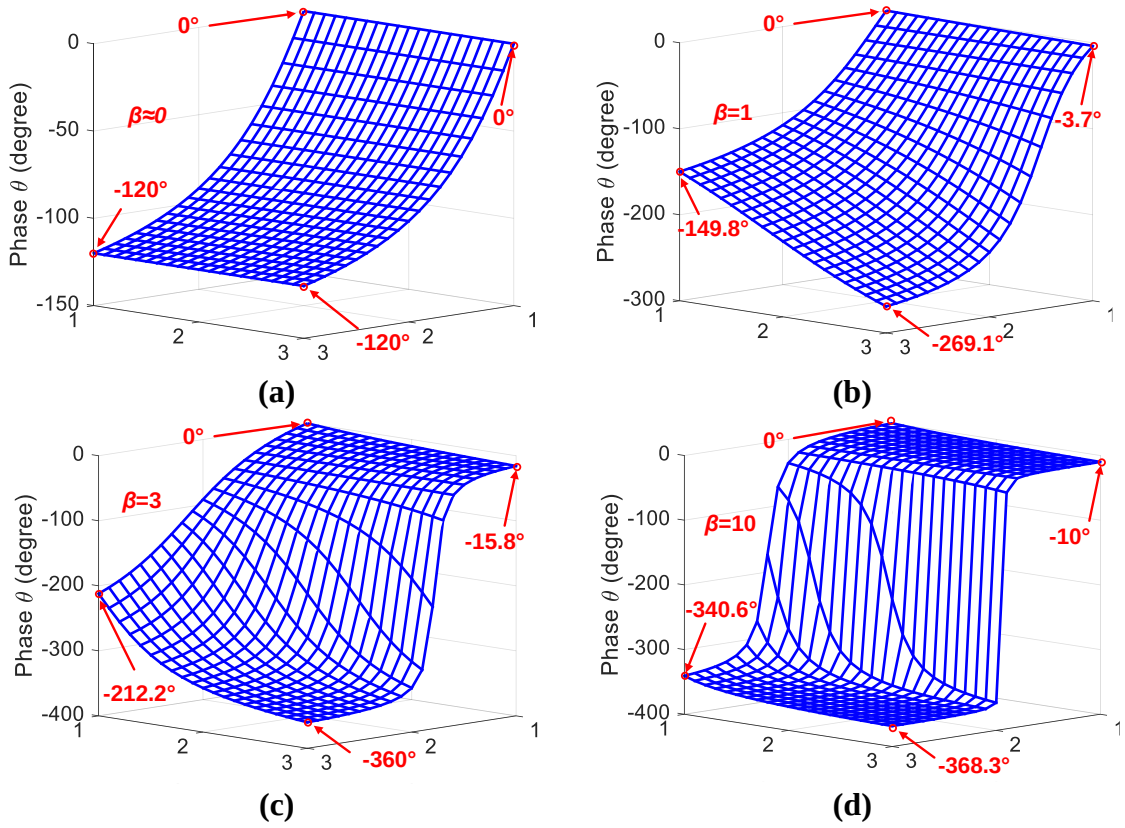


Figure 4.8 – The simulated CLC-2 phase shifting range versus the two capacitor tuning α_2 and α_3 at different capacitor ratios β (i.e., $\beta=C_3^{min}/C_2^{min}$) for a lossless CLC-2 RTPS load with (a) β=0, (b) β=1, (c) β=3, and (d) β=10. The α_{max} is 3 and the Δθ is referenced to zero for $\alpha_2=\alpha_3=1$, i.e., no capacitive tuning.

4.4.6. Transformer-based multi-resonance reflective load

Our proposed transformer-based multi-resonance load consists of a physical transformer and two parallel tunable capacitors as C_v and C_t (Figure 4.9a). The transformer can be modeled as an ideal 1:n/k transformer connected with a magnetizing inductor $L_m=k^2L_{p1}$ and a leakage inductor $L_k=(1-k^2)L_{p1}$; L_{p1} is the primary self-inductance; n and k are the secondary/primary turn ratio and magnetic coupling coefficient, respectively [174]-[178]. The capacitor C_v at the secondary-side can be converted by the ideal *1:n/k* transformer to the primary-side as C_v', i.e., $C_v'=(n/k)^2C_v$. Figure 9b shows the simplified load model from the primary side to help our following analysis the behavior of the transformer-based multi-resonance load.

The load reflection coefficient trajectory is shown on the Smith chart in Figure 4.10, with C_v' and C_t being varied independently. First, when L_m and C_v' form a parallel resonance, the load impedance Z_L is fully determined by C_t as Z_1. By varying C_t, the lower left part of the unit circle on the Smith chart can be covered. As C_v' increases, the L_m-C_v' parallel resonator becomes capacitive, which forms a series resonance with L_k and result in an S.C. load as Z_2. Moreover, if C_v' further increases, the L_k-L_m-C_v' branch becomes inductive, which can form a parallel resonance with C_t and produces an O.C. load as Z_3, assuming C_t is tuned to its maximum value C_t^{max} for this O.C. load for simplicity. On the other hand, decreasing C_v' makes the L_m-C_v' resonator behave inductive; this inductive L_m-C_v' resonator can combine with L_k in series and form a parallel resonance with C_t to realize another O.C. load as Z_4, assuming that C_t is tuned to its minimum value C_t^{min} for this O.C. load also for simplicity. The total RTPS phase shift is determined by the phase difference between Z_3 and Z_4. Thus, by covering three resonances, i.e., two O.C. points and one S.C.,

our proposed transformer-based multi-resonance load can achieve full span 360° phase shift, if it is employed in an RTPS design. Next, the design equations of our transformer-based multi-resonance RTPS load will be presented. The load impedance Z_L of the proposed transformer-based reflective load is expressed as

$$Z_L = \frac{j\omega_0 L_{p1}\left[1-\omega_0^2 n^2\left(1-k^2\right)L_{p1}C_v\right]}{1-\omega_0^2 n^2 L_{p1}C_v - \omega_0^2 L_{p1}C_t\left[1-\omega_0^2 n^2\left(1-k^2\right)L_{p1}C_v\right]}, \tag{4-17}$$

and the RTPS output phase can be expressed in equation (4-18).

$$\theta = 2\tan^{-1}\left(\frac{\omega_0 L_{p1}\left[1-\omega_0^2 n^2\left(1-k^2\right)L_{p1}C_v\right]}{Z_0\left\{1-\omega_0^2 n^2 L_{p1}C_v - \omega_0^2 L_{p1}C_t\left[1-\omega_0^2 n^2\left(1-k^2\right)L_{p1}C_v\right]\right\}}\right). \tag{4-18}$$

$$\begin{aligned}\Delta\theta = & \\ & 2\tan^{-1}\left\{\frac{\omega_0 L_{p1}\left[1-\omega_0^2 n^2\left(1-k^2\right)L_{p1}C_v^{\max}\right]/\left(Z_0 C_t^{\max}\right)}{1/C_t^{\max}-\omega_0^2 n^2 L_{p1}-\omega_0^2 L_{p1}\left[1-\omega_0^2 n^2\left(1-k^2\right)L_{p1}C_v^{\max}\right]}\right\} \\ & -2\tan^{-1}\left\{\frac{\omega_0 L_{p1}\left[1-\omega_0^2 n^2\left(1-k^2\right)L_{p1}C_v^{\min}\right]/\left(Z_0 C_t^{\min}\right)}{1/C_t^{\min}-\omega_0^2 n^2 L_{p1}-\omega_0^2 L_{p1}\left[1-\omega_0^2 n^2\left(1-k^2\right)L_{p1}C_v^{\min}\right]}\right\}.\end{aligned} \tag{4-19}$$

Thus, the phase shifting range of such an RTPS design can be expressed in equation (4-19). To facilitate our derivation, we assume that C_t is tuned to its maximum $C_t^{\max}$ when Z_L reaches the O.C. load Z_3, while C_t is tuned to its minimum $C_t^{\min}$ when Z_L achieves the O.C. load Z_4, guaranteeing a 360° phase shifting range. Furthermore, the load impedance Z_L' excluding C_t can be expressed as

$$Z_L' = j\omega_0 L_{p1}\left[\left(1-k^2\right)+k^2/\left(1-\omega_0^2 n^2 L_{p1}C_v\right)\right]. \tag{4-20}$$

At C_v^{min} and C_v^{max}, Z_{in}' can be found as

$$\begin{aligned} Z_L'\left(C_v^{min}\right) &= j\omega_0 L_{p1}\left[\left(1-k^2\right)+k^2/\left(1-\omega_0^2 n^2 L_{p1} C_v^{min}\right)\right], \\ Z_L'\left(C_v^{max}\right) &= j\omega_0 L_{p1}\left[\left(1-k^2\right)+k^2/\left(1-\omega_0^2 n^2 L_{p1} \alpha C_v^{min}\right)\right]. \end{aligned} \tag{4-21}$$

In Figure 4.10, for simplicity, we assume that C_t^{min} resonates with $Z_L'\left(C_v^{min}\right)$, and C_t^{max} resonates with $Z_L'(C_v^{max})$ to achieve the two O.C. resonance points (Z_3 and Z_4). Thus, one can obtain $C_t^{min}=1/\left[\omega_0 Z_L'\left(C_v^{min}\right)\right]$ and $C_t^{max}=1/[\omega_0 Z_L'(C_v^{max})]$. The tuning ranges of the two capacitors C_v and C_t should satisfy

$$\frac{1}{\alpha_t}=\frac{C_t^{min}}{C_t^{max}}=\frac{\left(1-k^2\right)+k^2/\left(1-\omega_0^2 n^2 L_{p1}\alpha_v C_v^{min}\right)}{\left(1-k^2\right)+k^2/\left(1-\omega_0^2 n^2 L_{p1} C_v^{min}\right)}, \tag{4-22}$$

where $\alpha_v \le \alpha_v^{max}=C_v^{max}/C_v^{min}$ is the tuning range for C_v and $\alpha_t \le \alpha_t^{max}=C_t^{max}/C_t^{min}$ is the tuning range for C_t. To simplify the evaluation, we also assume that C_v and C_t have the same maximum tuning range α_{max}, i.e., $\alpha_v^{max}=\alpha_v^{max}=\alpha_{max}$, although they are tuned independently to achieve the target phase shift. Assuming $C_v^{min}=1/\left(\sqrt{\alpha_{max}}Z_0\omega_0\right)$, based on equation (4-22), L_{p1} can be further obtained as

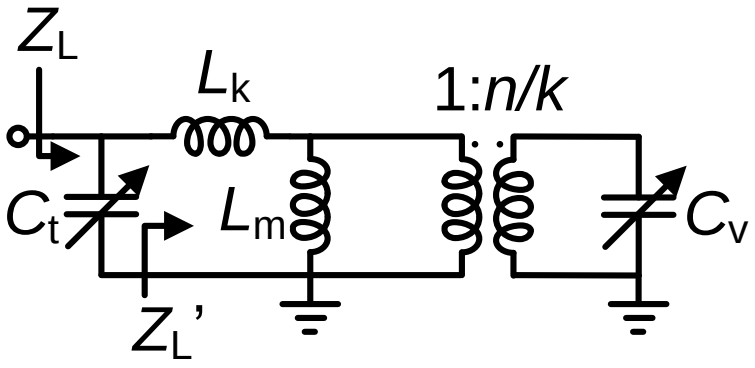
$$L_{p1}=Z_0\frac{\left(\alpha_{max}+1\right)+\sqrt{\left(\alpha_{max}+1\right)^2-4\alpha_{max}/\left(1-k^2\right)}}{2\sqrt{\alpha_{max}}\,\omega_0 n^2}, \tag{4-23}$$

and, by using equation (4-21), C_t^{min} can be found as

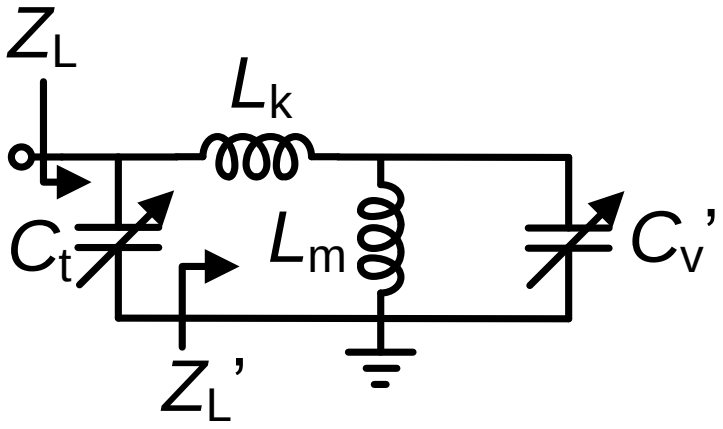
$$C_t^{min}=\frac{1-\omega_0 n^2 L_{p1}}{\omega_0^2 L_{p1}\left[Z_0\sqrt{\alpha_{max}}-\left(1-k^2\right)\omega_0 n^2 L_{p1}\right]}. \tag{4-24}$$

Figure 4.11 demonstrates the simulated phase shifting range $\Delta\theta$ of our proposed load by independently tuning the capacitors C_v and C_t with an exemplar design setting as α_{max}=3, k=0.5, and n=1. Note that the maximum capacitor tuning range is α_{max}=3. It can be observed that the phase angle of Z_3 (Figure 4.11a) as Z_L (C_v^{max}, C_t^{max}) is 0°. Similarly, the phase angle of Z_4 as Z_L (C_v^{min}, C_t^{min}) is -360°. Therefore, the $|\Delta\theta|$ of our proposed load achieves full span 360°, matching well with our qualitative analysis on the Smith chart (Figure 4.10). Unlike CLC-1 (Fig. 6) and CLC-2 (Fig. 8) RTPS, our proposed design avoids any sharp phase change during the capacitive tuning.

Figure 4.11(b) shows the total phase shifting range, when C_t^{min} is selected to be 1.5 times larger than the value obtained in equation (24); the resulting $|\Delta\theta|$ is 405.2° also with a smooth phase change during the tuning. Moreover, the above design equations (23) and (24) can serve as the design equations for our proposed transformer-based multi-resonance load, and these equations yield the load trajectory on Figure 4.11 and ensure a full span 360° phase shift. The other design parameters (i.e., k and n) can be optimized to further extend the total phase shifting range. The simulation results of a proof-of-concept RTPS design with our proposed transformer-based multi-resonance load will be shown in the following section. Table 4.1 summarizes the maximum phase shifting range $|\Delta\theta_{max}|$ of each reflective load when employed in an RTPS. Our transformer-based multi-resonance RTPS load achieves a full span 360° phase shift without any drastic phase change.



(a)



(b)

Figure 4.9 – The proposed transformer multi-resonance load in an RTPS with (a) single-ended schematic and (b) simplified schematic.

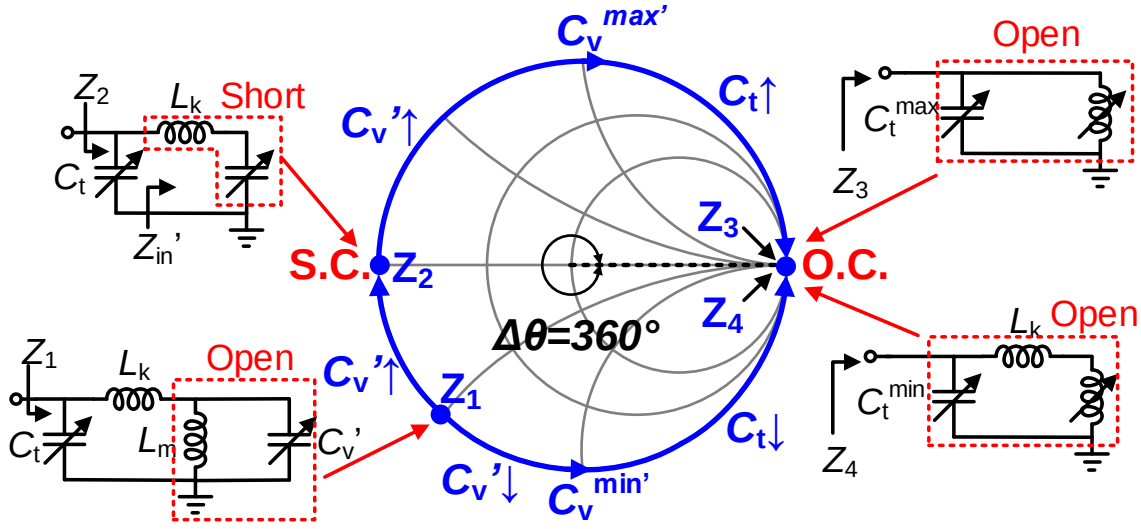


Figure 4.10 – The load impedance tuning range for the proposed transformer-based multi-resonance load by varying both C_t and C_v'. All the passive components are assumed to be lossless for simplicity.

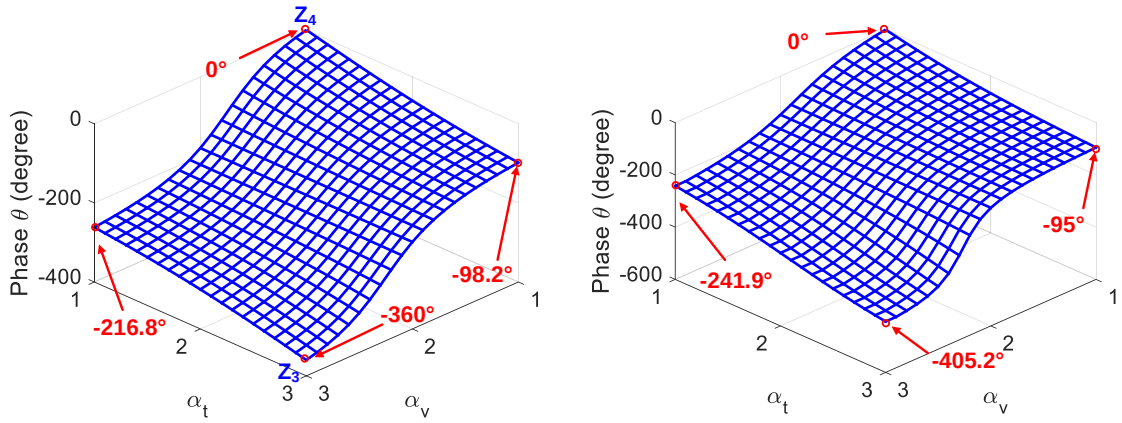


Figure 4.11 – The simulated phase shift of our proposed transformer-based multi-resonance load by independently varying C_v and C_t with a maximum capacitive tuning range $\alpha_t^{max}=\alpha_v^{max}=\alpha_{max}=3$. (a) C_t^{min} is obtained from equation (24), and (b) C_t^{min} is 1.5 times of the value obtained from equation (24).

Table 4.1 – Comparison table of maximum phase shift for different reflective loads in an RTPS

Reflective load type	Max. phase shift $\lvert\Delta\theta_{max}\rvert^{*}$	Phase change
CL	60°	Moderate
SLC	120°	Moderate
PLC	120°	Moderate
CLC-1	<360°	Drastic
CLC-2	≥360°	Drastic
Transformer-based multi-resonance load	≥360°	Moderate

*Assume that the maximum capacitor tuning range α_{max} equals 3.

4.5. Transformer-based 90° Coupler Design

We employ a transformer-based 90° coupler in the proposed RTPS design to achieve an ultra-compact size [176]. Figure 4.12(a) shows the coupler with the input, couple, through and isolation ports, denoted as *In*, *Cpl*, *Thru* and *Iso* respectively. The capacitors C_g and C_M are added to balance the output amplitude of the *Cpl* and *Thru* ports, achieve a high isolation at the *Iso* port, and obtain a good input matching at the *In* port. In practice, these two capacitors C_g and C_M absorb the parasitic capacitances of the transformer-based 90° coupler and the transformer-based reflective load. The 90° coupler utilizes the top three metal layers in a standard 130nm BiCMOS process, i.e., a 4μm-thick aluminum, a 1.42μm-thick aluminum, and a 0.55μm-thick copper layer. The 90° coupler only occupies a 120μm×120μm footprint for our proof-of-concept design at 62GHz. The outer diameter D_{out}, inner diameter D_{in}, width W and spacing S are 120μm, 80μm, 6μm and 4μm (Figure 4.12b). The simulated phase and amplitude of the 90° coupler are shown in Figure 4.13, when the *In* port is driven by an input signal.

Our transformer-based 90° coupler maintains a nearly constant 90° phase difference between the *Thru* and *Cpl* ports within ±1° phase error from 54GHz to 66GHz (Figure 4.13b). The *Thru* port and the *Cpl* port magnitude responses are -4.3dB and -4dB at the center frequency of 62GHz (Figure 4.13a). Considering the fundamental 3dB IL loss by the 1:2 power splitting, the additional loss due to the 90° coupler is only 1.3dB at 62GHz. The amplitude variation is within ±1.3dB from 51GHz to 70GHz. The return loss (RL) at the *In* port is 15.8dB, and the isolation is 10.2dB at 62GHz. The simulation verifies that the transformer-based 90° coupler exhibits excellent phase and amplitude balance and low passive loss from 50GHz to 70GHz.

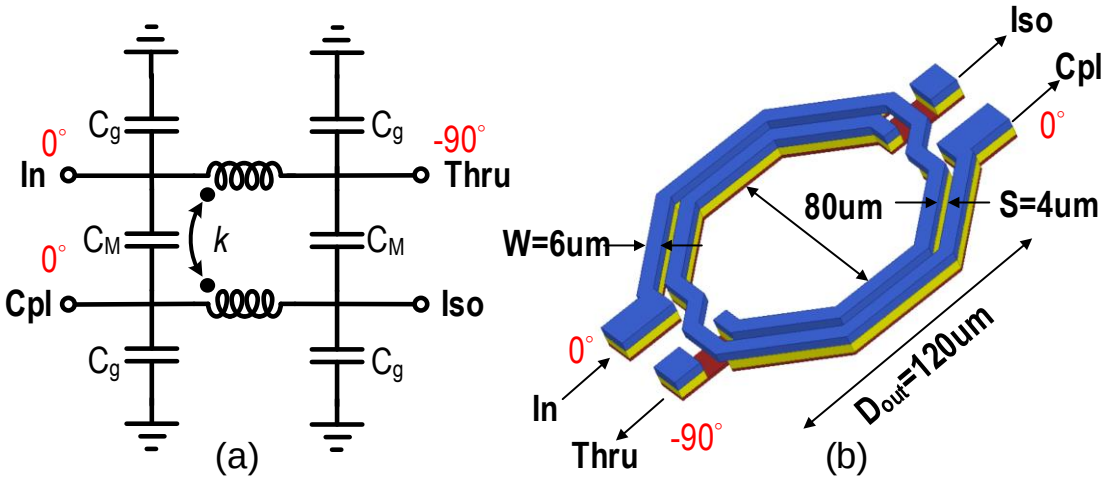
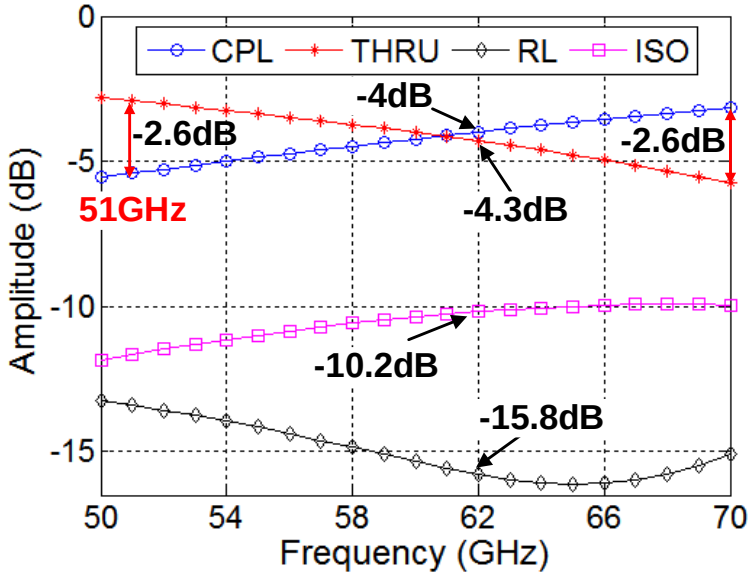
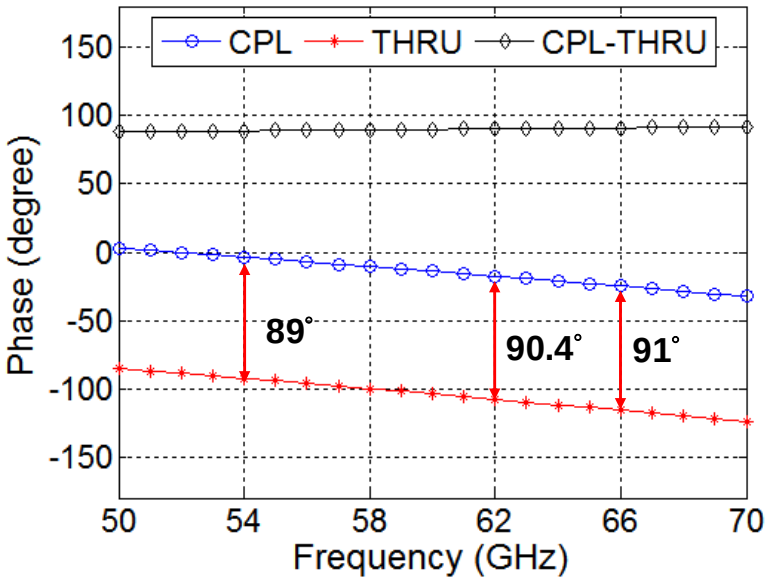


Figure 4.12 – A transformer-based 90° coupler with (a) the schematic and (b) 3D EM model in the proof-of-concept 60GHz RTPS design.



(a)



(b)

Figure 4.13 – (a) Simulated amplitudes for the Thru, Cpl, and Iso ports and the return loss at the In port. (b) Simulated phases for the Thru and Cpl ports.

4.6. Circuit Implementation and Simulation of the Proposed RTPS

Our proof-of-concept fully differential ultra-compact transformer-based RTPS is shown in Figure 4.14 [143]. It employs two identical transformer-based 90° couplers and two identical transformer-based multi-resonance reflective loads (Figure 4.14a). It is implemented as a fully differential and symmetric design in a standard 130nm SiGe BiCMOS process with a core area of 340μm×480μm. The symmetric layout also makes the input and output inter-changeable (Figure 4.14b and Figure 4.14c).

The 3D EM model of our proposed differential transformer-based multi-resonance load is shown in Figure 4.14(d). It employs a 2:1 transformer that is optimized to provide a maximum phase shifting range based on the design equations. It also offers a desired impedance conversion with the coupling coefficient k=0.63. The transformer center taps are used to provide the DC bias voltage for the differential varactors that are employed as the tuning capacitors C_v and C_t. The transformers for the multi-resonance loads utilize the same metal layers as the transformer-based 90° coupler, and they occupy 100μm×100μm chip size. The outer/inner diameter D_{out}/D_{in}, width W and space S are 100μm, 49μm, 5μm and 5μm. Figure 4.15 summarizes the simulated differential complex transmission coefficient, i.e., complex insertion loss IL, of our RTPS at 62GHz for different phase shifting configurations. Note that the amplitude of IL represents the RTPS passive loss, while its phase stands for the output phase shift of the RTPS.

The simulation includes 3D EM models for the transformers and signal routings as well as the extracted device parasitics. Each dot represents a complex IL value achieved by a given varactor setting of (C_v, C_t). The two control voltages V_{cv} and V_{ct} are

independently swept from -1V to 0.45V with a step of 10mV, making the effective C_v vary from 46fF to 129fF and the effective C_t vary from 21fF to 59fF, as shown in Figure 4.15.

Figure 4.16 shows the simulated capacitances (i.e., C_v and C_t) versus control voltage (i.e., V_{cv} and V_{ct}). The slopes (i.e., capacitance/V) around -0.8V and +0.8V are much smaller than set around -0.5 and 0V, the corresponding dots of complex IL are denser (Figure 4.15). On the contrary, when V_{cv} and V_{ct} are set around -0.8V and +0.8V, the corresponding dots of complex IL are sparser (Figure 4.15). The plots of the simulated P_{1dB} and IIP3 for different varactor control settings are shown in Figure 4.17. The P1dB is 13.8dBm and the IIP3 is 23.5dBm for the setting of V_{cv}=0.45V and V_{ct}=0.45V, respectively. Moreover, the P_{1dB} is 13.6dBm and the IIP3 is 21.9dBm for the setting of V_{cv}=-1V and V_{ct}=-1V, respectively. Note that the dots in Figure 4.15 are not uniformly distributed due to the nonlinear relationship between the varactor control voltages and the complex IL variations. A major reason is due to the nonlinear relationship between the varactor capacitance versus its control voltage value.

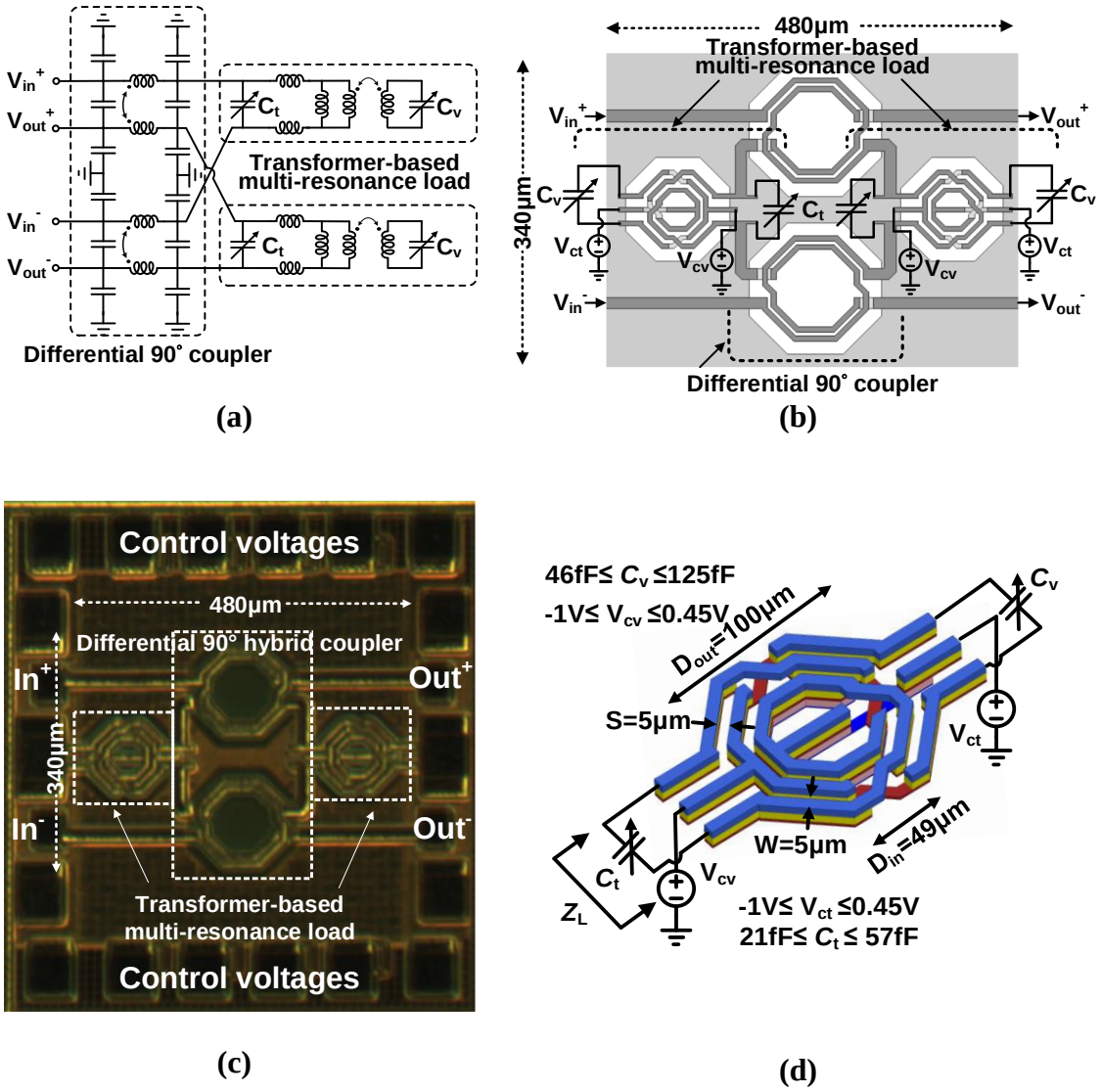


Figure 4.14 – Our proposed RTPS design with (a) the schematic, (b) the layout and EM model, (c) the chip microphotograph, and (d) the EM model of the proposed load.

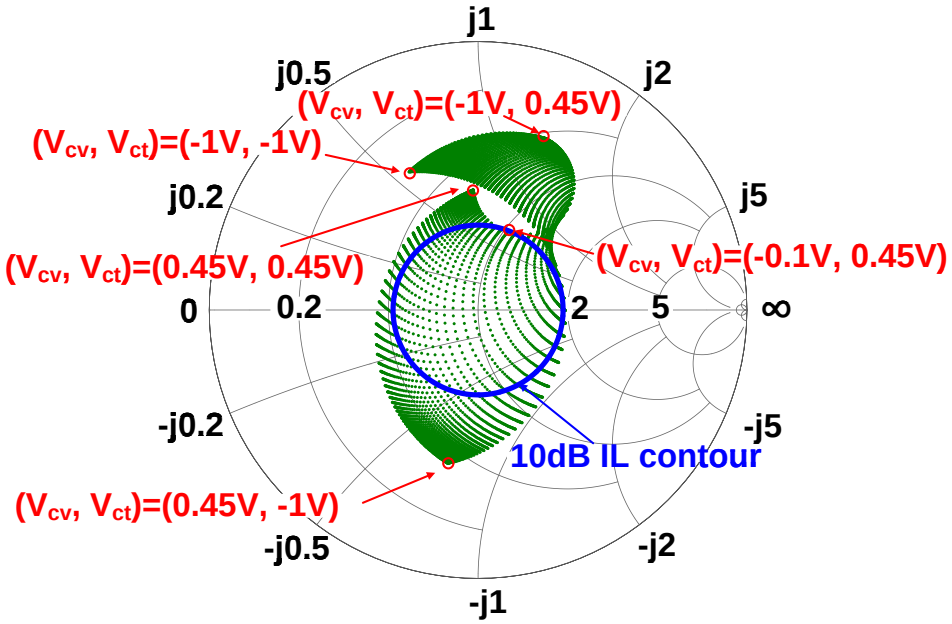


Figure 4.15 – The simulated complex IL at 62GHz for the proposed transformer-based RTPS. The simulation includes 3D EM modeling of the passive structures and device parasitic extraction.

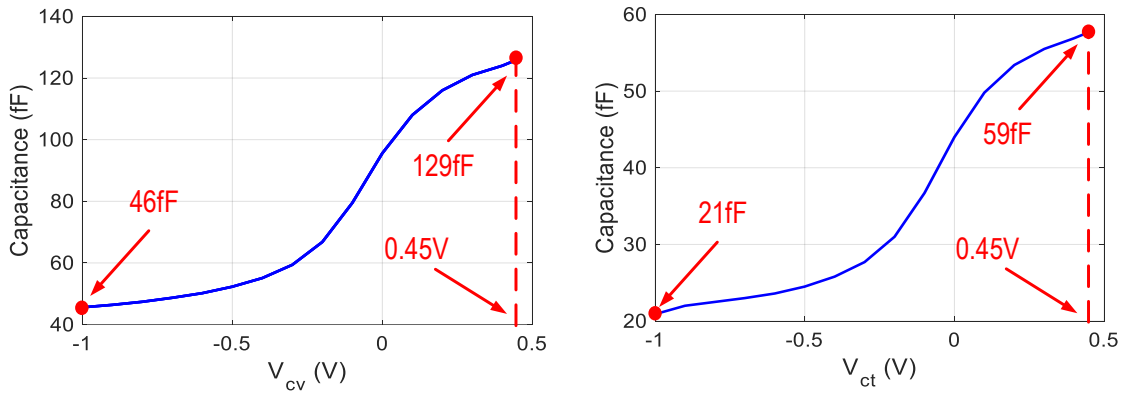
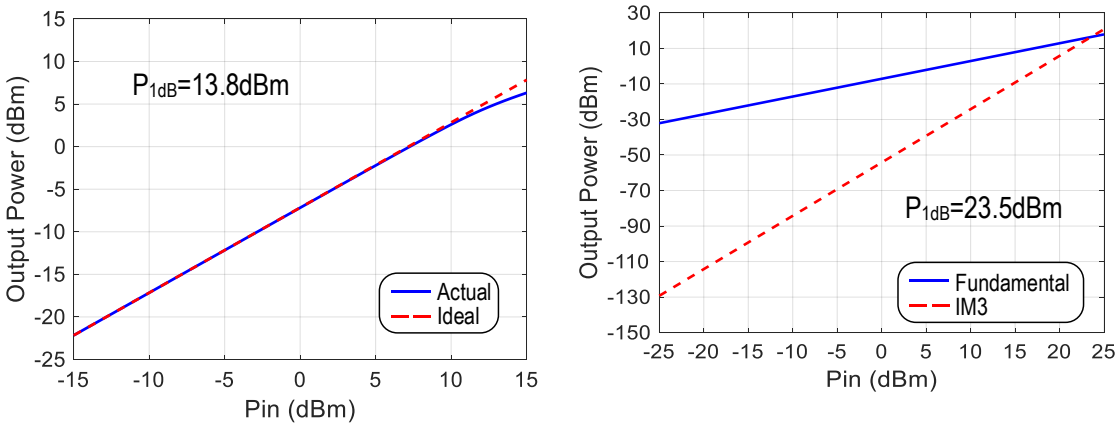
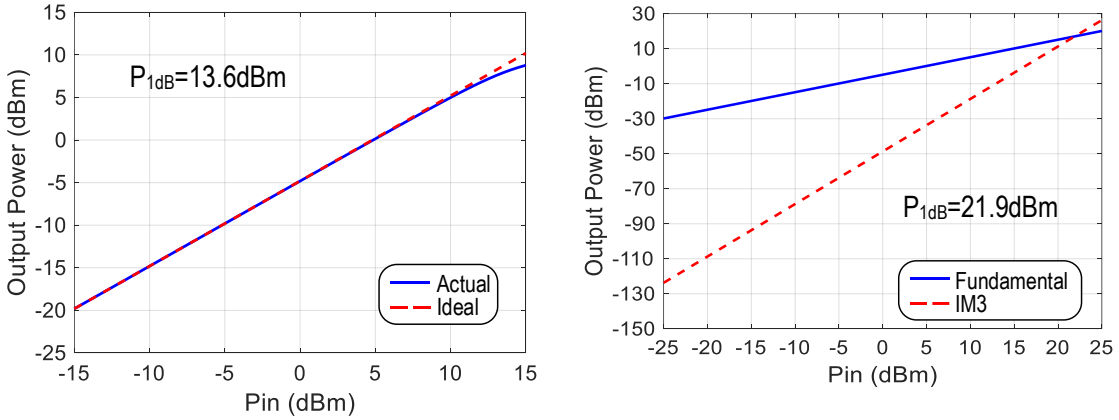


Figure 4.16 – The simulated capacitance vs. the control voltage of (a) V_{cv} and (b) V_{ct}.



(a)



(b)

Figure 4.17 – The simulated P_{1dB} and IIP3 with (a) V_{cv}=0.45V and V_{ct}=0.45V V_{cv}=0.45V and V_{ct}=0.45V, and (b) V_{cv}=-1V and V_{ct}=-1V.

4.7. Measurement Results

The RTPS chip is measured by direct probing with a 4-port network analyzer (Keysight PNA-X N5247A and R&S ZVA67). The network analyzer enables full 4-port S-parameter measurement up to 67GHz. To evaluate the phase shift performance, we tune the varactor control voltages V_{cv} and V_{ct} both from -1V to +0.45V at discrete voltage steps. The differential complex IL parameters are extracted from the S-parameter measurements to capture the RTPS phase shift and passive loss at different varactor settings. Figure 4.18 shows the measured complex IL results at 62GHz, and each point on the Smith chart represents one complex IL value for a given varactor setting (V_{cv}, V_{ct}). The varactor control voltages of V_{cv} and V_{ct} are swept from -1V to +0.45V.

Our RTPS design covers a total phase shift of 367° achieving full span phase shifting. The measured IL magnitudes also closely match the simulated values (Figure 4.18). Compared with the reported 60GHz RTPS designs [159]-[164], *our design is a fully integrated mm-Wave RTPS that first-ever successfully covers the 360° full range phase shifting.* In addition, Figure 4.18 also shows four different IL contours as the minimum IL (grey), 10dB constant IL (black), 11dB constant IL (red) and 12dB constant IL (blue) contours. The minimum IL circle settings for the full span 360° interpolation are the outmost IL points in Figure 4.20. In parallel, the dense phase interpolation allows one to select phase shift settings to achieve a full span 360° phase shift with a constant IL magnitude (10dB, 11dB, or 12dB). Note that the phase resolution is $\sim<5^{\circ}$ between two adjacent dots for the measurement, which presents fewer test dots. Those test dots are roughly uniformly distributed on the Smith chart.

Figure 4.19 shows the measured complex IL results at different frequencies from 58GHz to 64GHz for three independent RTPS test chips. All the three test chips exhibit closely matched measurement results, and a full span 360° phase shift is consistently achieved from 59GHz to 64GHz for all the chips. Figure 4.20 shows the measured IL under the minimum IL settings versus phase shift at different frequencies for the three independent test chips at 62GHz. Test chip 1 achieves a measured minimum IL from 3.7dB to 10.2dB over the 367° full-span phase shift. The measured minimum IL range is 4.1 dB to 11.05 dB for test chip 2 and 3.8dB to 10.55dB for test chip 3, respectively, showing a highly consistent performance.

To quantitatively evaluate an RTPS, its figure-of-merit (FoM) is defined as the maximum phase shifting range $|\Delta\theta_{max}|$ divided by the worst-case minimum insertion loss (IL_{min}) over the entire phase shifting range, i.e., FoM(°/dB)=$|\Delta\theta_{max}|/IL_{min}$ [179]. Figure 4.21shows the measured FoM over different frequencies (59GHz to 64GHz) for the three independent RTPS test chips. The achieved FoM values are between 34.5°/dB and 37.1°/dB, well outperforming the reported fully integrated 60GHz RTPS designs on bulk silicon processes (Table 4.2). The measured peak FoM is 37.1°/dB for our proposed RTPS, which is the state-of-the-art FoM among silicon-based fully integrated 60GHz RTPS.

In addition, the phase shift performance along constant IL contours is particularly useful, if an RTPS is used in a phased-array system. A dense phase shifting and a constant amplitude versus phase shift are both important, so that a matched and constant signal amplitude across the array elements can be achieved for high-quality beam-forming and beam-steering. Therefore, using our transformer-based RTPS design, one can choose the phase shift settings to achieve a full span 360° phase shift along a constant IL, i.e., 10dB,

11dB or 12dB. Note that this is possible due to the dense and repeatable phase interpolations of our RTPS design. The IL variations are largely reduced under the constant IL settings. The resulting maximum/average IL variation for test chip 1 is 0.7dB/0.1dB for the 10dB IL contour, 0.59dB/0.1dB for the 11dB IL contour, and 0.74dB/0.13dB for the 12dB IL contour, while the RTPS still covers a 360° full span phase shift. Consistent performance is achieved by test chip 2 and 3 (Figure 4.22).

The measured input matching for the three RTPS test chips at all the varactor settings over the frequencies are shown in Figure 4.23. The control voltages of the two varactors, i.e., V_{Cv} and V_{Ct}, are independently tuned from -1V to 0.45V. For all the varactor settings, the measured RL values for all the three chips are better than 9.1dB at 58GHz, 9.6dB at 60GHz, 10.4dB at 62GHz and 12.4dB at 64GHz (Figure 4.23), showing a good input matching compared with reported 60GHz RTPS designs [163].

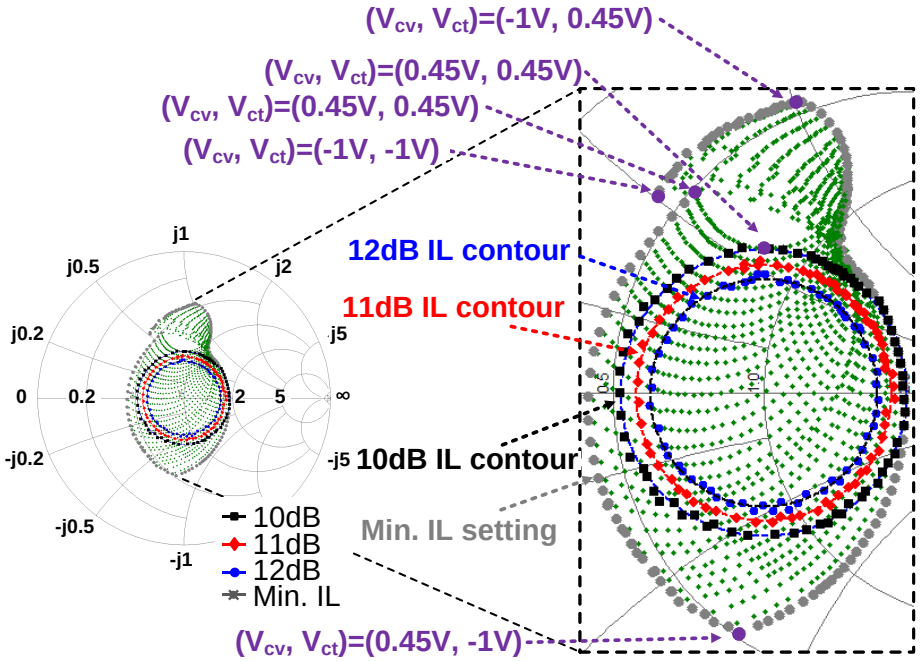
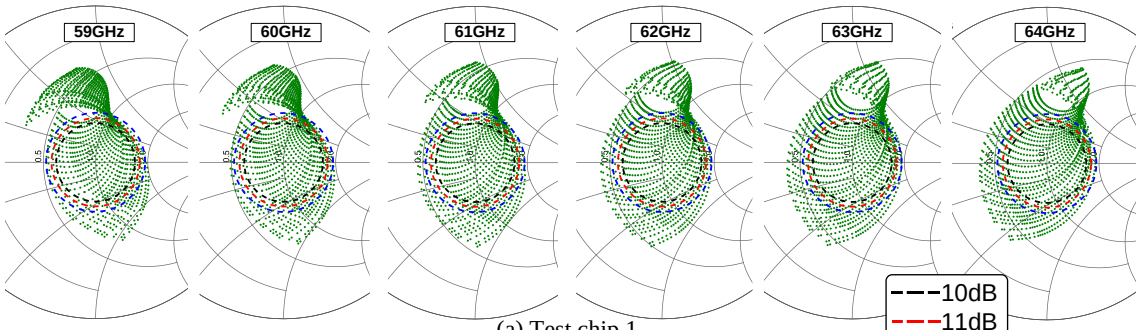
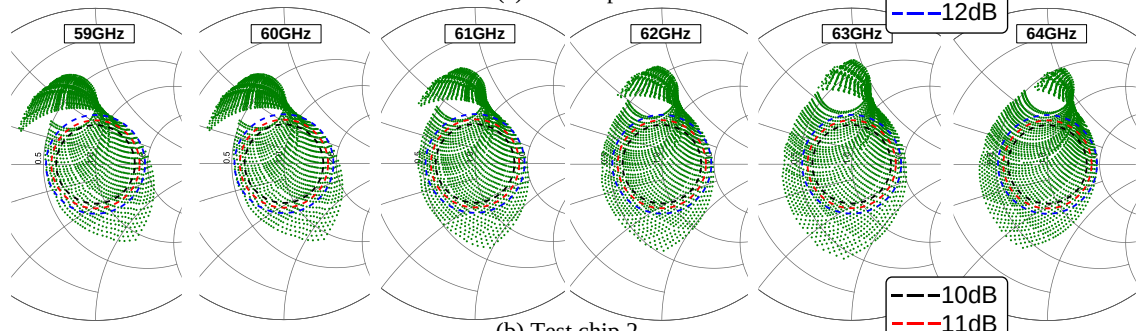


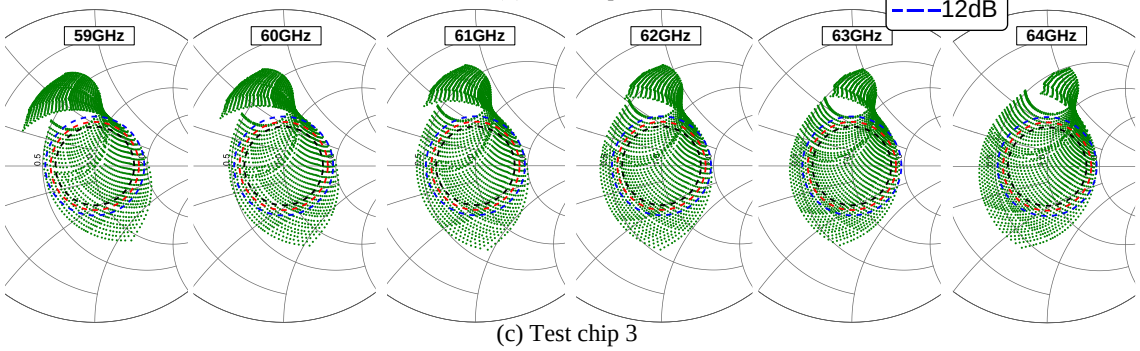
Figure 4.18 – Measured RTPS complex IL at 62GHz for the test chip 1. Minimum IL and constant IL contours (10dB, 11dB, and 12dB) are highlighted.



(a) Test chip 1



(b) Test chip 2



(c) Test chip 3

Figure 4.19 – Measured complex IL of three independent RTPS test chips at different frequencies. The constant IL contours (IL=10/11/12dB) are highlighted.

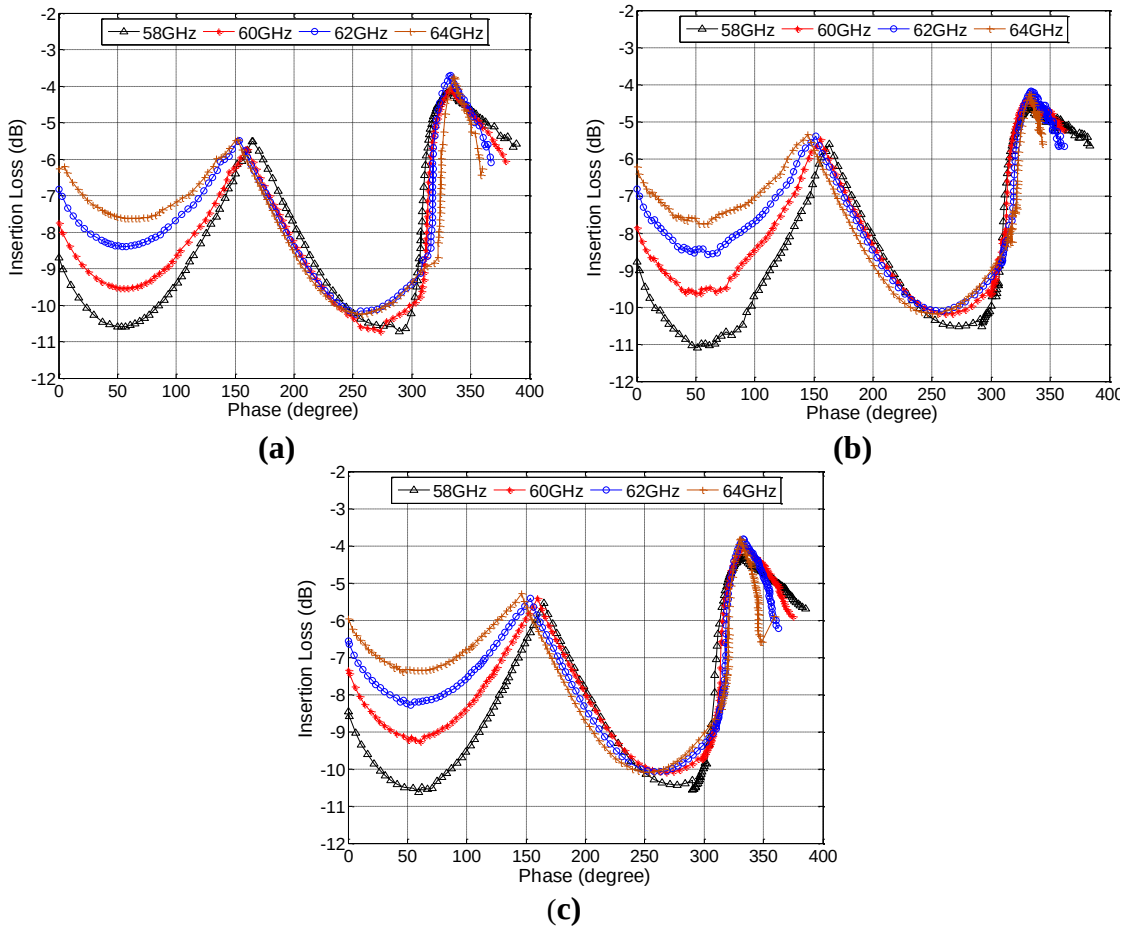


Figure 4.20 – Measured RTPS minimum IL vs. phase shift settings at various frequencies for 3 test chips, e.g., (a) Test chip 1, (b)Test chip 2 and (c)Test chip 3.

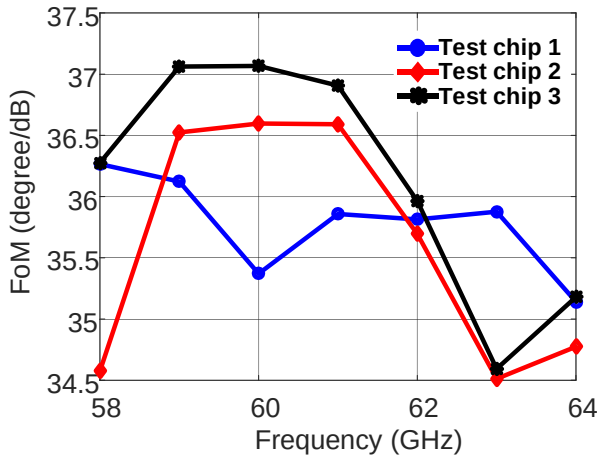


Figure 4.21 – FoM vs. frequency for our RTPS at different frequencies.

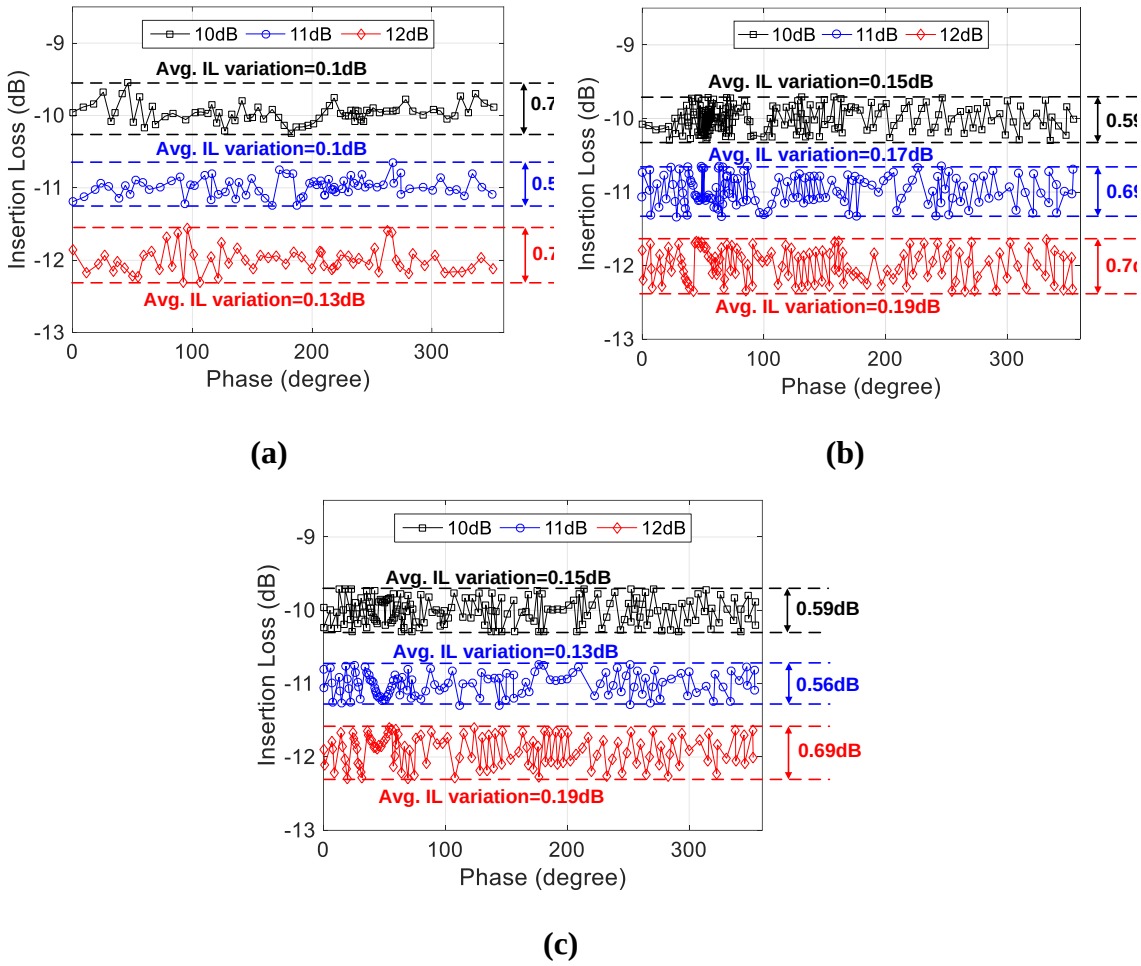


Figure 4.22 – Measured IL variation vs. 360° phase shifts for different constant IL contours (10, 11 and 12dB) at 62GHz for 3 test chips, e.g., (a) Test chip 1, (b)Test chip 2 and (c)Test chip 3.

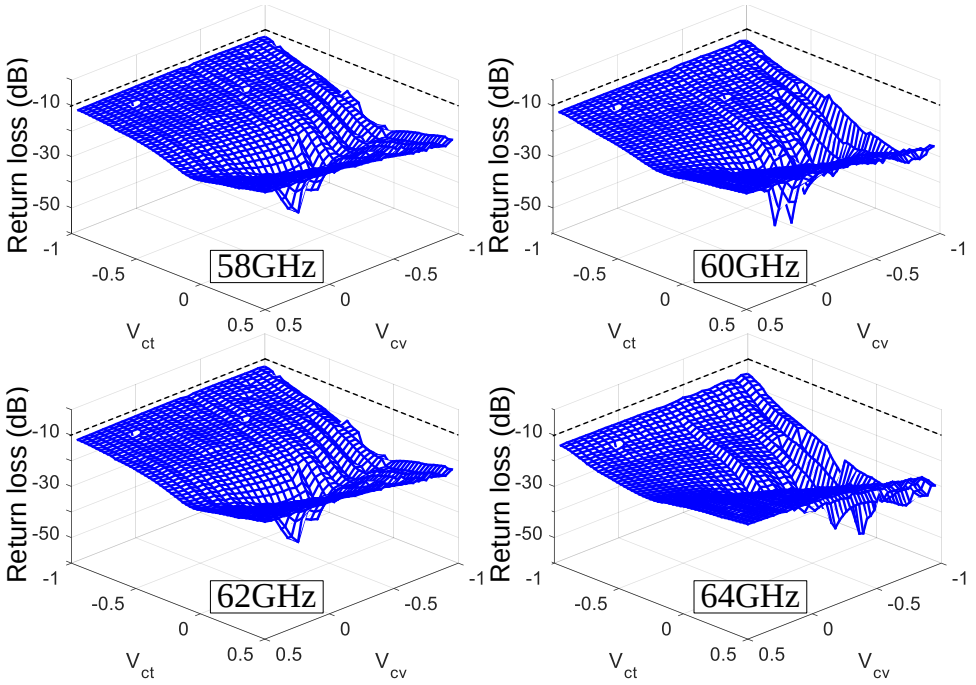


Figure 4.23 – Measured return loss vs. 2 independent control voltages (i.e., V_{cv} and V_{ct}) of three independent RTPS chip samples at 58, 60, 62 and 64GHz for Test chip 1.

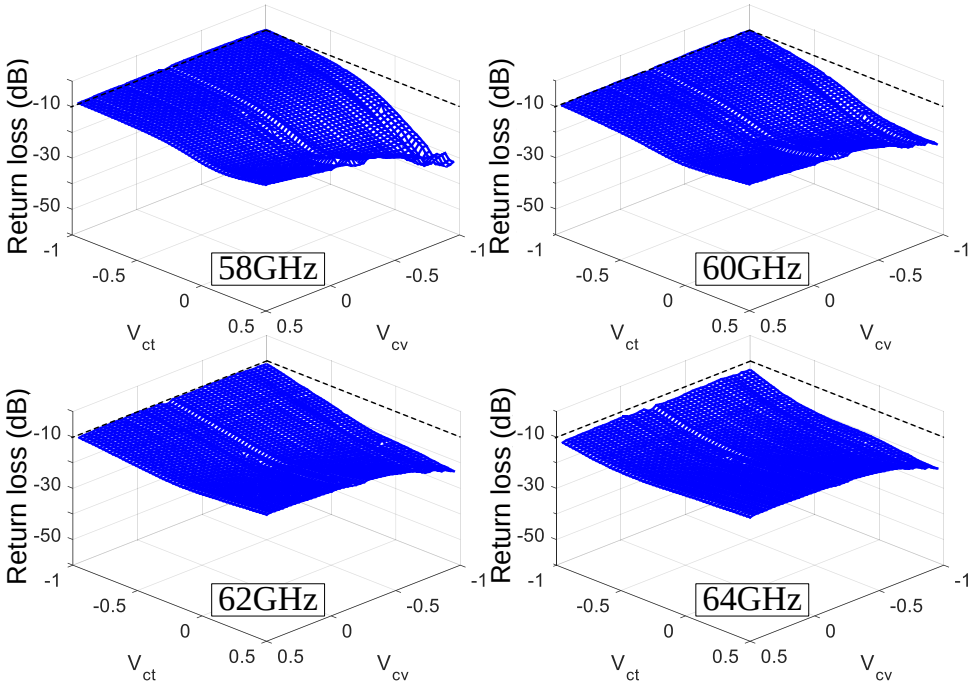


Figure 4.24 – Measured return loss vs. 2 independent control voltages (i.e., V_{cv} and V_{ct}) of three independent RTPS chip samples at 58, 60, 62 and 64GHz for Test chip 2.

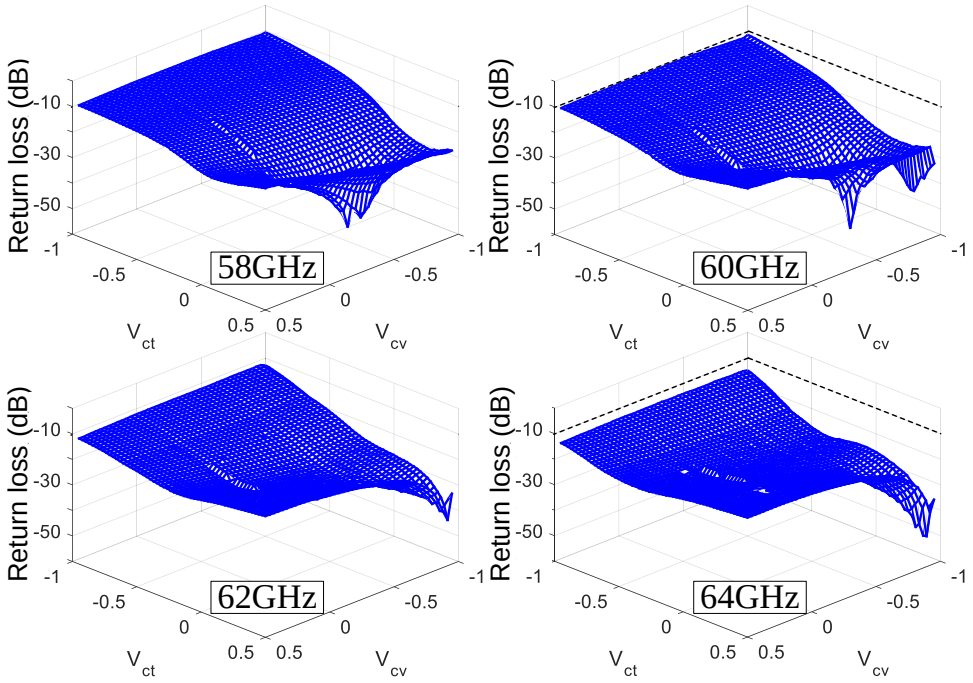


Figure 4.25 – Measured return loss vs. 2 independent control voltages (i.e., V_{cv} and V_{ct}) of three independent RTPS chip samples at 58, 60, 62 and 64GHz for Test chip 3.

Table 4.2 – Performance comparison of reported fully integrated RTPS designs in silicon

Reference	Freq. [GHz]	Max. phase shift [°][(5)]	IL [dB][(5)]	Max. IL variation [dB][(5)]	RL [dB][(5)]	Best FoM [°/dB]	Core chip area [mm^2]	Process
This work	**62**	**367**	**3.7-10.2[(1)] 9.6-10.3[(2)]**	**6.5[(1)] 0.7[(2)]**	**10.4[(5)]**	**37.1**	**0.16**	**130nm BiCMOS**
[160] RFIC 09'	60	180	4.2-7.5 (8.4-15)[(3)]	3.3	-	24	0.18	130nm BiCMOS
[159] CICC 11'	60	180	5-8.3 (10-16.6)[(3)]	3.3	9	21.7	0.031	65nm CMOS
		147	3.3-5.7	2.4	13	25.8	0.048	
[163] ARRAY 10'	60	156	4-6.2	2.2	5	25	0.33	130nm BiCMOS
[164] MWCL 14'	60	90	4.5-6.9 (18-27.6)[(4)]	1.4	12	13	0.25	130nm BiCMOS
[170] *I*MS 16'	60	200	8.2	1	15	24.4	0.28	130nm BiCMOS
[172] EuMC 14'	60	190	10.8	1.8	15	17.6	0.027	90nm CMOS
[169] EuMC 16'	40	60	5	-	17	12	0.18	55nm BiCMOS
[158] T-MTT 08'	2.5	340	8.6-12.6	4	-	27	0.66	180nm CMOS
[155] TCAS-I 07'	1.9	360	20.5	14	-	17.6	2.5	180nm CMOS

[(1)]Minimum IL settings; [(2)]Constant 10dB IL circle settings; [(3)]Assuming two RTPS designs are connected in cascade for 360˚phase shift; [(4)]Assuming four RTPS designs are connected in cascade for 360˚phase shift; [(5)]Evaluated at the center frequency of 62GHz.

4.8. Chapter Summary

We present a comprehensive discussion on different passive reflective loads reported for RTPS designs, their load impedance tuning ranges, and the resulting phase shifting range limits. To address the limitations of reported RTPS reflective loads, we propose a fully differential transformer-based mm-Wave RTPS topology that achieves a full span 360° phase shift, low loss, and a compact area. The proposed transformer-based mm-Wave RTPS is composed of two transformer-based 90° couplers and two transformer-based multi-resonance reflective loads. A proof-of-concept design at 62GHz is implemented in a standard 130nm BiCMOS process with a core area of 480μm-by-340μm, and it achieves a 367° phase shifting range and low IL (3.7dB<|IL|<10.2dB). It also performs a full span 360° phase shifting from 58GHz to 64GHz with a worst-case minimum IL of 10.7dB. Moreover, our RTPS design allows for 360° phase shifting over constant IL contours, e.g., 10dB, 11dB, and 12dB, with a small IL variation (<0.74dB). Compared with the reported fully integrated mm-Wave RTPS in silicon, our design achieves the first-ever full span 367° phase shift, the lowest insertion loss, and the best figure-of-merit (FoM) of 37.1°/dB. Three independent RTPS chips are measured, and highly repeatable results are achieved.

4.9. Appendix

The purpose of this Appendix is to investigate the RTPS performance if the component parasitic losses are included. The overall RTPS insertion loss IL includes the losses caused by the 90º coupler and the reflective loads and is shown as

$$IL = 2IL_{90^\circ} + Loss_{Load} = 2IL_{90^\circ} + \left|\Gamma\right|, \tag{4-25}$$

where all the parameters are in dB scale, and Γ is the reflection coefficient of the reflective load. Since the 90º coupler loss is independent of the reflective load and its setting, it can be considered as a constant additive loss. Therefore, we focus on the loss effect due to the reflective loads here. In Chapter 4.4, we analyze the maximum phase shift range $\Delta\theta_{\max}$ of an RTPS with the lossless reflective loads. Here, we evaluate the impact of lossy reflective loads on the RTPS performance. We follow the same reflective load assumptions and the definitions, and the derived capacitances and inductances in Chapter 4.4.

4.9.1. Capacitive load (CL)

As shown in Figure 4.26(a), the series loss resistance of a varactor is defined as $R_C(\alpha_Q,\alpha)= \alpha_Q/(\omega_0 Q_C^{\max}\alpha C^{\min})$, where α_Q stands for the ratio between the maximum and minimum quality factor Q_C, i.e., $1\le\alpha_Q\le\alpha_Q^{\max}=Q_C^{\max}/Q_C^{\min}$. $Q_C^{\max}$ occurs at $C=C^{\min}$ (i.e., $\alpha=\alpha_Q=1$), and $Q_C^{\min}$ occurs at $C=C^{\max}$ (i.e., $\alpha_Q=\alpha_Q^{\max}$ and $\alpha=\alpha_{\max}$). In addition, if α_Q equals α, R_C will be a fixed series resistor, i.e., $R_C=1/(\omega_0 Q_C^{\max}C^{\min})$. For a CL RTPS, including the loss of R_C, the $\Delta\theta_{\max}$ can be re-written as

$$\begin{aligned}\Delta\theta_{\max} = &\tan^{-1}\left(\frac{\sqrt{\alpha_{\max}}Q_C^{\max}}{Q_C^{\max}+\sqrt{\alpha_{\max}}}\right)+\tan^{-1}\left(\frac{\sqrt{\alpha_{\max}}Q_C^{\max}}{Q_C^{\max}-\sqrt{\alpha_{\max}}}\right)\\ &-\tan^{-1}\left(\frac{Q_C^{\max}}{\sqrt{\alpha_{\max}}Q_C^{\max}+\alpha_Q}\right)-\tan^{-1}\left(\frac{Q_C^{\max}}{\sqrt{\alpha_{\max}}Q_C^{\max}-\alpha_Q}\right).\end{aligned} \tag{4-26}$$

For a given $\alpha_{\max}$, and $Q_C^{\max}$, the $|\Gamma|$ of CL can be derived as

$$|\Gamma| = \sqrt{\frac{\alpha_{\max}\left(Q_{C,\max}^2\alpha_Q^2\right)+Q_{C,\max}\left(\alpha^2 Q_{C,\max}-2\alpha\alpha_Q\sqrt{\alpha_{\max}}\right)}{\alpha_{\max}\left(Q_{C,\max}^2\alpha_Q^2\right)+Q_{C,\max}\left(\alpha^2 Q_{C,\max}-2\alpha\alpha_Q\sqrt{\alpha_{\max}}\right)}}. \tag{4-27}$$

First, based on equations (26) and (27), if Q_C^{max} is large enough, the $\Delta\theta_{max}$ and $|\Gamma|$ of a CL RTPS is close to the ideal lossless case. Next, assuming α_{max}=3, Figure 4.26(b)-(c) show the $\Delta\theta_{max}$ of a lossy CL RTPS and the $|\Gamma|$ for different Q_C^{max} versus the α. The $\Delta\theta_{max}$ of a CL RTPS is almost constant versus different load quality factors, and $|\Gamma|$ varies from -2.3dB (Q_C^{max}=10) to -0.75dB (Q_C^{max}=30). Figure 4.26(d) depicts the load impedance trajectories on Smith chart. Thus, the lossy CL directly degrades the IL but does not reduce its phase shifting range.

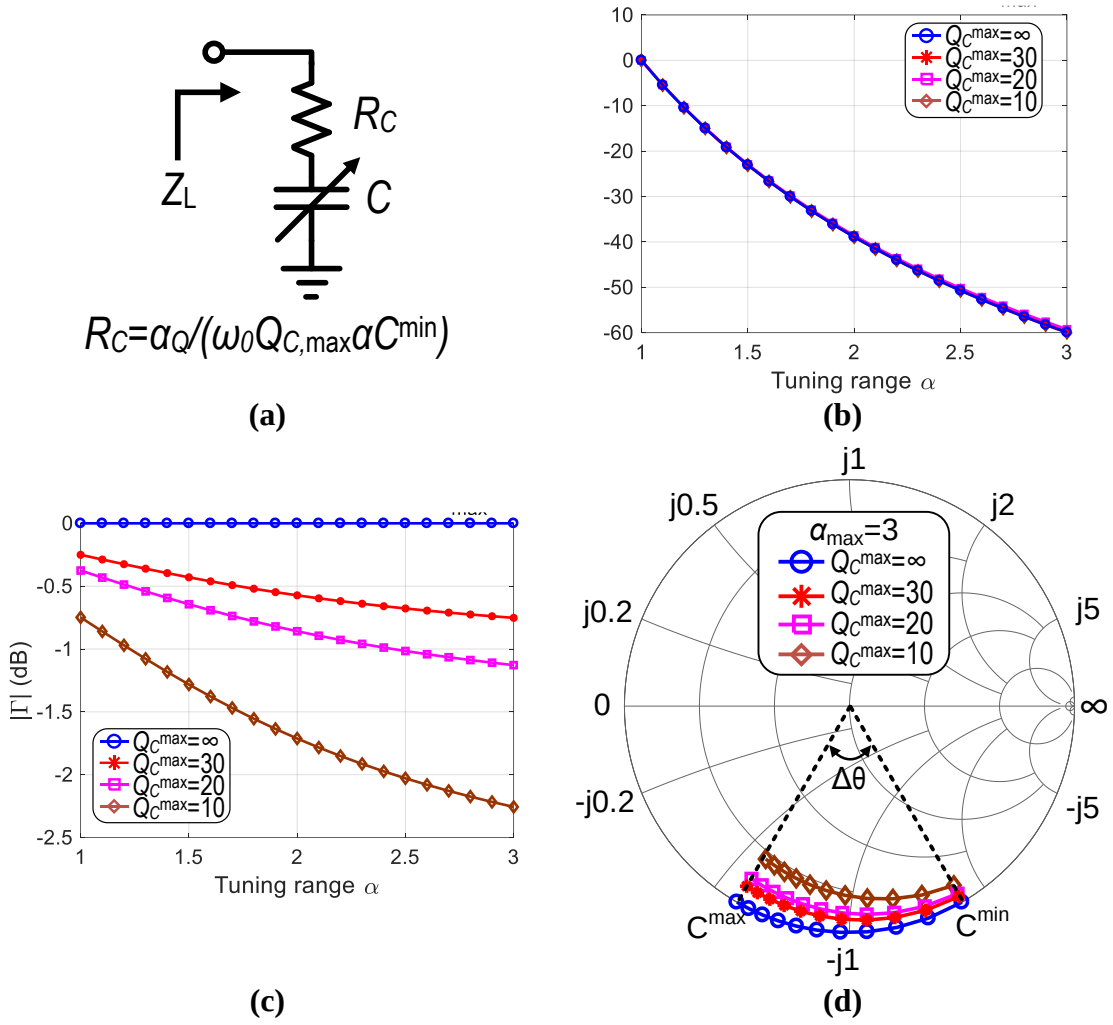


Figure 4.26 – (a) A lossy CL model, (b) the maximum phase shift $\Delta\theta_{max}$ vs. α, (c) the load reflection coefficient $|\Gamma|$ vs. α, and (d) the load impedance trajectory with different Q_C^{max}.

4.9.2. Series L-C resonant load (SLC)

A lossy SLC load is modeled in Figure 4.27(a). Considering the varactor series resistances R_{Cs} and the inductor series resistances R_{Ls}, we define $R_{Ls}=\omega_0 L_s/Q_L$, where Q_L is the quality factor of the inductor L_s at the operating frequency ω_0. The $\Delta\theta_{max}$ of SLC can be obtained in equation (4-28). For a given α_{max} and quality factors Q_L and Q_C^{max}, the $|\Gamma|$ of SLC can be derived in equation (4-29). Choosing $\alpha_{max}=3$ as an example, the $|\Gamma|$ of SLC versus the tuning range α for different quality factors (i.e., $Q_C^{max}=Q_L$) is plotted in Figure 4.27(b). The $\Delta\theta_{max}$ versus different Q_C^{max} (e.g., Q_L and Q_C^{max}) is plotted in Figure 4.27(c). For $\alpha_{max}=3$, the $|\Delta\theta_{max}|$ of an SLC RTPS only exhibits a minor variation (e.g., $\leq 6.3^o$) for different Q_L and Q_C^{max}, compared to the ideal case with lossless load (i.e., $|\Delta\theta_{max}|=120^o$). In addition, assuming $Q_L=Q_C^{max}$, the worst-case $|\Gamma|$ is equal to -5.1dB.

$$\begin{aligned}\Delta\theta_{max} = &\tan^{-1}\left[\frac{(\alpha_{max}-1)Q_L Q_C^{max}}{(1+\alpha_{max})Q_C^{max}+2\alpha_{max}Q_L+2\sqrt{\alpha_{max}}Q_L Q_C^{max}}\right]\\ &-\tan^{-1}\left[\frac{(\alpha_{max}-1)Q_L Q_C^{max}}{(1+\alpha_{max})Q_C^{max}+2\alpha_{max}Q_L-2\sqrt{\alpha_{max}}Q_L Q_C^{max}}\right]\\ &-\tan^{-1}\left[\frac{(\alpha_{max}-1)Q_L Q_C^{max}}{(1+\alpha_{max})Q_C^{max}+2\alpha_{Q}Q_L-2\sqrt{\alpha_{max}}Q_L Q_C^{max}}\right]\\ &+\tan^{-1}\left[\frac{(\alpha_{max}-1)Q_L Q_C^{max}}{(1+\alpha_{max})Q_C^{max}+2\alpha_{Q}Q_L+2\sqrt{\alpha_{max}}Q_L Q_C^{max}}\right].\end{aligned} \tag{4-28}$$

$$|\Gamma| = \sqrt{\frac{Z_0^2-\left[2\omega_0 L_s/Q_L+2\sqrt{\alpha_{max}}\alpha_Q Z_0/\alpha Q_C^{max}\right]Z_0+\left[\omega_0 L_s/Q_L+\sqrt{\alpha_{max}}\alpha_Q Z_0/\alpha Q_C^{max}\right]^2+\left(\omega_0 L_s-\sqrt{\alpha_{max}}Z_0/\alpha\right)^2}{Z_0^2-\left[2\omega_0 L_s/Q_L-2\sqrt{\alpha_{max}}\alpha_Q Z_0/\alpha Q_C^{max}\right]Z_0+\left[\omega_0 L_s/Q_L+\sqrt{\alpha_{max}}\alpha_Q Z_0/\alpha Q_C^{max}\right]^2+\left(\omega_0 L_s-\sqrt{\alpha_{max}}Z_0/\alpha\right)^2}}. \tag{4-29}$$

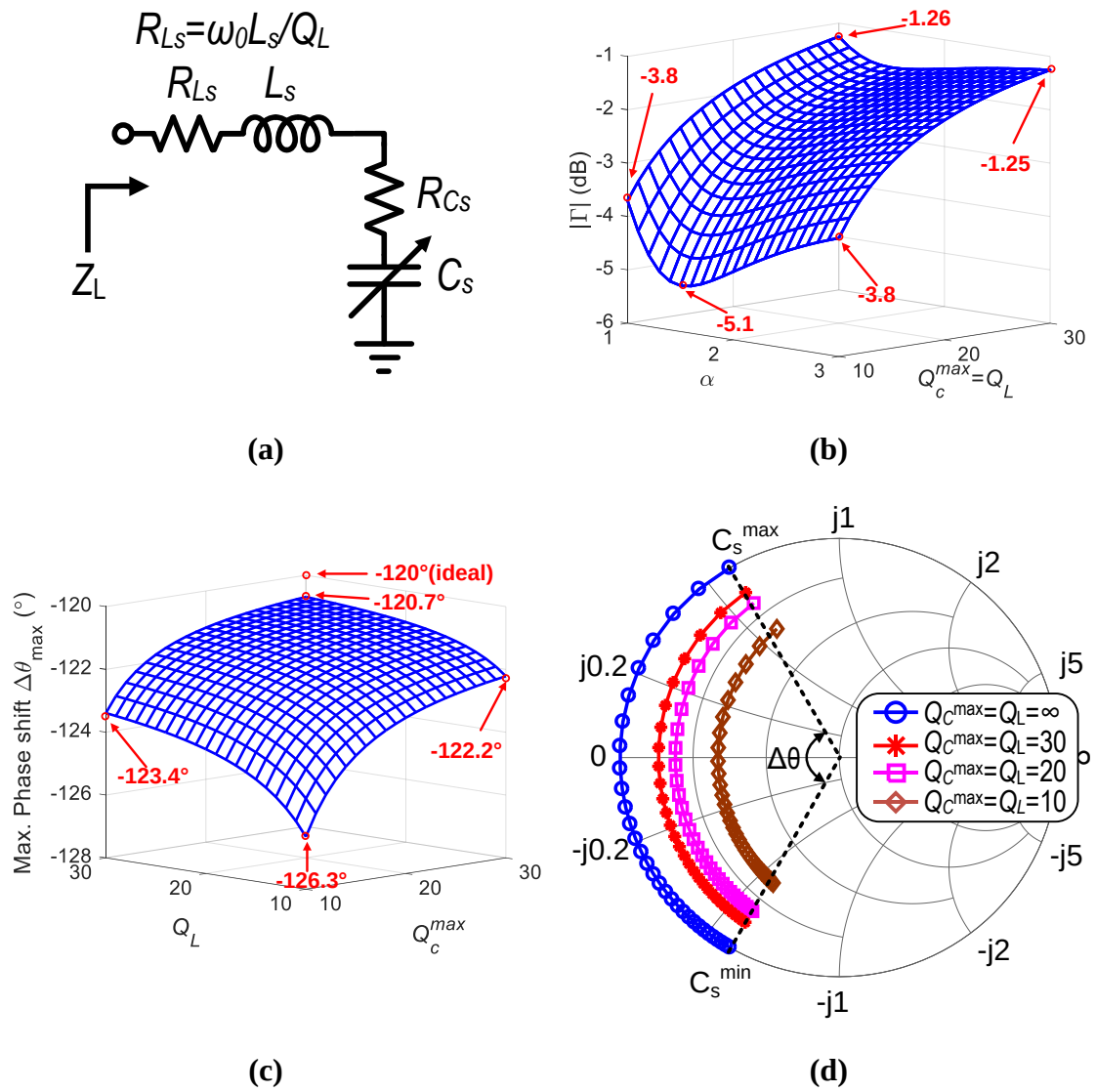


Figure 4.27 – (a) A lossy SLC model, (b) the load reflection coefficient |Γ| as α varies from 1 to α_{max}, (c) the $\Delta\theta_{max}$ versus different quality factors, and (d) the load impedance trajectory on Smith chart with the different Q_C^{max}.

4.9.3. Parallel L-C resonant load (PLC)

The lossy PLC load is modeled in Figure 4.28(a). Including the series resistances R_{Lp} of an inductor and the series resistance R_{Cp} of a varactor, the derived $\Delta\theta_{max}$ of a PCL RTPS in equation (4-10) can be re-written as equation (4-30), and |Γ| is expressed in equation (4-31). Based on the derived equations, for a given α_{max}, the |Γ| of a PLC load

versus the α and the quality factors (e.g., $Q^{\max}=Q_C{}^{\max}=Q_L$) are plotted in Figure 4.28(b). The $\Delta\theta_{\max}$ of an RTPS with PLC load versus different quality factors (e.g., Q_L and $Q_C{}^{\max}$) is plotted in Figure 4.28(c). Also, the load impedance trajectory with different quality factors (e.g., Q_L and $Q_C{}^{\max}$) are shown in Figure 4.28(d). Assuming $\alpha_{\max}=3$, the $\Delta\theta_{\max}$ of PLC also only occurs minor variation, i.e., $118.7^{\circ}\le|\Delta\theta_{\max}|\le123.7^{\circ}$, for different values of the quality factor (e.g., $10\le Q_L=Q_C{}^{\max}\le30$). The worst-case $|\Gamma|$ equals -8.9dB. Compared with SLC, if the resistances caused by finite quality factor are included, PCL exhibits a similar $\Delta\theta_{\max}$ variation but higher loss.

$$\begin{aligned}\Delta\theta_{\max} \cong & \tan^{-1}\left\{\frac{1+\left(\frac{\alpha_Q}{Q_C^{\max}}\right)^2-\frac{\sqrt{\alpha_{\max}}\omega_0 L_p}{Z_0}}{\frac{\sqrt{\alpha_{\max}}\omega_0 L_p}{Z_0}\left(\sqrt{\alpha_{\max}}+\frac{\alpha_Q}{Q_C^{\max}}\right)-2\sqrt{\alpha_{\max}}+\left(\frac{1}{Q_L}+\frac{Z_0}{\omega_0 L_p}\right)}\right\}\\ & -\tan^{-1}\left\{\frac{1-\frac{\omega_0 L_p}{\sqrt{\alpha_{\max}}Z_0}}{\frac{\omega_0 L_p}{\alpha_{\max}Z_0}-\frac{2}{\sqrt{\alpha_{\max}}}+\left(\frac{1}{Q_L}+\frac{Z_0}{\omega_0 L_p}\right)}\right\}\\ & +\tan^{-1}\left\{\frac{1+\left(\frac{\alpha_Q}{Q_C^{\max}}\right)^2-\frac{\sqrt{\alpha_{\max}}\omega_0 L_p}{Z_0}}{\frac{\sqrt{\alpha_{\max}}\omega_0 L_p}{Z_0}\left(\sqrt{\alpha_{\max}}-\frac{\alpha_Q}{Q_C^{\max}}\right)-2\sqrt{\alpha_{\max}}-\left(\frac{1}{Q_L}-\frac{Z_0}{\omega_0 L_p}\right)}\right\}\\ & -\tan^{-1}\left\{\frac{1-\frac{\omega_0 L_p}{\sqrt{\alpha_{\max}}Z_0}}{\frac{\omega_0 L_p}{\alpha_{\max}Z_0}-\frac{2}{\sqrt{\alpha_{\max}}}-\left(\frac{1}{Q_L}-\frac{Z_0}{\omega_0 L_p}\right)}\right\}.\end{aligned} \tag{4-30}$$

$$|\Gamma| \cong \sqrt{\frac{\dfrac{\alpha\omega_0^2 L_p}{\sqrt{\alpha_{\max}}}\left(\dfrac{\alpha\omega_0 Z_0 C_p^{\min}}{Q_L^2}-\dfrac{2\alpha_Q}{Q_C^{\max}}\right)-\dfrac{2\alpha\omega_0 Z_0 L_p}{\sqrt{\alpha_{\max}}}\left(1-\dfrac{\alpha_Q}{Q_C^{\max}Q_L}\right)+\left(\omega_0^2 L_p^2+Z_0^2-\dfrac{2\omega_0 Z_0 L_p}{Q_L}\right)\left[1+\left(\dfrac{\alpha_Q}{Q_C^{\max}}\right)^2\right]}{\dfrac{\alpha\omega_0^2 L_p}{\sqrt{\alpha_{\max}}}\left(\dfrac{\alpha\omega_0 Z_0 C_p^{\min}}{Q_L^2}+\dfrac{2\alpha_Q}{Q_C^{\max}}\right)-\dfrac{2\alpha\omega_0 Z_0 L_p}{\sqrt{\alpha_{\max}}}\left(1-\dfrac{\alpha_Q}{Q_C^{\max}Q_L}\right)+\left(\omega_0^2 L_p^2+Z_0^2+\dfrac{2\omega_0 Z_0 L_p}{Q_L}\right)\left[1+\left(\dfrac{\alpha_Q}{Q_C^{\max}}\right)^2\right]}} \quad (4\text{-}31)$$

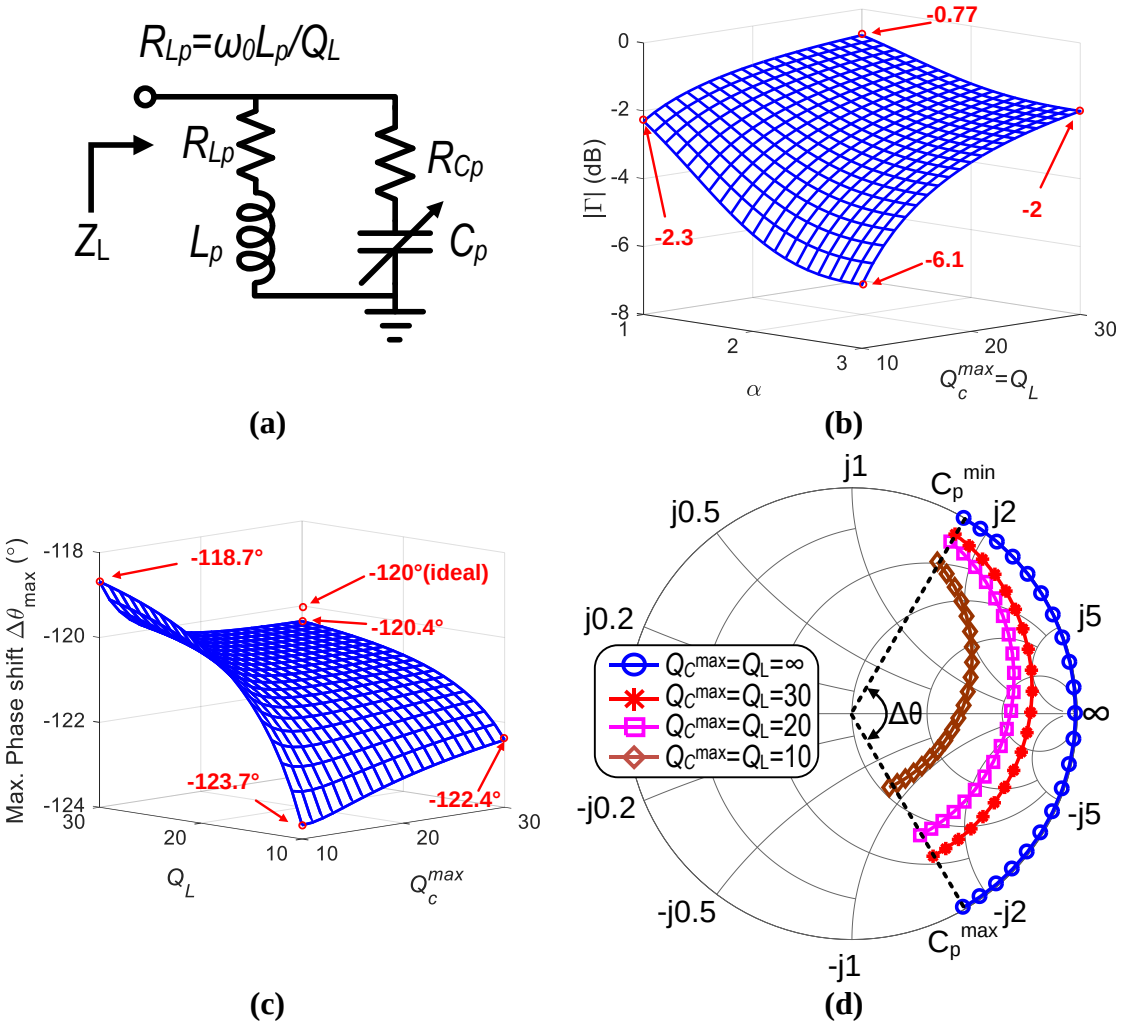


Figure 4.28 – (a) A lossy PLC model, (b) the load reflection coefficient |Γ| as α varies from 1 to α_{max}, (c) the $\Delta\theta_{max}$ versus different quality factors, and (d) the load impedance trajectory on Smith chart with the different $Q_C{}^{max}$.

4.9.4. CLC π-resonant load with one-side capacitive tuning)

The lossy CLC-1 model with the resistances R_{C2}, R_{C3} and R_{L1} is shown in Figure 4.29(a). For a given α_{max}=3, Figure 4.29(b)-(d) show the load impedance trajectories on Smith chart versus the α of C_2 and the quality factors (e.g., Q_{C3}, Q_L and Q_{C2}^{max}) for different β (i.e., $\beta=C_3/C_2^{min}$). A larger β for CLC-1 achieves a wider phase shift, but the losses increase accordingly. Also, with smaller quality factors (e.g., $Q\leq10$), the load reflection coefficient trajectory cannot circle the origin of the Smith chart, which substantially shrinks the phase shift. For example, the load impedance phase $\angle\Gamma(C_2^{min'})$ and $\angle\Gamma(C_2^{max'})$ for Q=10 are 190º and 279.4º, but, $\angle\Gamma(C_2^{min})$ and $\angle\Gamma(C_2^{max})$ for Q=20 are 195.7º and 283.1º, respectively. Thus, the $|\Delta\theta_{max}|$ for Q=20 is 272.6º while the $|\Delta\theta_{max}|$ for Q=10 is only 89.4º (Figure 4.29d).

4.9.5. CLC π-resonant load with two-side capacitive tuning

The lossy CLC-2 model is shown in Figure 4.30(a), which contains the series resistances R_{C2}, R_{C3} and R_L. For α_{max}=3 and β=1, Figure 4.30(b) shows the load impedance trajectory on the Smith chart versus the α of C_2 and C_3, i.e., $1\leq\alpha_3=\alpha_2=\alpha\leq\alpha_{max}$, and the quality factors, i.e., $Q_{C3}^{max}=Q_L=Q_{C2}^{max}$. Like CLC-1, for smaller quality factors (e.g., $Q\leq10$), the CLC-2 cannot circle the origin of the Smith chart, reducing its phase shift significantly Figure 4.30(b). Thus, the higher-order reflective loads can achieve a larger phase shift but introduce larger losses. The large passive loss may also reduce the phase shifting range.

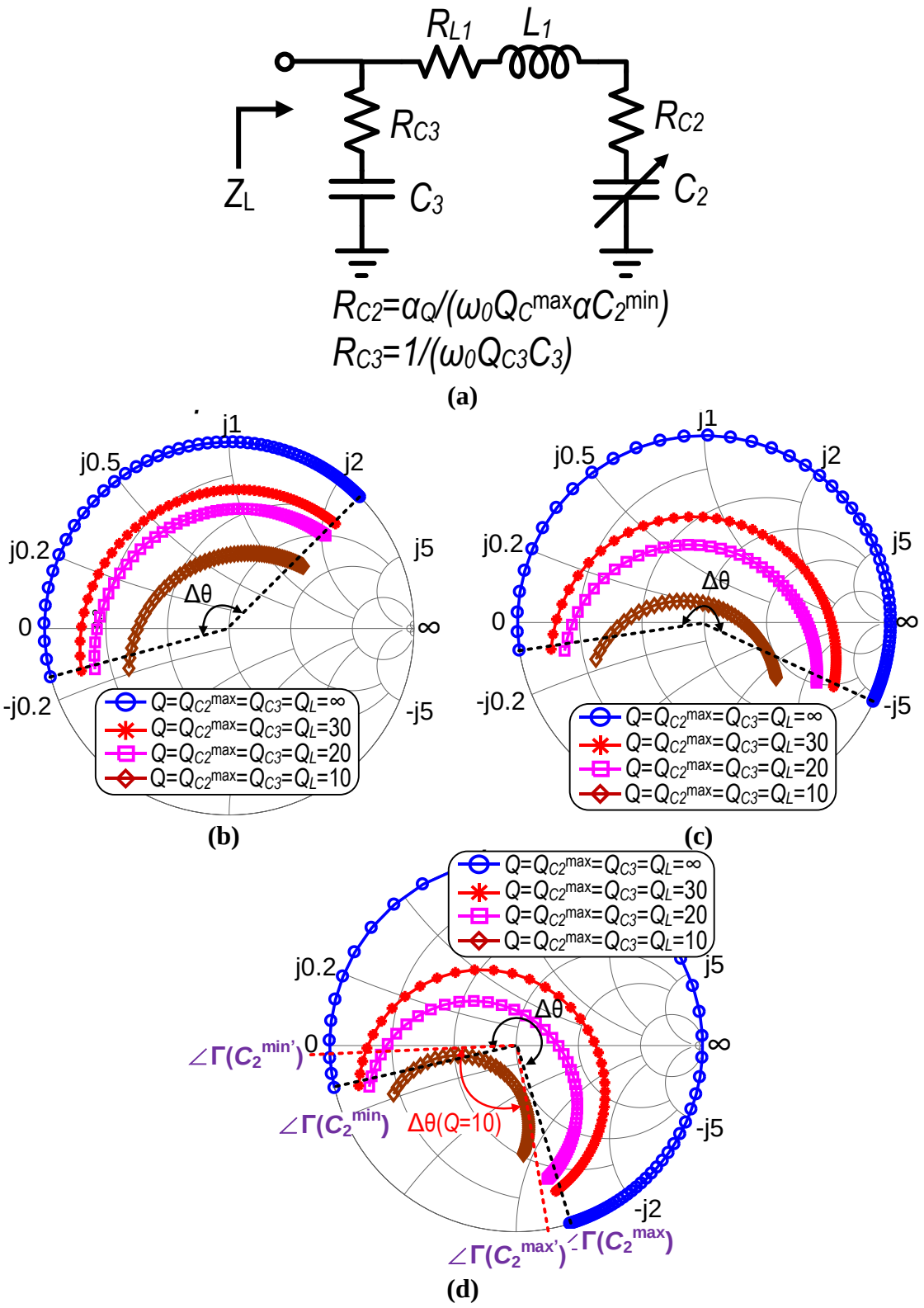
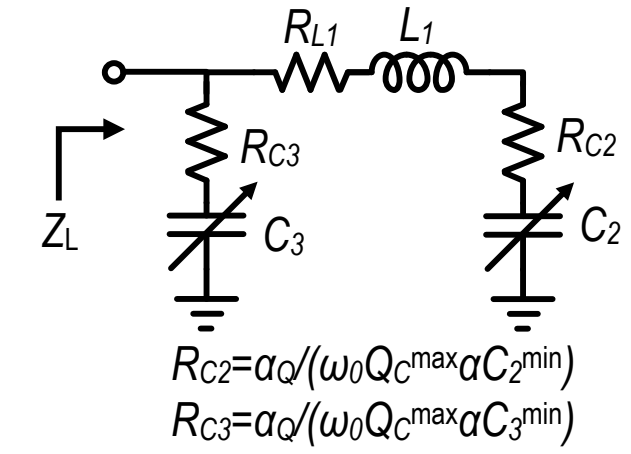
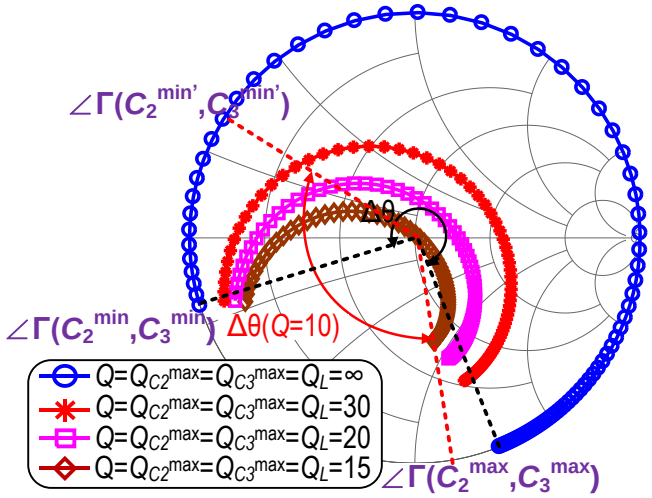


Figure 4.29 – (a) A lossy CLC-1 model, (b) the load impedance trajectory on Smith chart with different quality factors for α_{max}=3 and β=1, (c) β=2 and (d) β=3.



(a)



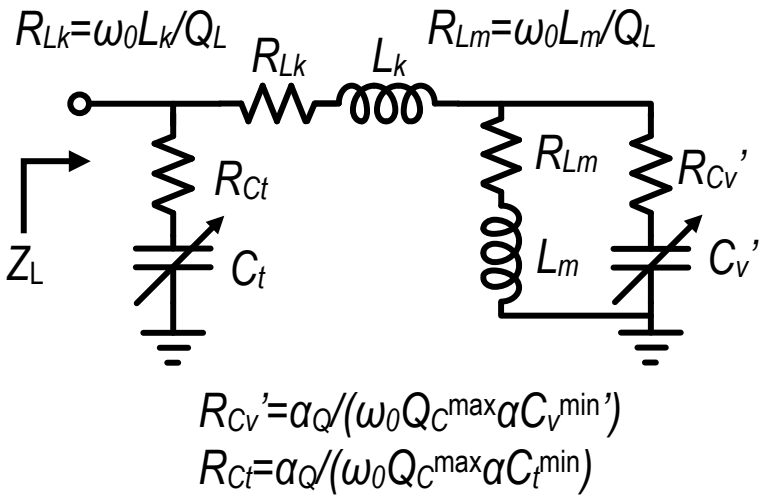
(b)

Figure 4.30 – (a) A lossy CLC-2 model and (b) the lossy CLC-2 load impedance trajectory on Smith chart with the different quality factors for α_{max}=3 and β=1.

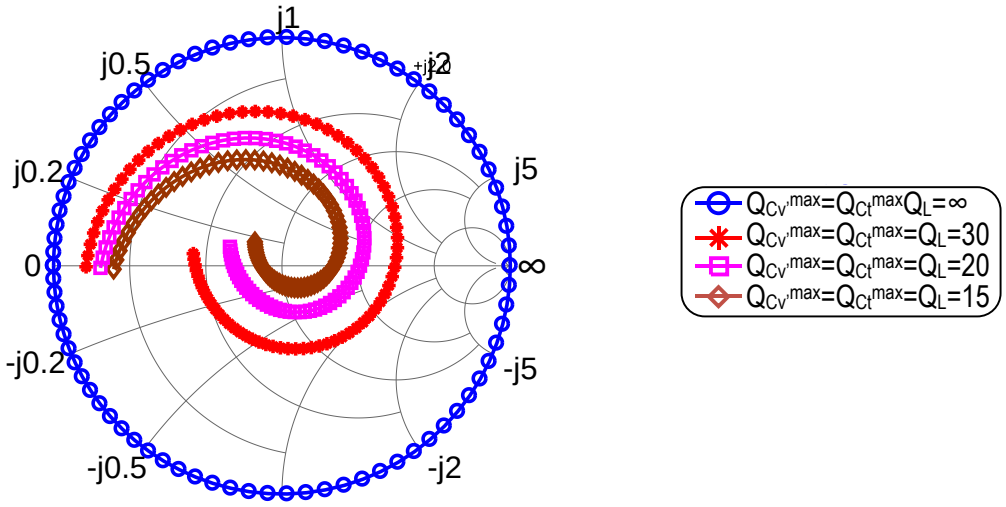
4.9.6. Transformer-based multi-resonance reflective load

Our proposed transformer-based multi-resonance reflective load, including the resistances, R_{Cv}', R_{Lm}, R_{Lk}, and R_{Ct}, is shown in Figure 4.31(a) Assuming α_{max}=3 and $\alpha_v=\alpha_t$, the load impedance trajectory with different quality factors (e.g., Q_L, $Q_{cv}{}^{max}$ and $Q_{ct}{}^{max}$)

are shown on the Smith chart Figure 4.31(b). Compared with CLC-2, with the same quality factors (e.g., Q_L, $Q_{cv}{}'^{max}$, $Q_{ct}{}^{max}$), an RTPS with our proposed reflective load can consistently achieve a full-span 360º phase shift as well as lower or similar passive loss. This shows the advantages of our proposed load for high-performance mm-Wave RTPS.



(a)



(b)

Figure 4.31 – (a) A lossy proposed transformer-based multi-resonance reflective model and (b) the load impedance trajectory on Smith chart with the different quality factors for α_{max}=3.

CHAPTER 5. CONCLUSIONS

In this dissertation, we discussed our PA output networks for continuous-mode harmonically-tuned operations, PA linearity improvement technique and reflective loads innovations towards the development of silicon-based PAs and RTPS for 5G emerging applications at mm-Wave frequency ranges.

First, we present three mm-wave continuous-mode PAs for 5G MIMO applications, including a two-stage differential continuous-mode Class-F^{-1} PA in 130-nm SiGe process, a single-stage differential continuous-mode hybrid Class-F/F^{-1} PA in 45-nm SOI CMOS process, and a two-stage differential continuous-mode hybrid Class-F/F^{-1} PA in 45-nmSOI CMOS process. The first PA design covers 19-29.5 GHz, while the other two designs cover 23-41 GHz, all covering multiple 5G bands (24/28/37/39GHz). All the presented PA designs are based on a proposed transformer-based continuous-mode harmonically tuned PA output network. This network provides proper harmonic impedance terminations for the fundamental, second-order, and third-order harmonic impedances, whichsupportscontinuous-modeClass-F^{-1} or hybrid Class-F/F^{-1} PA operations to achieve ultra-wide bandwidth yet high efficiency. The first PA design achieves awidePsat1-dB bandwidth of 19–29.5 GHz (43.3%) and high peak PAE (43.5%). The second design achieves an ultrawide P_{sat} 1-dB bandwidth of 23.5-41 GHz (53.3%) and high peak PAE (46%). Moreover, it achieves 43.4% PAE and 18.6dBm P_{sat} at 27 GHz, 40.2% PAE and 18.6dBm P_{sat} at 37GHz, and 41.2% PAE and 18.5dBm P_{sat} at 39 GHz, respectively. The third PA design also achieves an ultra-wide P_{sat} 1-dB bandwidth of 23.5-41 GHz (53.3%) and high peak PAE (43.2%). It achieves 43% PAE and 18.9dBm P_{sat} at 27 GHz, 37% PAE

and 19dBm P_{sat} at 37 GHz, and 36% PAE and 18.9dBm P_{sat} at 39 GHz, respectively. Extensive 64- and 256-QAM modulation tests demonstrate the high PA linearity. Our proposed PA designs outperform the reported mm-wave silicon-based 5G PAs in terms of high efficiency over an ultrawide bandwidth.

Finally, we present a millimeter-wave fully differential transformer-based passive RTPS capable of performing full span 360° continuous phase shift from 58GHz to 64GHz. It consists of two transformer-based 90° couplers and two transformer-based multi-resonance reflective loads to provide 360° phase shift with low loss and ultra-compact chip size. Our proof-of-concept design is implemented in a standard 130nm BiCMOS process with a core area of 480μm-by-340μm. It achieves a wide phase shifting range of 367° and a low insertion loss IL (3.7dB<|IL|<10.2dB) at 62GHz and maintains a full span 360° phase shifting range from 58GHz to 64GHz. Moreover, it supports 360° phase shifting with a constant IL, i.e., |IL|=10, 11, 12dB, at an IL variation of less than 0.74dB at 62GHz. To the best of our knowledge, this design achieves a first-ever full span 360° phase shifting (up to 367°), the lowest IL, the smallest IL variation, and the best figure-of-merit (FoM) of 37.1°/dB among reported 60GHz fully integrated RTPS in silicon.

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