IMPLEMENTATION OF CMOS RF CIRCUITS WITH OCTAVE AND MULTI-OCTAVE BANDWIDTH FOR PHASED ARRAY ANTENNAS

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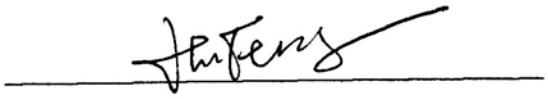
Declaration

I hereby declare that the thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.



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Summary

Ultra-wideband phased array systems have attracted more and more interest in the modern radio development. With the extensive growth of low cost silicon (Si) based Complementary Metal-Oxide-Semiconductor (CMOS) in the industry, it is beneficial to integrate ultra-wideband phased array systems into CMOS. This thesis focuses on the implementations of radio frequency components with ultra-wide bandwidth performance for such systems.

The first part of the thesis focuses on the research and design of high selective bandpass filters (BPFs) with 66% fractional bandwidth. Two design methods are demonstrated. The first method is based on active inductors (AIs) with a focus on the active series inductors because active bandpass filters with an arbitrary bandwidth would be feasible when both the series and shunt inductors have their active realizations. The second technique is based on the proposed active resonators. The limitations of the active inductor based technique are alleviated by using this method. Both design approaches generate a highly selective bandpass response in CMOS with a bandwidth larger than an octave.

The second part of the thesis deals with another key component for the ultra-wideband phased arrays, the true time delay (TTD). The proposed design techniques are based on second order all pass networks (APNs), because the higher order response of their group delay makes it easier to achieve wider

bandwidth, flatter group delay and smaller area. Different switching topologies for high resolution, high delay true time delay chains are investigated. Each of them has their own advantages and disadvantages. Exploiting their advantages, they are integrated in a single delay chain to obtain a large delay, a high resolution and a compact size simultaneously.

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List of Abbreviations

AI.	Active Inductor
APN.	All-Pass Network
BPF.	Bandpass Filter
CDMA.	Code Division Multiple Access
CMOS.	Complementary Metal-Oxide Semiconductor
EM.	Electromagnetic
FBW.	Fractional Bandwidth
FET.	Field Effect Transistor
IL.	Insertion Loss
IR.	Impulse Radio
LOS.	Light-of-Sight
LSB.	Lowest Significant Bit
MSB.	Most Significant Bit
OFDM.	Orthogonal Frequency Division Multiplexing
OTA.	Operational Transconductance Amplifier
PCB.	Printed Circuit Board
RL.	Return Loss
SAW.	Surface Acoustic Wave
Si.	Silicon
SNR.	Signal-to-Noise Ratio

TL.	Transmission Line
TTD.	True Time Delay
UWB.	Ultra-Wideband
WPAN.	Wideband Personal Area Networking

Chapter 1 Introduction

Radio technology has been extensively developed in the past decades since the establishment of electromagnetic theory [1]. The radio enables wireless detection and wireless information exchange. The typical examples are radar systems and wireless communication systems, which have been of major interest throughout the history of radio.

1.1 Phased Array Antennas

In modern radars and wireless communication systems, phased array antennas increasingly find adoptions. In such an array, multiple antennas are placed in proximity and each of the antenna elements is contributing with a weighting factor for the system performance.

The principle of a one-dimensional linear phased array is shown in Figure 1.1. The N antennas are equally spaced with a distance of d. With an incident wave arriving at an angle of θ, the phase difference of the signals between adjacent antennas will be

$$\Delta\varphi = kd\sin\theta \tag{1.1}$$

where $k=2\pi/\lambda$, and λ is the wavelength. With proper phase compensation for individual antenna channels, the final summation of the N channels can therefore select the incident wave at a certain arrival angle and reject other directions. For the n^{th} channel ($1 < n \le N$), the compensation phase referred

to the first channel is

$$\Delta\varphi_n = (n-1)kd\sin\theta \tag{1.2}$$

The preceding discussion of the receiving mode also applies for the case of transmission.

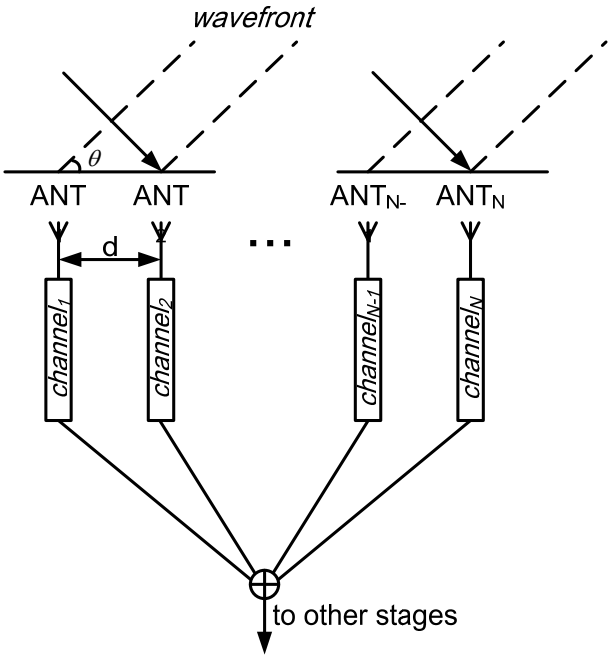

Figure 1.1. Simplified principle of the linear phased array.

For a narrow band signal, the phase compensation in equation (1.2) can be provided with phase shifters. The corresponding implementations would be much easier because only the limited phase shifting range of 0-2π is needed [2].

However, the frequency dependent parameter k in equation (1.2) requires a varying phase compensation in case of wideband applications. In this scenario, a true time delay compensation is more appropriate [3], in which the phase shift for each channel is replaced by the time delay. The time delay for the n^{th}

channel in the array will be

$$\Delta\tau_n = \frac{(n-1)d\sin\theta}{c} \tag{1.3}$$

where c is the speed of the electromagnetic (EM) wave in the radiation channel.

Because of the contribution of multiple antennas, the overall gain of the phased array antenna is higher than that of a single antenna. The normalized array factor for the linear N-element phased array antennas is [4]

$$AF(\theta) = \frac{\sin(N/2(kd\sin\theta - \phi_c))}{N\sin(1/2(kd\sin\theta - \phi_c))} \tag{1.4}$$

where ϕ_c is the phase difference between adjacent antenna elements and θ is the angle between the observation direction and the array. We can see that the direction of the beam is determined by

$$\theta_o = \arcsin\frac{\phi_c}{kd} \tag{1.5}$$

The radiation and receiving direction of the phased array is thus flexible and electrically controllable, which is one of the main advantages compared to the conventional mechanically rotated antennas.

Another merit of phased array antennas is the possibility to perform multiple functions simultaneously. Appropriate weighting factors are applied for the antenna elements in the array and with such an implementation, adaptive array antennas are realizable [5].

Moreover, the overall system signal-to-noise ratio (SNR) performance is enhanced in the phased array, especially for the active phased array system. This is because the noise of individual channels is uncorrelated while the

useful signals from each channel are additive. The improvement is typically between N to N^2 (where N is the number of antennas) [6].

1.2 Ultra-Broadband Radio

Another trend of modern radio growth is the increasing demand for larger bandwidths. One of the benefits of the wideband radio can be understood with the well-known Shannon's channel capacity equation [7], whose simplified form is shown as:

$$C = B\log_2(1+SNR) \tag{1.6}$$

where C is the channel capacity in bits, B is the bandwidth in Hertz and SNR is the signal to noise ratio. It can be seen that a higher data rate can be achieved with wideband radio compared to the narrow bandwidth counterpart. From another perspective, the wideband system has a less stringent SNR requirement compared to the narrowband system if it works at the same data transmission rate.

One realization of the ultra-broadband radio concept is the ultra-wideband (UWB) technology. The loose definition of UWB refers to any wireless communication scheme that occupies a fractional bandwidth (FBW) larger than 25% or an absolute bandwidth larger than 1.5 GHz. The FBW is defined as

$$FBW = 2\frac{f_h - f_l}{f_h + f_l} \tag{1.7}$$

where f_h and f_l are the higher and lower cutoff frequencies respectively.

Its potential applications in the wireless communication have been forecasted and discussed several years ago [8], [9]. More UWB related schemes were subsequently proposed like the wide-band orthogonal frequency division multiplexing (OFDM) and the code division multiple access (CDMA) for areas like wideband personal area networking (WPAN) [10]. Other than those, the impulse-radio (IR) UWB has been of major interest [11], [12]. The first reason is that the IR-UWB is relatively immune to the multipath effects of the wireless communication channels, because IR-UWB can discriminate between the line-of-sight (LOS) signal and the reflected waves from other obstacles in the environment. Additionally, power consumption adaptivity is achievable when the duty cycles of the IR-UWB systems are tuned. This makes it attractive for battery-operated equipment like bio-medical sensors. And finally, the ultra-wide bandwidth makes the communication channel more secure because it is much more difficult for eavesdroppers to monitor all the frequency bands.

Wideband radio also finds its own attractiveness in the radar applications. It is found that the resolution of the IR radar is generally correlated with the bandwidth of the pulse as [13]

$$R = \frac{c}{2B} \tag{1.8}$$

Where c is the speed of radio wave and the B is the bandwidth. The bandwidth of the IR radar can also be extended by pulse compression techniques [14],

[15], if the pulse width cannot be further shortened. The IR-UWB radars also have less interference with each other because of the low probability of pulse-on-pulse situations. Furthermore, the UWB radar system also advances with a higher ability to detect objects with slow velocities or even stationary objects [16].

1.3 Motivation of the Thesis

Multi-antenna based phased arrays with broader bandwidth are one of the most promising directions in the radio system evolution [2], [4], [10], [17]. It is thus beneficial to implement them using mature low cost CMOS technology. This thesis aims to deal with the implementation issues for some of the key components for ultra-broadband phased array systems in standard CMOS.

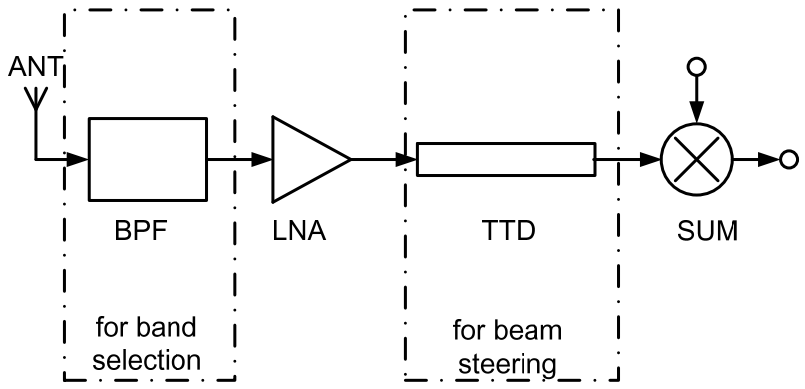

Figure 1.2. A typcial block diagram of the ultra-broadband phased array receiver channel.

The typical block diagram of the ultra-broadband phased array receiver channel is shown in Figure 1.2. A bandpass filter is located in front of the low noise amplifier (LNA) to select the specific frequency band for the application. In

order to effectively reject the unwanted signals from other frequency ranges, the band select BPF should be high selective. The noise performance of the receiver chain is then improved by the subsequent LNA. As described previously, a broadband application of the phased array requires the TTD to replace the phase shifter. The summation happens at the end of the channel to add signals from other channels.

One of the key parameters of the receiver chain is the effective noise figure *F*. The cascaded noise figure can be estimated with equation (1.9).

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots \frac{F_N - 1}{G_1 G_2 \ldots G_{N-1}} \tag{1.9}$$

The first stage of the receiver (the BPF in this case) will contribute the most of the noise floor to the system. Consequently, the noise performance of the BPF should be taken into account. For example, an active BPF with relatively high noise figure might be suitable for applications with less constraint on noise performance, like short-range low data rate communications.

On the other hand, the large signal behavior of the receiver can be characterized with

$$P = \frac{1}{\frac{1}{P_1 G_2 G_3 \ldots G_N} + \frac{1}{P_2 G_3 \ldots G_N} + \ldots + \frac{1}{P_N}} \tag{1.10}$$

where P is the effective output compression point (OP_{1dB} or OP_{3dB}) of the receiver. P_n *and* G_n $(0 \le n \le N)$ are the corresponding compression points and gain of each stage. It can be seen that the terms that contribute the most are those before the stage with loss, i.e. the stage with $G_n < 1$.

The main components under consideration in this thesis are the BPF and the TTD. Implementations of these two components on CMOS are investigated in this thesis.

1.3.1 Active Bandpass Filters with Ultra-wide Bandwidth for Ultra-wideband Phased Array System Integration

One of the key components in the radio system, whether for wideband or for narrow band applications, is the bandpass filter (BPF). As a frequency selective component, its frequency selectivity is of significant importance, which can be represented by the shape factor. The shape factor is defined in this thesis as the ratio between the 3 dB bandwidth and the 20 dB bandwidth of the BPF.

Due to the large loss in CMOS, the high selective BPFs in radio systems are more frequently implemented with "off-chip" processes like Surface Acoustic Wave (SAW) and Printed Circuit Board (PCB) [18], [19].

With the demand for a higher integration level of radio systems, CMOS BPFs are extensively investigated and active BPFs are commonly proposed. The active BPFs can be categorized into three types. The first type is the transconductance-C (G_m-C) type [20]. The bandpass response is generated with analog methods in voltage domain, like the integrators [21] and biquadratic cells [22]. The G_m-C type BPFs are mostly adopted in the low frequency range or for lowpass applications [23]-[29]. The second type is called Q-enhanced type. This category of BPFs use negative resistance compensation on the passive resonators based on spiral inductors or transmission lines [30], [31],

[32]. The major drawback is that the adopted passive resonators consume large chip area. In addition, the wideband implementations are limitedly presented. The third type active BPFs involve the use of active inductors (AIs) [33], [34] . However, implementations of the AI-based BPFs with bandwidth that can be classified as UWB are limited.

Consequently, one of the aims of this thesis is the development of highly selective active bandpass filters with fractional bandwidth larger than 66%.

1.3.2 Ultra Wideband True Time Delay Chain with High Delay/Size Efficiency for Compact Phased Array System

As mentioned before, the true-time-delay (TTD) based phased array is more suitable for broadband applications. The straightforward way to generate TTDs is by using transmission lines (TLs) [35], [36]. However, the dimensions of such implementations are mainly determined by the corresponding substrates because the equivalent phase velocity is related to the substrate dielectric constant ε_r by $V_{ph} = \frac{c}{\sqrt{\varepsilon_r}}$. More compact solutions are proposed with artificial transmission lines realized with on-chip discrete inductors and capacitors [37]. The design constraints lie in the limited quality of CMOS inductors. Due to the intrinsic low-pass structure of the artificial transmission line, the generated delay is generally limited by its cutoff frequency [38]. Additionally the usable bandwidth in terms of input/output return loss is also affected.

The second order all pass network (APN) provides a higher order group delay

response and superior input/output matching performance. Switched and self-switched second order APN based TTDs are demonstrated in MMIC processes [39], [40]. However its application in CMOS technology is not sufficiently investigated.

As a result, this thesis also aims to develop TTDs in CMOS using second order APNs to achieve large delays, high resolution and compact size simultaneously.

1.4 Contributions

This thesis investigates the implementations of the key components for ultra-wideband phased array transceiver in CMOS process.

The first component considered here is the ultra-wideband active BPF. Two design techniques are proposed based on the gyrator topology. Both of them achieve a shape factor larger than 0.75 and a FBW of 66%. The insertion losses for the two implementations are within 1 dB. Their compact sizes are well suitable for compact ultra-wideband phased array transceiver integration.

The other component considered here is the ultra-broadband TTD. Different implementations based on second order APNs are presented. The maximum time delay achieved is as large as 370 ps and the bandwidth is extended towards 22 GHz. They enable the design of phased array system with ultra-wide bandwidth and broader sweeping angle.

Publications:

[1] F. Hu, K. Mouthaan, “Lossless CMOS active reciprocal two-port

inductor and application in a series LC filter," *Microwave Conference (EuMC), 2012 42nd European* , pp. 364-367, 2012.

[2] F. Hu, K. Mouthaan, "A high-selectivity active bandpass filter using gyrator based resonators in 0.13-μm CMOS," *Wireless Symposium (IWS), 2014 IEEE International*, pp. 1-4, 2014.

[3] F. Hu, K. Mouthaan, "L-band bandpass filter with high out-of-band rejection based on CMOS active series and shunt inductors," *Microwave Symposium (IMS), 2014 IEEE MTT-S International,* pp.1-3, 2014.

[4] F. Hu, K. Mouthaan, "3-bit all-pass-network based 1-20 GHz switched true-time-delay phase shifter with 3-dB inter-state IL variation", Electronic Letters, is preparing.

[5] F. Hu, K. Mouthaan, "3-bit 2-22 GHz true-time-delay phase shifter using all-pass-network in trombone topology", Microwave and Wireless Component Letters, is preparing.

Chapter 2 High Order Octave Bandwidth Bandpass Filter Using Active Inductors in CMOS

2.1 Introduction

There are two main parameters of bandpass filters in terms of S-parameters. One parameter is the bandwidth. The bandwidth determines which frequency components in a signal can pass the filter. In the early days, the bandwidth of a bandpass filter usually was narrow. This is because the single-frequency carrier scheme dominated the wireless communication in the past decades [41]. In this scheme, a narrow baseband signal is used to modulate the single-frequency carrier. The resulting transmission signal is thus narrow bandwidth with several tens of Megahertz. The carrier frequencies for up-link (transmitting) and down-link (receiving) can be different, so separate BPFs are utilized in the system for receiving and transmitting modes respectively. However, more and more wireless systems nowadays are using wideband signals. A typical example is the Ultra-Wideband (UWB) system in which the operating frequency spans over a fractional bandwidth larger than 25% or more than 1.5 GHz. Thus the additional design challenge in this scenario is the wide bandwidth.

The other main parameter for bandpass filters is the shape factor. The shape factor, together with the out-of-band rejection, reflects the selectivity of the

BPFs. They determine how well the bandpass filter can filter out the unwanted signals for the system. Throughout this dissertation, the shape factor of the bandpass filter is defined as the ratio between its 3 dB bandwidth and 20 dB bandwidth (BW_{3dB}/BW_{20dB}). A larger shape factor reflects a higher suppression of the out of band signal close to the edge of the pass band. And a higher out-of-band rejection reflects a higher suppression of the out of band signal far to the edge of the pass band. A better selectivity of the BPFs may in turn loosen the design restraints of the following blocks, like the mixer.

Conventional passive bandpass filters realized in CMOS technology can hardly achieve appealing S-parameter response. The major issue is the loss of the on-chip passive resonators. The loss factors are mainly due to the limited metal trace thickness and the lossy semiconductor substrate. The most commonly adopted solution is to introduce negative resistance to compensate the loss in the passive resonators, which is called Q-enhanced technique. The passive resonators to be compensated can be lumped LC networks or transmission line based resonators [31], [42]. However, ultra-wide bandwidth applications are not sufficiently presented. In addition, because of the passive resonators, a better frequency selectivity (larger shape factor) requires a higher order design, which corresponds to a larger chip area. Another popular solution is to realize a pure active bandpass filter based on active inductors. In this category, the majority of reported works utilize the top-C coupled bandpass topology and they mostly adopt active shunt inductors [43]-[45].

Although they have a relatively good quality factor (ratio between center frequency and 3 dB bandwidth), the actual shape factor is not very appealing. Furthermore, the top-C coupled prototype is not applicable for the design of bandpass filter with wide bandwidth.

Thus, the goal of this chapter is to implement bandpass filter with:

- A good shape factor larger than 0.7;
- Wide bandwidth (60% fractional bandwidth as demonstration);
- Compact sizes, i.e. realization without on-chip inductors or TL based resonators.

The straightforward way to achieve these goals is to replace the passive inductors in a LC prototype with active inductors. However, as has been pointed out, only active shunt inductors are well investigated and their applications in narrow bandwidth bandpass filters have been reported extensively. The design of the active inductor based bandpass filter with wider bandwidth requires active series inductors. Thus the focus of this chapter will be on the development of active series inductors. The challenges for the implementation of wide bandwidth bandpass filters can then be reduced.

2.2 Active Inductor: Theory and Review

Active inductors have found their application in various CMOS high speed analog circuits. They range from amplifiers [46], oscillators [47] to phase shifters [48] and filters [49]. Compared to their counterparts, the CMOS on-chip passive inductors, active inductors draw more attention from circuit designers because of their achievable large inductance, small chip size, high quality factor, and inductance tunability [50], [51]. According to the connection styles in the real circuit design, the inductors can be categorized into shunt inductors and series inductors. A shunt inductor is a one-port device. As shown in Figure 2.1, a shunt inductor can be realized in either single ended form or floating form. The inductance appears only at the input port.

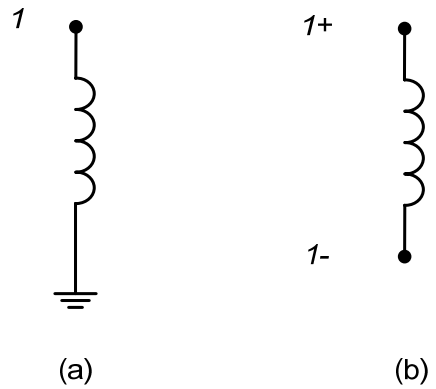

Figure 2.1. Shunt inductor (a) single ended form (b) floating form.

A series inductor, on the other hand, is a two-port device. As shown in Figure 2.2, a series inductor can be realized in either single ended form or floating form. The inductance appears at both ports of the inductor.

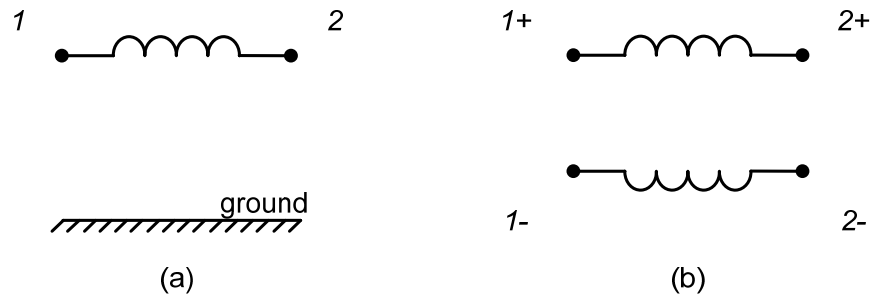

Figure 2.2. Series inductor (a) single ended form (b) floating form.

Both categories of inductors are needed in practical circuit design. For example, two bandwidth extension techniques can be used in wideband amplifier design. The first one is the shunt-peaking topology where a shunt inductor is used in parallel with the output capacitor to shorten the charging time of the output capacitor. The other approach is the series-peaking topology, in which a series inductor is used to split the output capacitor and the load. The idea behind them is the same: to direct more current through the output capacitor to shorten the charging time. In order to achieve a better bandwidth extension, these two techniques are usually combined and applied simultaneously [52].

The above discussion illustrates the necessity to develop both active shunt inductors and active series inductors. The following two sub sections will focus on the theory and review these two types of active inductors.

2.2.1 Active Shunt Inductors

The most common way to realize an active shunt inductor is to use the gyrator-C topology. An ideal gyrator is defined as a linear two port network

which couples the electrical signal on one port to the electrical signal on the other port and the other way back with a 180^o phase shift [53]. The electrical signal can be voltage or current. A practical gyrator couples the voltage on one port to the current on the other and vice versa with a 180^o phase shift. Thus the Y parameter of a lossless gyrator can be written as:

$$Y = \begin{bmatrix} 0 & G_1 \\ G_2 & 0 \end{bmatrix} \tag{2.1}$$

Where $G_1G_2<0$.

The ideal gyrator-C active shunt inductor is shown in Figure 2.3. Where the coupling between two ports is implemented with ideal transconductors G_{m1} and G_{m2}. A load capacitor C_L is added.

The analysis will be on the single ended version, as the differential case will not differ. The node voltages and path currents of the circuit shown in Figure 2.3(a) can be expressed as:

$$I_{o1} = G_{m1}V_1 \tag{2.2}$$

$$I_{o2} = G_{m2}V_2 \tag{2.3}$$

$$V_2 = -I_{o1}\frac{1}{j\omega C_L} \tag{2.4}$$

$$V_{in} = V_1 \tag{2.5}$$

$$I_{in} = I_{o2} \tag{2.6}$$

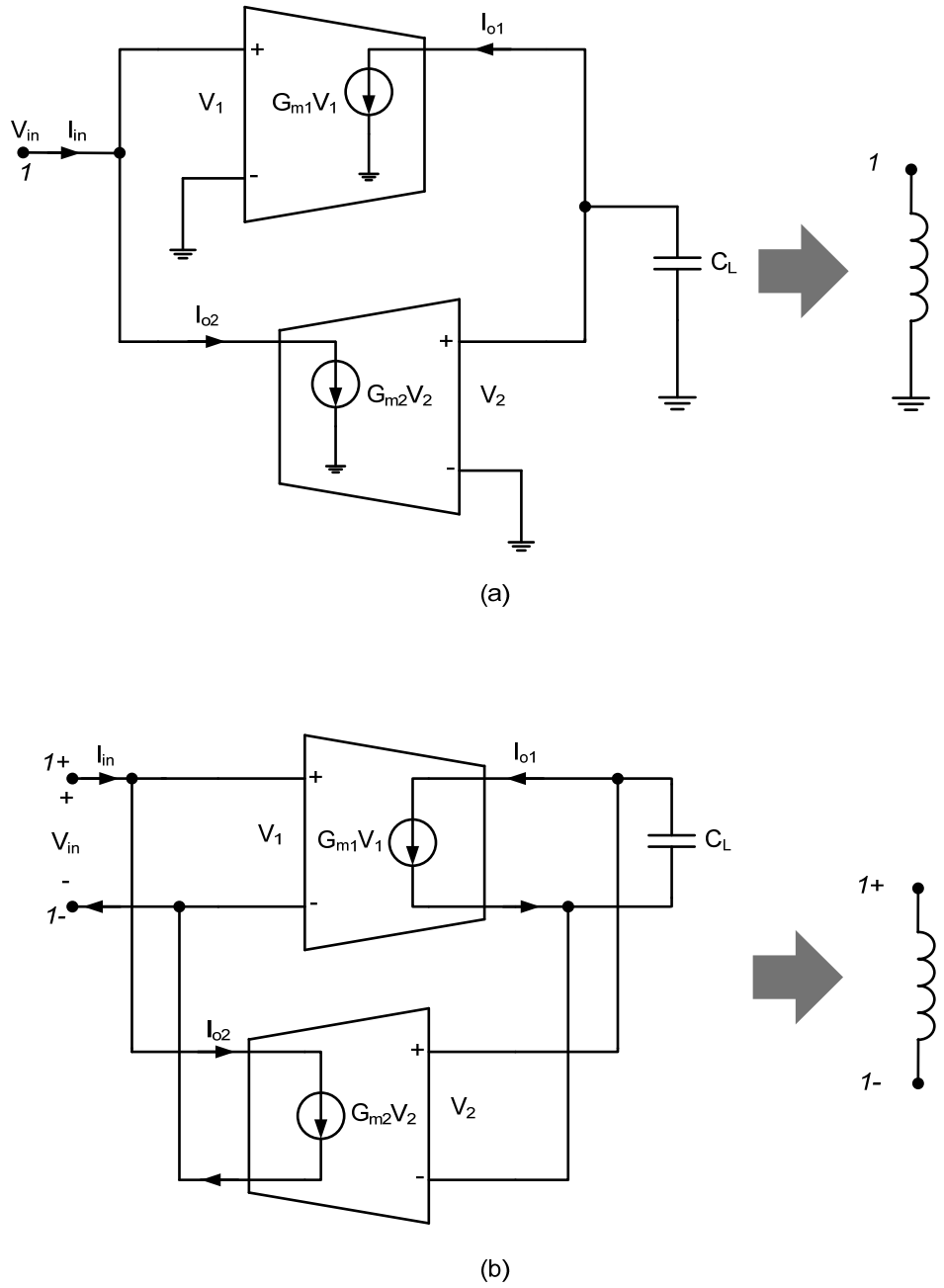

Figure 2.3. Ideal lossless gyrator-C active shunt inductor (a) single ended (b) floating.

With simple manipulations we arrive at:

$$I_{in} = -G_{m1}G_{m2}\frac{1}{j\omega C_L}V_{in} \tag{2.7}$$

and the final input impedance is

$$Z_{in} = -j\omega \frac{C_L}{G_{m1}G_{m2}} \tag{2.8}$$

Obviously, the input impedance will be an inductance if $G_{m1}G_{m2}<0$. And the equivalent inductance is:

$$L_{eq} = \frac{C_L}{|G_{m1}G_{m2}|} \tag{2.9}$$

The same result can be obtained for the differential topology. Equation (2.9) indicates that a single gyrator together with a load capacitor can be used to synthesize a shunt inductor. The resulting active inductance is proportional to the load capacitance C_L and inverse proportional to the product of the two transconductances. However, it should be noted that the two transconductances are required to have opposite signs.

We have ignored the parasitics of the transconductors used in the ideal gyrator discussed above. The typical parasitic components of a real transconductor, however, can be simplified as its input capacitance and output conductance. The non-ideal gyrator-C active shunt inductor is then shown in Figure 2.4 together with its modified equivalent R (resistance)-L (inductance)-C (capacitance) (RLC) model. Again, the differential case can be easily derived. The node equivalent parallel capacitance and conductance associated with the input capacitance and output conductance of each transconductor are simplified as C_{p1}, G_{p1} for port 1 and C_{p2}, G_{p2} for the load side.

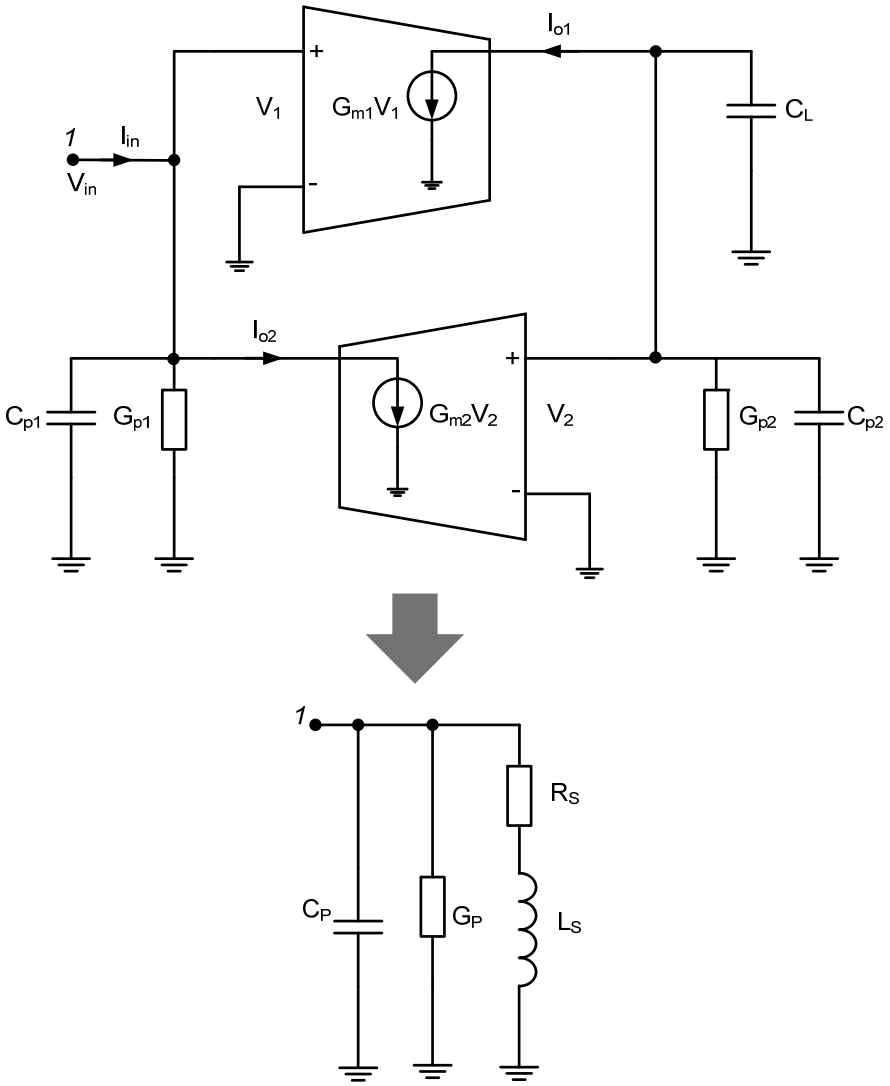

Figure 2.4. Non-ideal gyrator-C active shunt inductor with parasitics.

The node equations are then modified as:

$$I_{in} = I_{o2} + V_{in}(j\omega C_L + G_{P1}) \tag{2.10}$$

$$-I_{o1} = V_2(j\omega C_L + j\omega C_{P2} + G_{P2}) \tag{2.11}$$

At the input port we have:

$$I_{in} = V_{in}(j\omega C_{P1} + G_{P1} - \frac{G_{m1}G_{m2}}{j\omega(\mathrm{C}_L + \mathrm{C}_{P2}) + \mathrm{G}_{P2}}) \tag{2.12}$$

The input behavior will be clearer when shown in admittance form, which is:

$$Y_{in} = j\omega C_{P1} + G_{P1} - \frac{G_{m1}G_{m2}}{j\omega(\mathrm{C}_L + \mathrm{C}_{P2}) + \mathrm{G}_{P2}} \tag{2.13}$$

An inductance is obtained when $G_{m1}G_{m2}<0$, and the components values in the equivalent RLC model can be extracted as:

$$C_P = C_{P1} \tag{2.14}$$

$$G_P = G_{P1} \tag{2.15}$$

$$L_S = \frac{\mathrm{C}_L + \mathrm{C}_{P2}}{|G_{m1}G_{m2}|} \tag{2.16}$$

$$R_S = \frac{\mathrm{G}_{P2}}{|G_{m1}G_{m2}|} \tag{2.17}$$

It can be seen from the analysis that a non-ideal gyrator results in a lossy active inductor whose lossy components are mainly identified as a parallel conductance G_P and a series resistance R_S. They are solely due to the output conductance of each transconductor that constitutes the gyrator. The self-resonant frequency of the resulting active shunt inductor is:

$$\omega_o = \sqrt{\frac{|G_{m1}G_{m2}|}{(\mathrm{C}_L + \mathrm{C}_{P2})\mathrm{C}_{P1}}} \tag{2.18}$$

When the load capacitor C_L is neglected, the maximum self-resonant frequency is obtained as:

$$\omega_o = \sqrt{\frac{|G_{m1}G_{m2}|}{\mathrm{C}_{P1}\mathrm{C}_{P2}}} = \sqrt{\omega_{t1}\omega_{t2}} \tag{2.19}$$

where $\omega_{t1,2}$ are the cut-off frequencies of the two transconductors. This indicates that a higher self-resonant frequency of the resulting active shunt inductor requires a higher cut-off frequency of the transconductors used.

The active shunt inductor has been extensively investigated in the past

decades in the literature. Some of them are reviewed in the following.

Wu current reuse active inductor

The Wu current reuse active inductor uses single stage transconductors to realize the gyrator [33], [54]. The positive transconductance is provided by a common gate stage while the negative transconductance is generated with a common source stage. The simplified schematics in nMOS and pMOS versions are shown in Figure 2.5.

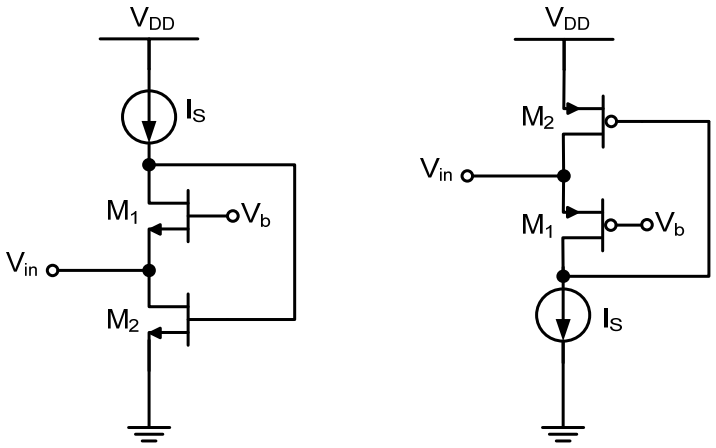

Figure 2.5. Simplified schematic of Wu current reuse active inductor.

When only the gate-source capacitance C_{gs} and output conductance g_{ds} of each transistor are considered, it is clear that here we have $G_{m1}=-g_{m1}$, $G_{m2}=g_{m2}$, $C_{P1}=C_{gs1}$, $G_{P1}=(g_{m1}+g_{ds2})$, $C_{P2}=C_{gs2}$ and $G_{P2}=g_{ds1}$ when referring back to Figure 2.4. And thus the equivalent RLC network can be obtained as:

$$C_P = C_{gs1} \tag{2.20}$$

$$G_P = g_{m1} + g_{ds2} \approx g_{m1} \tag{2.21}$$

$$L_S = \frac{C_{P2}}{g_{m1}g_{m2}} \tag{2.22}$$

$$R_S = \frac{g_{ds1}}{g_{m1}g_{m2}} \tag{2.23}$$

Equation (2.21) holds when $g_{m1} >> g_{ds2}$, which is always the case in real circuits. The most important drawback of the Wu current reuse active inductor is the large conductance $G_P = g_{m1}$, which is in parallel with the equivalent active inductor. The resulting quality factor is thus very low at the low frequency end.

Lin-Payne Active Inductor

The positive transconductor is realized with a source follower stage in the Lin-Payne active inductor [55], [56].

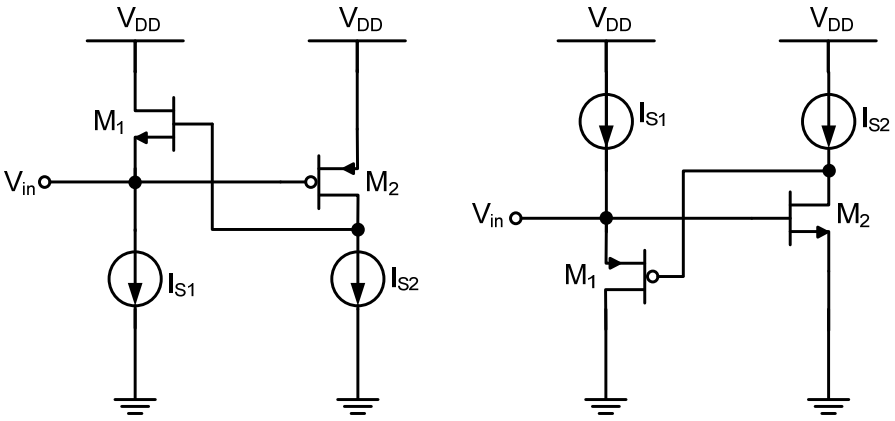

Figure 2.6. Simplified schematic of Lin-Payne active inductor.

The simplified schematic of the Lin-Payne active inductor is shown in Figure 2.6. The analysis results are similar to those of the Wu current reuse active inductor. The output conductance of the source follower stage transconductor

is g_{m1} which will become the conductance in parallel with the equivalent active inductor. The quality factor of this kind of active inductor suffers from this issue as well.

Karsilayan-Schaumann Active Inductor

The positive transconductor in the gyrator can be realized with a differential pair, as in the Karsilayan-Schaumann active inductor [57]. Applications of such type active inductors are found in [58]. The simplified schematic is shown in Figure 2.7.

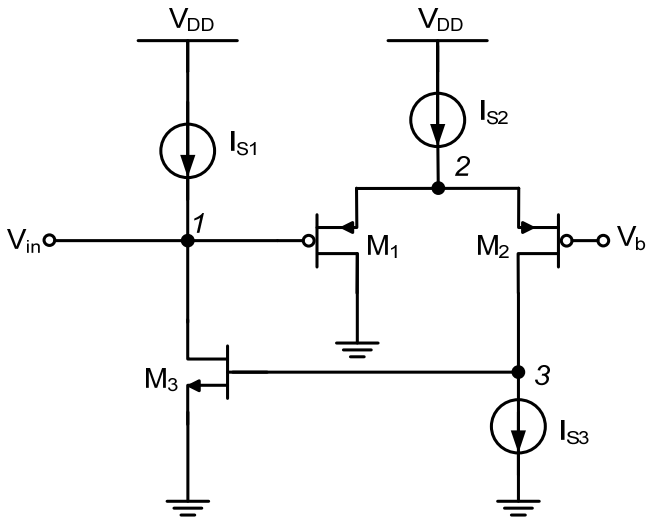

Figure 2.7. Simplified schematic of Karsilayan-Schaumann active inductor.

The differential pair M_1-M_2 provides the positive transconductance. Let C_1 denote the capacitance between node 1 and node 2, C_2 denotes the total shunt capacitance at node 2 and C_3 represents the total shunt capacitance at node 3. When only considering the output conductance of transistors M_1 and M_2, the input admittance can be approximated by:

$$Y_{in} \approx \frac{1}{j\omega(\frac{2C_3}{g_m g_{m3}}) + \frac{G(\omega)}{g_m g_{m3}}} \tag{2.24}$$

where

$$G(\omega) = g_{ds2} + 2g_{ds4} - \omega^3 C_3(\frac{C_1 + C_2}{g_m}) \tag{2.25}$$

Then the equivalent active inductance L_S and series resistance R_S can be expressed as:

$$L_S = \frac{2C_3}{g_m g_{m3}} \tag{2.26}$$

$$R_S = \frac{G(\omega)}{g_m g_{m3}} \tag{2.27}$$

Clearly, the maximum quality factor appears when R_S=0. And this corresponds to

$$C_1 + C_2 = \frac{(g_{ds2} + 2g_{ds4})g_m}{\omega^3 C_3} \tag{2.28}$$

It can be seen that this condition can only be satisfied within a very narrow bandwidth. The resulting active inductor is not suitable for wideband circuit design consequently.

Hsiao Resistance Feedback Active Inductor

Many approaches have been investigated to improve the quality factor of active inductors. One of them is the so-called resistance feedback technique. A typical example is the Hsiao resistance feedback active inductor [59]. The simplified schematic is shown in Figure 2.8. The cascade structure is adopted

to reduce the output conductance of the transconductor stage.

Assuming ideal biasing transistors i.e. with infinite output impedance, the equivalent RLC network can be determined.

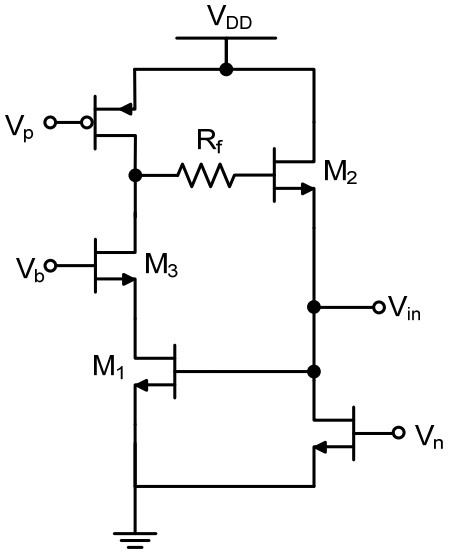

Figure 2.8. Simplified schematic of Hsiao resistance feedback active inductor.

$$C_P = C_{gs3} \tag{2.29}$$

$$G_P = \frac{2g_{ds2} + R_f g_{ds2}^2}{R_f g_{ds2} + 1} \tag{2.30}$$

$$L_S = \frac{g_{m1}g_{m2}C_{gs1} + \omega^2 C_{gs1}^2 C_{gs2}(\mathrm{R}_f \mathrm{g}_{ds2} + 1)}{\mathrm{g}_{m1}^2 \mathrm{g}_{m2}\mathrm{g}_{m3} + \omega^3 g_{m2}g_{m3}C_{gs1}^2} \tag{2.31}$$

$$R_S = \frac{g_{m1}g_{ds2}g_{ds3} + \omega^2[g_{m2}C_{gs1}^2 - g_{m1}C_{gs1}C_{gs2}(\mathrm{R}_f \mathrm{g}_{ds2} + 1)]}{\mathrm{g}_{m1}^2 \mathrm{g}_{m2}\mathrm{g}_{m3} + \omega^3 g_{m2}g_{m3}C_{gs1}^2} \tag{2.32}$$

It can be seen that the feedback resistor R_f helps to lower the R_S value and thus to improve the quality factor. However, the complex frequency dependency makes it difficult for wideband circuit design.

There are more active shunt inductors presented in the literature like [60], [61].

However, the design principles are more or less similar to each other and they are not discussed in this thesis.

2.2.2 Active Series Inductors

Compared to the active shunt inductors, much fewer publications are available on active series inductors. An approach to synthesize active series inductors is presented in [62] and the synthesizing model is shown in Figure 2.9.

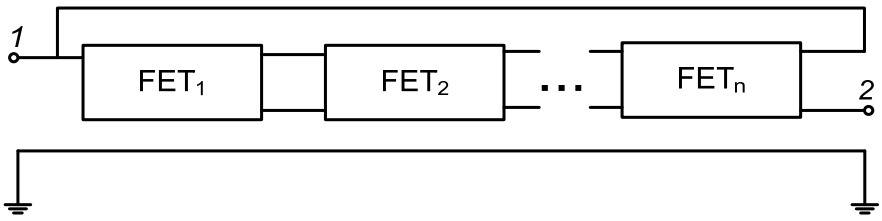

Figure 2.9. Simplified synthesizing model of the active series inductor presented in [62].

For each transistor cell FET_n, any single stage transistor topology can be used, such as common source and common gate configurations. The final topologies that can successfully generate an inductance at the testing ports are then screened out and reported. To demonstrate the principle, one of those combinations is selected and discussed here. The simplified circuit diagram is shown in Figure 2.10. The equivalent RLC model is also included. When only considering the transconductance g_m and gate-source capacitance C_{gs} of each transistor, the component values in the RTL model can be readily obtained as:

$$C_P = C_{gs1} \tag{2.33}$$

$$R_P = \frac{1}{g_{m1}} \tag{2.34}$$

$$L_S = \frac{C_{gs2}}{g_{m1}g_{m2}} \tag{2.35}$$

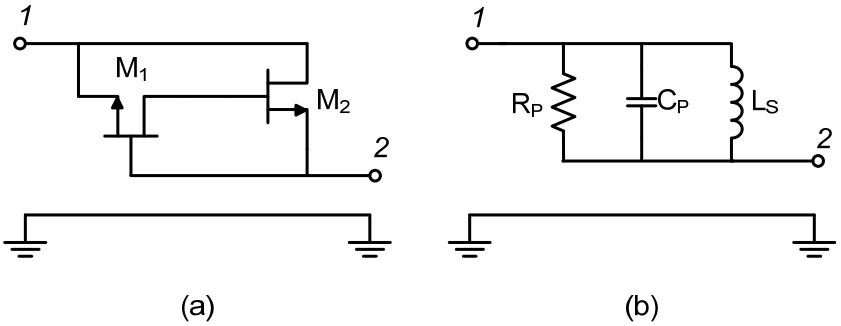

Figure 2.10. Simplified circuit diagram of active series inductor presented in [62]: (a) transistor level model (b) equivalent RLC model.

The self-resonant frequency of the active series inductor is then

$$\omega_o = \sqrt{\frac{g_{m1}g_{m2}}{C_{gs1}C_{gs2}}} \tag{2.36}$$

The quality factor is determined by the parallel resistor R_P.

There are two major issues related to this design method. The first one is that the bias circuitry is neglected in the analysis. It requires ideal biasing components like current sources to achieve the "floating" property. Such extra components added for biasing purposes can drastically deteriorate the quality of the active series inductor. The second issue is that this technique is not suitable for CMOS realization. The channel length modulation effect is more and more evident along with the shrinking of CMOS process. The output conductance of the transistors should then be included in the analysis and the final results will worsen.

Similar topologies are also presented in [63], [64] and [65]. The topology presented in [63] is slightly different because the feedback path, compared to

other works is indirect,. The implementation is also quoted here and shown in Figure 2.11. A common gate transistor M_3 is used in the feedback path to increase the inductance value and to decrease the loss.

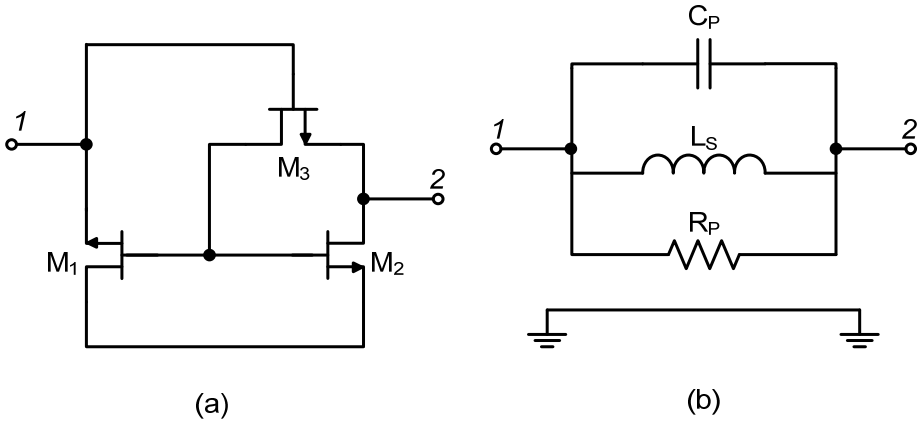

Figure 2.11. Simplified circuitry of active series inductor presented in [63]: (a) transistor level model (b) equivalent RLC model.

When only involve the transconductance and gate-source capacitance of the transistors, a simplified expression of the equivalent RLC model can be derived. Assuming transistors M_1 and M_2 to have the same dimensions and bias conditions, the RLC model is given by:

$$C_P = C_{gs3} \tag{2.37}$$

$$R_P = \frac{1}{g_{m3}(1-\frac{1}{4+(\omega/\omega_t)^2})} \tag{2.38}$$

$$L_S = \frac{C_{gs1,2}}{g_{m1,2}g_{m3}}(2+\frac{1}{2}(\frac{\omega}{\omega_t})^2) \tag{2.39}$$

Where ω_t is the cut-off frequency of the transistors M_1 and M_2. The most important issue of this active series inductor is that two of the three components (R_P and L_S) in the RLC model are frequency dependent. This

makes the active series inductor not suitable for wideband applications.

The gyrator-C topology can also be used to produce active series inductors. This approach is easier to synthesize and the non-ideal effects, like finite transistor output impedance, parasitic capacitance, as well as the effects of biasing circuitry, can be well identified and characterized [66].

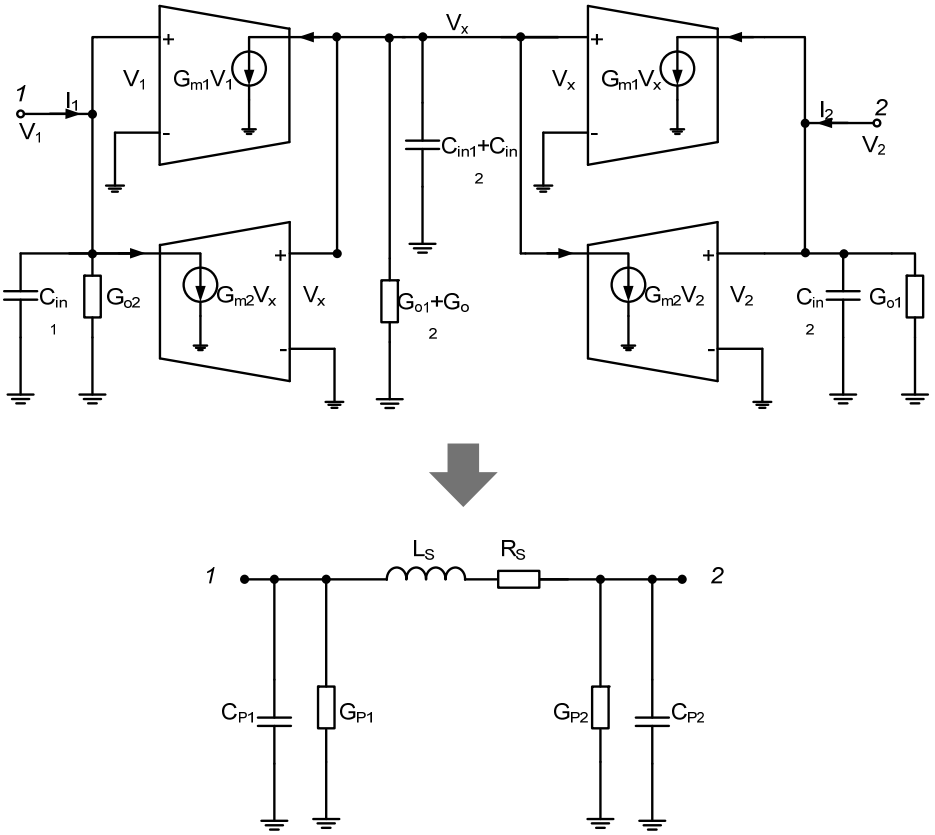

Figure 2.12. Gyrator-C based active series inductor with equivalent lumped model.

The gyrator-C based active series inductor is shown in Figure 2.12. Its equivalent lumped model is also included. The active series inductor consists of two identical gyrators cascaded in series. The parasitics of the two transconductors, G_{m1} and G_{m2}, are simplified as input capacitance C_{in1}, C_{in2} and

output conductance G_{o1}, G_{o2} respectively. The node equations are:

$$I_1 = G_{m2}V_x + V_1(G_{o2} + j\omega C_{in1}) \tag{2.40}$$

$$I_2 = G_{m1}V_x + V_2(G_{o1} + j\omega C_{in2}) \tag{2.41}$$

$$0 = G_{m1}V_1 + G_{m2}V_2 + V_x[j\omega(C_{in1} + C_{in2}) + G_{o1} + G_{o2}] \tag{2.42}$$

We further assume that the two transconductors have the same input/output characteristics and their transconductances have the same magnitude. Which means $\pm G_{m1} = \square G_{m2} = G_m$, $C_{in1} = C_{in2} = C_{in}$, and $G_{o1} = G_{o2} = G_{out}$. The Y parameters of the gyrator-C topology can then be written as

$$Y = \begin{bmatrix} G_{out} + j\omega C_{in} + \dfrac{G_m^2}{2(G_{out} + j\omega C_{in})} & \dfrac{-G_m^2}{2(G_{out} + j\omega C_{in})} \\ \dfrac{-G_m^2}{2(G_{out} + j\omega C_{in})} & G_{out} + j\omega C_{in} + \dfrac{G_m^2}{2(G_{out} + j\omega C_{in})} \end{bmatrix} \tag{2.43}$$

The elements Y_{21} and Y_{12} in equation (2.43) indicate that an inductive component has been generated between Port 1 and Port 2. It is also noted that the gyrator-C network is a reciprocal network with symmetry. However, this conclusion only holds if transconductor G_{m1} and transconductor G_{m2} have the same input/output characteristics (C_{in} and G_{out}).

In real circuit design, designers are more comfortable with an equivalent lumped model. The equivalent lumped model can be extracted based on the equation of (2.43), and the component values of the equivalent network are listed as:

$$R_s = \frac{2G_{out}}{G_m^2} \tag{2.44}$$

$$L_s = \frac{2C_{in}}{G_m^2} \tag{2.45}$$

$$C_p = C_{in} \tag{2.46}$$

$$G_p = G_{out} \tag{2.47}$$

Compared to the techniques presented in [62], gyrator-C based techniques have better control of the equivalent model component values. The loss of the resulting active series inductor is mainly controlled by the output conductance G_{out} of the constituted transconductors. One option to improve the quality factor of the gyrator based active series inductor is thus to minimize the output conductance of the transconductance cell.

2.3 Lossless Reciprocal Active Series Inductor in 0.13 μm CMOS

2.3.1 Operational Transconductance Amplifier (OTA)

The key component in the gyrator based active inductor topology is the transconductor cell. As has been illustrated, both positive and negative transconductors are required in the gyrator-C active inductor realization. The negative transconductor is less challenging because a single transistor itself can provide negative transconductance. As for the positive transconductor, the common gate and common source single stage topologies are not suitable. The main reason is that the low input or output impedance will worsen the quality factor of the resulting active inductor dramatically. Another option for the positive transconductor is to cascade an even number of stages of negative transconductors. However, the parasitics at the interface can limit the bandwidth of the positive transconductance and this option is thus not suitable for wideband design. Another transconductance generation can be found in [67]. The main problems remain as the transconductance tunability and output parasitics.

The transconductor cell is then realized with the operational transconductance amplifier (OTA) in differential configuration. The most important benefit of the differential configuration is that the input and output characteristics of the transconductor remains the same for positive and negative transconductances, namely $+G_m$ and $-G_m$.

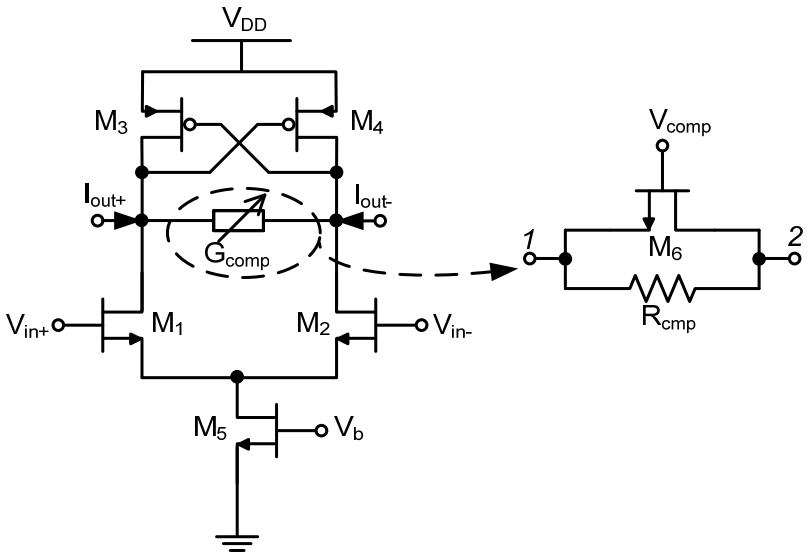

Figure 2.13. Operational transconductance amplifier.

The schematic of the differential OTA is depicted in Figure 2.13. The transistor pair M_1-M_2 provide the required transconductance. The output is loaded with cross-coupled transistor pair M_3-M_4 together with a tunable conductor G_{comp}, which is composed of a resistor and a triode-biased transistor M_6. The biasing current is provided and controlled by the tail transistor M_5. The analysis later will show that the transistors M_1, M_2, M_3 and M_4 are working in the saturation region with the gate-source voltage being equal to the drain-source voltage. In order to maintain the low supply voltage, the headroom of the tail transistor M_5 is limited to the minimum. On the other hand, the biasing current needs to be as large as possible to keep the sizes of the other transistors minimum. As a result, M_5 is biased in the triode region.

Small signal behavior

The small signal behavior of the OTA can be analyzed by substituting each

transistor with its small signal model. For simplicity, we only consider the gate-source capacitance C_{gs}, transconductance g_m and output conductance g_{ds} for each transistor. In order to refer back to the gyrator-C diagram shown in Figure 2.12, we extract the differential input capacitance C_{in}, equivalent transconductance $G_{m,}$ and output conductance G_{out}. The differential output capacitance C_{out} is also provided. They are:

$$C_{in} = \frac{C_{gsn}}{2} \tag{2.48}$$

$$G_m = \frac{g_{mn}}{2} \tag{2.49}$$

$$G_{out} = \frac{(g_{dsn} + g_{dsp} + G_{comp} - g_{mp})}{2} \tag{2.50}$$

$$C_{out} = \frac{C_{gsp}}{2} \tag{2.51}$$

Where C_{gsn}, g_{mn}, g_{dsn} are associated with the nMOS transistors M_1, M_2 and the C_{gsp}, g_{mp}, g_{dsp} are associated with the pMOS transistors M_3, M_4 respectively. The negative transconductance is readily generated by exchanging the output nodes.

Equation (2.50) indicates that the output conductance of the differential OTA can be tuned to be zero when

$$g_{dsn} + g_{dsp} + G_{comp} = g_{mp} \tag{2.52}$$

Under this condition, the gyrator-C active series inductor using the OTA is lossless and the quality factor is infinite.

Large signal behavior

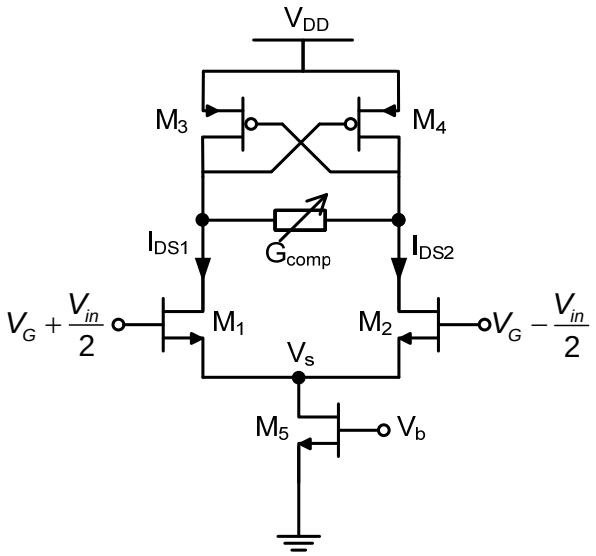

Figure 2.14. Circuit for large signal analysis of the OTA.

The large signal response of the OTA can be observed by injecting an input signal V_{in} at the input port. Thus the input AC voltage at the gate is $+\frac{V_{in}}{2}$ for M_1 and $-\frac{V_{in}}{2}$ for M_2. Ignoring the channel modulation in the saturation region, the currents flowing through the two branches are given by:

$$I_{DS1} = \frac{1}{2}\mu_n C_{ox}\frac{W_1}{L_1}(V_G + \frac{V_{in}}{2} - V_s - V_{th,n})^2 \tag{2.53}$$

$$I_{DS2} = \frac{1}{2}\mu_n C_{ox}\frac{W_2}{L_2}(V_G - \frac{V_{in}}{2} - V_s - V_{th,n})^2 \tag{2.54}$$

$$I_{DS1} + I_{DS2} = \mu_n C_{ox}\frac{W_5}{L_5}[(V_b - V_{th,n}) - \frac{1}{2}V_s^2] \tag{2.55}$$

Let $\frac{W_1}{L_1} = \frac{W_2}{L_2} = \beta$ and $\frac{W_5}{L_5} = \beta_5$. The output current is $I_{out} = I_{DS1} - I_{DS2}$ and is written as:

$$I_{out} = \frac{\mu_n C_{ox}}{2}\beta(V_G - V_s - V_{th,n})V_{in} \tag{2.56}$$

It can be seen that the major cause for the nonlinearity of the transconductance is $k = V_G - V_{th,n} - V_s$. A more detailed expression for *k* is

$$k = \sqrt{(\frac{\alpha}{1+\alpha}V_{od} + \frac{1}{1+\alpha}V_{od,5})^2 - \frac{1}{1+\alpha}(V_{od}^2 + \frac{1}{4}V_{in}^2)} + \frac{1}{1+\alpha}(V_{od} - V_{od,5}) \quad (2.57)$$

Where $V_{od} = V_G - V_{th,n}$, $V_{od,5} = V_b - V_{th,n}$ and $\alpha = \frac{2\beta}{\beta_5}$.

According to equation (2.56) and (2.57), the nonlinearity of the OTA is affected by two major factors. The first one is the bias conditions which are reflected in the equations by V_{od} and $V_{od,5}$. Because of the required biasing current, they are less controllable. The other factor is the sizing ratio between the transconductance transistors M_1-M_2 and the tail transistor M_5. The parameter α in the equations accounts for this effect.

The equivalent transconductance of the OTA is simulated using SpectreRF with different values of α ranging from 1 to 5. The transconductance is normalized to its small signal value in each case for comparison, and the result is shown in Figure 2.15.

The transconductance drops at lower input signal level with higher values of α. This is reasonable because a higher value of α means a smaller size of M_5. The size reduction of M_5 makes the node voltage V_s more sensitive to the current change. The DC component arising from the squared I-V property of M_1-M_2 when large input signal occurs can induce a considerable voltage change at V_s. This will affect the effective overdrive voltages of M_1-M_2 and

thus the overall transconductance is affected.

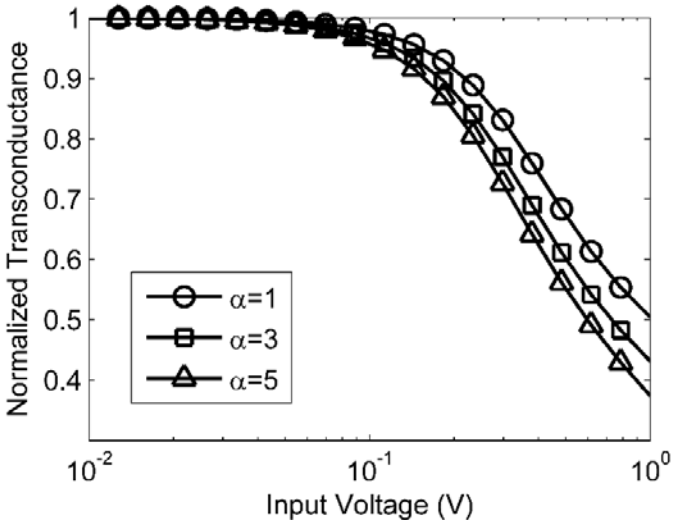

Figure 2.15. Normalized transconductance of the OTA for different values of α.

As a result, the parameter α should be as high as possible if other conditions permit.

2.3.2 Stability Issues of the OTA based Gyrator

Two of the preceding differential OTAs are connected in feedback configuration to form a gyrator cell as shown in Figure 2.16(a). The differential operation of the gyrator is achieved with the control of the output conductance of each OTA. They are kept as $G_{out} \cong 0$ to maintain the differential mode stability.

The common mode operation of the gyrator is illustrated in Figure 2.16(b). The transistor pair M_1-M_2 are merged as $M_{OTAn,1\text{-}2}$ and the transistor pair M_3-M_4 are merged as $M_{OTAn,3\text{-}4}$ in the simplified schematic. The tail transistor

is not affected. It is noted that the sizes of $M_{OTAn,1-2}$ and $M_{OTAn,3-4}$ are double the size of the original transistors. It can be seen that the transistors $M_{OTA1,1-2}$ and $M_{OTA2,1-2}$ build up a positive feedback loop. The feedback loop can cause the common mode voltages $V_{OTA1,cm}$ and $V_{OTA2,cm}$ to deviate from each other and finally the two OTAs are not correctly biased.

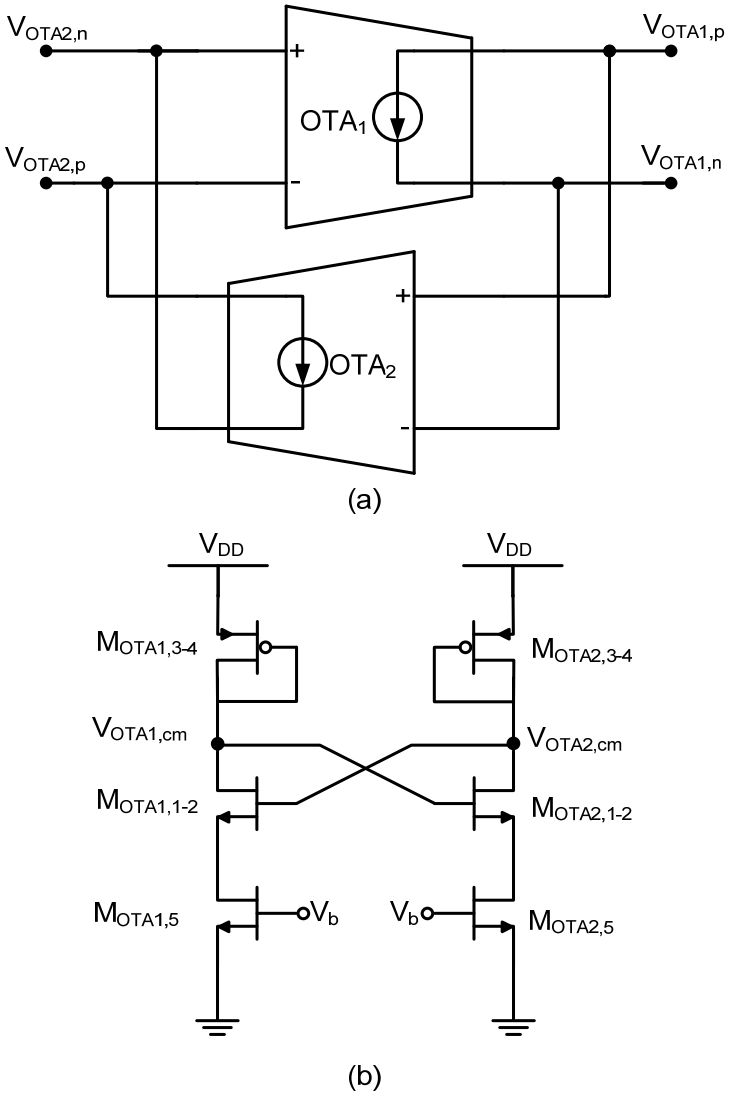

Figure 2.16. Gyrator realized with two OTAs: (a) differential mode operation, (b) common mode operation.

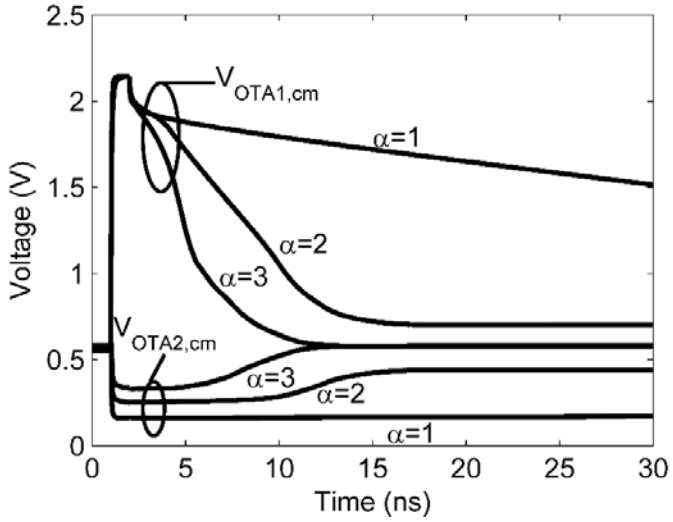

Figure 2.17. SpectreRF transient simulation of the gyrator in common mode operation.

The unstable DC can be alleviated by $M_{OTAn,5}$ which provides a negative feedback in the common mode operation. A transient simulation is performed to verify this effect. The parameter α is still used here as a parameter. The simulation results are shown in Figure 2.17. It is observed that a higher value of α provides a more stable biasing condition in the common mode. This is also understandable because a smaller size of the tail transistor generates a more sensitive drain-source voltage when the channel current fluctuates.

As a conclusion, the triode biasing of the M_5 is used because:

(1). Provide current control of the OTA. If extra current mirrors are used for such purpose, more complex parasitics will be introduced and the bandpass performance of the final BPF will be deteriorated.

(2). Provide common mode feedback to achieve common mode suppression. The alternative pseudo differential topology will not provide enough common mode suppression.

(3). Provide negative feedback in common mode to stabilize the OTA when constructing a gyrator.

(4). Save voltage drop to lower the total supply voltage. The supply voltage of the design is maintained as 1.2 V. Lower power consumption can thus be achieved.

2.3.3 Gyrator-C Active Series Inductor and Its Application in a Series LC Resonator

The performance of the proposed active series inductor is characterized by implementing it in a series LC resonator. The topology is shown in Figure 2.18. The differential realization of the series LC resonator is directly obtained with the proposed differential active series inductor.

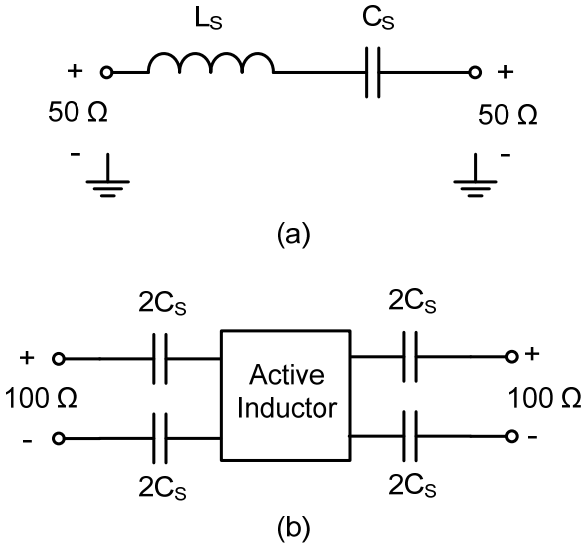

Figure 2.18. Series LC resonator: (a) single ended version (b) its differential realization with active inductor.

As shown in Figure 2.18, the series capacitor is split into the two sides of the

active inductor. The purpose is to distribute the parasitic effects of the capacitor into the two ports of the series LC resonator and better reciprocity is then obtained.

The capacitor C_s is chosen as 193.75 fF. The series LC resonator is fabricated in a standard 0.13 μm CMOS process. The micrograph of the fabricated circuit is shown in Figure 2.19.

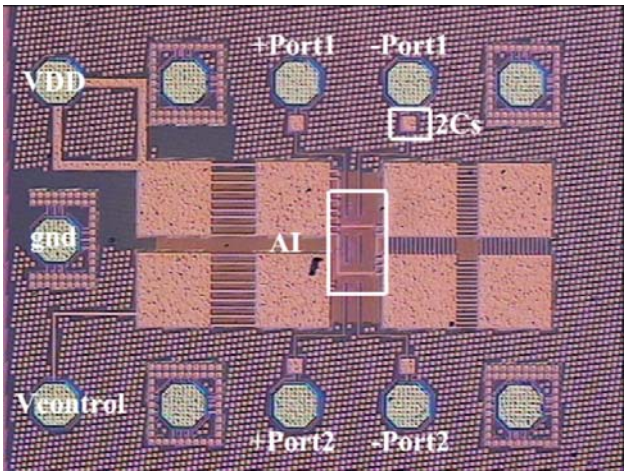

Figure 2.19. Micrograph of the fabricated series LC resonator.

The core of the active series inductor, indicated by the larger rectangle, is 150x50 μm^2. The whole active series LC resonator consumes 2.5 mA at a 1.2 V supply.

The fabricated differential active series LC resonator is measured with a four-port vector network analyzer. The full-port S-parameters are obtained to better characterize the performance of the active inductor. The ideal performance of a series LC resonator with the same component values is also included for a comparison.

The differential mode operation of the active series LC resonator is shown in

Figure 2.20 and Figure 2.21. The active series LC resonator shows a gain of 0.26 dB and an input return loss of 17 dB at the center frequency of 2.45 GHz. The active resonator itself shows a certain level of imbalance between the two ports. There are two major reasons. The first one is the layout of the active inductor. Any asymmetric interconnections and vias can lead to an imbalance between the two ports of the active series inductor. The second reason is the process variation. Which not only affects the active components, it may also make the series capacitors at the two ports of the resonator deviate from each other. However, the response of the proposed active series LC resonator is very close to the ideal LC realization. The discrepancies become obvious in the high frequency range. This is mostly due to the parasitic capacitance whose effect is more dominant at high frequencies.

The common mode operation of the active series LC resonator is shown in Figure 2.22 and Figure 2.23. In this case, the active series LC resonator performs different from the ideal LC resonator. It can be seen that the ideal LC resonator behaves the same in the common mode as in the differential mode. However, the proposed active series LC resonator provides a suppression of the common mode signal. The suppression is larger than 27 dB across the whole frequency range.

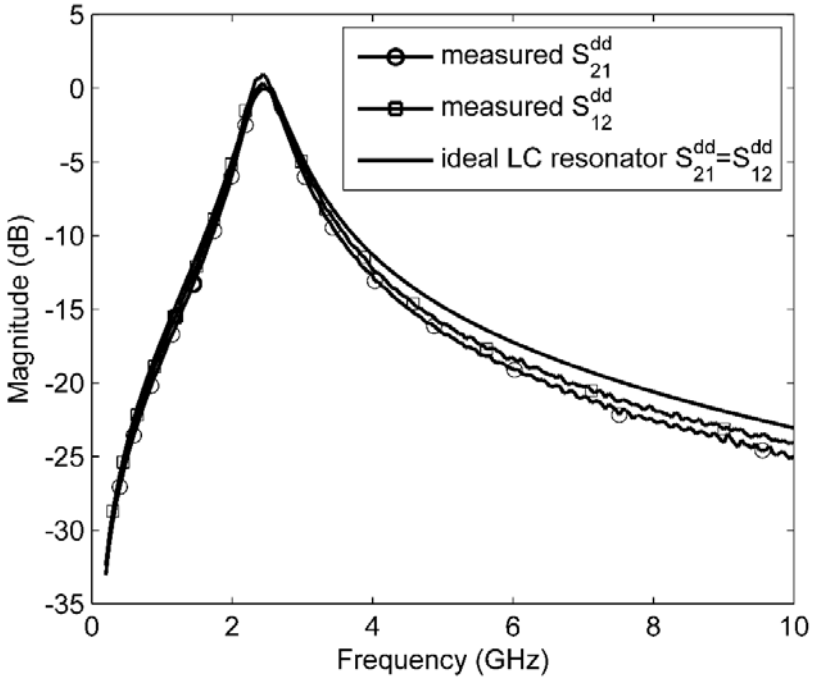

Figure 2.20. Differential mode S-parameters of the active inductor resonator and the ideal LC resonator: S_{21}^{dd} and S_{12}^{dd}.

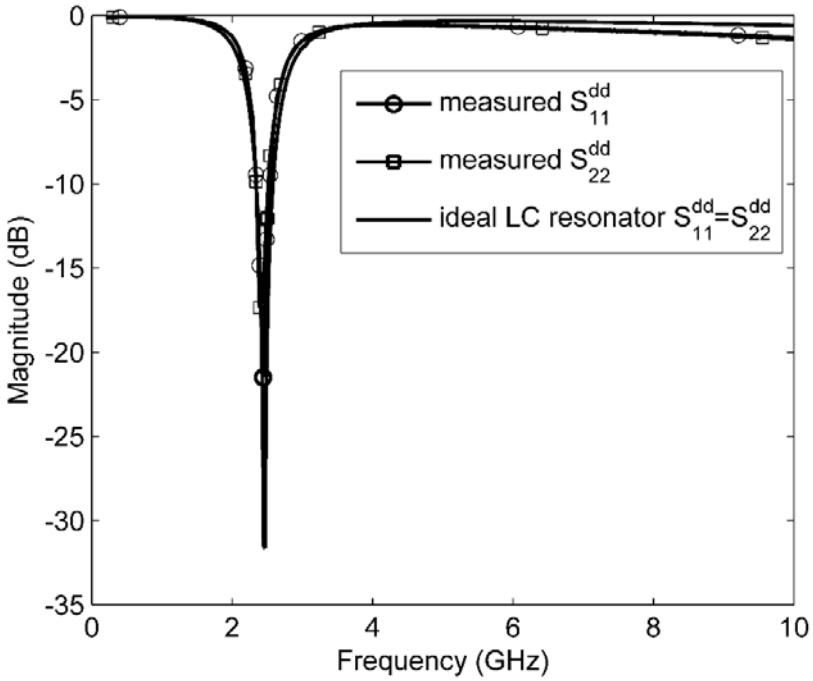

Figure 2.21. Differential mode S-parameters of the active inductor resonator and the ideal LC resonator: S_{11}^{dd} and S_{22}^{dd}.

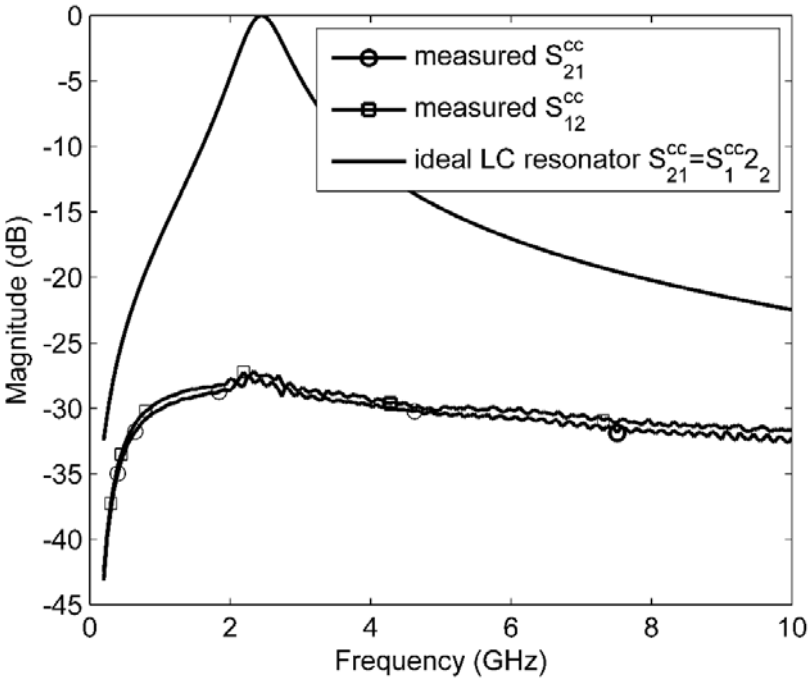

Figure 2.22. Common mode S-parameters of the active inductor resonator and the ideal LC resonator: S_{21}^{cc} and S_{12}^{cc}.

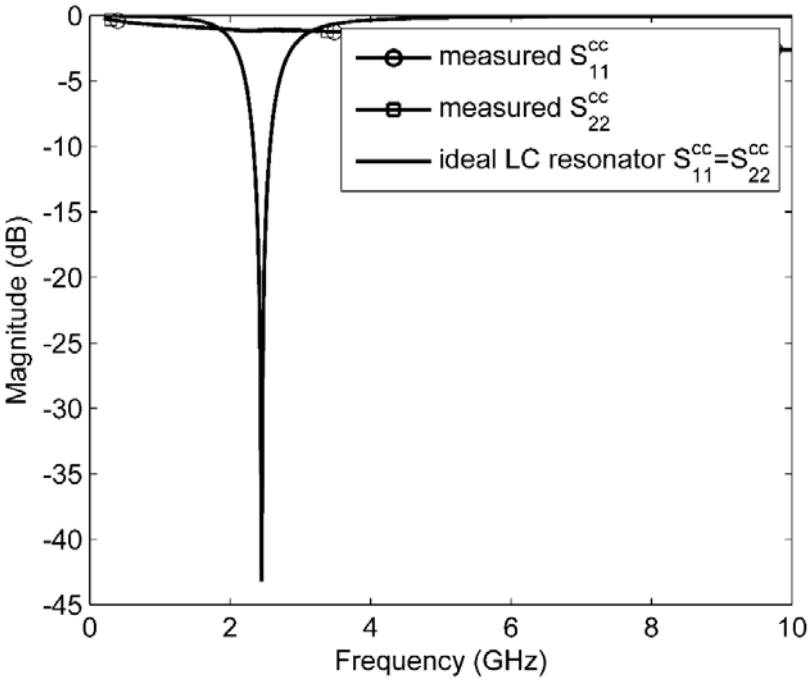

Figure 2.23. Common mode S-parameters of the active inductor resonator and the ideal LC resonator: S_{11}^{cc} and S_{22}^{cc}.

2.3.4 Verification of the Equivalent model of the Active Series Inductor

The proposed active series inductor is going to be used in other circuit designs. The equivalent model in Figure 2.12 can provide a useful guideline for this purpose. Based on the measurements of the active series LC resonator, this equivalent model is verified. The model of the whole series LC resonator is shown in Figure 2.24.

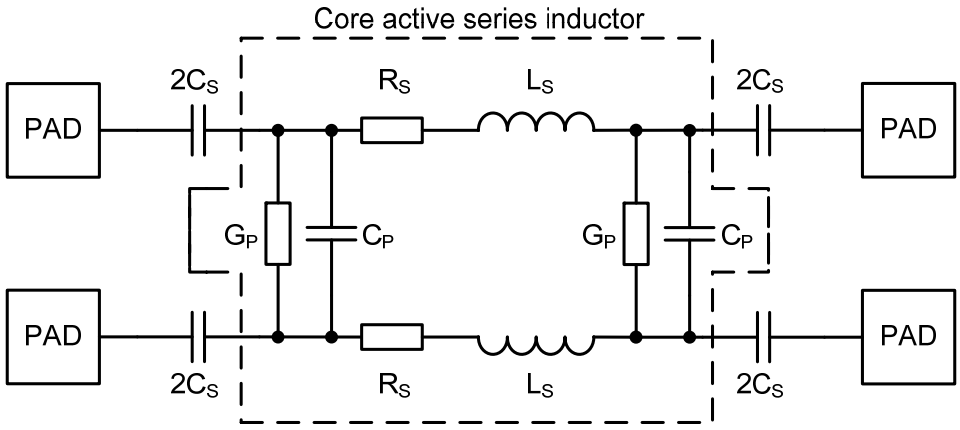

Figure 2.24. Equivalent model of the series LC resonator.

The core active series inductor model is simplified as a parallel GC network (G_P and C_P) and a series RL network (R_S and L_S). The pads and on-chip capacitors C_S are de-embedded with the S-parameters from the foundry model.

TABLE 2-1 EXTRACTED MODEL VALUES OF THE ACTIVE SERIES INDUCTOR.

Component	L_S	R_S	C_P	G_P
Value	22.24 nH	-5 Ω	20 fF	-3 μS

The extracted values are listed in Table 2-1. The S-parameters of the

equivalent model in Figure 2.24 are then compared with the measurement results.

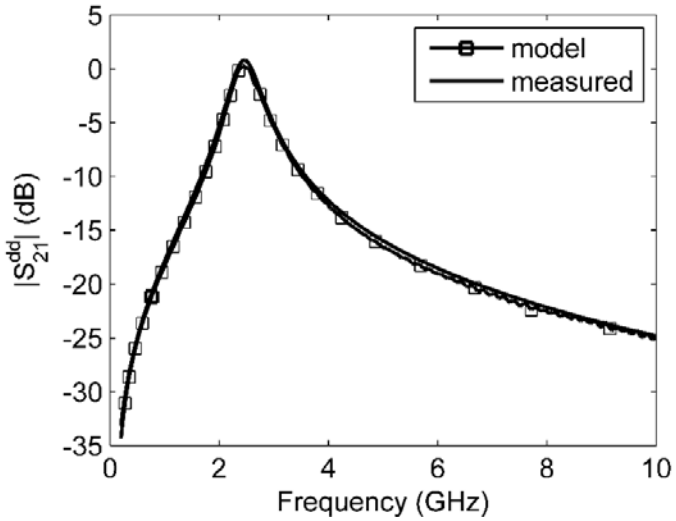

Figure 2.25. Measurement and model results: S_{21}^{dd}.

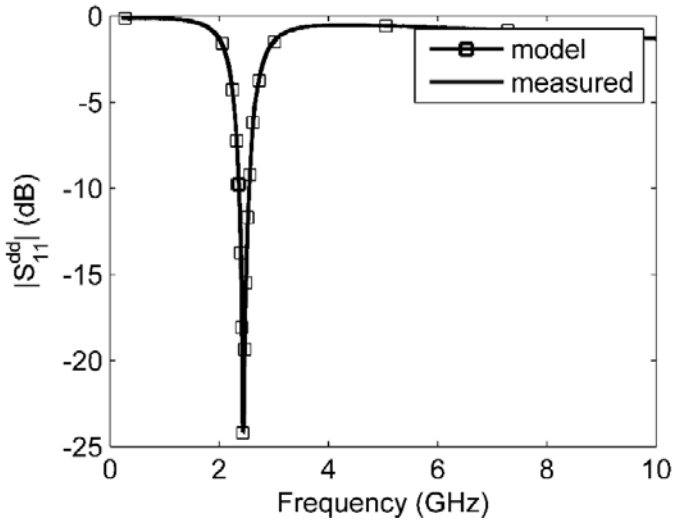

Figure 2.26. Measurement and model results: S_{11}^{dd}.

The measurement and the model results are shown in Figure 2.25 and Figure 2.26. As can be seen, the equivalent model of the active series inductor can serve as a useful guideline for its application in real circuit design. The effects of other parasitics can be considered as minor and may be neglected.

2.4 L-band High Selectivity Wideband Bandpass Filter Using Active Series and Shunt Inductors in CMOS

2.4.1 Review and Motivation

In order to realize high selectivity RF bandpass filters in a CMOS process, many solutions have been proposed and presented in the literature.

One of them is the negative resistance compensation technique or Q-enhanced technique. The idea behind it is straightforward, to introduce negative resistance to compensate the loss of the on-chip passive resonators [31], [32], [42], [43]. The negative resistance can be applied to spiral inductors as in [42] and [32] and transmission line resonators as in [31].

In [42], the quality factor of the on-chip spiral inductors that form the filter resonators is enhanced by using a cross-coupled differential pair. The differential cross-coupled pair is degenerated by a second LC tank. The resulting frequency dependent compensation achieves a Q-enhanced resonator that has a behavior closer to the ideal resonator in the passband of interest. The authors of [32] also introduce a special negative resistance generating circuit that can enhance the quality factor of on-chip passive resonators while not distorting the bandpass response. The technique is based on the coupled-inductor configuration.

The Q-enhanced technique still uses large on-chip metal traces and thus consumes a large chip area. In addition, the fixed physical property of the on-chip passive devices, like spiral inductors, transformers and transmission

lines, limits the effective control of the electrical characteristics of these devices.

Another technique to realize a CMOS bandpass filter involves the use of G_m-C structures. However, most of the filters lying in this category are in voltage operation mode and require high input/output impedance [25], [68]-[70]. In addition, the applicable frequency range for most G_m-C type filters are limited in the sub-GHz range [21], [23], [25]-[29], [71]-[76].

The previous section has demonstrated the performance of the active series inductor that resembles an ideal inductor. Ultra-wideband BPF is then feasible based on active inductors because the design techniques are also applicable for active shunt inductors.

2.4.2 Bandpass Filter Implementation

An L band wideband bandpass filter is implemented as a design example of bandpass design using active series and shunt inductors. The performance target of the bandpass filter are listed in Table 2-2.

The most convenient approach to synthesize a bandpass filter is starting from the classical prototype. However, the problem occurs when replacing the passive inductors with active realizations. We note that non-ideal parasitics will be introduced when adopting active inductors in circuit design. A typical case is shown in Figure 2.24. The most important parasitic components are the parallel capacitors C_P. This capacitor can modify the response of the resonator in the

active inductor.

TABLE 2-2 TARGET PERFORMANCE OF THE L-BAND BANDPASS FILTER.

Parameter	Value
BW_{3dB} (GHz)	1-2
BW_{40dB} (GHz)	0.7-2.25
Ripple (dB)	0.5
Shape Factor (BW_{3dB}/BW_{40dB})	0.75
DC Supply (V)	1.2

Consider a simple parallel LC resonator connected in series to generate a transmission zero as shown Figure 2.27. Although the responses match well at the center frequency, they deviate from each other at other frequencies. This is mainly due to the extra shunt capacitance of the active inductor.

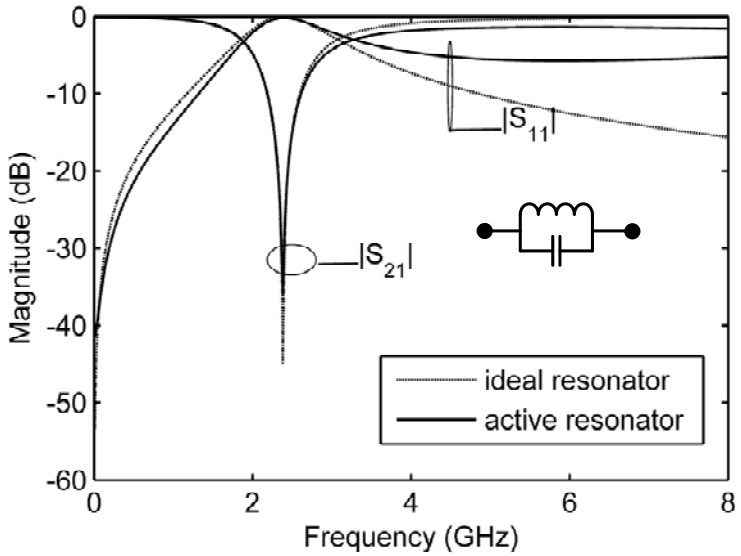

Figure 2.27. S-parameters of active inductor based resonator and ideal resonator.

In order to absorb the effects of the parasitic shunt capacitors, the prototype of the bandpass filter is carefully designed. The simplified schematic of the differential 7-stage high selectivity bandpass filter is shown in Figure 2.28.

The shunt capacitors C_1 and C_3 are capable of absorbing the parasitic shunt capacitance introduced by the active inductors. Two types of active inductors are used. The inductors L_1 and L_3 are realized as differential active shunt inductors, while the inductors L_2 and L_4 are realized as differential active series inductors. The design of the active series inductors has been demonstrated in section 2.3. The active shunt inductors are implemented using similar theory and the design process is not elaborated further here.

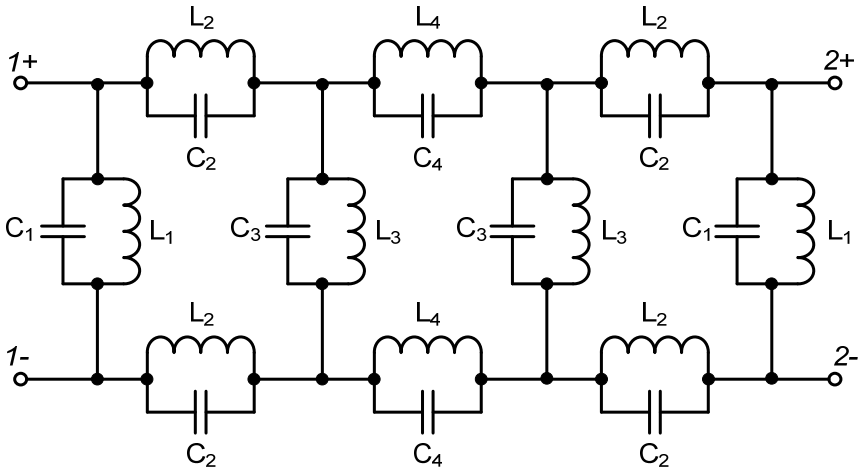

Figure 2.28. Simplified schematic of the proposed bandpass filter.

2.4.3 Measurement Results

The differential 7-stage active inductor based bandpass filter is fabricated in a standard 0.13 μm CMOS. The micrograph of the chip is shown in Figure 2.29.

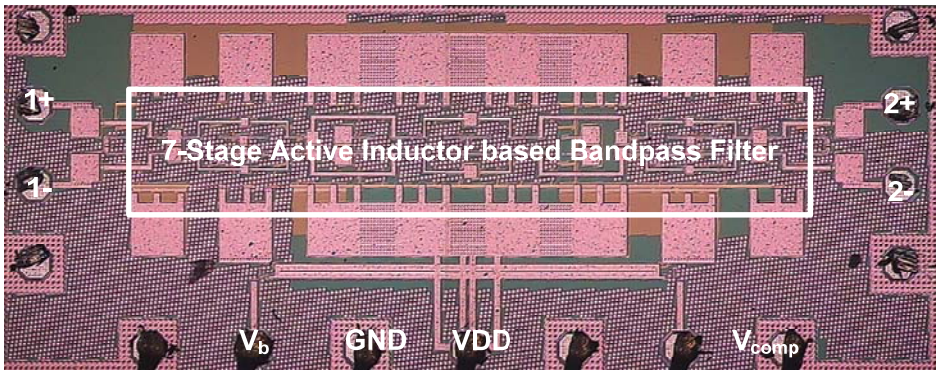

Figure 2.29. Micrograph of the fabricated 7-stage bandpass filter.

The core part of the active filter including filter capacitors is 0.18 mm^2. On wafer measurement is carried out to characterize the differential active bandpass filter. A four port VNA is used to obtain the full port parameters. The DC bias is provided from a standard PCB via bonding wires. The whole active filter consumes 25 mA current at a 1.2 V supply voltage.

The measured four-port S-parameters are converted into differential mode and common mode two-port S-parameters. The differential input/output matching is shown in Figure 2.30. The input return loss is better than 10 dB from 1.1 GHz to 1.98 GHz. The input return loss degrades toward the two edges of the passband. The worst return loss is 8 dB. As can be seen from Figure 2.30, the measured input and output matching deviate from the simulated results. This may be due to the performance variations of R_{comp} in the active inductors of

different stages. The active filter shares the same R_{comp} control voltage V_{comp} for different stages. Thus the amount of compensation may be off from the desired value in some stages.

The differential mode transmission response is shown in Figure 2.31. The passband is measured to be 1-2 GHz. The out-of-band rejection is better than 40 dB below 0.7 GHz and above 2.24 GHz. The shape factor (BW_{3dB}/BW_{20dB}) is calculated as 0.78. The passband of the active filter is enlarged in Figure 2.32. The passband ripple is within 0.5 dB. Also shown in the inserted group delay.

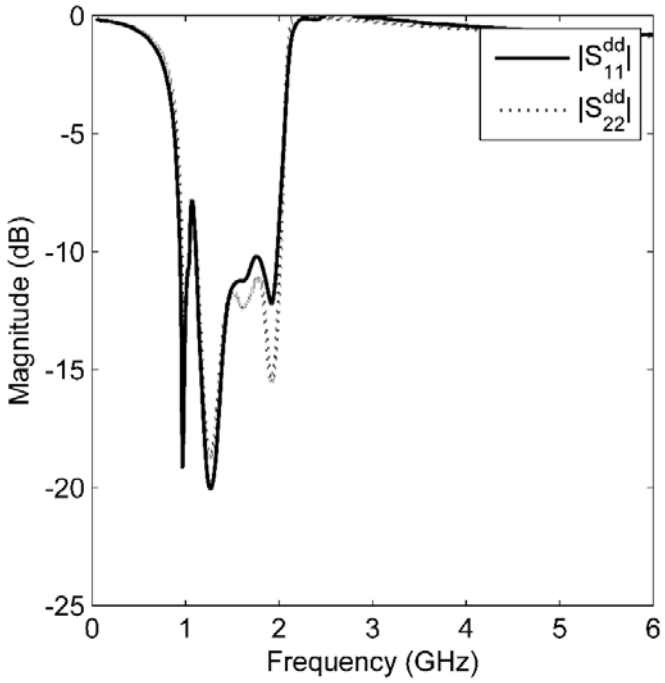

Figure 2.30. Measured differential mode response: $|S_{11}^{dd}|$ and $|S_{22}^{dd}|$.

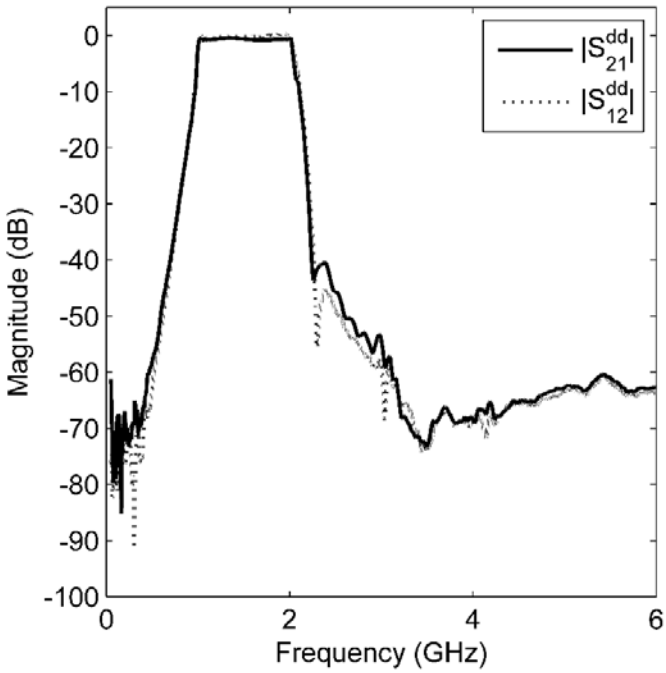

Figure 2.31. Measured differential mode response: $|S_{21}^{dd}|$ and $|S_{12}^{dd}|$.

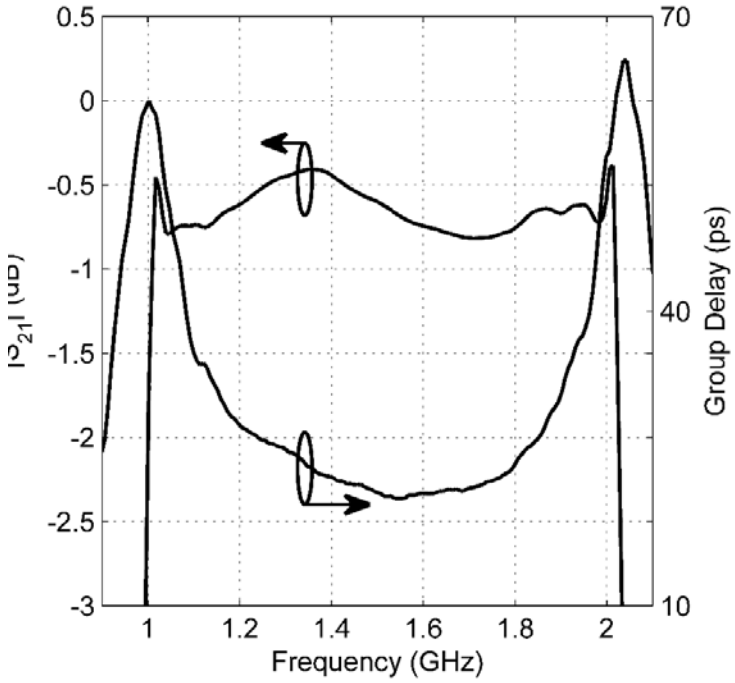

Figure 2.32. Insertion loss and group delay within the passband.

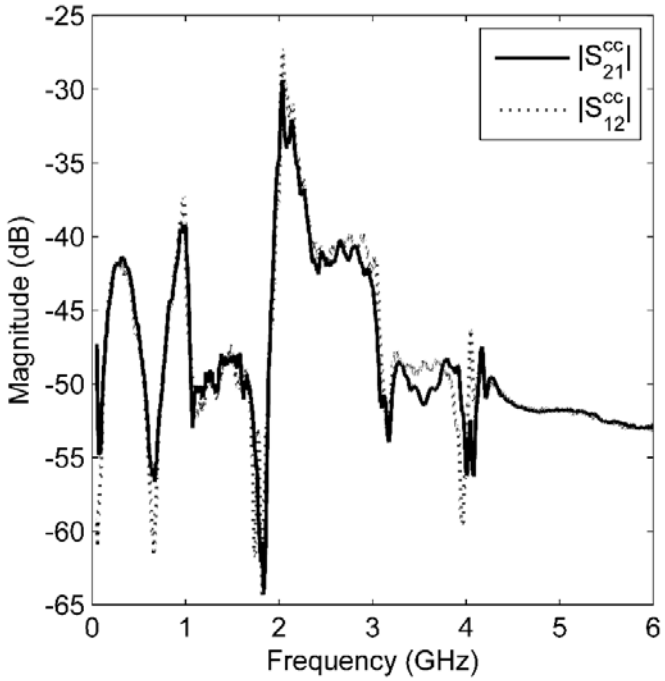

Figure 2.33. Measured common mode response: $|S_{21}^{cc}|$ and $|S_{12}^{cc}|$.

The common mode transmission performance is illustrated in Figure 2.33. The results are similar to the active inductor based resonator introduced in section 2.3. The common mode suppression of the active bandpass filter is better than 27 dB. The nonlinearity of the active bandpass filter is characterized with the help of a wideband balun. The measured 1 dB compression point is shown in Figure 2.34. The input 1 dB compression point is -21 dBm.

The stability of the active bandpass filter is also examined. With the help of different stability verification methods like k-factor and μ-factor, the active bandpass filter was found to be unconditionally stable in the out-of-band region while conditionally stable within the passband. The stability circles of the measured frequency range of 0.1-6 GHz are shown in Figure 2.35. The stable region includes the origin point of $\Gamma=0$. It can be seen that the unstable

region mostly lies at the boundary of the Smith chart.

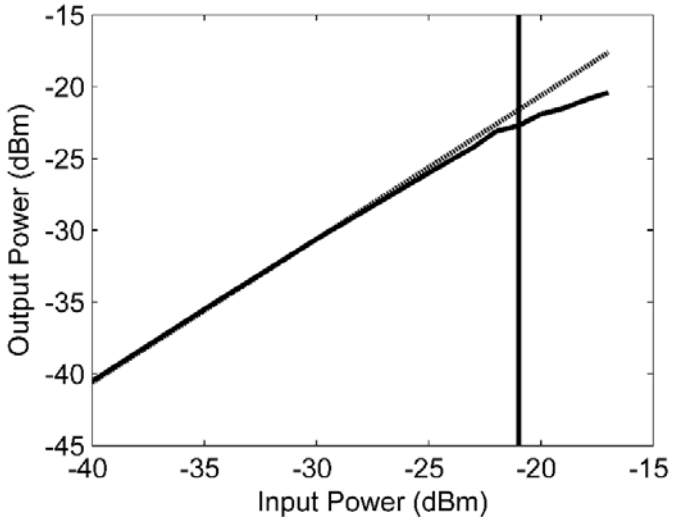

Figure 2.34. Measured input referred 1 dB compression point.

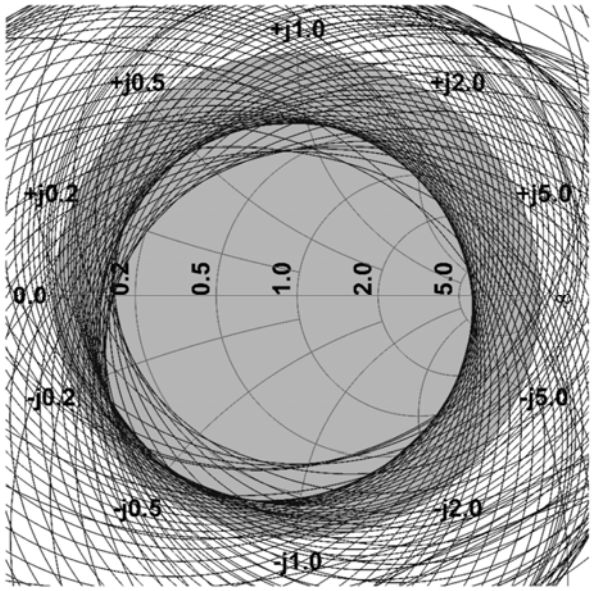

Figure 2.35. Measured stability circles of the active bandpass filter from 0.1 GHz to 6 GHz.

2.5 Conclusions and Recommendations

This chapter explores the feasibility of designing CMOS high order bandpass filters with active inductors.

Although there are many of works in the literature that have presented decent results [77], results of higher order wideband bandpass filters are limited. The reported active inductor based bandpass filters are mostly in the top-C coupled structure because they only the active shunt inductor are used. The top-C coupled structure limits their achievable bandwidth [32]. The implementation of active series inductors can overcome the design limitations. As has been demonstrated in this chapter, using the active series inductors, a bandpass filter with a passband of 1-2 GHz can be achieved. And theoretically, bandpass filters with any bandwidth and order can be realized.

However, several issues still need to be improved. The first issue is the noise performance. The simulated in band noise figure of the active bandpass filter is 19 dB. Considering the high order of the filter, the result is reasonable compared to other similar active filters. Because the conventional low noise strategy, such as noise cancelling [78], introduces extra loads and parasitics. This is not suitable for the wideband active bandpass filter implementation. Novel low noise techniques thus need to be explored to improve the noise performance. The second issue is the nonlinearity. Because there is no gain for each stage in the active bandpass filter, the nonlinearity is determined by the first stage. The nonlinearity of each active inductor is thus of major

importance. To improve this, extra power may be needed. Because techniques like source degeneration and feed forward both require extra current flow [79]. Another practical solution might be the complementary configuration [80], in which nMOS and pMOS transistors conduct in turn to improve the overall nonlinearity performance.

Chapter 3 CMOS Octave Bandwidth High Selectivity Bandpass Filter Using Gyrator Based Resonators

3.1 Motivation

In the previous chapter, active inductor based bandpass filter design is demonstrated. The major goal is to achieve a high frequency selectivity in a small chip area. This is difficult to realize with negative resistance compensated semi-passive designs. However, further improvements can be made.

One drawback of the active inductor based filter design is due to the parasitics, especially the parasitic capacitances. Although a proper bandpass filter prototype is developed in the previous chapter to prevent these parasitic capacitances from deteriorating the response of the filter, there is another parasitic capacitance related issue worth investigating.

This issue can be revealed by taking a closer look at the gyrator based active inductor structure. Here the active shunt inductor is taken as example. The simplified circuit configuration can be referred back to section 2.2. As shown in Figure 2.4, the design of a practical gyrator based active shunt inductor will result in a resonator resembling a parallel LC structure. The inevitable parallel capacitance C_p resulting from the parasitic capacitance of the OTA cells (C_{in}) has been discussed in the previous chapter.

However, another component is also affected, which is the equivalent inductor value. In order to minimize the power consumption, it is desirable to use only the parasitic capacitance as the load capacitance to generate the inductance needed. In this case the resulting equivalent inductance is:

$$L_{eq} = \frac{C_{in}}{g_m^2} \tag{3.1}$$

An optimistic assumption is that the parasitic capacitance of the OTA is merely the gate-source capacitance of the input transistor. Given the cutoff frequency of

$$\omega_T = \frac{g_m}{C_{in}} \tag{3.2}$$

Equation (3.1) can be modified as

$$L_{eq} = \frac{1}{\omega_T g_m} \tag{3.3}$$

It is observed from equation (3.3) that the minimum achievable equivalent inductance is inverse proportional to the angular cutoff frequency of the process (ω_T). This means that, for the same desired inductance, higher g_m is needed for the process with lower cutoff frequency. This will increase the power consumption in the end. In addition, the minimum achievable inductance is inverse proportional to the transconductance used. It can be seen from Figure 3.1 that the minimum achievable inductance drops when the transconductance increases initially. However, this trend slows down when the transconductance goes higher. This issue limits the applicable frequency range for the active inductors.

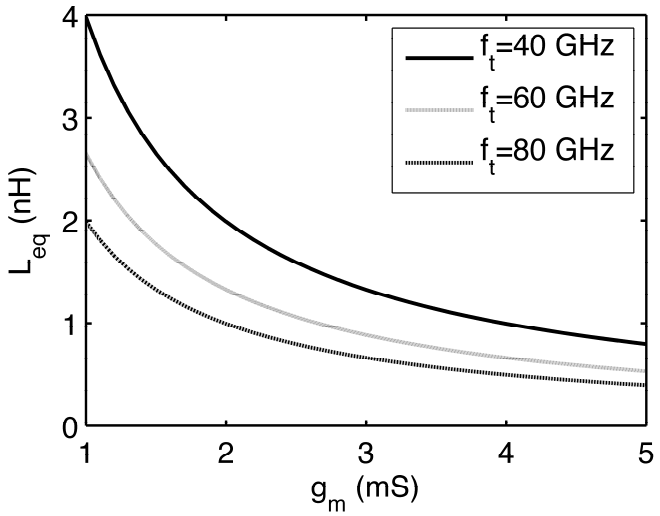

Figure 3.1. Achievable inductance versus transconductance for different cut-off frequencies.

For example, for a simple LC resonator the maximum center frequency is written as:

$$f_{o,\max} = \frac{1}{2\pi\sqrt{L_{eq,\min}C}} = \frac{1}{2\pi\sqrt{\frac{C_{gs}}{g_m^2}C}} = \frac{1}{2\pi}\sqrt{\frac{1}{\omega_T}}\sqrt{\frac{g_m}{C}} \tag{3.4}$$

which means that the maximum center frequency is proportional to the square root of transconductance g_m. This relation, however, does not exist in the transconductance-C (G_m-C) type filter design [24], [80], [81]. But their unmatched input/output characteristics and limited bandwidths remain as the main drawbacks.

As a result, the motivation of this chapter is to build reciprocal resonators without using active inductors. A high order bandpass filter can then be developed based on the proposed resonator.

3.2 Gyrator based Resonator

3.2.1 Single Stage Gyrator-resonator with One Transmission Pole

The impedance inverting property of the gyrator cell is capable of translating a capacitance into an inductance. Without using a real lumped inductor, the gyrator-based resonator shown in Figure 3.2 can behave like a resonator and provide bandpass response. Assume that G_{m1}=-G_{m2}=G_m, the ABCD matrix of the active resonator is written by:

$$ABCD = \begin{bmatrix} \dfrac{s^2 C_{P2}(C_{S1}+C_{P1})+G_m^2}{sG_m C_{S1}} & \dfrac{s^2(C_{S2}+C_{P2})(C_{S1}+C_{P1})+G_m^2}{s^2 G_m C_{S1} C_{S2}} \\ \dfrac{s^2 C_{P1} C_{P2}+G_m^2}{G_m} & \dfrac{s^2 C_{P1}(C_{S2}+C_{P2})+G_m^2}{sG_m C_{S2}} \end{bmatrix} \quad (3.5)$$

It is easy to show that the ABCD matrix satisfies

$$AD - BC = 1 \quad (3.6)$$

The resulting two-port network is thus reciprocal.

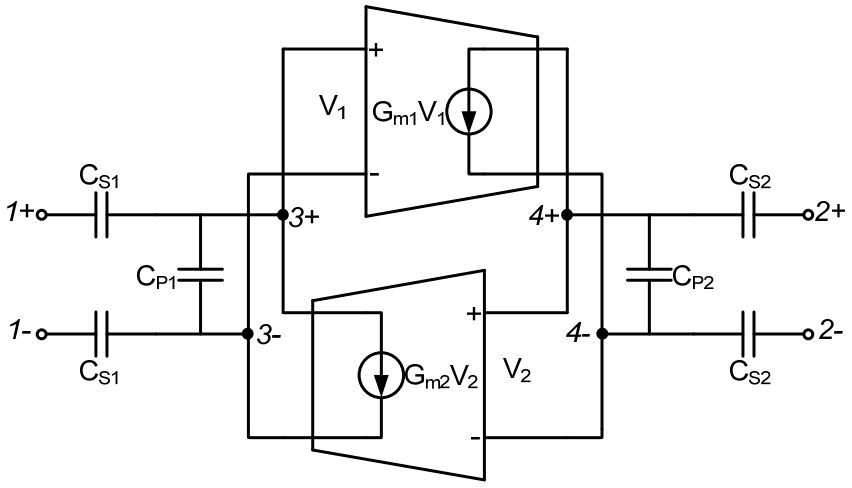

Figure 3.2. Simplified schematic of the gyrator based resonator.

For simplicity, the capacitors at the two ports of the resonator are assumed symmetric, i.e., C_{S1}=C_{S2} and C_{P1}=C_{P2}. A typical response of the

gyrator-resonator is simulated with SpectreRF and shown in Figure 3.3.

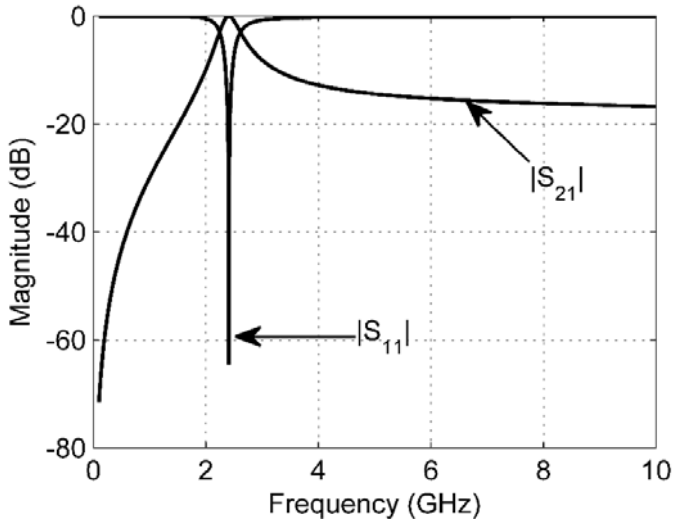

Figure 3.3. A typical response of the gyrator-resonator with G_m=6 mS, C_{S1}=200 fF and C_{S2}=200 fF.

It is observed that the single resonator has a frequency response similar to a bandpass filter with a single transmission pole. However, the suppression at higher frequencies does not improve. This is understandable when making a qualitative analysis of Figure 3.2. At high frequencies, capacitors are considered as very low impedance. The impedance at node 4 seen towards node 2 can be considered low and lowers further when frequency increases. With the inserted gyrator, the impedance at node 3 seen towards node 2 can be considered as infinity. The voltage at node 3 is thus determined by the impedance ratio between the capacitors C_{S1}, C_{P1} and the source resistance. These three components form a first order lowpass filter. As a result, the final forward transmission coefficient is therefore similar.

As can be seen from equation (3.5), the center frequency of the single stage

resonator is determined not only by the transconductance G_m but also the series and shunt capacitors as well.

A single stage gyrator-resonator is simulated in SpectreRF with the same capacitors as C_{SI}=C_{PI}=200 fF. The transconductance is swept from 2 mS to 6 mS and the results are shown in Figure 3.4. It can be seen that the center frequency is proportional to the G_m value, which can be predicted by equation (3.5).

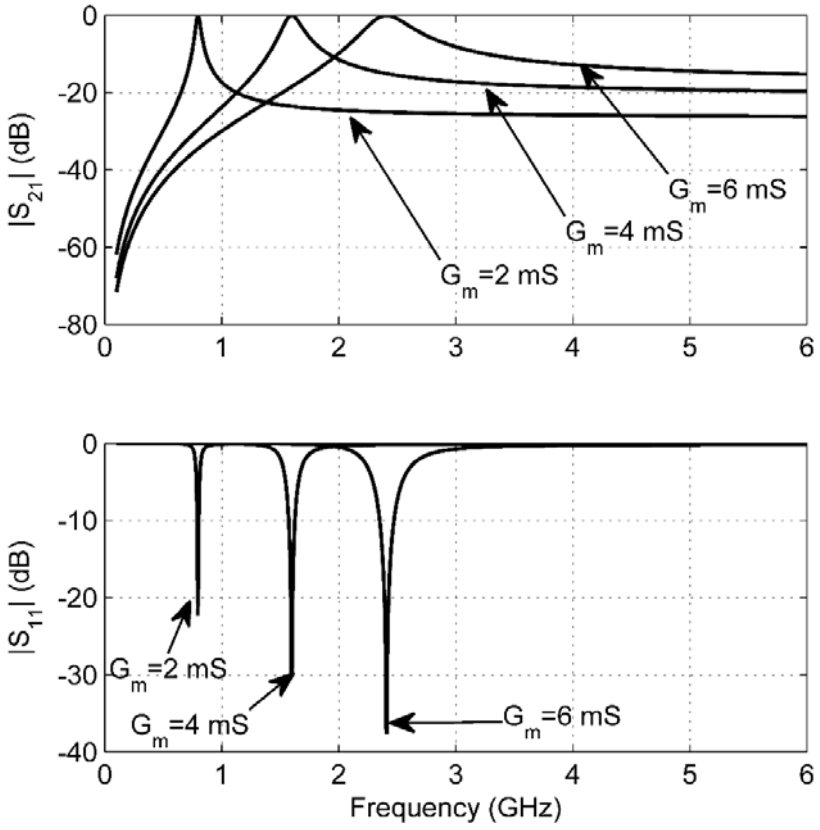

Figure 3.4. Simulation results of single stage gyrator-resonator with different G_m values at C_{SI}=C_{PI}=200 fF.

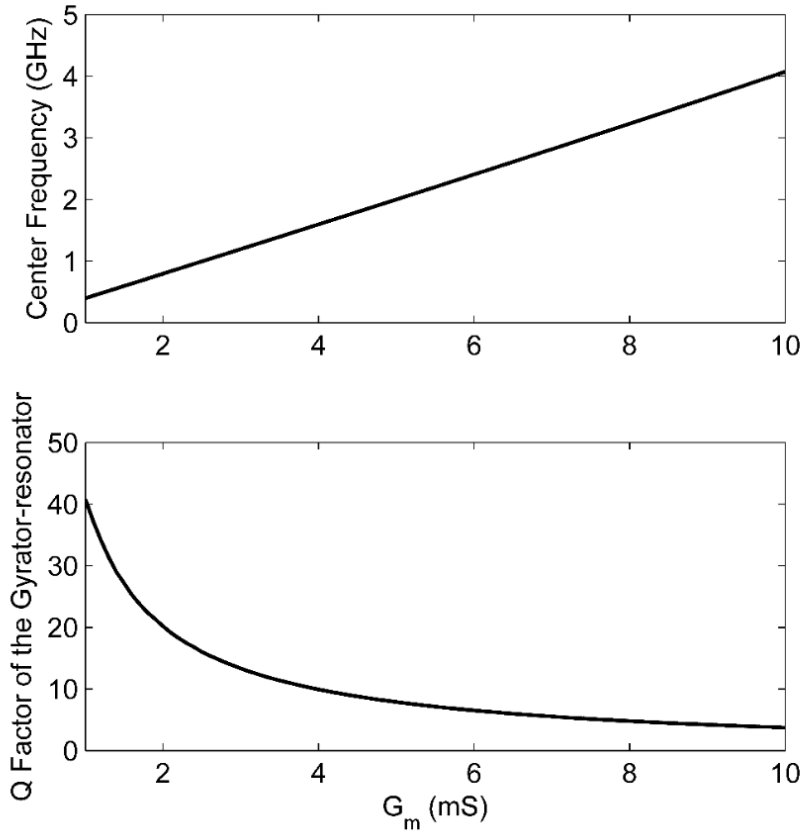

Figure 3.5. Center frequency and quality factor of the gyrator-resonator versus G_m with C_{S1}=C_{P1}=200 fF.

It is also observed that the loaded quality factor of the gyrator-resonator is also affected by the transconductance G_m. A more detailed simulation is carried out and the results are shown in Figure 3.5.

Figure 3.5 clearly shows the linear relation between the center frequency f_o and the transconductance G_m. Note that for the case of active inductor based resonators (as shown in equation (3.4)), the maximum center frequency is limited by the cut-off frequency and is proportional to the square root of the transconductance.

On the other hand, the loaded Q-factor is inverse proportional to the

transconductance used. The loaded Q-factor is also an indicator of the strength of the external coupling coefficient of the gyrator-resonator.

The effect of the series and shunt capacitors C_{S1} (C_{S2}) and C_{P1} (C_{P2}) is also characterized and shown in Figure 3.6.

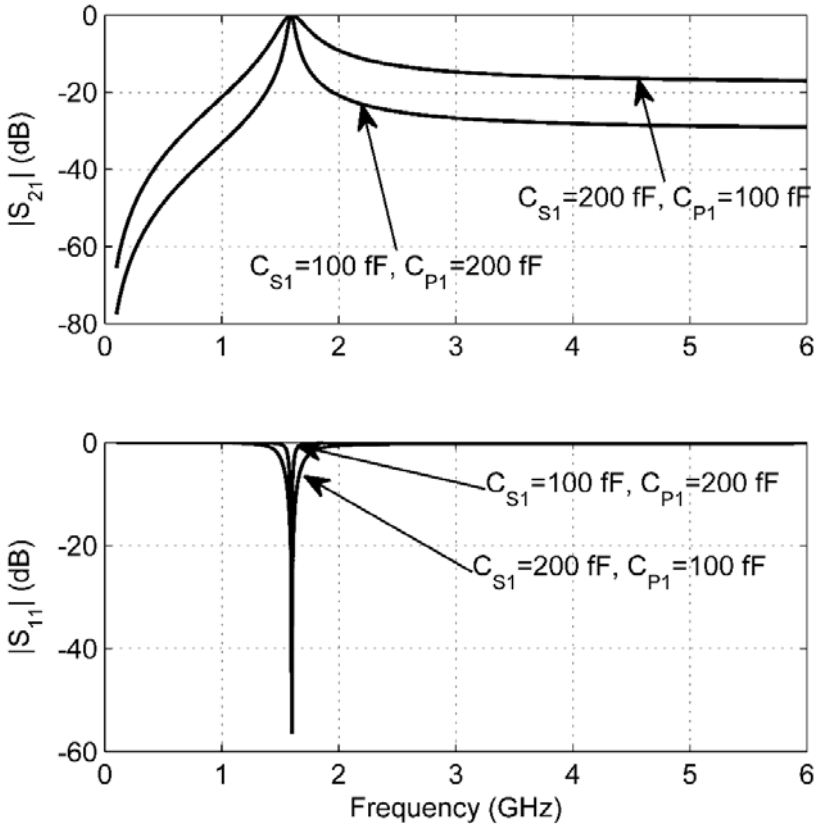

Figure 3.6. SpectreRF simulation results of single stage gyrator-resonator with different series and shunt capacitors values at G_m=3 mS.

The center frequency is maintained by keeping the term (C_{S1}+C_{P1}) unchanged. However, the loaded Q-factors are different for the simulated two combinations. Higher series capacitance generates lower loaded Q-factor and higher shunt capacitance is associated with higher loaded Q-factor. A more

detailed simulation is shown in Figure 3.7.

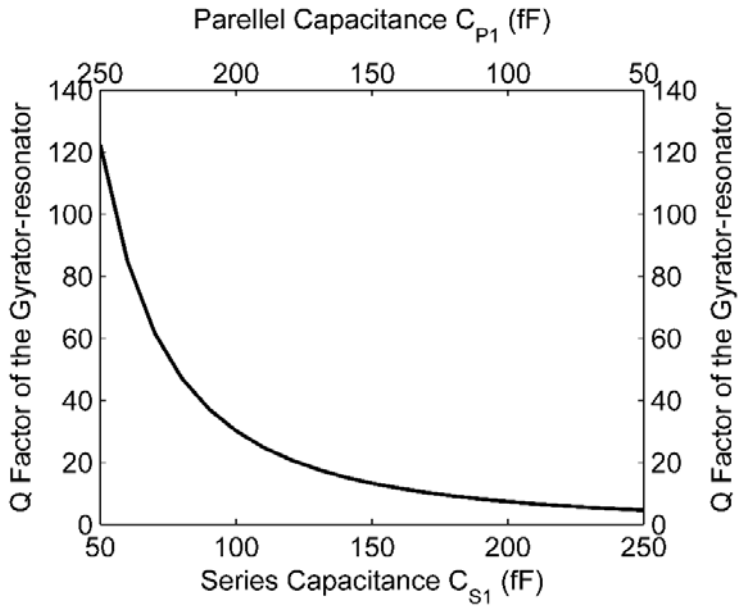

Figure 3.7. Quality factor of the gyrator-resonator versus series capacitance and parallel capacitance at G_m=3 mS.

The previous analysis and simulations have shown that the two key parameters the center frequency f_o and the quality factor are determined by the transconductance G_m, the series capacitor C_{S1} (C_{S2}=C_{S1}) and the shunt capacitor C_{P1} (C_{P2}=C_{P1}) at the same time.

3.2.2 Two-stage Gyrator-resonator

A higher order bandpass response can be obtained by cascading multiple stages of the gyrator-resonators. A two-stage gyrator-resonator is shown in Figure 3.8, which is a cascaded connection of two identical single stage gyrator-resonators shown in Figure 3.2. The whole structure is kept symmetric to maintain

reciprocity.

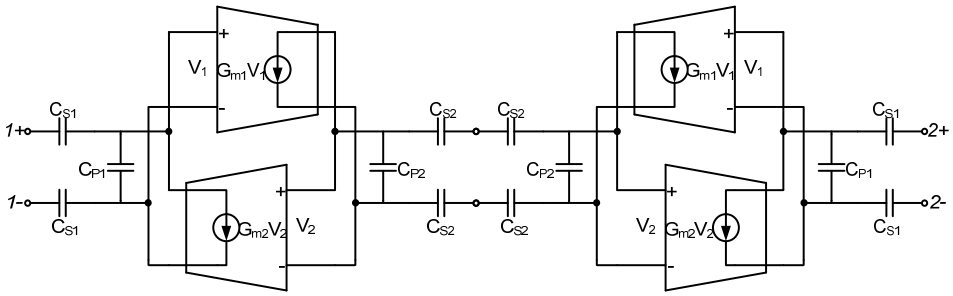

Figure 3.8. Simplified schematic of the 2-stage gyrator-resonator.

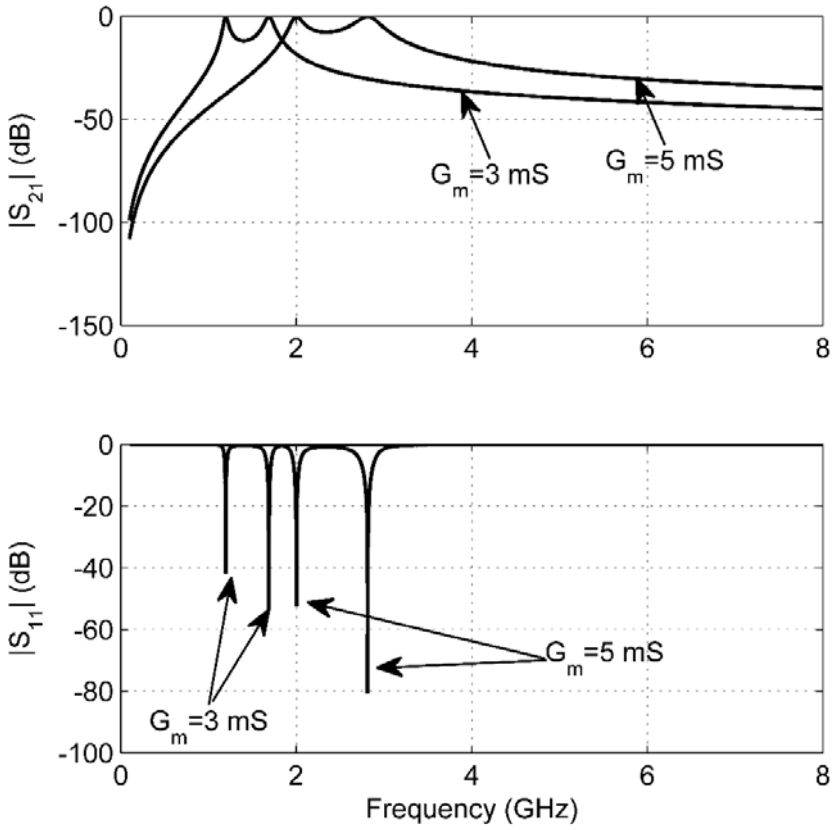

Figure 3.9. SpectreRF simulation of 2-stage gyrator-resonator with different G_m values at C_{S1}=C_{P1}= C_{S2}=C_{P2}=200 fF.

For the following analysis, we still assume that G_{m1}=G_{m2}=G_m. As shown in Figure 3.9, the cascaded two-stage gyrator-resonator behaves like coupled

resonators, as expected. Different G_m values are used while the capacitances are kept the same.

There are two transmission poles generated by the two-stage gyrator-resonator. Their locations are noted as f_L and f_H. By increasing the G_m value, f_L and f_H also increase. The coupling coefficient of the two-stage gyrator-resonator can be defined as

$$k_c = \frac{f_H^2 - f_L^2}{f_H^2 + f_L^2} \tag{3.7}$$

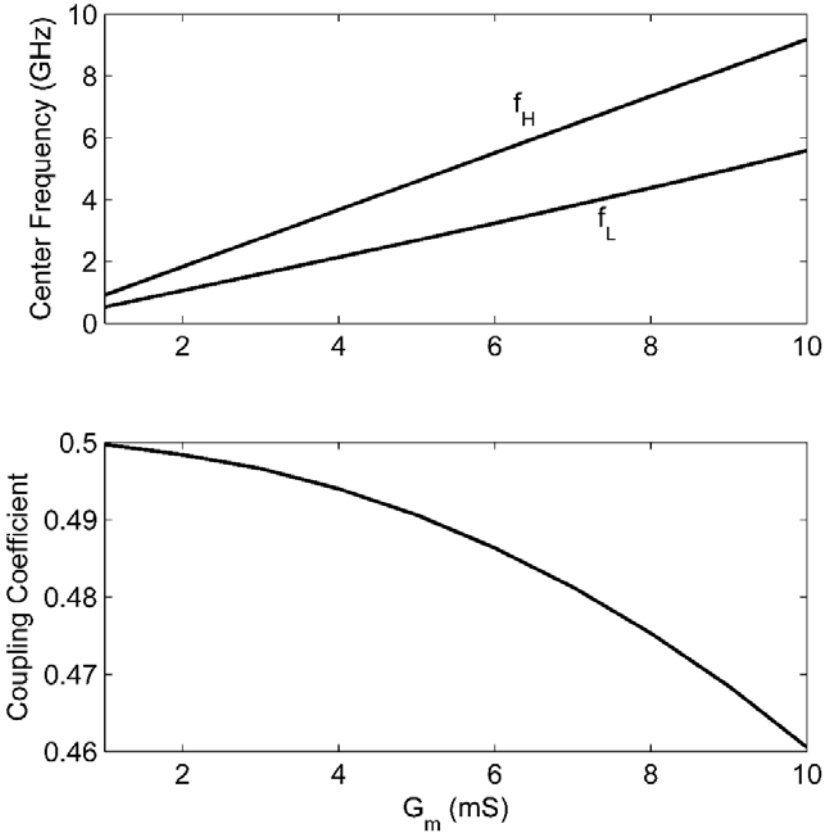

Figure 3.10. Simulated two-stage gyrator-resonator with different G_m values at C_{S1}=C_{P1}=C_{S2}=C_{P2}=200 fF.

Figure 3.10 shows a more detailed simulation results of the two-stage

gyrator-resonator with different G_m values. As can be seen, the two transmission poles both have a linear relation with the G_m value. The coupling coefficient of the two transmission poles are relatively constant when G_m increases.

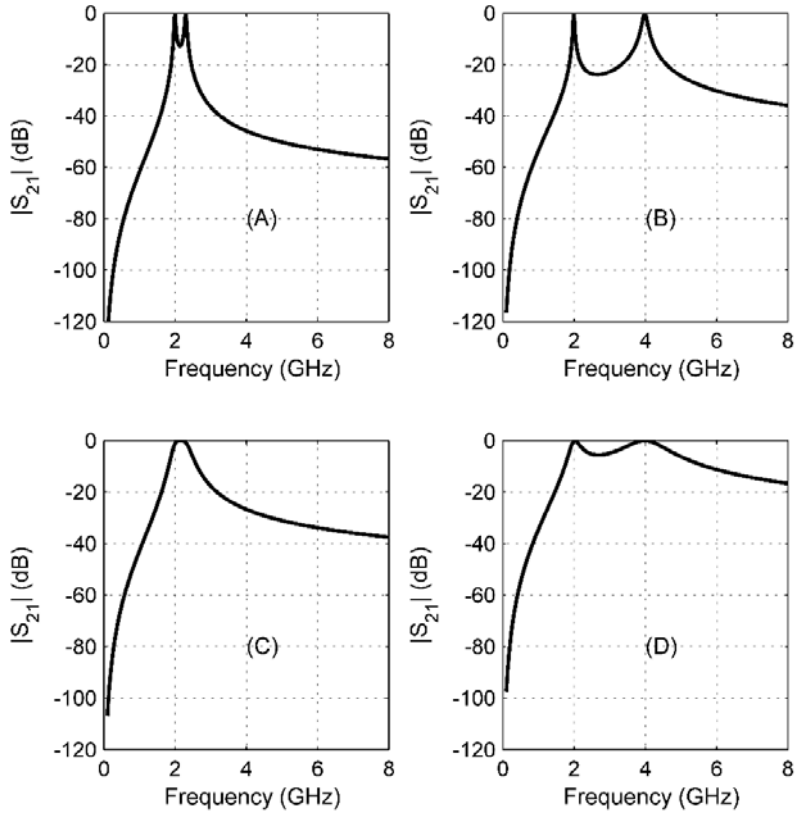

Figure 3.11. Simulated transmission coefficient of the two-stage gyrator-reonator at G_m=5 mS: (a) C_{S1}=100 fF, C_{P1}=300 fF, C_{S2}=100 fF, C_{P2}=300 fF. (b) C_{S1}=100 fF, C_{P1}=300 fF, C_{S2}=300 fF, C_{P2}=100 fF. (c) C_{S1}=300 fF, C_{P1}=100 fF, C_{S2}=100 fF, C_{P2}=300 fF. (d) C_{S1}=300 fF, C_{P1}=100 Ff, C_{S2}=300 fF, C_{P2}=100 fF.

The two-stage gyrator-resonator is investigated with different combinations of the series and shunt capacitors values in SpectreRF simulations. The series and shunt capacitors can be devided into two groups. The first group is the external

coupling group consisting of C_{S1} and C_{P1} while the other group is the internal coupling group consisting of C_{S2} and C_{P2}. The simulation is performed with G_m=5 mS and the transmission poles f_L and f_H are maintained at the same locations.

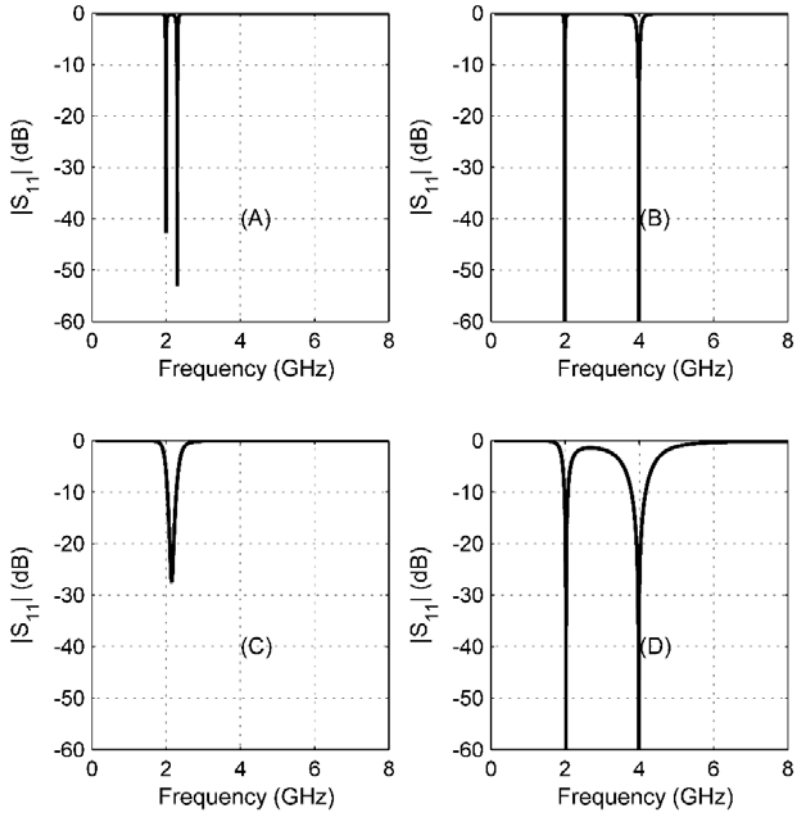

Figure 3.12. Simulated reflection coefficient of the two-stage gyrator-reonator at G_m=5 mS: (a) C_{S1}=100 fF, C_{P1}=300 fF, C_{S2}=100 fF, C_{P2}=300 fF. (b) C_{S1}=100 fF, C_{P1}=300 fF, C_{S2}=300 fF, C_{P2}=100 fF. (c) C_{S1}=300 fF, C_{P1}=100 fF, C_{S2}=100 fF, C_{P2}=300 fF. (d) C_{S1}=300 fF, C_{P1}=100 Ff, C_{S2}=300 fF, C_{P2}=100 fF.

The transmission and reflection coefficients with different combinations of capacitors values are shown in Figure 3.11 and Figure 3.12. Four cases are considered: (A) low external coupling and low internal coupling; (B) low

external coupling and high internal coupling; (C) high external coupling and low internal coupling and (D) high external coupling and high internal coupling.

It is observed that the external coupling controls the quality factors of the two transmission poles while the internal coupling controls the relative locations of the two transmission poles. This property provides a tuning guideline for higher order bandpass filter design.

3.2.3 Single Stage Gyrator-resonator with One Transmission Zero

In order to improve the frequency selectivity and out-of-band rejection of the bandpass filter, transmission zeroes are always introduced. The generation of a transmission zero can be easily achieved by a series parallel LC or a shunt series LC. However, the active realization of the inductors (or even the typical on-chip spiral inductors) will introduce extra parasitic capacitances. The simplified schematics are shown in Figure 3.13.

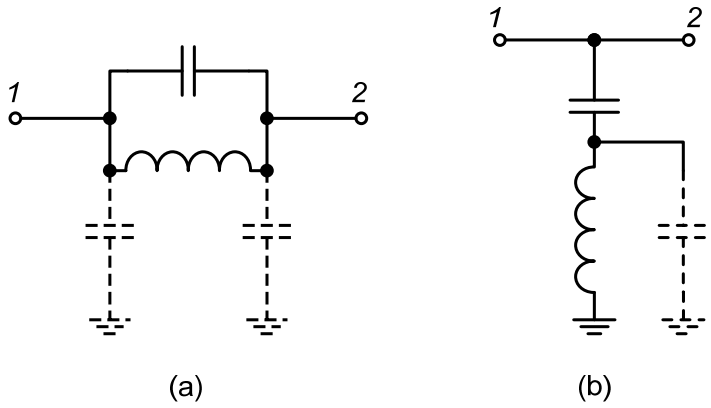

Figure 3.13. Simple LC network to generate transmission zero with parasitic capacitance: (a) series parallel LC (b) shunt series LC.

As illustrated in Figure 3.13, the parasitic capacitances of the inductors are shown with a dashed line. The quality of the generated transmission zeros thus deteriorates due to these parasitic capacitors. An alternative way to generate a transmission zero with the gyrator-resonator is shown in Figure 3.14. The approach is to short the two ports of the original gyrator-resonator. The resulting network can be considered as the dual of the original gyrator-resonator but generating a transmission zero instead. Here we still assume that G_{m1}=-G_{m2}=G_m, C_{S1}=C_{S2} and C_{P1}=C_{P2} for simplicity.

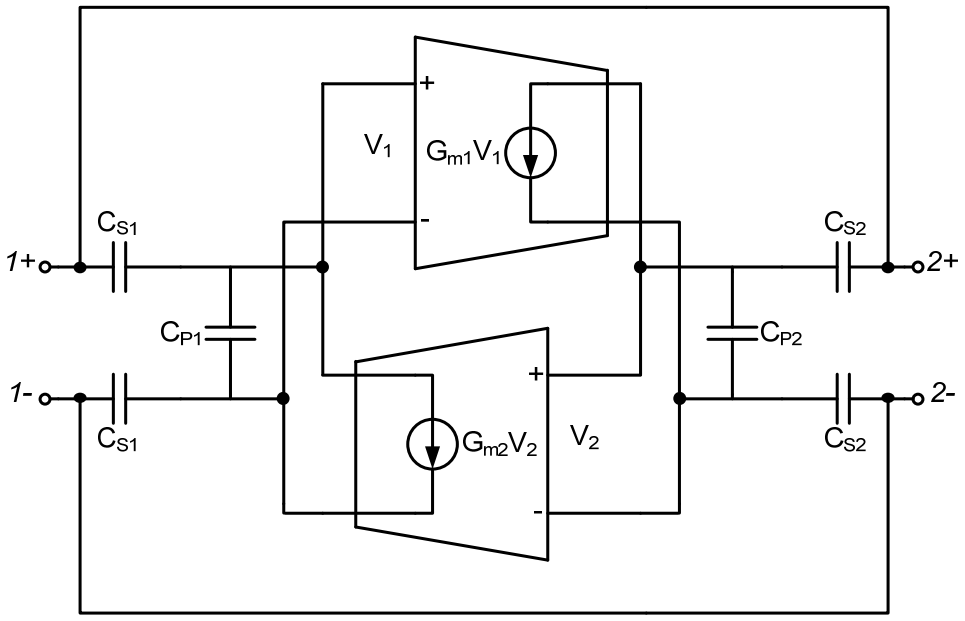

Figure 3.14. Simplified schematic of the single gyrator-resonator generating a tranmission zero.

As can be expected, the tuning property of the gyrator-resonator generating the transmission zero is similar to that of the normal single-stage gyrator-resonator generating the transmission pole. The SpectreRF simulation results are shown in Figure 3.15. The transmission zero can be controlled by the transconductance used. Another normal single-stage gyrator-resonator with G_m=3 mS and C_{S1}=C_{S2}=C_{P1}=C_{P2}=200 fF is cascaded with the transmission zero. The resulting transmission and refection coefficients are shown in Figure 3.16. The transmission pole of the cascaded network is independent of the tuning of the transmission zero.

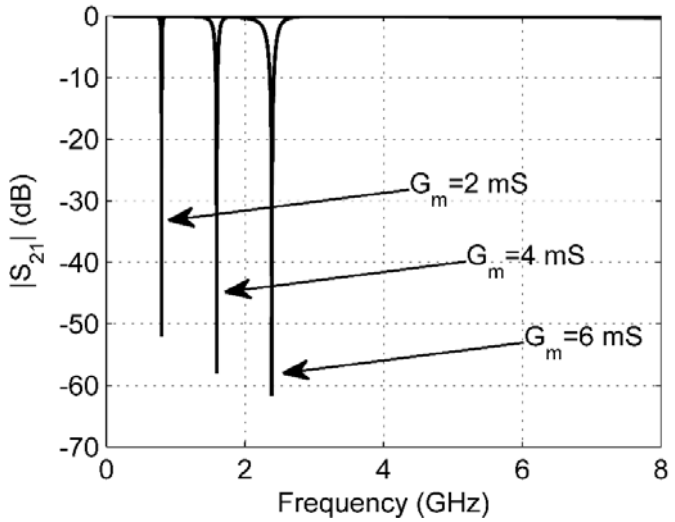

Figure 3.15. Simulated $|S_{21}|$ of single-stage gyrator-resonator generating transmission zero with different G_m at C_{S1}=C_{P1}=C_{S2}=C_{P2}=200 fF.

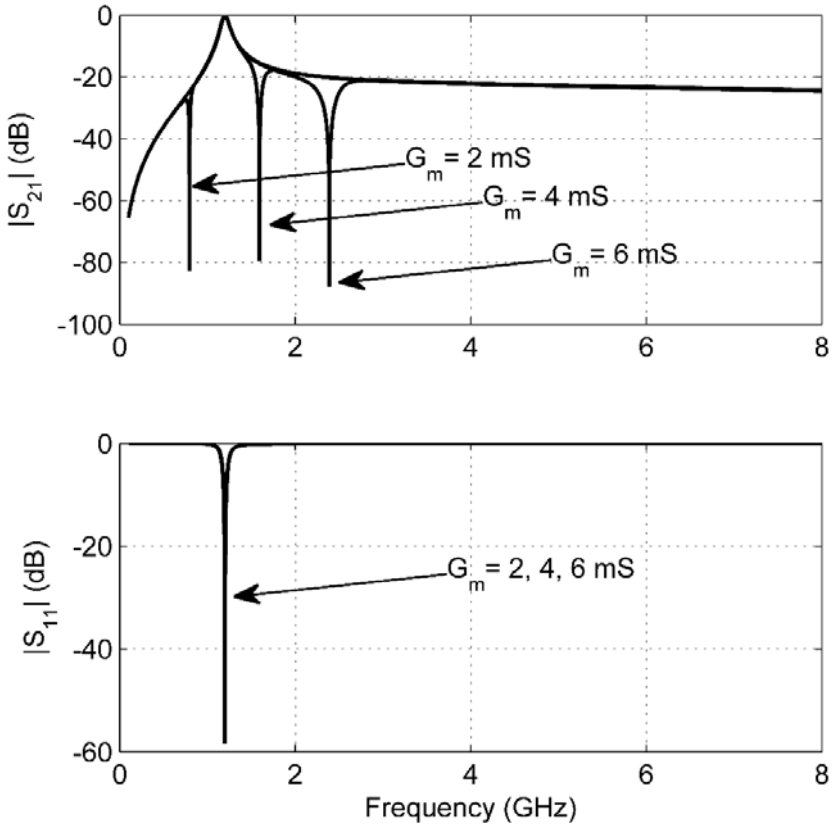

Figure 3.16. Simulated results of a gyrator-resonator generating a transmission zero cascaded with a normal single-stage gyrator-resonator.

3.3 Bandpass Filter Implementation

The previous section has introduced the basic building blocks for a bandpass filter. The transmission poles are generated with the normal gyrator-resonators and cascaded normal gyrator-resonators. Additional transmission zeroes can be provided with the shorted gyrator-resonator topology. In order to verify the application of the gyrator-resonators, a bandpass filter is implemented. The specs of the bandpass filter are set similar to those in section 2.4, except that the center frequency is at 2 GHz. The target specifications of the bandpass filter are summarized in the following table.

TABLE 3-1 TARGET PERFORMANCE OF THE BAND BANDPASS FILTER.

Parameter	Value
Center Frequency (GHz)	2
Fractional Bandwidth (%)	66
Shape Factor (BW_{3dB}/BW_{20dB})	0.75
DC Supply (V)	1.2

A 9-stage bandpass filter is realized with the previously introduced gyrator-resonators to satisfy the desired specifications of the bandpass filter. It consists of three transmission zero cells and six transmission pole cells. The bandpass filter structure is symmetric and the complete schematic is shown in Figure 3.17. The three transmission zero cells generate three transmission zeroes. Two of them are located at the same locations of z_1 and the other one is

allocated at z_2. Six transmission pole cells are grouped into three pairs. They are used to form the passband and located at p_1, p_2 and p_3 respectively.

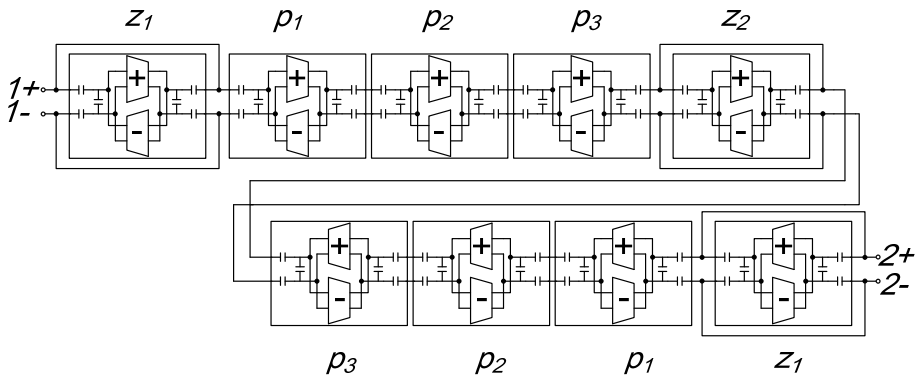

Figure 3.17. 9-stage bandpass filter based on gyrator-resonators.

The transmission poles of p_1, p_2 and p_3 are initially set in the vicinity of the lower passband edge. The other transmission poles are generated by the internal coupling between these transmission pole cells. This scheme has been demonstrated in section 3.2.2. Because the main poles are at the lower frequency, the power consumption can be kept relatively low.

The frequency selectivity is improved by the insertion of transmission zeroes z_1 and z_2. z_1 is located at the high out-of-band and z_2 is set at the lower part. This is because the suppression at high frequency of the gyrator-resonator is weaker than at the low frequencies. Two transmission poles are then allocated in the high frequency range.

The design of the differential transconductor for the individual gyrator-resonator is the same as the transconductor introduced in section 2.3.1.

3.4 Experimental Results

The high order bandpass filter is fabricated in a standard 0.13 μm CMOS. The die photo is shown in Figure 3.18.

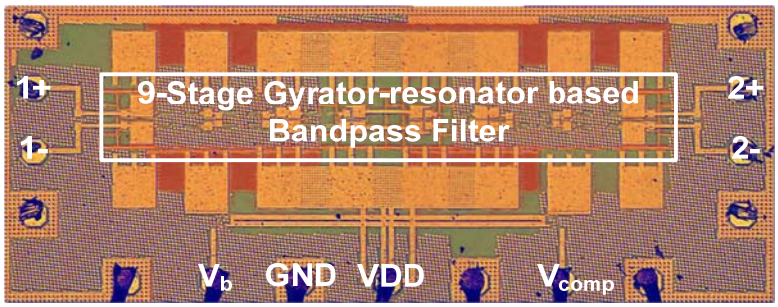

Figure 3.18. Micrograph of the fabricated 9-stage gyrator-resonator based active bandpass filter.

The core part of the differential active filter including filter capacitors is 1.4x0.12 mm^2. On-wafer measurements are performed to characterize the bandpass filter response. The four-port S-parameters are obtained with a four port VNA. The DC bias is provided by using a standard PCB via bonding wires. The whole active filter draws a 24 mA current at a 1.2 V supply voltage.

The differential mode and common mode operations of the bandpass filter are characterized by converting the measured four-port S-parameters into two-port S-parameters in the two operation modes. The differential mode S-parameters are shown in Figure 3.19 and Figure 3.20 respectively.

Mismatches are observed between the two ports. The major reason is in the layout of the gyrator cells. Different layers of metal are used for the signal routing, which, in turn, causes the asymmetric performances for the two ports in the differential mode operation. It is also observed that the reflection

coefficients are more sensitive to the mismatch. The forward transmission has a 3 dB bandwidth of 67% from 1.29 GHz to 2.6 GHz. The center frequency is thus 1.94 GHz which is slightly shifted from the designed center frequency. The 20 dB bandwidth is measured from 1.14 GHz to 2.79 GHz and this corresponds to a shape factor of 0.79. To the best of the author's knowledge, this is the highest shape factor that has been reported in the literature. In addition, the out-of-band rejection is better than 40 dB below 1.06 GHz and above 2.89 GHz. Due to the mismatches in the layout, the input and output matching of the bandpass filter deviate more from each other. The worst input return loss is 8 dB while the worst output return loss is 7 dB

The common mode operation of the active bandpass filter is also extracted and the results are shown in Figure 3.21. The common mode suppression is better than 45 dB across the whole measurement frequency range.

With the help of a wideband balun, the nonlinearity of the active filter is also measured. As shown in Figure 3.22, this input 1 dB compression point $P_{i,1dB}$ is measured as -16 dBm.

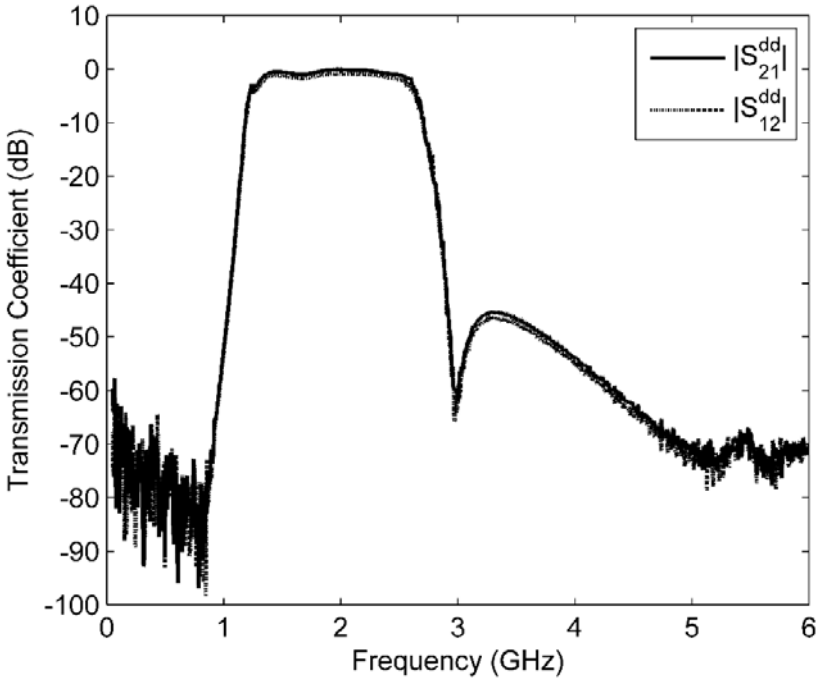

Figure 3.19. Measured differential mode transmission coefficients.

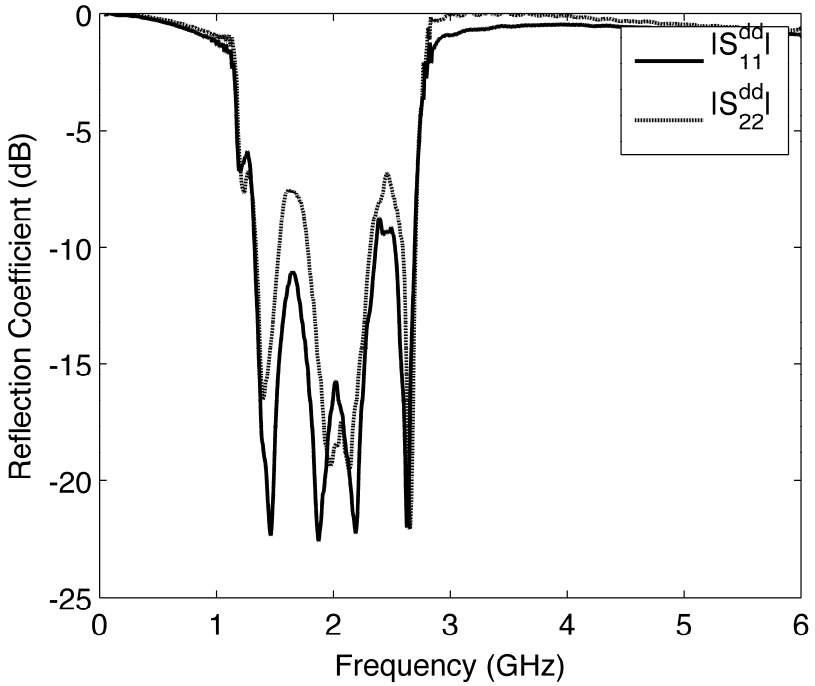

Figure 3.20. Measured differential mode reflection coefficients.

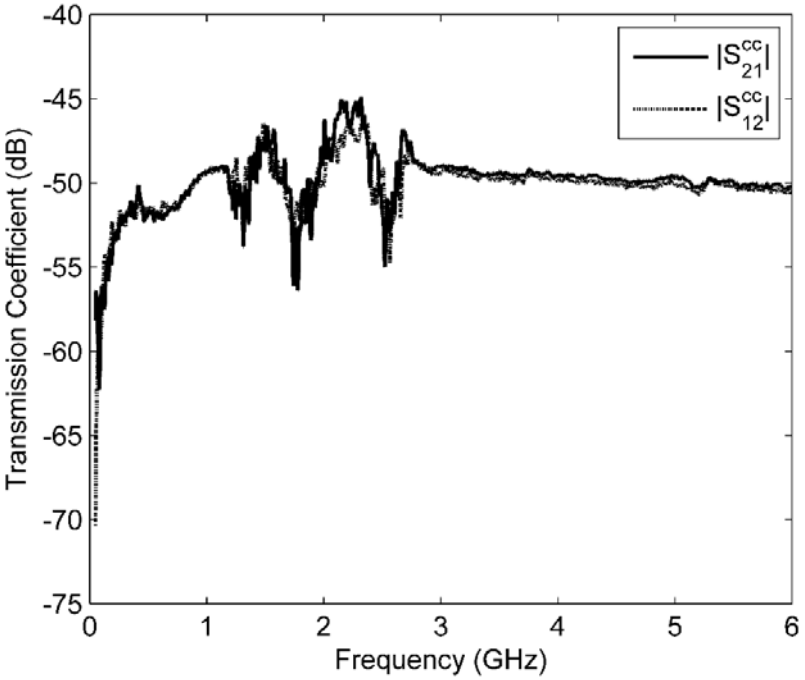

Figure 3.21. Measured common mode transmission coefficients.

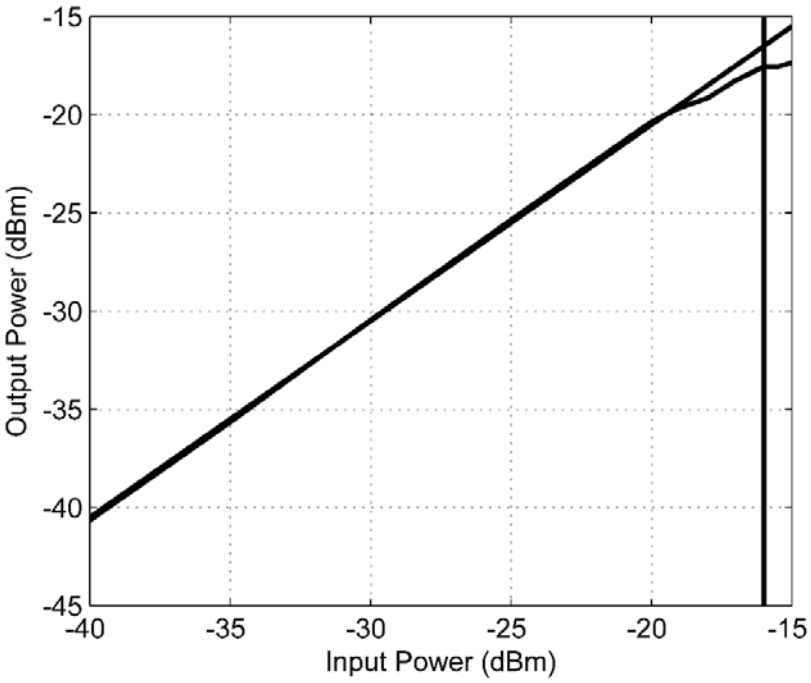

Figure 3.22. Measured 1 dB compression point.

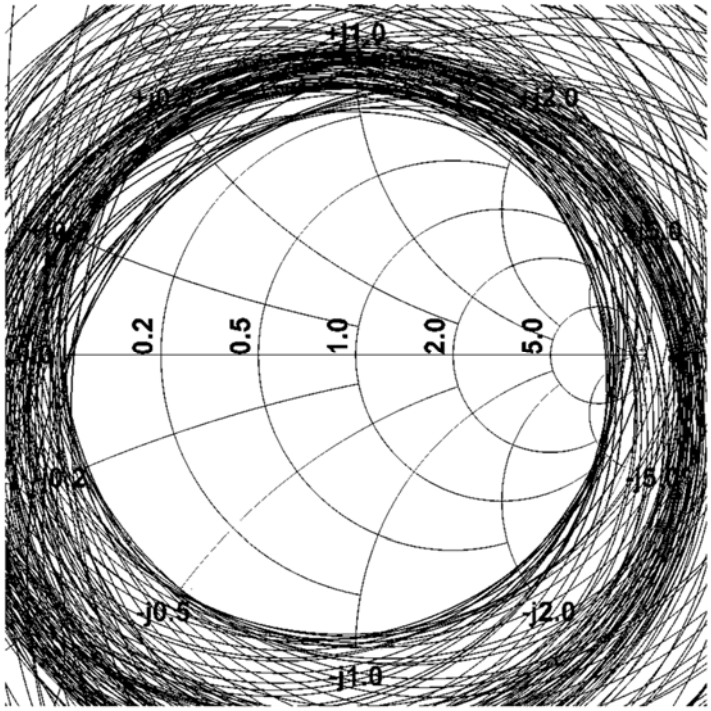

Figure 3.23. Measured stability circles of the active bandpass filter from 0.1 GHz to 6 GHz.

The stability of the active bandpass filter is also examined. With the help of different stability verification methods, like k-factor and μ-factor, the active bandpass filter is unconditionally stable in the out-of-band while conditionally stable within the passband. The stability circles of the measured frequency range 0.1-6 GHz are shown in Figure 3.23. The stable region includes the origin point of $\Gamma=0$. It can be seen that the unstable region mostly lies at the boundary of the Smith chart.

3.5 Conclusions and Recommendations

The motivation of this chapter is to avoid using active inductors when implementing high selective compact active bandpass filters. Although the conventional G_m-C type filter realization is one of the options, their input/output interfaces are always in the form of high impedance [74], [82]-[84]. As a result, active resonators behaving like conventional passive resonators are needed. This chapter proposes the gyrator-resonator to fulfill this purpose.

It is also noted that the center frequency of the active inductor based resonator is proportional to the square root of the transconductance forming the gyrator. Such a low frequency-power efficiency is improved by using the proposed gyrator resonator, for which the center frequency of the resonator is proportional to the first order of the transconductance.

The gyrator-resonator evolving from the gyrator topology is investigated. The position of the transmission pole is linear with the transconductance value as desired. The frequency limitations of the active inductors are thus alleviated. As a result, the bandpass filter realized in this chapter achieves a similar frequency selectivity as that of the active inductor based realization in the previous chapter. The center frequency of the gyrator-resonator based bandpass filter is 1.94 GHz, which is higher than the previous filter. The same center frequency of the active inductor based solution will require a higher power consumption.

It is also observed that the input return loss is not good. Similar results are also measured for the active inductor based BPF in Chapter 2. In addition, clear asymmetry can be seen from the measured input/output return loss. They are more sensitive to the parameter variations.

One possible solution is to allocate individual biasing controls for each gyrator-resonator stage. A necessary calibration process can then be carried out to remove some of the variations due to layout and fabrications. The two biasing controls V_{comp} and V_b (Figure 2.13) can be used to compensate the process variations. The first step is to tune V_b to generate the necessary transconductance value as the effective transconductance value is determined by the biasing current. After that, the output conductance is adjusted by setting the voltage V_{comp}. Consequently, the overall transconductance value, as well as the output conductance, of the OTA can be controlled by the two control voltages V_{comp} and V_b. As a result, by individually control each of the stages in the BPF, a better frequency response can be achieved. However, this process should is better to be carried out with on-chip automatic frequency tuning circuitry such as in [25], [29].

Other issues, like nonlinearity and noise performances, are also similar to those of the active inductor based bandpass filter demonstrated in section 2.4. The improvement requires a further optimization of the elementary building block: the operational transconductance amplifier. The optional techniques include complementary configuration [80], source degeneration and noise

cancelling. However, these techniques will introduce negative impacts such as extra power consumption and additional parasitics.

The more significant effect is the additional parasitics. The parasitic internal poles can easily be induced like in the source degeneration structure. And there might be resistive losses that cannot be compensated across a large frequency range. Consequently, those more advanced techniques may be more suitable for a narrow band application. While for the wideband design, like in this work, it is still challenging to adopt those techniques.

3.6 Performance Summary of the Active BPFs

In order to have a clearer view of the active bandpass filters, the performance of some selected active BPFs from the literature, together with the proposed active BPFs from this thesis, are summarized and shown in the following table. The design techniques of these filters are categorized into three groups: G_m-C type, Q-enhanced type and Active Inductor (AI) type.

The center frequencies of these BPFs differ not much and most of them are for the RF applications, expect [25]. The highest center frequency is presented by [43] as 2.54 GHz. The Q-enhanced technique generally presents relatively high frequency results while the G_m-C type BPFs are toward the low frequency range. The latest published [85] achieves a 2.4 GHz center frequency partially because of its sophisticated BiCMOS process.

Another observation is that there is a lack of ultra-wideband active BPFs in the literature. The FBW of 50 presented in [33] is calculated from the reported quality factor of 2 for its BPF. However, the low order response resembles simple resonators with do not provide desirable frequency selectivity. The achieved 66% FBW of the BPFs from this thesis are the largest in the literature for active BPF realization.

One merit of active circuits is their ability to provide a gain. As demonstrated in [45], [70], [25] and [85], they have achieved signal amplifications. However, those BPFs are generally in voltage-mode operations and the gain obtained is for voltage amplification. The rest works follow the traditional BPF synthesis

with source/load impedance of 50 Ω**.** The theoretical best performance should be 0 dB insertion loss, as shown in [32]. For the two BPFs in this thesis, a 0.5 dB insertion loss is designed to ensure the stability of the active BPFs. The stability issues, however, are not specifically discussed or addressed in some of the selected works like [43] and [42].

As a significant parameter for BPFs, the shape factor is also summarized. The orders of the BPFs are also used because the shape factors of some works are difficult to extract. We should note that the shape factors can differ even the BPFs have the same order. As can be seen, the BPFs proposed in this thesis show the best frequency selectivity both in terms of shape factor and filter order. The out-of-band rejections are neglected here because all the presented BPFs do not have parasitic transmission poles or the transmission amplitude at the parasitic transmission poles are well below the requirements.

Compared to the conventional passive realizations, the major drawbacks of the active BPFs include the additional noise, nonlinearity and power consumption. The additional noise is characterized by the in-band noise figure (NF). Some of the works listed in the table provide the noise floor alternatively. The NFs of the BPFs are generally in plus-ten dB range. Higher NFs are observed for the pure active BPF implementations like G_m-C type and AI type. The Q-enhanced type, on the other hand, shows relatively better NF performance even they have the same or higher filter order. This can be attributed to their less noisy passive components like spiral inductors and TLs. In addition, the passive resonators

also lead to a better nonlinearity performance compared to the G_m-C type and AI type BPFs. The two BPFs proposed in this thesis achieve reasonable NF and P_{1dB} performance considering their high order and large shape factor. The power consumptions of the proposed BPFs are regarded as good when considering the power consumption per order for the BPFs.

Finally, the G_m-C and AI type BPFs consume less chip area compared to the Q-enhanced implementations. This situation will become more obvious if the order of the BPF is increased. This is because the Q-enhanced BPF will involve more passive resonators and the coupling between these resonators needs to be reduced by separating them with a larger distance.

Recently, another category of active filters began to draw researchers' attention. They are called N-path filters or sampled-data filters [86]. They can deliver better linearity and noise performance than the conventional g_m-C types or AI types. However, most of the presented works in this category are narrowband bandpass filter and their operation frequency is limited [87]-[89]. Besides, the shape factors of such bandpass filters are relatively small because the equivalent model of such bandpass filter is a high Q parallel LC tank at the clock frequency [86]. The out-of-band rejection is further more limited due to the harmonic mixing with the clock frequency. However, the N-path filter can be regarded as a potential solution if higher order filtering response is achievable.

TABLE 3-2 SUMMARY OF ACTIVE BANDPASS FILTERS.

	[85]	[25]	[31]	[43]	[42]	[33]	[45]	[90]	KL Microwave 8IB30-1500	Mini-Circuits BFCN-152W	BPF of Chapter 2	BPF of Chapter 3
Technique	G_m-C	G_m-C	Q-enhanced	Q-enhanced	Q-enhanced	AI	AI	N-path	Passive	Passive	AI	Active Resonator
Process	BiCMOS	0.5 μm HP	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.35 μm CMOS	0.18 μm CMOS	65 nm CMOS	N.A.	LTCC	0.13 μm CMOS	0.13 μm CMOS
f_c (GHz)	0.8/2.4	0.07	1.58	2.54	2	0.1/1.1	2.44	0.4/1.2	1.5	1.475	1.5	1.94
FBW (%)	18.75/6.25	0.29	8	13	6.5	1.25/50	2.46	1.75/5.25	66	78	66	67
Maximum Gain (dB)	16*	30*	-0.68	0.8	0.3	-15	6	N.A.	-0.6	-1.9	-0.5	-0.5
Shape Factor /Order	N.A. /3	N.A. /6	0.48 /3	0.46 /3	0.4 /4	N.A. /2	0.051 /2	N.A. /4	0.67 /N.A.	0.56 /N.A.	0.78 /7	0.79 /7
NF (dB)	17.58/20.51	N.A.	14	15	15	N.A.	18	10	N.A.	N.A.	19&	14&
Input P_{1dB} (dBm)	N.A.	N.A.	-13.83	-14	-6.6	N.A.	-15	N.A.	N.A.	N.A.	-21	-16
IIP_3 (dBm)	-1.16/-1.93	-10	-2.8	N.A.	N.A.	-15	N.A.	9	N.A.	N.A.	N.A.	N.A.
P_{DC} (mW)	297/385	120	14.4	19.8	17	45.9	10.8	21.4	0	0	30	28.8
Core Size (mm^2)	0.21	0.96#	0.92	0.5015	0.81	0.028	0.03	0.127	N.A.	5.12	0.18	0.168

* Voltage Gain
** Noise Floor in dBm/Hz
& Simulated
# Area with Pads

Chapter 4 Multi-Octave Bandwidth True Time Delay Chain in CMOS Technology for Phased Array Systems

4.1 Introduction and Review

As one of the key components in phased array systems, the true time delay chain has been under investigation for decades [3]. There are two major challenges for the ultra-wideband true time delay chain realization, which are discussed in the following.

4.1.1 True Time Delay Networks

The first issue is the true time delay itself. The true time delay of a network is defined as:

$$\tau = -\frac{d\theta}{d\omega} \tag{4.1}$$

where θ is the phase difference between the output and input while ω is the angular frequency. There are two types of networks that have been widely adopted to provide a true time delay with low variation across a wide bandwidth.

Transmission Line based True Time Delay

The first one is the most straightforward one, the transmission line [35]. The time delay generated by a transmission line with length L can easily be

obtained:

$$\tau = \frac{L}{V_p} \tag{4.2}$$

where the V_p is the phase velocity of the wave in the substrate. In theory, the transmission line based true time delay cell has no trade-off between the time delay and bandwidth. Higher true time delay can easily be achieved with a longer transmission line. The only sacrifices are the physical dimension and the loss. Slow-wave concepts have also been introduced to address these issues [91]-[93]. However, the bandwidth is reduced when using the slow-wave structures.

Artificial Transmission Line based True Time Delay

The second one is the artificial transmission line. The elementary cells to construct an artificial transmission line are based on lumped inductors and capacitors [38]. They can be realized as a T network or a pi network as shown in Figure 4.1.

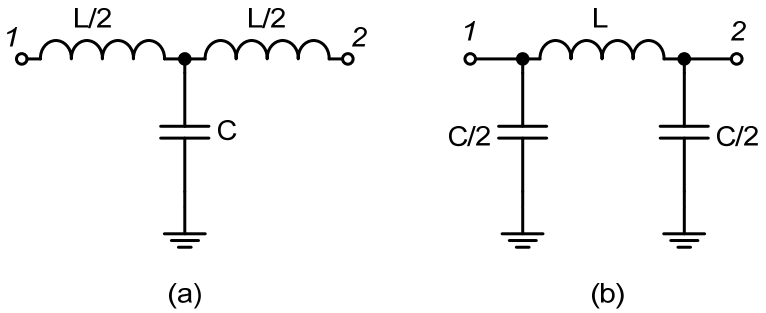

Figure 4.1. Elementary cell to construct artificial transmissin line: (a) T network (b) pi network.

The image impedance concept can be used to characterize these two types of elementary cell. The requirement is that when one port is loaded with a certain impedance Z_i, the input impedance seen at the other port is the same. With some simple algebra manipulations, the image impedance of the two types of elementary cells can be expressed as:

$$Z_{i,T} = \sqrt{\frac{L}{C}}\sqrt{\frac{4-\omega^2 LC}{4}} \tag{4.3}$$

$$Z_{i,pi} = \sqrt{\frac{L}{C}}\sqrt{\frac{4}{4-\omega^2 LC}} \tag{4.4}$$

An artificial transmission line can be realized by cascading multiple elementary cells in series. The characteristic impedance of the resulting transmission line can be defined as

$$Z_o = \sqrt{\frac{L}{C}} \tag{4.5}$$

The time delay provided by a single elemental cell is

$$\tau_o = \sqrt{LC} \tag{4.6}$$

As can be seen from equations (4.3) and (4.4), the image impedance is frequency dependent. So the characteristic impedance of the resulting transmission line given by equation (4.5) is only valid within a limited frequency range. The cut-off frequency of the artificial transmission line is the frequency where the transmission line is no longer capable to transmit power and the image impedance of the basic elemental cell becomes purely imaginary. This cut-off frequency is thus expressed as:

$$\omega_c = \frac{2}{\sqrt{LC}} \tag{4.7}$$

The image impedance of the T network and pi network are simulated with the same characteristic impedance of Z_o=50 Ω. The image impedances of the two networks are shown in Figure 4.2. It can be seen that the image impedance deviates from the DC value, which is the characteristic impedance. This means that the resulting artificial transmission line can only achieve good matching within a limited frequency range. The corresponding input return loss for the same settings are shown in Figure 4.3.

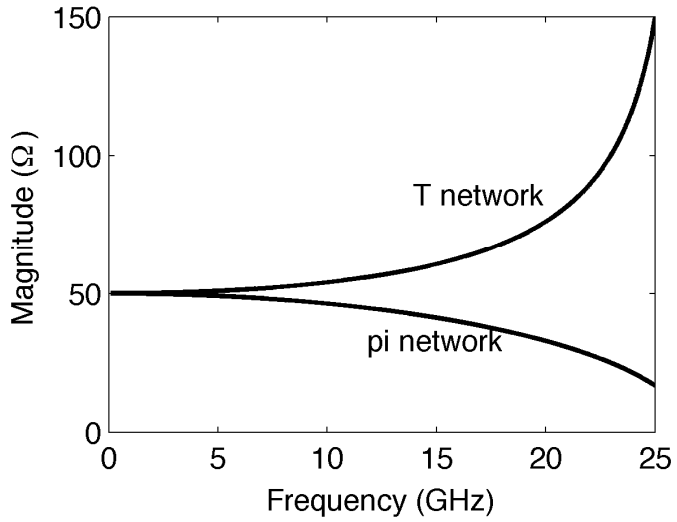

Figure 4.2. Image impedance of the two types of elementary networks with L=600 pH and Z_o=50 Ω.

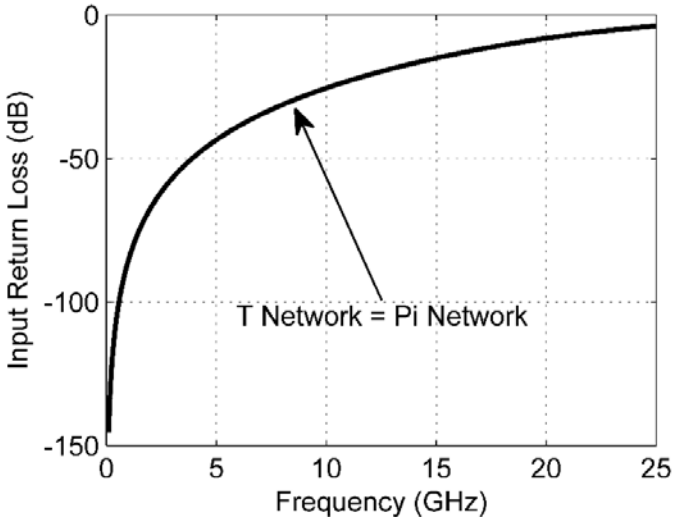

Figure 4.3. Input return loss of the two types elementary neworks with L=600 pH and Z_o=50 Ω..

Although the image impedances are different for the two types elementary networks, the resulting input return losses are the same as clearly shown by Figure 4.3. The input or output matching remains the major issue for the artificial transmission line techniques.

4.1.2 Switching Techniques

The second issue to implement the ultra-wideband true time delay chain is the switching networks. The bandwidth of the switching networks should be not less than the bandwidth of the delay chain [94]. In addition, the insertion loss introduced by the switching networks needs to be minimized to assure that the final insertion loss stays within the requirements. Even though the final insertion loss of the delay chain is high, the insertion loss of different delay states should not deviate from each other too much, because it would be much easier to compensate the whole delay chain with a single amplifier. Several

switching techniques have been reported in the literature and are briefly considered here.

Switched Topology based on SPDT Switches

The most commonly used switching technique is the switched topology using SPDT switches. The switched true time delay segment is shown in Figure 4.4. Longer delay chain is easily obtained by cascading more switched segments.

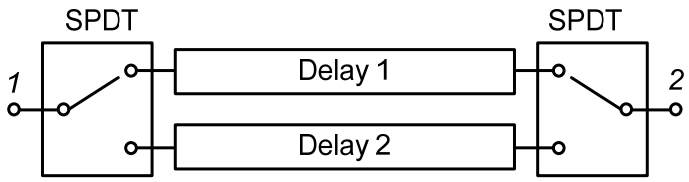

Figure 4.4. Switched true time delay segment.

The key component of the switching true time delay segment is the SPDT switches. High quality realizations with MEMs are relatively easier than the Si based versions ,[36], [95] . In CMOS, the typical SPDT realization is the series-shunt configuration which is illustrated in Figure 4.5.

The transistors work as resistors when their applied gate voltages are high, while they work as capacitors when their gate voltages are low. Normally, a larger size of the transistor corresponds to smaller “on state” resistance and larger “off state” capacitance. As a result, there is a trade-off between the loss in the “on state” and the isolation in the “off state”.

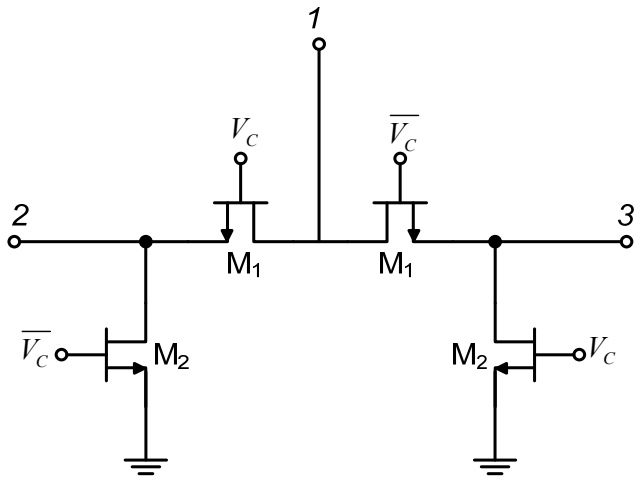

Figure 4.5. Simplified schematic of a series-shunt SPDT switch.

The switching topology also needs another delay path as its reference state. This might lead to extra chip size.

Switched Topology based on Amplifiers

Besides the SPDT switches, amplifiers can be used to fulfill the switching functions [4], [96]. The switching topology requires two types of amplifiers to fully replace the SPDT switches [37].

The first one is the single-in-double-out amplifier. This requirement can be satisfied with two cascode stages sharing the same gain transistor. A typical realization is shown in Figure 4.6.

The resistive feedback is applied at the input port via the feedback resistor R_f. The purpose is to achieve a relatively wideband input matching.

The other type of amplifier is the double-in-single-out amplifier at the output port of the switching true time delay segment. The implementation theory is similar to that of the single-in-double-out amplifier. A typical realization is

shown in Figure 4.7. The resistive feedback is applied at the two input ports 1 and 2.

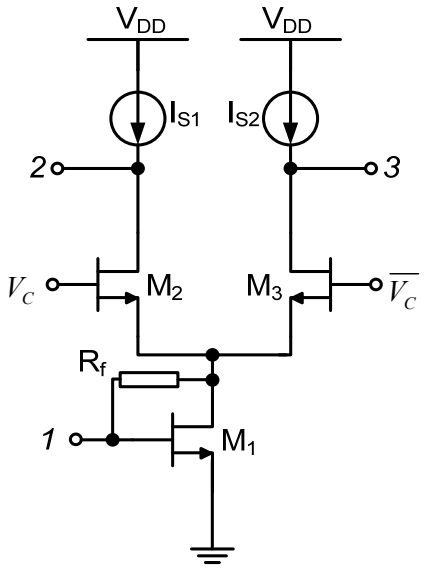

Figure 4.6. Simplified schematic of the single-in-double-out amplifier.

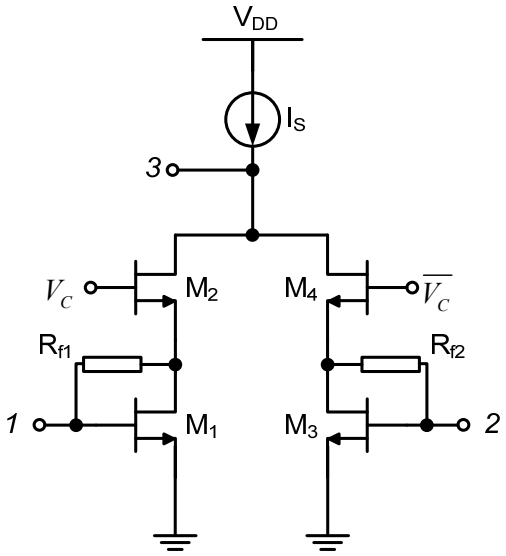

Figure 4.7. Simplified schematic of the double-in-single-out amplifier.

The major challenge of the switching amplifier is the input and output matching. Although wideband-matching techniques can be used, the effective usable bandwidth is always lower than the true time delay networks. Another

issue of the switching amplifier is the transducer gain bandwidth. This bandwidth is of minor consideration because extra amplifiers can be used for insertion loss compensation. However, the transducer gain bandwidth may result in the distortion of the final true time delay. A wider gain bandwidth will result in a more flat group delay response.

Trombone Topology

The common attribute of the previously introduced switching true time delay topology is the use of two delay paths. The actual delay of the switching delay segment shown in Figure 4.4 is the difference between the two delay paths. When more switching delay segments are cascaded, the reference paths can occupy a considerable chip area.

The trombone topology, on the other hand, uses only one reference path for all delay states [4], [17], [38]. The simplified block diagram of the trombone topology is shown in Figure 4.8.

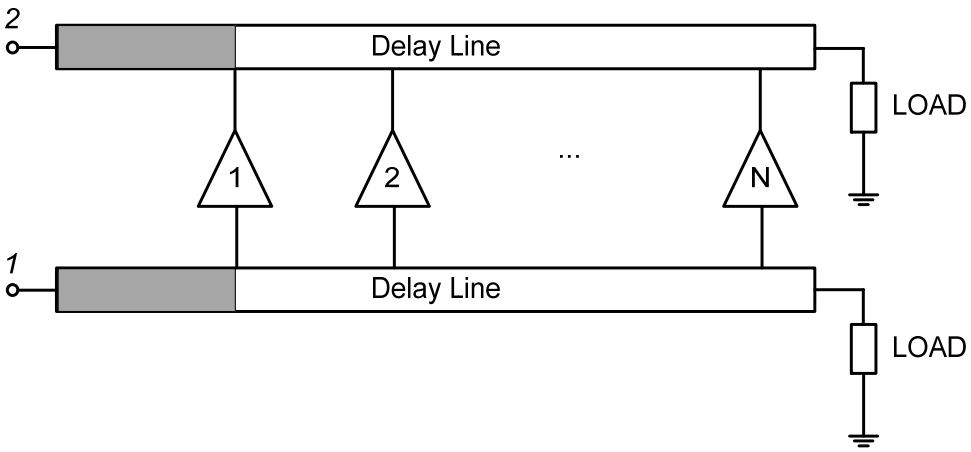

Figure 4.8. Simplified block diagram of the trombone topology.

As shown in Figure 4.8, the trombone topology consists of two delay lines and multiple switching elements (indicated with the numbered triangles). The different delay states are realized by choosing different tapping points along the two delay lines. The main merit of this configuration is that there is only one reference path for all different delay states. The reference path is shown in Figure 4.8 with shaded area. Another strength of the trombone topology is that only one switching element appears in the final signal path while there are multiple switching elements in the case of switching topologies.

However, the trombone topology requires the use of extra resistive loads. The intrinsic insertion loss of the ideal trombone topology is 3 dB.

4.1.3 Conclusion

The two major challenges of the true time delay chain have been discussed in the previous sections.

For true time delay networks, the major design consideration lies in the trade-off between the highest delay and the maximum bandwidth. Although this is not a serious challenge for the transmission line based delay network, the transmission line would occupy a very large chip area. Actually, the lack of the trade-off between the bandwidth and delay is a drawback of the transmission line. With a delay-bandwidth trade-off, like for the artificial transmission line technique, the bandwidth can be traded for a higher delay to reduce the chip area, because a practical design always has a finite bandwidth.

Then the question is how to achieve a better trade-off between the delay and bandwidth.

For the switching techniques, the trombone topology succeeds in terms of compact physical size, relatively low insertion loss and low delay distortion. The improvements can be made on the delay line design and switching element realization.

4.2 Synthesizing High Order All Pass Networks

4.2.1 Theory of Second Order All Pass Network

Although the artificial transmission line networks have been vastly used in true time delay chain design, the major drawback is the input/output matching. This is due to the frequency dependent image impedance of the fundamental T network or pi network. The drawback can be alleviated with the all pass network.

An all pass network can theoretically achieve a good input/output matching across an infinite frequency range. Different synthesizing techniques have been investigated based on transmission lines [97], [98] and lumped components [99]. They hardly generate ultra-broadband performance. The more frequently adopted is the second order APN [39], [40], which is shown in Figure 4.9(a).

The second order all pass network consists of a coupled inductor pair and two capacitors. The equivalent half circuit divided by the symmetry plane is shown in Figure 4.9(b). The analysis of the second order all pass network can be carried out with the even-odd mode characterization.

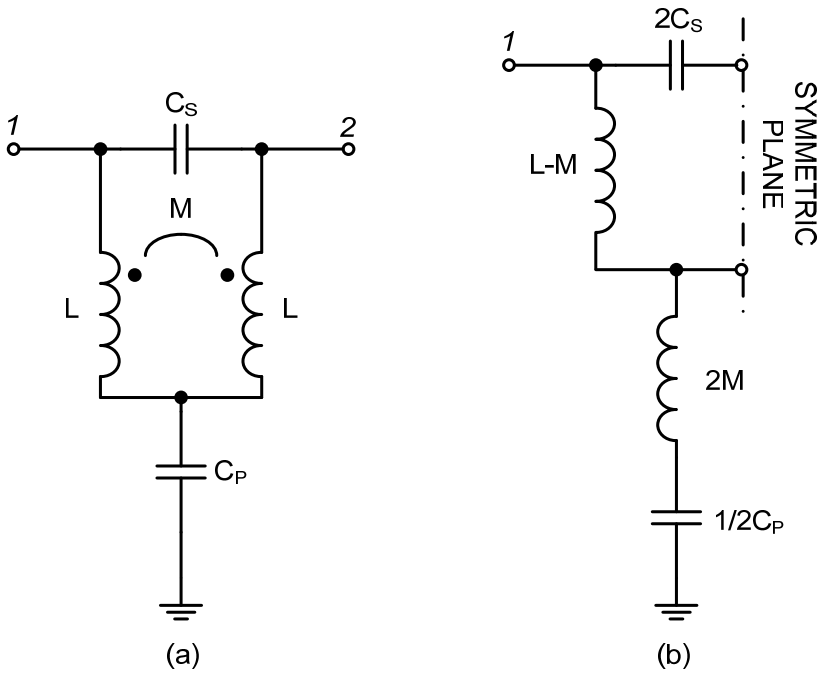

Figure 4.9. Second order all pass network: (a) schematic (b) equivalent half circuit divided by the symmetric plane.

In the even mode operation, the symmetry plane can be considered open. The even mode input impedance is thus:

$$Z_{in,e} = \frac{1-\omega^2 \frac{1}{2} C_P (L+M)}{j\omega \frac{1}{2} C_P} \tag{4.8}$$

In the odd mode operation, the symmetry plane is taken as grounded. The odd mode input impedance is then:

$$Z_{in,o} = \frac{j\omega(L-M)}{1-\omega^2 2C_S(L-M)} \tag{4.9}$$

The reflection coefficients of the two modes are then calculated by

$$\Gamma_{in,e} = \frac{Z_{in,e} - Z_o}{Z_{in,e} + Z_o} \tag{4.10}$$

$$\Gamma_{in,o} = \frac{Z_{in,o} - Z_o}{Z_{in,o} + Z_o} \tag{4.11}$$

where Z_o is the source and load impedance.

The S-parameters of the second order all pass network are

$$S_{11} = S_{22} = \frac{1}{2}(\Gamma_{in,e} + \Gamma_{in,o}) \tag{4.12}$$

$$S_{21} = S_{21} = \frac{1}{2}(\Gamma_{in,e} - \Gamma_{in,o}) \tag{4.13}$$

To achieve S_{11}=S_{22}=0, equation (4.12) leads to

$$Z_{in,e} Z_{in,o} = Z_o^2 \tag{4.14}$$

This corresponds to

$$Z_o = \sqrt{\frac{2(L-M)}{C_P}} \tag{4.15}$$

and

$$\frac{C_P(L+M)}{4C_S(L-M)} = 1 \tag{4.16}$$

The resulting transmission coefficient is

$$S_{21} = \frac{[1-\omega^2 \frac{1}{2} C_P(L+M)] - j\omega \frac{1}{2} C_P Z_o}{[1-\omega^2 \frac{1}{2} C_P(L+M)] + j\omega \frac{1}{2} C_P Z_o} \tag{4.17}$$

The insertion phase and group delay of the second order all pass network are thus

$$\Phi = 2\arctan\left(\frac{\omega \frac{1}{2} C_P Z_o}{1-\omega^2 \frac{1}{2} C_P(L+M)} \right) \tag{4.18}$$

$$\tau = -\frac{d\Phi}{d\omega} \tag{4.19}$$

To simplify the expression of the group delay, we introduce new variables:

$$\tau_o = C_P Z_o \tag{4.20}$$

$$\Omega = \omega \tau_o \tag{4.21}$$

and

$$Q = \frac{C_S}{C_P} \tag{4.22}$$

Then the final group delay can be expressed as:

$$\tau = \tau_o \frac{1 + Q\Omega^2}{1 + (1/4 - 2Q)\Omega^2 + Q^2\Omega^4} \tag{4.23}$$

The group delay response of the second order all pass network is illustrated in Figure 4.10. The delay is normalized to its DC value τ_o.

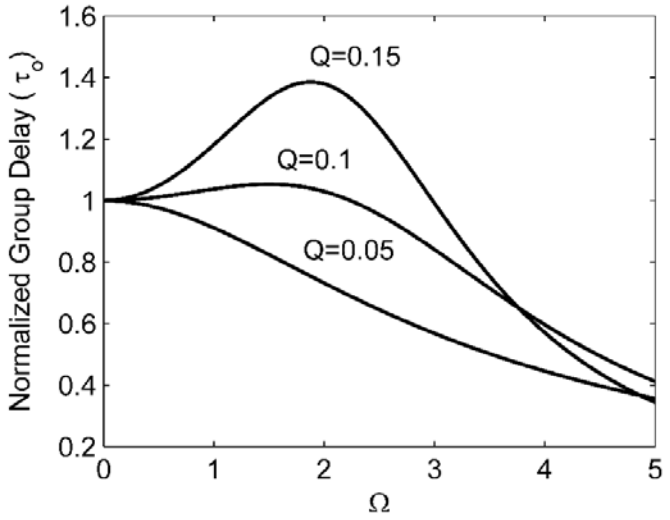

Figure 4.10. Group delay response of the second order all pass network with different Q values.

It can be seen that there is a peaking point for the group delay and this is one of the reasons that the all pass network can achieve a more flat group delay response compared to the artificial transmission line topology. The Q value affects the peaking strength of the group delay. A relatively flat group delay

requires a Q value close to 0.1. It is also observed that the usable bandwidth of the second order all pass network is lower than Ω=2. This corresponds to $\frac{2}{\tau_o}$. For example, in order to design a 20 GHz true time delay, the maximum delay achievable per all pass network is thus $\frac{1}{\pi 20GHz} \approx 16ps$.

4.2.2 CMOS Second Order All Pass Network

The key component to realize a second order all pass network is the coupled inductor. It can also be considered as a transformer with the reference node connected together. The previous section indicates that a Q value of around 0.1 corresponds to a relatively flat group delay response. According to equation (4.16) and (4.22), the transformer should have

$$\frac{(L+M)}{(L-M)} = \frac{4C_S}{C_P} = 0.4 \tag{4.24}$$

and

$$M \approx -0.43L \tag{4.25}$$

The mutual coupling factor k is thus 0.43 and it is a negative coupling.

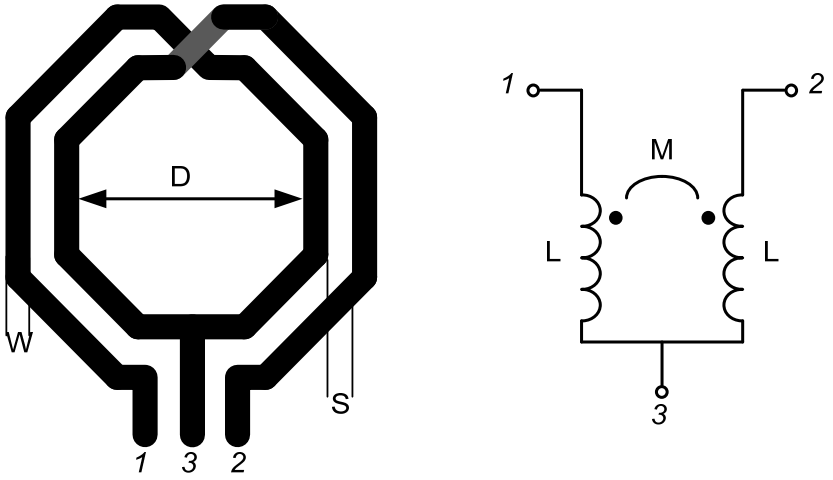

Figure 4.11. Two-turn center-tapped inductor working as a pair of negative coupled inductors.

The second order all pass network can be realized by a center-tapped inductor in CMOS process. The layout implementation and its simple equivalent lumped model are shown in Figure 4.11. The demonstrated example is a two-turn realization of center-tapped inductor. The mutual coupling is mainly controlled by the space between the metal traces S.

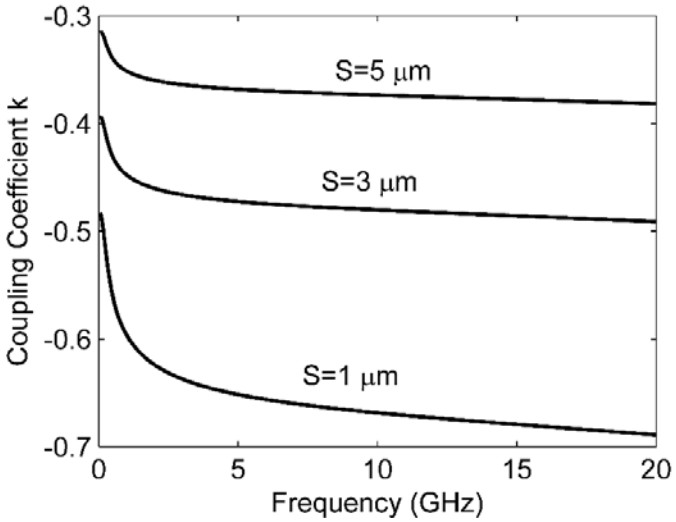

Figure 4.12. Sonnet simulation of mutual coupling coefficient with different S values at D=60 μm and W=9 μm.

The coupling coefficient k is simulated for different spacing S at a fixed D=60 μm and W=9 μm. The results are shown in Figure 4.12. The results are in accordance with the expectation: a smaller space between the traces leads to tighter coupling and a higher k. Further simulations indicate that the k is less dependent on the other two parameters D and W. With the help of equation (4.25), the desired S value is chosen to be 3 μm to achieve a flat group delay.

The bandwidth of the CMOS all pass network is thus determined by the maximum group delay obtained. With a 20 GHz highest frequency target, the maximum delay is around 16 ps.

An all pass network true time delay cell is realized in a standard 0.13 μm CMOS process as a design example. The center-tapped inductor has a dimension of D=100 μm, W=9 μm and S=3 μm. Because of the parasitics of the on-chip inductor realization, the capacitors are chosen as C_P=220 fF and C_S=20 fF. The performance of the all pass network true time delay cell is simulated with SpectreRF and shown in Figure 4.13.

The input matching of the delay cell is not infinity as in the ideal all pass network case. This is due to the parasitics of the on-chip inductor and losses. The resulting insertion loss is within 1 dB from DC to 20 GHz. The group delay achieved is flat across the whole simulated bandwidth. The obtained 16 ps delay is in accordance with the previous estimation.

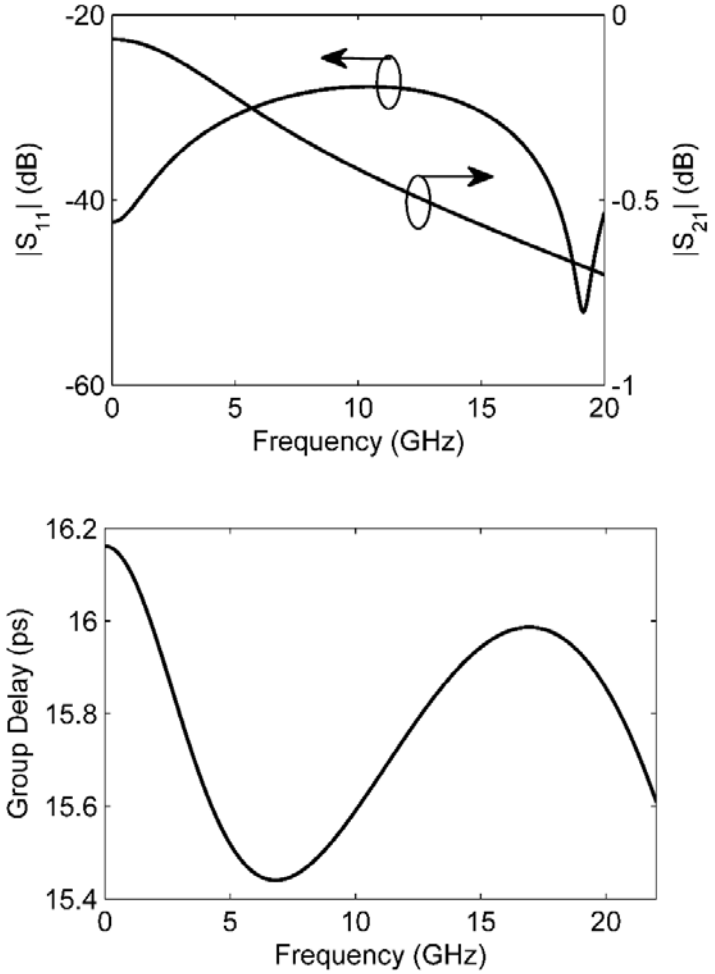

Figure 4.13. Design example of a CMOS all pass network true time delay cell.

4.2.3 Synthesizing Higher Order All Pass Network

The second order all pass network has a better efficiency than the artificial transmission line cell not only in terms of the input/output matching. The other advantage is indicated by equation (4.23). It can be seen that the group delay has a higher order low pass response which provides more degrees of freedom for designers. As the group delay response of all pass networks similar to the magnitude of low pass filters, a higher order all pass networks can result in a

more flat group delay.

General Forms of Higher Order All Pass Network

The development of higher order all pass network can be started by observing a general form of the second order all pass networks. This general form is shown in Figure 4.14. The general form is split into even and odd modes.

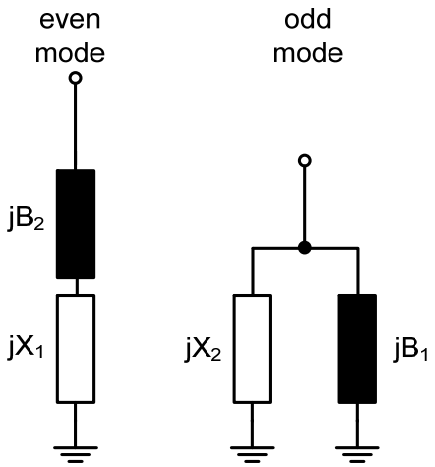

Figure 4.14. General form of the second order all pass network illustrated in even-odd mode formats.

Here component X_n stands for inductive components while B_n stands for capacitive components. The all pass response is achieved by ensuring the two networks in the even and odd mode are dual networks in terms of the characteristic impedance Z_o. For Figure 4.14 this corresponds to

$$\frac{Z_{in,e}}{Y_{in,o}} = Z_o^2 = \frac{jX_1 - j\dfrac{1}{B_2}}{jB_1 - j\dfrac{1}{X_2}} \tag{4.26}$$

which leads to

$$\frac{X_1}{B_1} = \frac{X_2}{B_2} = Z_o^2 \tag{4.27}$$

With these requirements, a third order all pass network can be easily obtained in terms of even-odd mode networks. The basic idea is to realize third order dual networks based on second order dual networks. The implementation is shown in Figure 4.15.

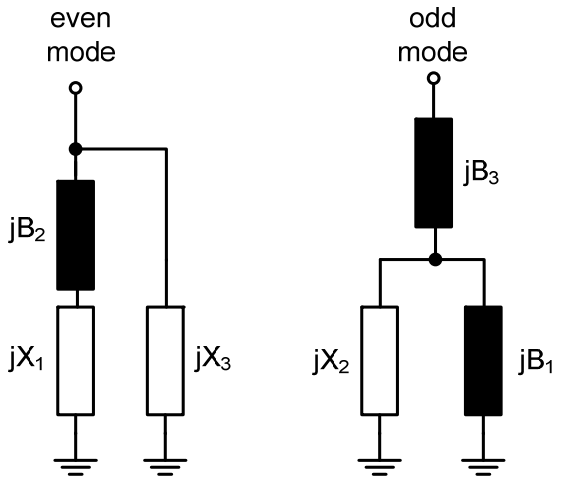

Figure 4.15. General form of the third order all pass network illustrated in even-odd mode format.

The parallel connection of an inductive component X_3 corresponds to the series connection of a capacitive component B_3. It can be easily shown that the all pass response can be obtained when

$$\frac{X_1}{B_1} = \frac{X_2}{B_2} = \frac{X_3}{B_3} = Z_o^2 \tag{4.28}$$

The same approach can be used to derive the general form of a fourth order all pass network in even and mode format as shown in Figure 4.16. And equation (4.28) can also be extended with $\frac{X_4}{B_4} = Z_o^2$.

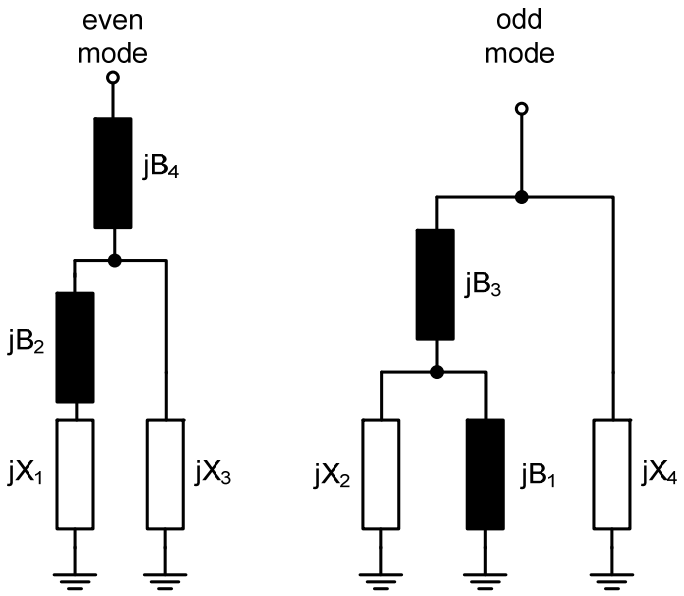

Figure 4.16. General form of the fourth order all pass network illustrated in even-odd mode format.

Further extensions can be made to realize the general forms of higher order all pass networks.

There are several points need to be noted. First of all, the subscripts of the components can be considered as the order in which it is added. For example, X_3 is added to obtain a third order response while B_4 is added for a fourth order response. Secondly, the sequence of X and B are exchangeable after the second order realization. For instance, in Figure 4.16, the even mode general form is X_1-B_2-X_3-B_4. The sequence can also be X_1-B_2-B_3-X_4 or X_1-B_2-X_3-X_4. The odd mode general form will be modified accordingly. As a result, the choice of the actual circuit arrangement can vary. The all pass response can be guaranteed as long as the general forms are satisfied with equation (4.28).

4.2.4 Design Example of Fourth Order All Pass Network

As an example, a fourth order all pass network is designed and implemented with standard PCB in this section. Figure 4.17 shows one option of the general form for the fourth order all pass network with lumped components.

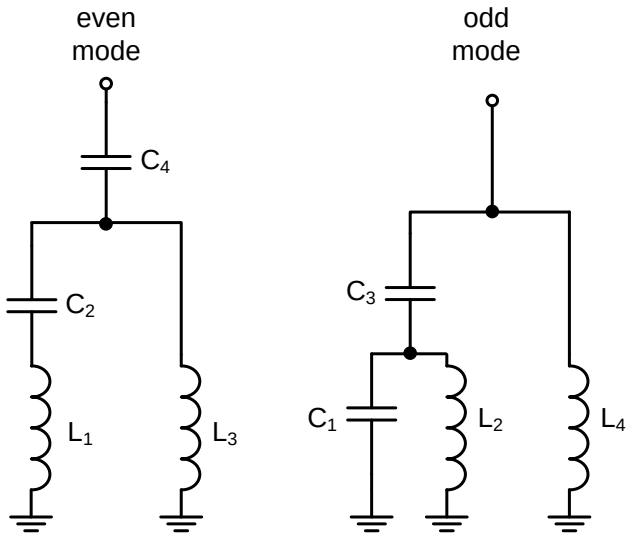

Figure 4.17. General form of the fourth order all pass network with lumped components.

As mentioned previously, the component values need to satisfy

$$\frac{L_1}{C_1} = \frac{L_2}{C_2} = \frac{L_3}{C_3} = \frac{L_4}{C_4} = Z_o^2 \tag{4.29}$$

The circuit realization for the general form can be realized with different methods. One of the options is shown in Figure 4.18.

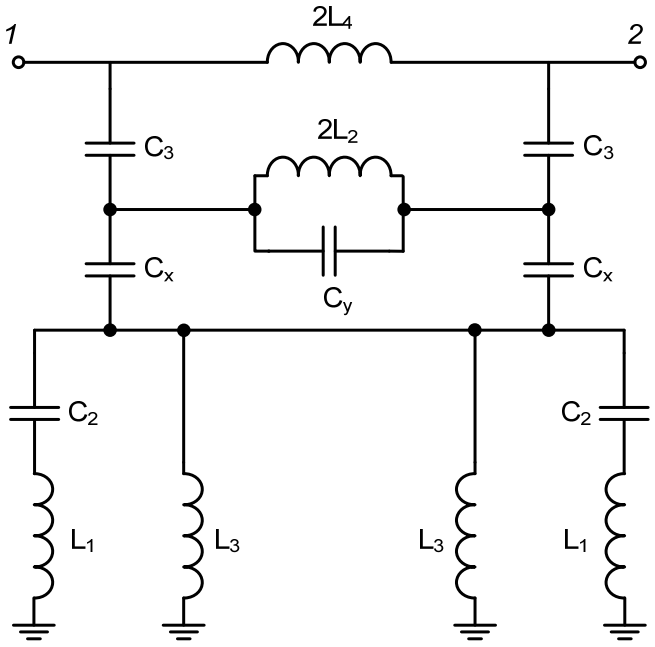

Figure 4.18. Complete schematic of the fourth order all pass network.

Except for the numbered components, there are two variable capacitors C_x and C_y. By comparing the schematic with the general form, we have

$$C_x = \frac{C_3 C_4}{C_3 - C_4} \tag{4.30}$$

$$C_y = \frac{C_1 - C_x}{2} \tag{4.31}$$

In the real discrete circuit realization, the choice of components values need to keep $C_x>0$ and thus we have a limitation of $C_3>C_4$.

The fourth order all pass networks are implemented with normal discrete components on Rogers 5330 PCB board. The fabricated PCB board is shown in Figure 4.19.

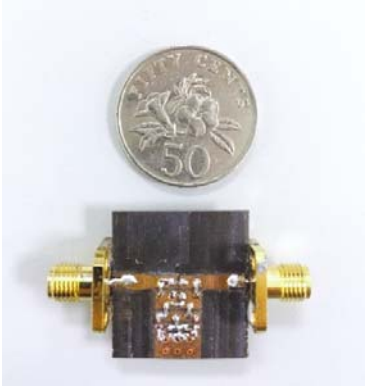

Figure 4.19. PCB implementation of the fourth order all pass network.

The all pass network is measured from DC to 10 GHz and the measured transmission and reflection coefficients are shown in Figure 4.20 and Figure 4.21, respectively. It can be seen that the "all pass" response is not ideal. This is because of two major reasons. The first reason is that the interconnections between the discrete components play a significant role. Their impact includes the loss and the parasitic capacitance and inductance. The other reason is that the parasitics of the discrete components already exist in their core parts. Not to mention the package introduced parasitics. Furthermore, the accuracy of the components values are with at least 10% error. This error can induce mismatches between the equivalent even and odd mode circuits of the resulted all pass network.

As a result, the usable bandwidth of the lumped fourth order all pass network is DC-3 GHz. The insertion loss is better than 0.2 dB and the return loss is higher than 30 dB. The group delay response is also shown in Figure 4.22. The group delay varies from 0.2 ns to 0.23 ns within the bandwidth of DC-3 GHz.

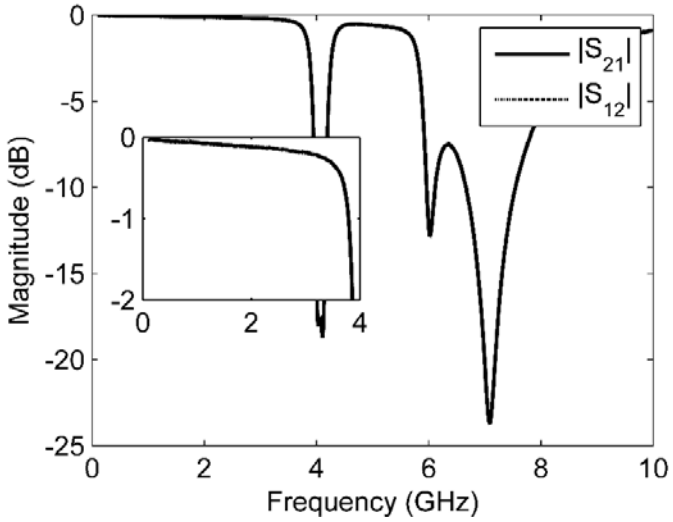

Figure 4.20. Measured transmission coefficients of the lumped element fourth order all pass network.

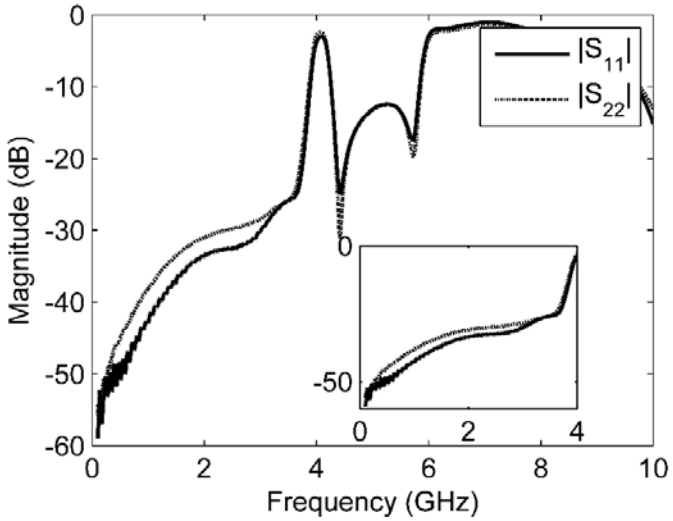

Figure 4.21. Measured reflection coefficient of the lumped element fourth order all pass network.

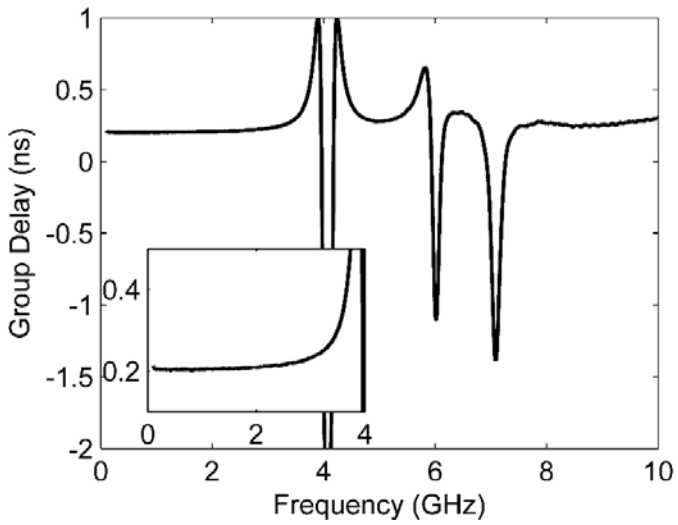

Figure 4.22. Measured group delay of the lumped element fourth order all pass network.

4.2.5 Conclusions and Recommendations

This section has provided an in-depth investigation on the all pass network.

A synthesizing approach is proposed to develop high order all pass networks. The proposed method is based on the even-odd mode analysis. A fourth order all pass network is designed as an example. The all pass network is implemented with commercial lumped elements and fabricated on a standard PCB. Due to the limitations of the PCB and discrete components, the measured all pass response is from DC to 3 GHz. The maximum insertion loss within this bandwidth is 0.2 dB and the minimum return loss is 30 dB. The single stage fourth order all pass network achieves a group delay from 0.2 ns to 0.22 ns across the bandwidth.

The major limitation of the high order all pass networks is in the realizable components values. The desired response requires negative capacitance or negative inductance values. The realization of such components needs careful analysis and the possible solutions may be investigated in more depth in the future.

4.3 3-bit All Pass Network based 1-20 GHz Switched True Time Delay with 3 dB Inter-State IL Variation

Because of their advantage of providing wideband input/output matching for the all pass networks (Figure 4.13), they are used in the multi-octave bandwidth true time delay chain design. The target bandwidth is 1-20 GHz. In order to alleviate the requirements of the gain compensation amplifier in the system, the insertion loss variation between different time delay states are kept as low as possible The total delay is set as 37.5 ps with a 5.5 ps resolution.

4.3.1 Series-Shunt SPDT Switch

In order to achieve the multi-octave bandwidth of the final true time delay chain, the SPDT switch shown in Figure 4.5 is not sufficient. Assume that the on state of the transistor can be represented with a resistor R_{on} and the off state of the transistor can be replaced with a capacitor C_{off}, the equivalent network of the SPDT with port 2 on and port 3 off is be depicted as Figure 4.23.

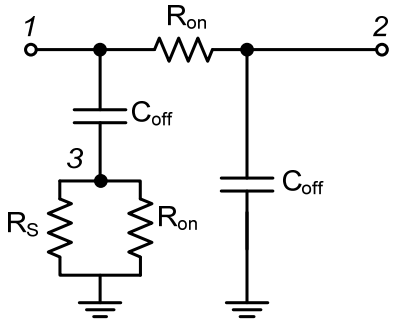

Figure 4.23. Simplified equivalent circuit of the SPDT switch with port 2 on and port 3 off.

R_S is the source resistance of the system and is 50 Ω in most cases. The

resulting network only consists of resistors and capacitors. A reasonable estimation of the bandwidth for such a network can be made by calculating the equivalent resistance seen by each of the capacitors. For the capacitor C_{off} at port 1, its loading resistance can be simplified as $\frac{R_S}{2}$; while for the capacitor C_{off} at port 2, the same results also apply. Note that we have assumed that $R_{on} << R_S$. The 3 dB bandwidth is thus estimated as

$$\omega_c \approx \frac{1}{\frac{1}{2}R_S C_{off} + \frac{1}{2}R_S C_{off}} = \frac{1}{R_S C_{off}} \tag{4.32}$$

The actual bandwidth is lower than this because of the other parasitics that have not been included in the simplified circuit. For example, R_{on} will increase the equivalent resistance seen by each capacitor and the on state capacitors are already ignored.

Another, more important, issue is the matching requirement at each of the three ports. Unlike the amplitude response, the phase response is more sensitive to the interface matching between stages. The matching condition can easily deteriorates due to the parasitic capacitors like C_{off}.

An effective solution is to add matching inductors at each port as shown Figure 4.24(a). The equivalent circuit of Figure 4.23 is then modified as shown in Figure 4.24(b).

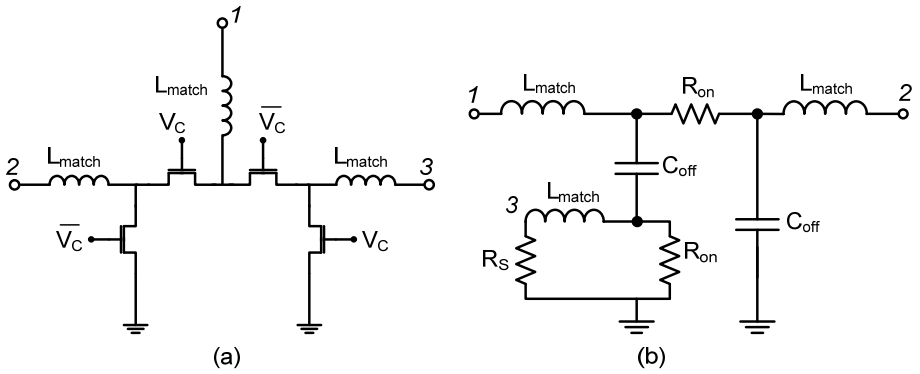

Figure 4.24. (a) Series-shunt SPDT switch with matching inductors (b) its equivalent circuit when port 2 is on and port 3 is off.

When the on state resistance R_{on} is small enough, the resulting network can be considered as a T network used for artificial transmission line realization. As can be expected, the input/output matching at port 1 and port 2 would be improved. The reflection coefficients of the SPDT with and without the matching inductors are shown in Figure 4.25.

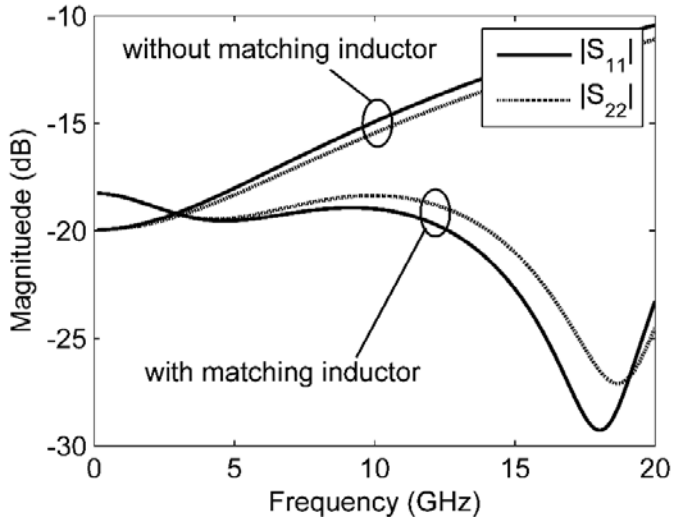

Figure 4.25. The input/output matching of the SPDT switch with and without matching inductors.

As can be seen, the matching inductors have improved the return loss for both ports at the high frequency range. This technique helps to extend the usable

bandwidth of the series-shunt SPDT switches. However, the additional three inductors increase the chip size if multiple switching delay stages are used. On the other hand, the return loss of the input and output ports are still below 10 dB at 20 GHz without the matching inductor. So the use of extra matching inductors should depend on practical requirements.

4.3.2 All Pass Network based Switched True Time Delay

Because the all pass network can achieve a good input/output matching (RL>20 dB) across the desired bandwidth of 1-20 GHz, the matching of the final switched true time delay chain would not worsen from the performance of the switches very much. As a result, the use of all pass networks can alleviate the input and output matching requirements for the series-shunt SPDT switches.

In order to maintain the insertion loss variation between different states as low as possible, both the delay paths and the reference path are realized with the all pass networks. This approach can also make it easier to obtain a small relative delay. In this 3-bit true time with 37.5 ps maximum delay, the lowest significant bit (LSB) should have a delay of 5.5 ps.

The block diagram of the LSB is shown Figure 4.26. The two all pass networks APN_1 and APN_2 are realized with the schematic of Figure 4.9. Their coupled inductors are of the same dimensions and they differ in the capacitors values.

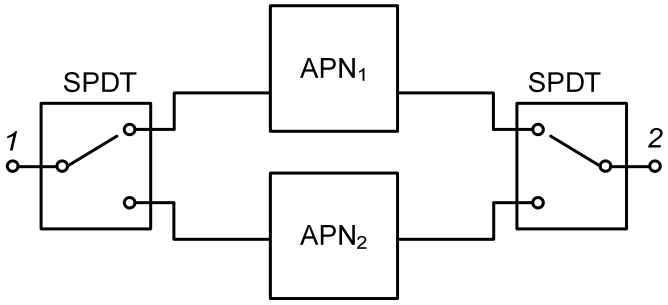

Figure 4.26. Block diagram of the LSB of the 3-bit switched true time delay.

The SPDT switches in the LSB do not include the matching inductors. The resulting input and output return loss can still be maintained above 10 dB because the good matching of the all pass networks introduce little impact on the final input and output matching.

The second bit and the most significant bit (MSB) are then constructed with the same method. All of the series-shunt switches are of the configuration shown in Figure 4.5 without matching inductors. The chip area therefore has been kept low to a very large extent.

4.3.3 Experimental Results

The 3-bit switched true time delay phase shifter is fabricated in a standard 0.13 μm CMOS process. The die photograph is shown in Figure 4.27. The core chip size is 1.6x0.5 mm^2. There are 14 inductors in total. However, if the matching inductors are used, there would be 16 more inductors. The chip size is likely to double comparing to the implementation of Figure 4.27.

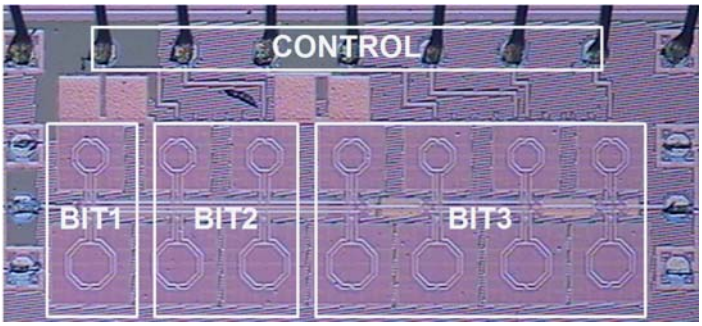

Figure 4.27. Micrograph of the 3-bit switched true time delay.

The 3-bit true time delay is characterized with on-wafer measurement. The measurement setup is shown in Figure 4.28. The chip was attached to the VNA through RF probes. Extra PCB board is used to provide the necessary DC supplies.

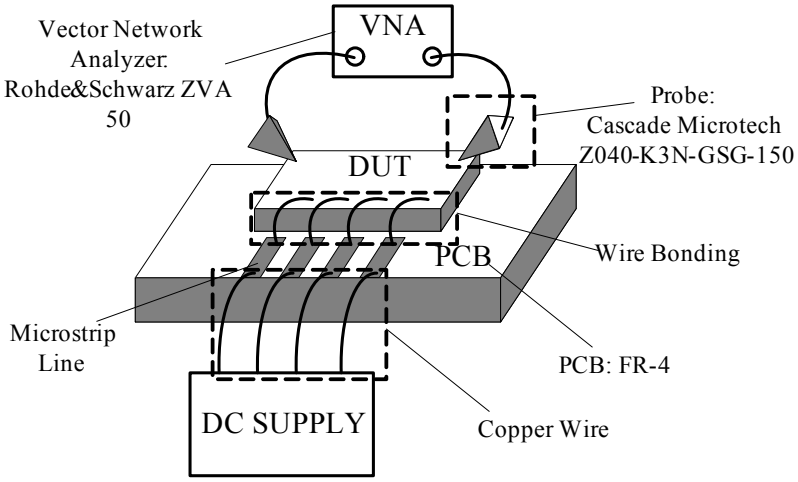

Figure 4.28 Measurement setup for the TTD measurement.

The measured input return loss is shown in Figure 4.29. The input return loss is better than 10 dB from 1 GHz up to 20 GHz.

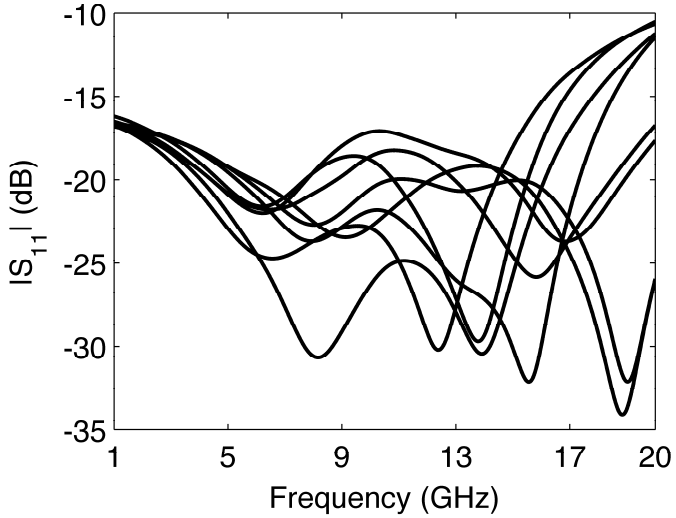

Figure 4.29. Measured reflection coefficient of the 3-bit true time delay for all 8 states.

The transmission coefficients for the 8 delay states are shown in Figure 4.30. It can be seen that the insertion loss of different states cluster together along the frequency. This is because both the delay and reference paths of the true time delay are implemented with all pass networks. The variations between different states are within 3 dB. And the maximum insertion loss is 18 dB at 20 GHz.

The phase shift for 8 states are extracted and shown in Figure 4.31. It can be seen that the phase shift between different states is proportional to the frequency. This property helps to alleviate the squint issue in wideband phased array systems.

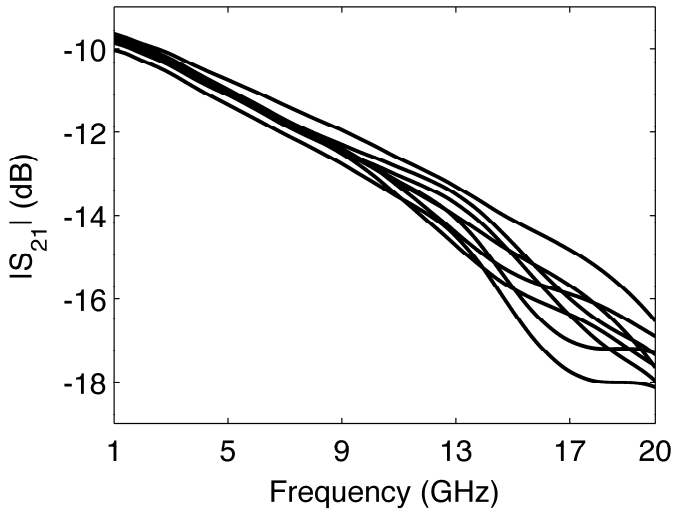

Figure 4.30. Measured transmission coefficient of the 3-bit true time delay for all 8 states.

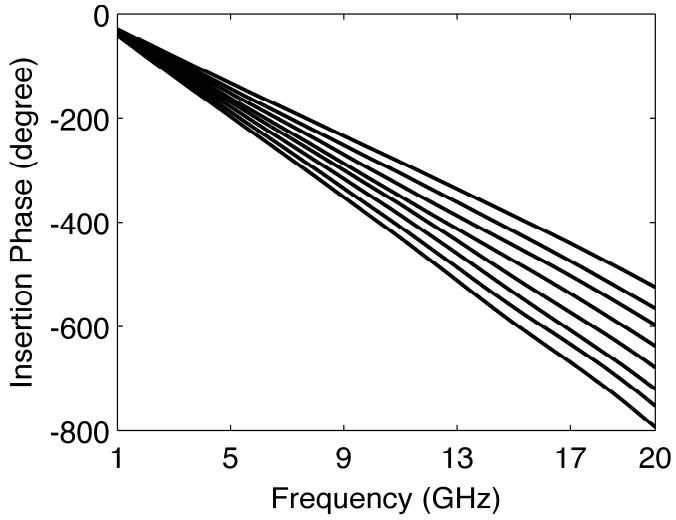

Figure 4.31. Measured phase shift of the 3-bit true time delay for all 8 states.

The phase shift of the true time delay phase shifter can also be expressed in the relative delay format. The results are shown in Figure 4.32. The delay for each state remains relatively constant across the measured frequency range of 1-20 GHz. The maximum delay of the true time delay phase shifter is 37.5 ps and the resolution is 5.5 ps.

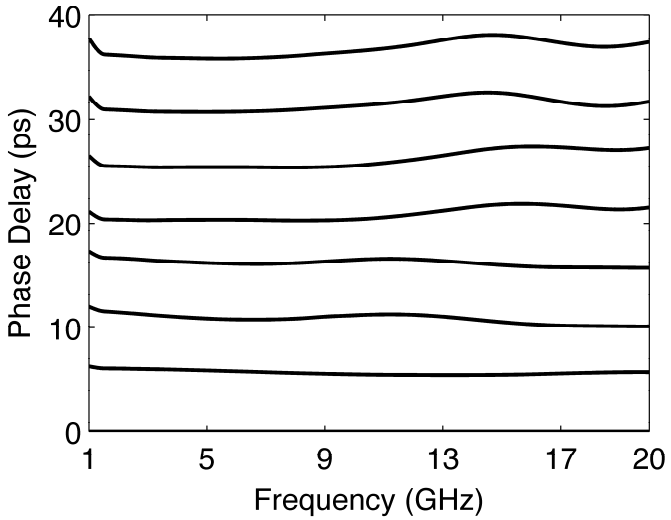

Figure 4.32. Measured relative phase delay of the 3-bit true time delay.

In order to quantitatively evaluate the phase delay accuracy of the true time delay, the phase errors for all 8 states are calculated and shown in Figure 4.33. The errors are within 10% across the measured bandwidth.

The nonlinearity of the true time delay phase shifter is also characterized. The measurement is performed at 5 GHz, 10 GHz and 15 GHz. The output referred 1 dB compression points are shown in Figure 4.34. The OP_{1dB} is decreasing with the increase of frequency. Taking into account the measured insertion loss of the true time delay, the input referred 1 dB compression point varies less.

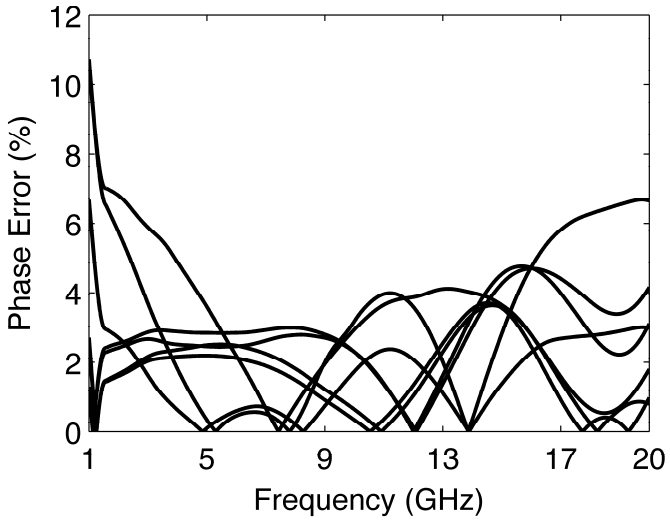

Figure 4.33. The absolution phase error of the 3-bit true time delay for all 8 states.

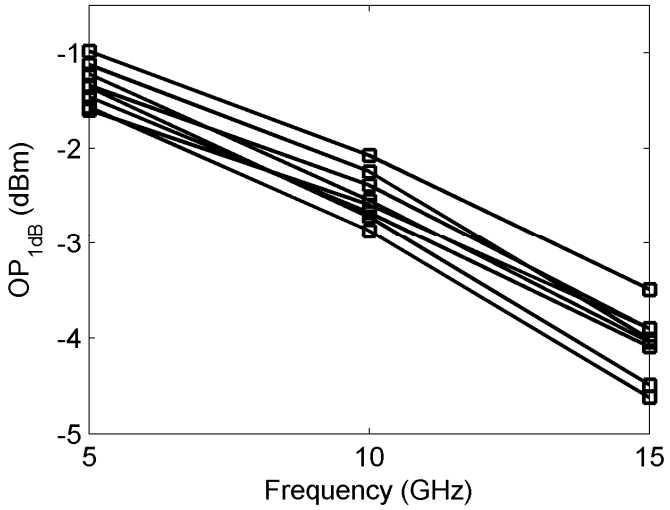

Figure 4.34. Measured output referred 1 dB compression point of the 3-bit true time delay for all 8 states.

4.3.4 Conclusion

A 3-bit true time delay phase shifter is realized with minimum insertion loss variation. The switched topology is used for different delay settings selection. Both the delay path and the reference path are implemented with all-pass-networks. The insertion loss variation is thus reduced between the two delay settings. The 3-bit true time delay phase shifter has a maximum delay of 37.5 ps with 5.5 ps delay resolution. The phase error is less than 10% from 1-20 GHz for all delay settings. The maximum insertion loss variation between different delay stats is 3 dB. The true time delay chain occupies an area of 1.6x0.5 mm^2.

4.4 3-bit 1-21 GHz True Time Delay Using All Pass Network in Trombone Topology

As mentioned previously, an advantage of the trombone topology is its short reference path because the switched topology requires the use of reference paths. This is clearer if we take a look at the 3-bit true time delay demonstrated in section 4.3. Of the 14 inductors used, 7 are in the reference paths. This means nearly half of the core chip area is used for the reference paths. If the trombone topology is used, only two inductors are needed for the reference path.

On the other hand, the design philosophy of section 4.3 is not suitable to develop true time delays with large delays. Because both the delay path and the reference path are realized with all pass networks and their delay difference is small if the insertion loss difference is required to be small.

Consequently, this section focuses on the implementation of a trombone delay chain with large delays.

4.4.1 Gate/Drain Line Based on All Pass Network

As shown in Figure 4.8, the trombone topology consists of two delay lines. With reference to the switching elements, which are usually realized with transistors, the two delay lines are called the gate line and the drain line respectively. Intrinsically, the gate line is tapped to the gate of transistors and the drain line is tapped to the drain of transistors. The signal travels from the gate line to the drain line in most cases.

Gate/Drain Line Based on Artificial Transmission Line

Conventional gate/drain lines are always realized with artificial transmission lines. The design theory is similar to that of the distributed amplifier [52] and the switching elements are implemented with transconductors. When the input and output conductance of the transconductors are considered as small, the input and output capacitances are then absorbed by the intrinsic shunt capacitance of the artificial transmission line without much negative loading effect.

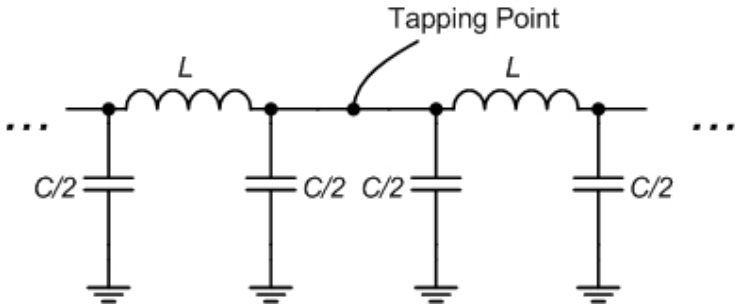

Figure 4.35. Tapping point of the pi network based on the artificial transmissin line.

The typical tapping point of the artificial transmission line is shown in Figure 4.35. The illustrated example is based on the pi network. Similar results also are obtained for the T network. In order to not degrade the properties of the artificial transmission line, the input or output capacitance of the tapping transconductor should satisfy

$$C_{in,out} \leq C \tag{4.33}$$

As the input of the transconductor is usually the gate of a transistor and the output is the drain, the input capacitance dominates the design trade off.

Because a higher transconductance corresponds to a large size of the transistor and this leads to the increase of the input capacitance. In addition, the parasitic shunt capacitance of the on-ship inductors also contribute to the artificial transmission line. Therefore the value of the shunt capacitance C is further limited. For example, in the work of [4], the available shunt capacitance budget for the switching amplifier is 12 fF for a 15 GHz bandwidth application.

On the other hand, the limited value of the shunt capacitance C makes the artificial transmission line sensitive to the parasitic capacitance of the circuit. These parasitics can come from the interconnections for signal routing and the parasitics of the capacitors themselves.

Gate/Drain Line Based on All Pass Network

It is noted in section 4.2.2 that the shunt capacitance C_P of the CMOS second order all pass network is much higher than the shunt capacitance of the artificial transmission line with the same bandwidth. It is thus attractive to investigate the possibility to allocate the tapping point at this shunt capacitor as shown in Figure 4.36. The node voltages are denoted at each node. The voltage $V_{tapping}$ at the tapping point is of major interest. The even-odd mode analysis can be carried out to obtain the tapping node voltage. In the even mode, the node voltages V_1 and V_2 can be split into two even mode voltages $\frac{V_1 + V_2}{2}$ at the two ports of the APN. While in the odd mode, the node

voltages V_1 and V_2 can be split into odd mode voltages $\frac{V_1 - V_2}{2}$ and $-\frac{V_1 - V_2}{2}$ at the two ports respectively. However, it is easily seen that only the even mode can induce the tapping voltage $V_{tapping}$. The equivalent model to calculate $V_{tapping}$ is shown in Figure 4.37.

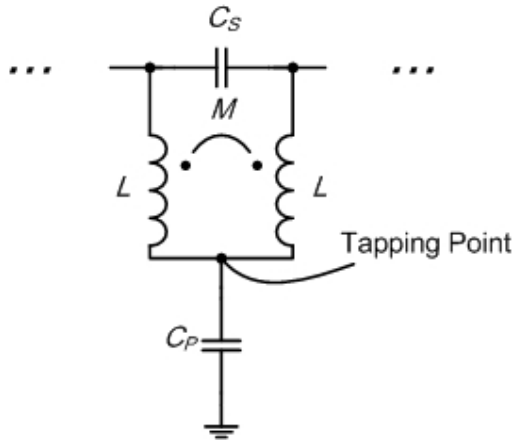

Figure 4.36. Tapping point of the all pass network based gate/drain line.

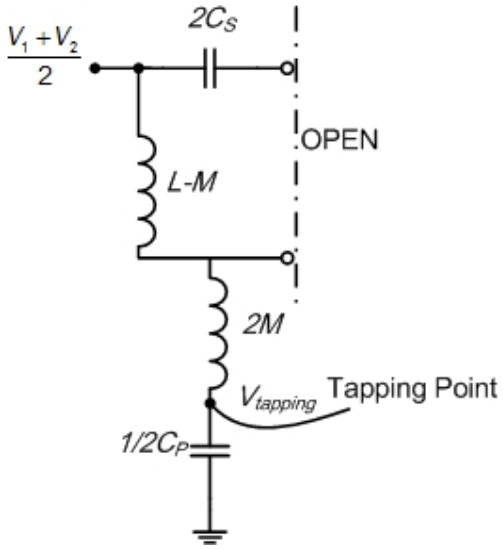

Figure 4.37. Circuit to calculate the tapping voltage in the even mode.

Then $V_{tapping}$ is expressed as equation (4.34). With the design equations (4.15)-(4.22), the first term HS_1 can be further simplified as equation (4.35).

$$V_{taping} = HS_1 \frac{V_1 + V_2}{2} \tag{4.34}$$

$$HS_1 = \frac{1}{1 - \omega^2 \frac{1}{2} C_P (L + M)} = \frac{1}{1 - \omega^2 Q \tau_o^2} \tag{4.35}$$

In the lossless case, the voltages V_1 and V_2 at the two ports of the APN should have the same amplitude but with a phase difference of θ. So we have the second term expressed as

$$HS_2 = |V_1| \frac{1}{2}(1 + e^{j\theta}) \tag{4.36}$$

With the help of (4.18), the phase difference between V_1 and V_2 can be also simplified as

$$\theta = 2 \arctan\left(\frac{\frac{1}{2}\omega\tau_o}{1 - \omega^2 Q \tau_o^2}\right) \tag{4.37}$$

The first term HS_1 has a transfer pole at $\omega_p = \frac{1}{\sqrt{Q}} \frac{1}{\tau_o}$. The amplitude of the first term increases when the operating frequency is below this pole. It can be seen the position of the pole is well above the usable bandwidth of the all pass network $\frac{2}{\tau_o}$ because the Q is usually chosen as around 0.1. So the first term keeps increasing within the bandwidth of interest.

The amplitude response of the second term HS_s is more complicated. However, it is easy to see that the amplitude of HS_2 continues dropping with the increase of frequency before θ increase to 180°. The frequency at which $|HS_2|$ drops half is:

$$\theta(\omega_{1/2}) = \arccos(-\frac{1}{2}) = 120^\circ \tag{4.38}$$

The estimated time delay at 20 GHz with 120^{o} phase shift is around 16.6 ps. Which is the maximum delay that can be achieved with 20 GHz bandwidth. This indicates that the second term introduces 6 dB amplitude degrade at the highest design frequency. However, this amplitude drop can be compensated partially by the first term. The amplitude response of those transfer-functions HS_1, HS_2 and $HS=HS_1HS_2$ are simulated. The example all pass network is designed to have the maximum delay of 16.6 ps for the 20 GHz bandwidth. The results are shown in Figure 4.38. It can be seen that the response for $|HS_1|$ and $|HS_2|$ are in consistence with the previous analysis. The net effects of the two terms introduce less than 2 dB deterioration for the amplitude of $V_{tapping}$ compared to the signal level along the delay line ($|V_1|$). While for the artificial transmission line based delay line, there is no such an amplitude degrade. However, considering the better matching performance and the higher achievable time delay, the all pass network based delay line is chosen to realize the gate/drain line for the trombone true time delay chain.

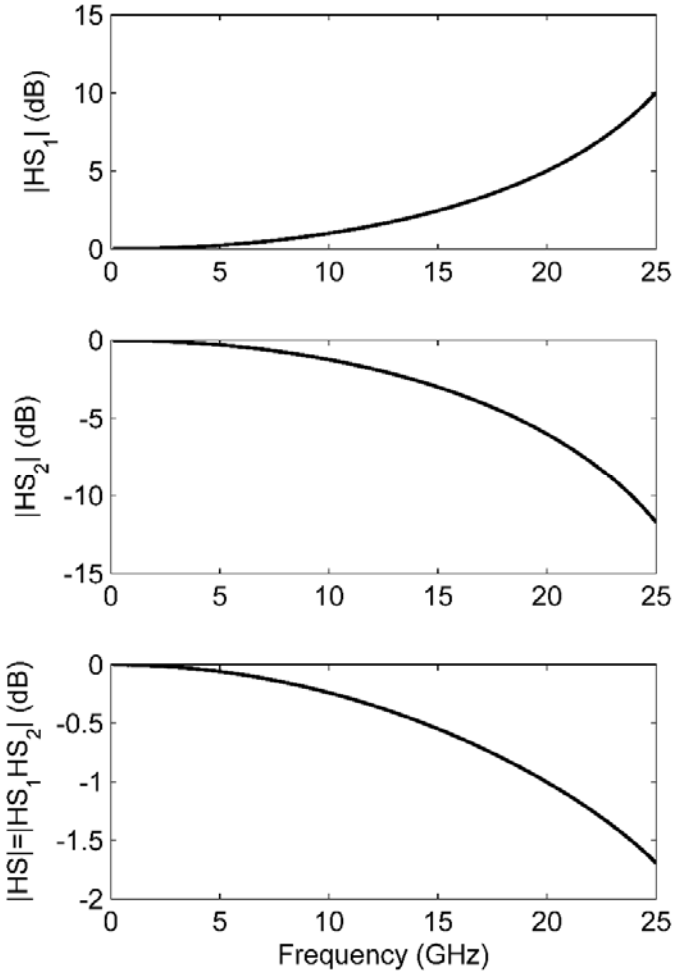

Figure 4.38. Amplitude response of the transfer function for the taping voltage with 17 ps group delay.

4.4.2 Implementation of the 3-bit Trombone True Time Delay

The gate and drain lines of the 3-bit trombone true time delay chain are implemented with the previous introduced all pass network. The switching element is realized with a single stage cascode transconductor and its simplified schematic is shown in Figure 4.39.

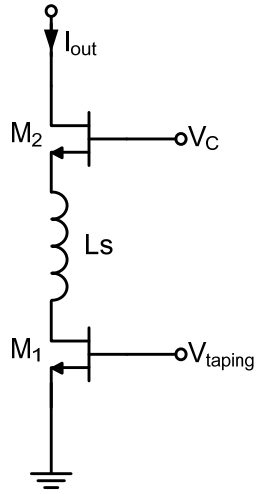

Figure 4.39. Simplified schmatic of the switching transconductor with inductance peaking.

The cascode structure advantages in its high output impedance. The loading effects of such switching transconductor is thus reduced. The extra inductor Ls acts as a peaking inductance to reduce the insertion loss variation across the frequency. The complete structure of the 3-bit trombone true time delay is illustrated in Figure 4.40. The gate/drain line consists of 8 stages of all pass networks to facilitate the 3-bit function. The switching transconductors for each cell are differently sized to minimize the insertion loss variations between different states.

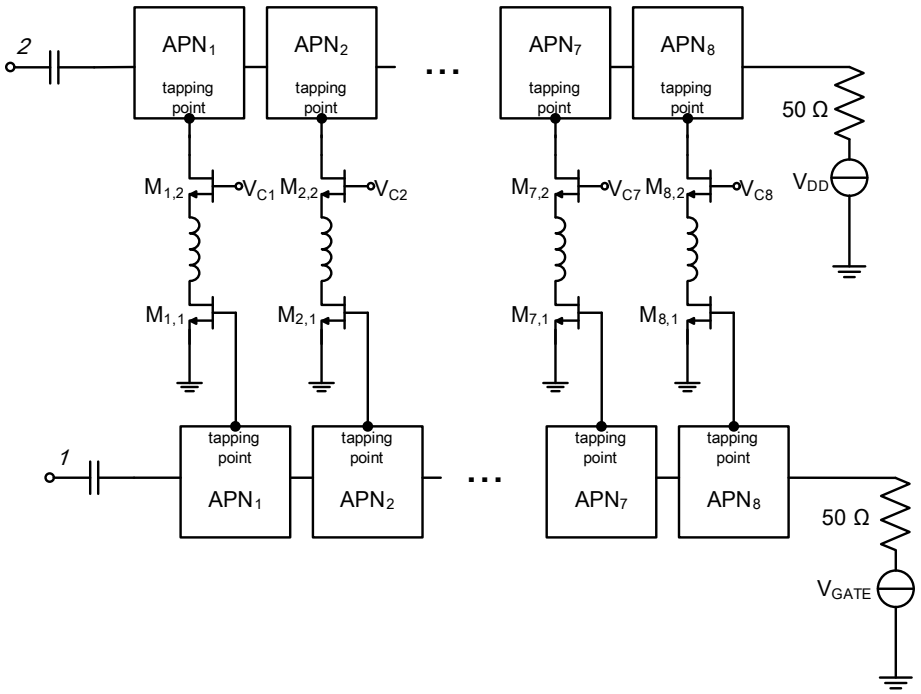

Figure 4.40. Complete structure of the 3-bit trombone true time delay.

4.4.3 Measurement Results

The trombone delay chain is fabricated in a standard 0.13 μm CMOS process. The layout is shown in Figure 4.41.

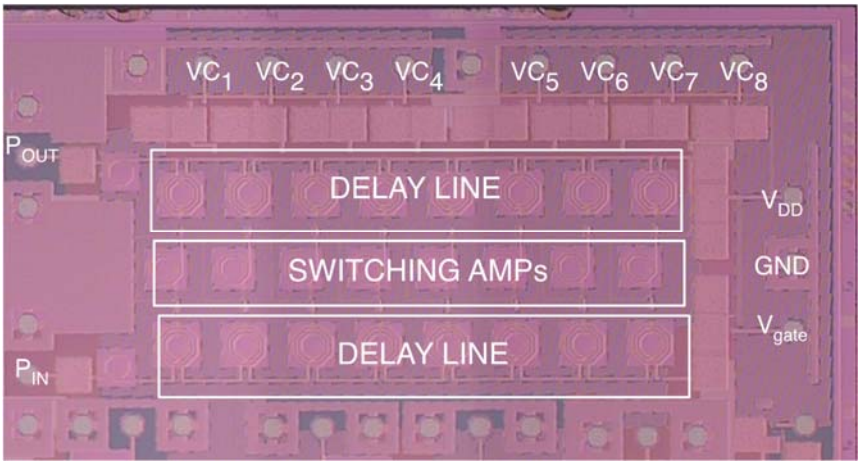

Figure 4.41. Micrograph of the fabricaed 3-bit trombone true time delay.

The 3-bit delay chain occupies an area of 2000x730 μm^2 excluding the pads.

Eight control voltages V_{C1}-V_{C8} are used to switch the delay chain through the 8 different delay states. The delay chain consumes a current from 1.66 mA to 5.19 mA for the all eight states. The biasing voltage is 1.2 V.

The 3-bit trombone true time delay characterized with cooperated simulation by Cadence and Sonnet. The interconnections of the layout are carefully considered with EM simulations.

The measured input and output matching is shown in Figure 4.42. It can be seen the input and output return loss is better than 12 dB from 1 GHz to 21 GHz. This can be attributed to the well matched property of the all pass networks used.

The transmission coefficient is shown in Figure 4.43. The worst insertion loss is 27 dB at 21 GHz which occurs in the maximum delay state. This is because the maximum delay state involves the most number of all pass networks. The inter-state variation is within 7.5 dB across 1-21 GHz. This is achieved by the differently sized switching transconductors for each state.

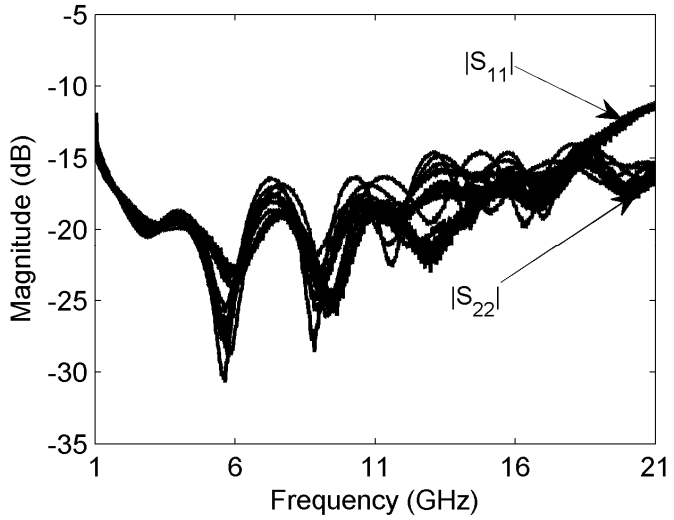

Figure 4.42. Measured input/output matching of the 3-bit trombone true time delay.

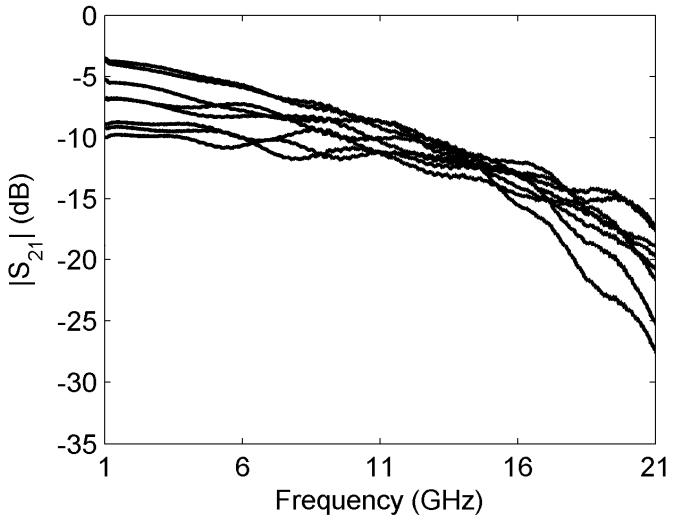

Figure 4.43. Measured transmission coefficient of the 3-bit trombone true time delay.

The phase delay performance of the 3-bit delay chain is shown in Figure 4.44. The maximum relative delay obtained is 276 ps and the resolution is 39 ps. The high delay can also be attributed to the good delay efficiency of the all pass networks. The absolute phase delay error are calculated and shown in Figure 4.45. The delay errors for all states across the whole bandwidth is within 6%.

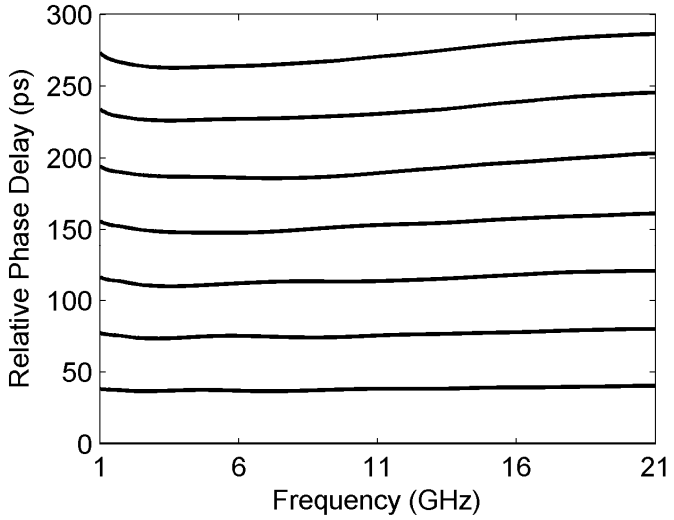

Figure 4.44. Measured phase delay of the 3-bit trombone true time delay.

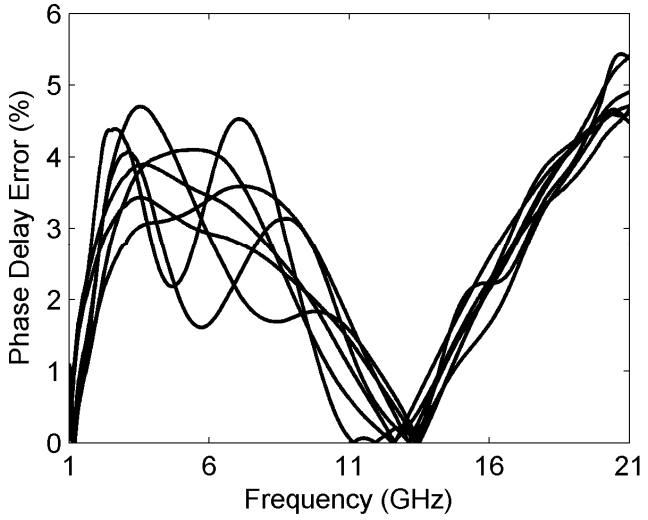

Figure 4.45. Measured phase delay error of the 3-bit trombone true time delay.

The group delays of the 8 delay states are also measured. The results are shown in Figure 4.46. The group delay indicates the distortion of the wideband signal travelling through the 3-bit trombone true time delay chain. The group delay for higher delay settings maintain as flat across the whole bandwidth. However, ripples occur in the low delay settings. Because at the front part of the gate/drain lines, the loading effects of the remaining parts of

the lines are more obvious.

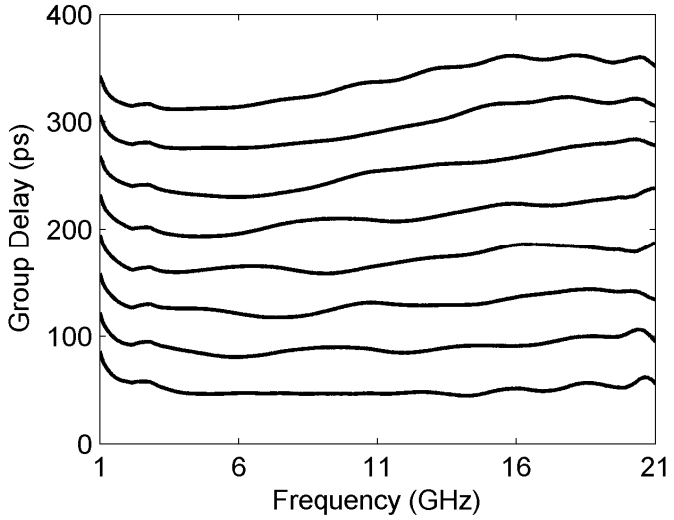

Figure 4.46. Measured group delay of the 3-bit trombone true time delay.

4.4.4 Conclusion

This section demonstrates the implementation of a 3-bit trombone true time delay using second order all pass networks. The true time delay obtained a bandwidth of 1-21 GHz. The input return loss is better than 12 dB which is one of the best reported performances. The highest insertion loss is for the highest delay state and is 27 dB at 21 GHz. The inter-state insertion loss variation is within 7.5 dB. The maximum delay is 276 ps which is the highest delay value that have been reported with a single trombone topology. The phase delay error is within ±6% for all the 8 delay states across the whole bandwidth. The core part of 3-bit trombone true time delay occupies an area of 2000x730 μm^2 and the power consumption varies from 2 mW to 6.3 mW at a 1.2 V supply for the different delay states.

4.5 1-20 GHz True Time Delay Chain with 400 ps Delay and Continuous Tuning

The previous two sections have demonstrated the true time delay realized with switched scheme and trombone topology respectively. As has been illustrated and concluded, the two switching methods have their own advantages and drawbacks.

The switched 3-bit true time delay resulted in a 37.5 ps delay with a 18 dB insertion loss while the 3-bit trombone delay resulted in a 276 ps delay with an insertion loss of 25 dB. The efficiency of the trombone structure in terms of delay per dB is much higher than the switched topology. However, we also notice that the resolution of the trombone structure is in conflict with its maximum delay value. This means a higher maximum delay of the trombone leads to a low resolution if the same number of stages are used. While the resolution of the switched scheme can be arbitrarily small because it is controlled by the difference between the two delay paths.

Consequently, the combination of the two structure can help to obtain a more comprehensive performance for the true time delay. With this idea, a true time delay chain with 400 ps delay and continuous tuning property is implemented in this section. The simplified block diagram of the true time delay chain is shown in Figure 4.47. The coarse tuning of the delay chain is provided by the 10 states trombone delay line generating 360 ps delay with 40 ps resolution. The 3-bit switched delay line covers the mid-range of the whole delay chain

with 40 ps delay. A continuous tuning network facilitates the delay chain to seamlessly cover the 400 ps delay values.

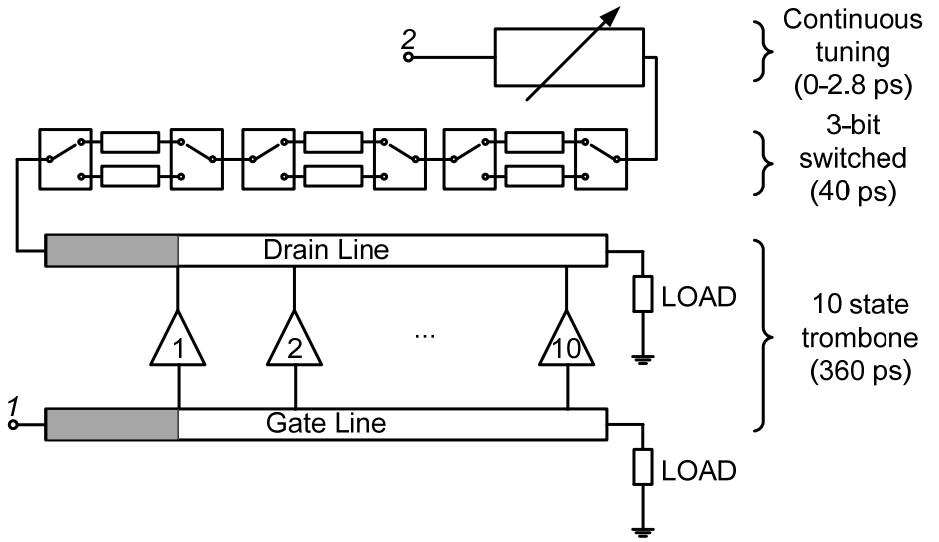

Figure 4.47. Simplified block diagram of the 400 ps true time delay chain with continuous tuning.

4.5.1 Coarse Tuning by Trombone Delay with 360 ps Delay

As the high delay is the advantage of the trombone structure, the coarse delay part of the whole true time delay chain is realized with a 10-state trombone delay. The design theory is the same as introduced in 4.4. The 8-state trombone in 4.4 is extended to 10-state.

4.5.2 Continuous Tuning with All Pass Network

As has been shown in equation (4.20), the delay of the second order all pass network is determined by the shunt capacitance C_P. The continuous tuning can thus be achieved by using varactors for those shunt capacitors. However, the tuning range is limited. Because the other components are linked to those

shunt capacitors through input and output matching condition. In order to extend the delay tuning range to cover the required delay space of 0-5 ps, three stages of second all pass networks are cascaded. The structure is shown in Figure 4.48. The shunt capacitors are implemented with MOS varactors and the capacitors C_C are for AC ground.

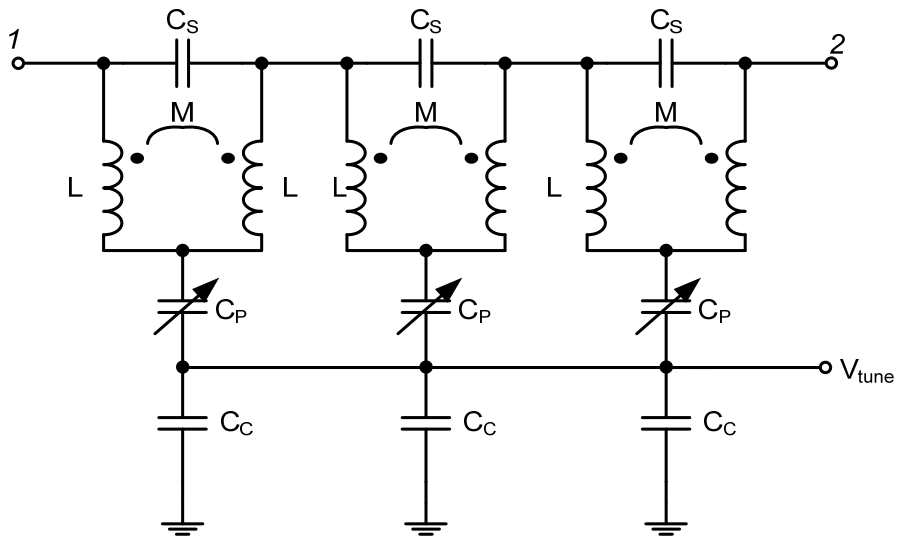

Figure 4.48. Group delay continuous tuning with three cascaded second order all pass networks.

The capacitance tuning range of the on-chip MOS varactor is around an octave. When applied into the continuous tuning stage, the simulated group delay tuning performance is shown in Figure 4.49. The obtained tuning range is higher than 5 ps. The reflection and transmission coefficients for the continuous tuning stage in different states are also simulated and shown in Figure 4.50. It can be seen that the input return loss can be maintained better than 18 dB and the insertion loss variation is within 0.3 dB. The dip of the S_{11} occurs with the optimum biasing voltage of the varactor in which case the

equivalent capacitance best satisfies the equation (4.15). The same results can hardly be achieved with the artificial transmission line based techniques.

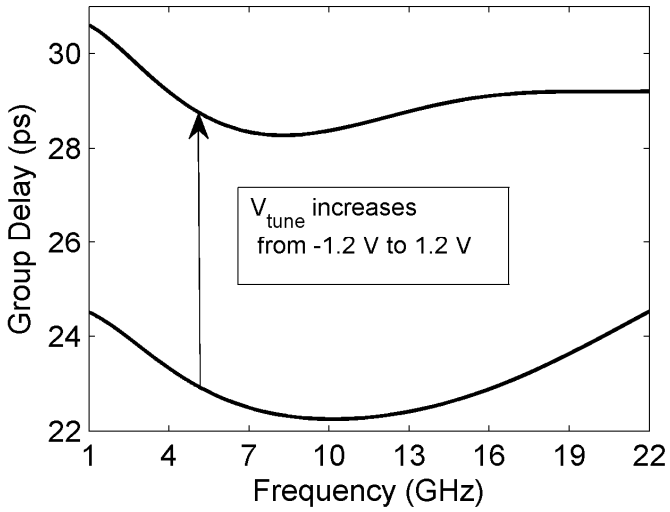

Figure 4.49. SpectreRF simulation of the group delay continuous tuning range of the continuous tuning stage.

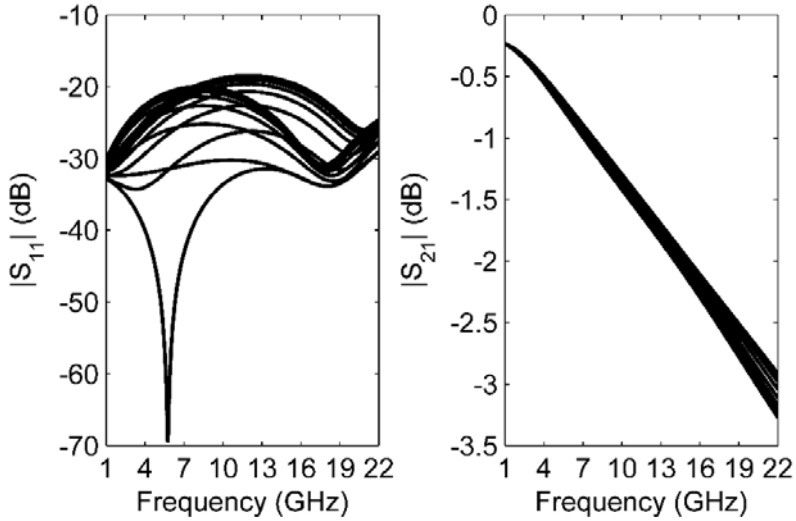

Figure 4.50. Simulated input matching and forward transmissin coefficient variations for the continuous tuning stage.

4.5.3 Measurement Results

The 400 ps true time delay chain is fabricated in a standard 0.13 μm CMOS.

The micrograph of the whole chip is shown in

Figure 4.51.

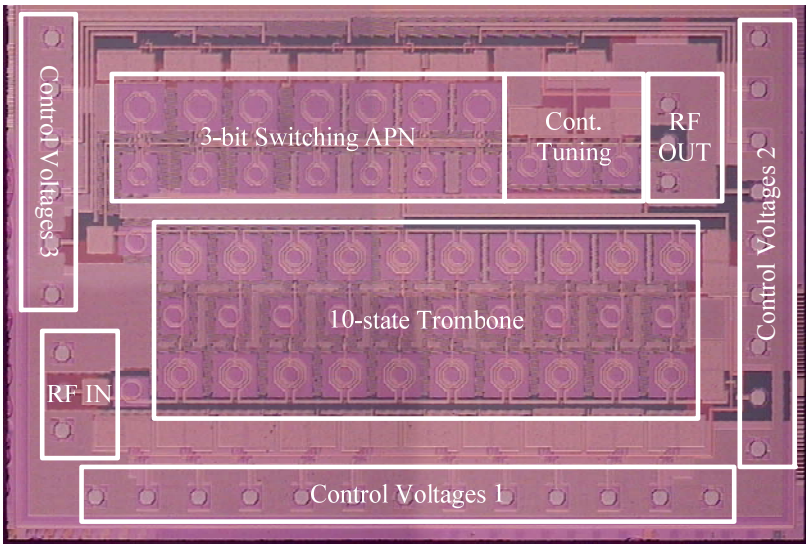

Figure 4.51. Micrograph of the 400 ps true time delay chain.

The whole chip including the pads occupies an area of 3x1.8 mm^2. The actual functional part is smaller. The purpose is to satisfy the design of rules check for the fabrication requirement. The supply voltage of the chip is 1.2 V and the only power consuming part is the trombone coarse tuning stage. The power consumption varies from 2 mW to 6.5 mW.

80 discrete states of the true time delay chain was measured. The picture of the measurement setup is shown in Figure 4.52.

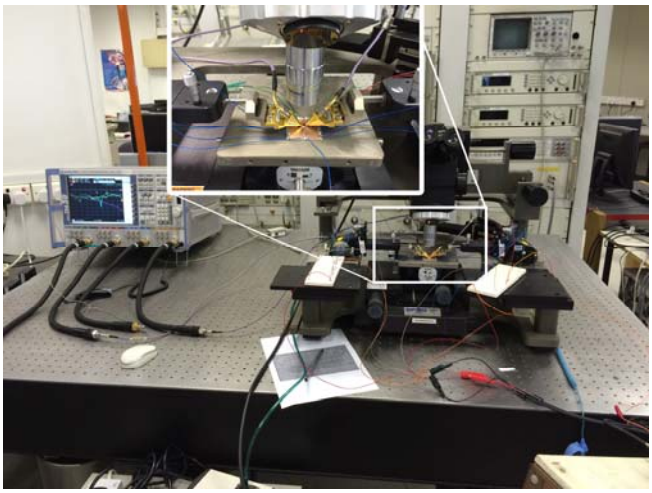

Figure 4.52. Picture of the measurement setup of the TTD.

The measured input and output matching are shown in Figure 4.53 and Figure 4.54. It can be seen that the return loss are kept below 13 dB across the measured 1-20 GHz range. This can be attributed to the all pass network based configuration of the true time delay chain.

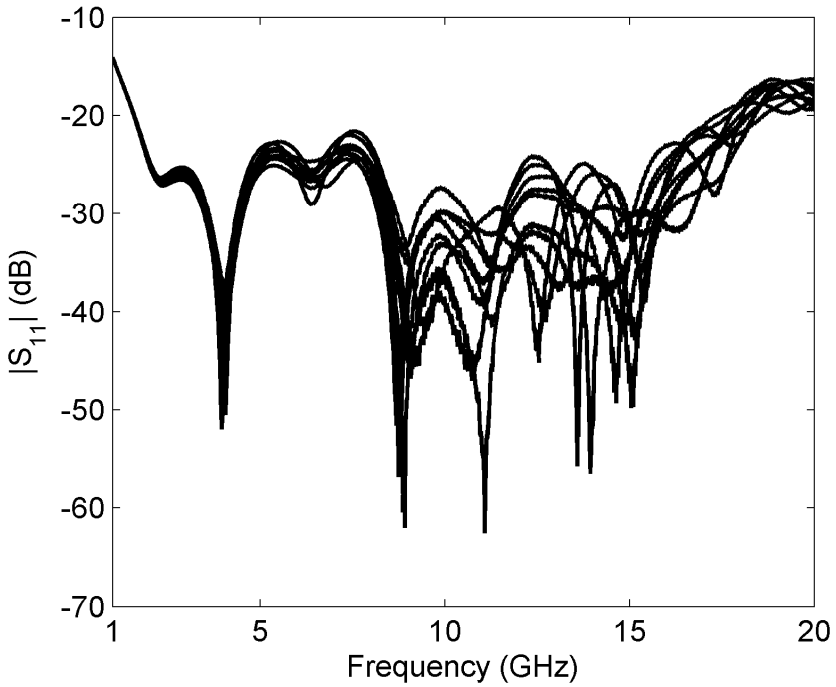

Figure 4.53. Measured input port matching of the true time delay chain.

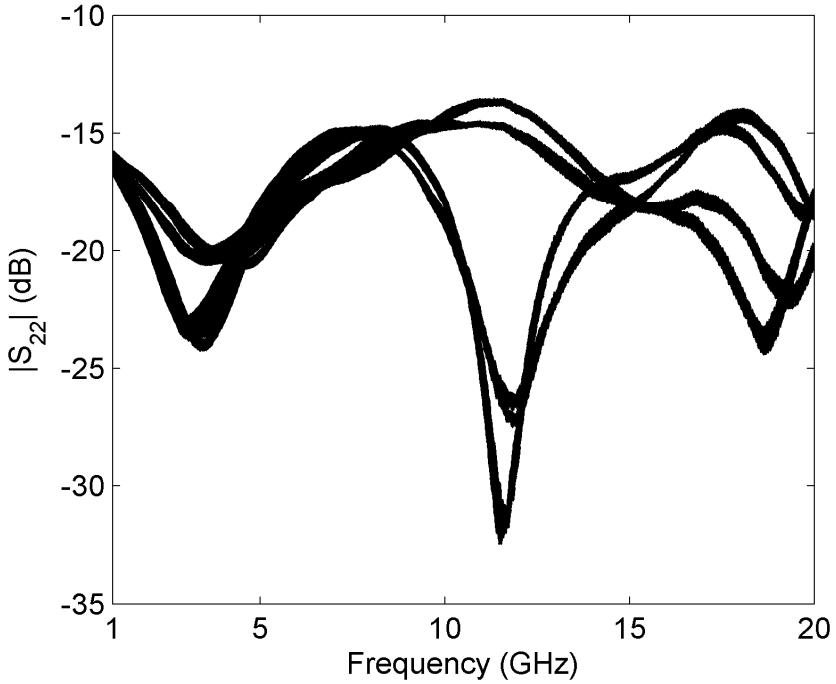

Figure 4.54. Measured output port matching of the true time delay chain.

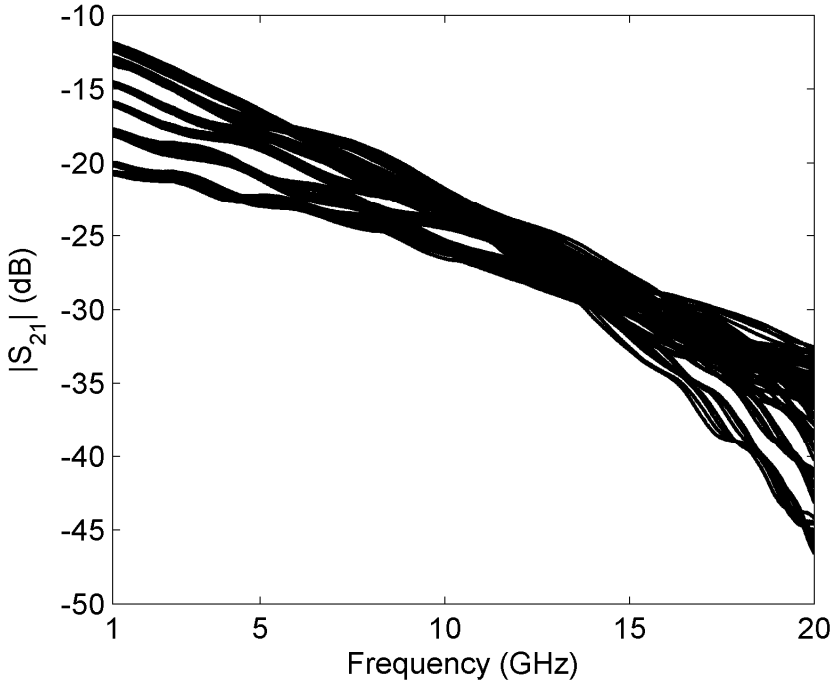

Figure 4.55. Measured forward transmission coefficient of the true time delay chain.

The forward transmission coefficient is shown in Figure 4.55. The maximum insertion loss is 45 dB at 20 GHz. The inter-state IL variation is below 10 dB. The insertion phase shift of the 80 states are shown in Figure 4.56. Straight phase shift with frequency is observed for all the states. The relative phase delay is then calculated and shown in Figure 4.57. The maximum relative delay is 400 ps. The group delay performance of the true time delay chain is also measured. As shown in Figure 4.58, distortions are observed. The mismatches between stages are the major reasons for the ripples in the group delay.

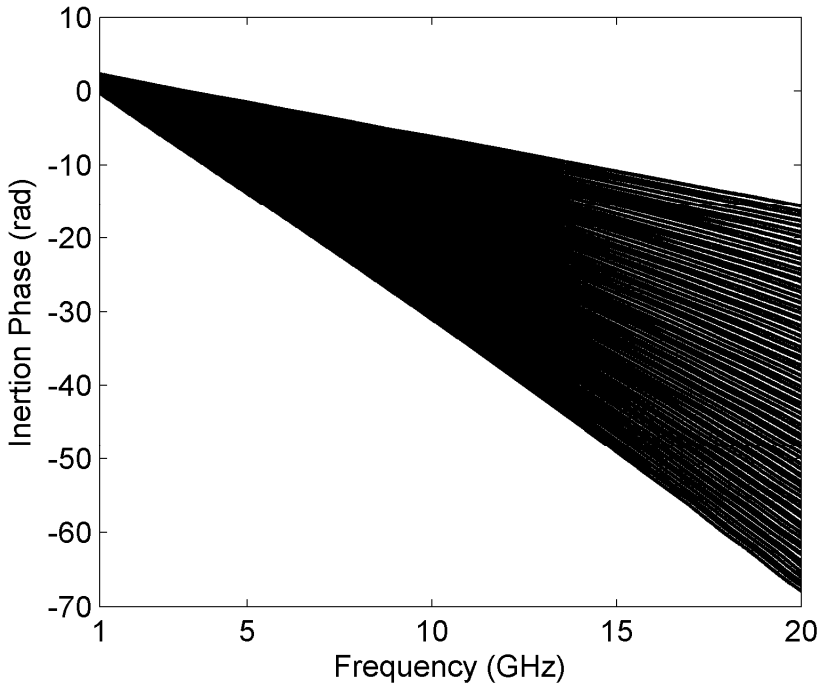

Figure 4.56. Measured phase shift of the true time delay chain.

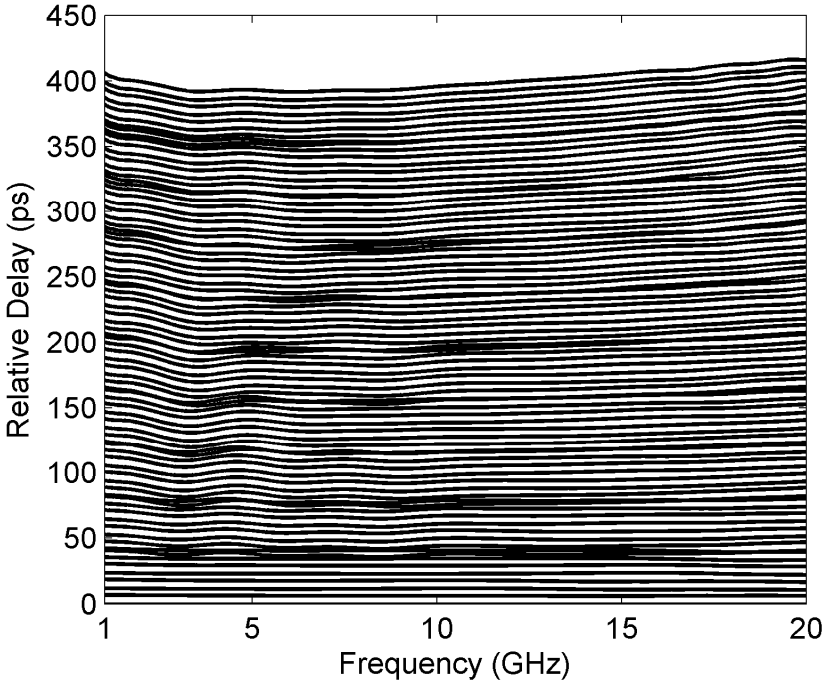

Figure 4.57. Measured phase delay of the true time delay chain.

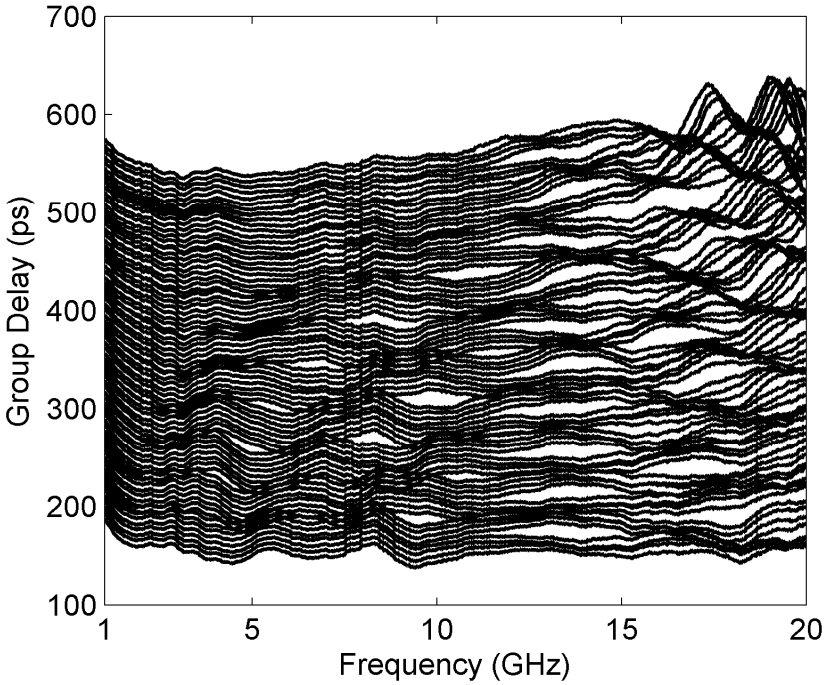

Figure 4.58. Measured group delay of the true time delay chain.

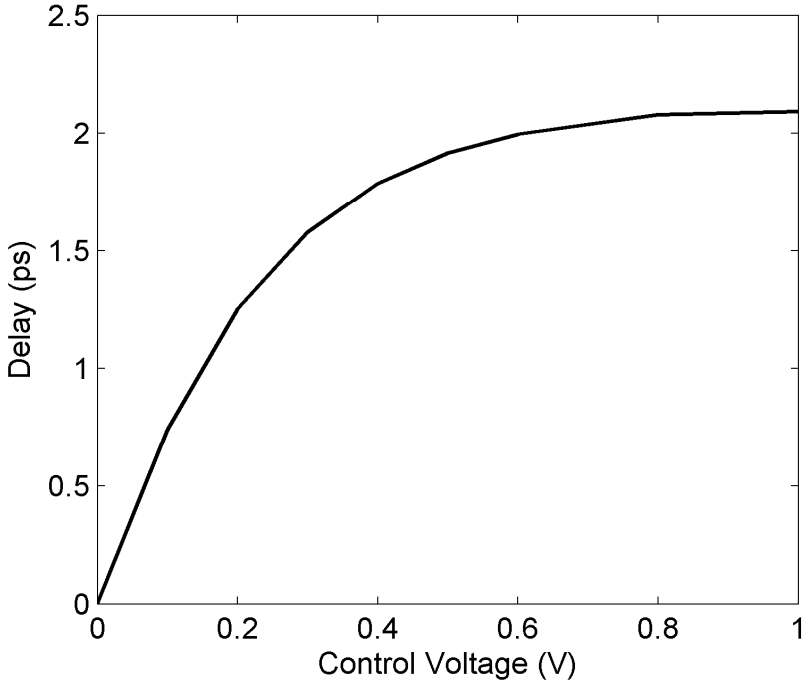

Figure 4.59. Continuous tuning property of the TTD.

The continuous tuning property of the TTD is shown in Figure 4.59. The control voltage of the continuous tuning stage is from 0 V to 1 V. The measured tuning range is 0-2.0 ps. This is different from the simulated value. The major reason is the parasitic capacitance of the continuous tuning stage is larger than expected. Another reason might be that the capacitance variance range of the varactor is smaller than the simulated value due to the inaccuracy of the model. The tuning range can be extended by cascading more stages of continuous tuning APNs shown in Figure 4.48.

4.5.4 Conclusion

This section combines the design of the switched delay line topology (section 4.3) and the trombone topology (section 4.4) to implement a multi-octave bandwidth true time delay chain with very high delay values. Additional continuous tuning stage is added to achieve a continuous tuning delay. The final chip generates a delay of 400 ps. Both of the input and output return loss is better than 13 dB. The inter-state IL variation is within 10 dB.

The relative delay of the TTD remains flat across the measured bandwidth of 1-20 GHz. The main discrepancy between the measurement and the simulation is the continuous tuning property. A tuning range of 0-2.8 ps is obtained in the simulation while the measured results show a tuning range of 0-2 ps. The major reason is the parasitic capacitance of the continuous tuning stage is larger than expected. Another reason might be that the capacitance variance range of the varactor is smaller than the simulated value due to the inaccuracy of the model. The tuning range can be extended by cascading more stages of continuous tuning APNs shown in Figure 4.48.

4.6 Conclusions and Recommendations

This chapter aims to implement TTD chain with high delay, high resolution and compact size at the same time.

The second order APN is adopted as the fundamental delay cell. Its high order group delay response helps to achieve a better delay/size efficiency compared to the artificial transmission line based delay chain.

The advantages of the switched topology and trombone topology are combined together to balance between the highest delay and resolution. Additional continuous tuning stages are used to obtain a seamless coverage in the delay domain.

However, the insertion loss performance is of minor consideration in the scope of this thesis. The most challenging point is the insertion loss slope. Take a simple delay cell, the transmission line, as an example. The transmission coefficient of a lossy transmission line with length L can be written as

$$H = e^{-(\alpha + j\beta)L} = e^{-\alpha L} e^{-j\beta L} \tag{4.39}$$

The second term $e^{-j\beta L}$ accounts for the inserted delay that is desired. The accompanied first term $e^{-\alpha L}$ is the insertion loss. Usually, the loss constant α is frequency dependant and it will induce a frequency dependant insertion loss response. As a lemma, with a lossy process (or method), the generation of a flat group delay will introduce a frequency dependant insertion loss. The only method to conquer such lemma is to use a lossless approach. A typical

example is [100], where the power is translated into voltage domain and g_m-C structures are adopted to provide the "lossless" characteristic. Bandwidth limitation remains the main drawback of such approach as a higher order all-pass response is difficult to realize.

Extra broadband amplifiers are needed for the insertion loss compensation. The most promising candidate is the distributed amplifier structure [101] as the additional introduced group delay distortion would be minimum than other wideband techniques. Another direction might be to integrate amplification stages into the delay chain itself. However, the group delay distortion should be carefully considered.

4.7 Performance Summary of the TTDs

The performances of the TTDs proposed in this thesis are compared with some works in the literature and some of their key parameters are shown in Table 4-. The largest bandwidth is provided with TL based delay cell [35]. This is because the TL does not have the trade-off between the maximum delay and bandwidth. The major drawback is the size. In addition, the quality of the TLs is heavily affected by the switching components. The work of [35] uses high quality MEMS switches to reduce this impact. However, this is not easy to achieve in standard CMOS process. This might be one of the reasons why there are few works that implement TL based TTDs in CMOS.

It is also seen that most of the TTDs presented in the literature are based on ATLs. The achieved maximum delay is relatively small. Although [37] obtains a higher delay, its small bandwidth is a result of the trade-off between maximum delay and bandwidth. On the other hand, as shown by [39], the APN based solutions can provide relatively large delays and wide bandwidth simultaneously. However, more APN based design examples cannot be found in CMOS. And the self-switched technique of [39] is not suitable for CMOS implementation because it requires high quality switching transistors. Note that the TTDs of [102] and [100], though, can be considered as APN based technique, their active realization introduces severe bandwidth limitations. This can cancel the advantages of the intrinsic all-pass response.

Another observation is that the trombone-type switching scheme is mostly

adopted in CMOS [4], [17], [38]. This is partially because that the transistor-based switches in CMOS generally have higher loss and their bandwidths are limited. The other reason might be that the trombone-type configuration can save more chip size than other passive configurations.

The major drawback of the trombone based TTDs is the delay resolution. Without using continuous tuning stage, [4] achieves a resolution of 4 ps. This is because [4] used small delay segments to construct the gate/drain lines and the input capacitance of the tapping transistor is limited within 12 fF . However is difficult to implement similar circuits in a standard CMOS process.

As a result, this thesis investigates different switching schemes to realize TTDs in standard CMOS. The designs make use of the intrinsic advantages of the APNs. The larges bandwidth and the highest delay are both achieved in the final implementation from this thesis (section 4.5). However, we also note that the uncompensated insertion losses of the proposed TTDs remain high. Additional power consumption is required if power compensation is needed.

TABLE 4-1 SUMMARY OF TTDS

	[39]	[35]	[4]	[38]	[102]	[37]	[100]	[17]	TTD of section 4.3	TTD of section 4.4	TTD of section 4.5
Technology	0.2 μm PHEMT	MEMS	0.18 μm SiGe	0.18 μm CMOS	0.8 μm SiGe	0.13 μm CMOS	0.14 μm CMOS	0.13 μm CMOS	0.13 μm CMOS	0.13 μm CMOS	0.13 μm CMOS
Technique	Self-switched APN	Switched TL	VGA+Trombone on ATL	VGA+Trombone on ATL	Active APN	Switched Amp on ATL	G_m-RC	Trombone on ATL	Switched APN	Trombone on APN	Trombone/ Switched APN
Frequency Range (GHz)	2-20	0-40	1-13	1-15	3-10	3-5	1-2.5	15-40	1-20	2-22	1-20
Maximum Delay (ps)	145	87	64	75	25	255	550	42	37.5	276	400
Resolution (ps)	2.16	5.8	4	15	Cont.	Cont.	14	6	5.5	39	2.8
Maximum Gain (dB)	-5	-1.6	10	13.5	-2.3	18.5	15	-13	-10	-2.5	-10
Minimum Gain (dB)	-25	-5.1	5	4.5	-6.5	16.5	N.A.	-14	-18	-25	-45
Return Loss (dB)	N.A.	>15	>11	>9	>1.5	>10	>15	>10	>10	>17	>13
Average IP_{1dB} (dBm)	N.A.	N.A.	-24	-16	-1	N.A.	-21	N.A.	10	2	2
P_{DC} per Channel (mW)	Passive	Passive	87.5	138	38.8	34.2	90	8.6/24.6	Passive	2/6.3	2/6.5
Size (mm^2)	N.A.	30	2.25	2.48	0.42	N.A.	N.A.	0.99	0.8	1.46	5.4

Chapter 5 Conclusion and Future Work

5.1 Conclusions

This thesis focuses on the CMOS realizations of two key building blocks for the ultra-wideband phased array system.

The first one is the ultra-wideband BPF. Pure active implementations of high selectivity BPFs with octave bandwidth are presented. Two design approaches are proposed. The first method is based on the active inductors. Both active shunt and series inductors are investigated. So the bandwidth limitations of active inductor based BPFs are alleviated. The second approach for active BPF design proposed is based on the gyrator-resonator. The proposed gyrator-resonator has a more flexibility in its tuning property. The resulted BPF achieves very high out-of-band rejection as well. Both of the two design techniques lead to the compact realizations of high selectivity BPFs in CMOS and they provide a possible direction for the integration of miniature phased array systems.

The second block is the ultra-wideband true-time-delay based phase shifter. The objective is to obtain high delay, high resolution and compact size. The application is for integrated ultra-wideband phased array that requires wide sweeping angle. The true-time-delay phase shifter is based on the second order all-pass-network. Which has a high order group delay response that can lead to a better delay/bandwidth efficiency compared to transmission lines and

artificial transmission lines. Different switching techniques are adopted in the final design to balance between maximum delay and resolution. An extra continuous delay cell is added for a seamless coverage of the tuning range.

5.2 Future Work

The author also notes that there is some more issues that can be investigated for the two building blocks discussed in the thesis.

5.2.1 Ultra-Broadband Active BPFs

Three possible topics can be further investigated for the active BPFs.

Noise

The noise performance of the active BPFs plays a significant role in the conventional receivers [103]. The effective noise figure (*NF*) of a cascaded stages can be given by [104]

$$F_{effective} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots \frac{F_N - 1}{\prod G_m} \tag{5.1}$$

Equation (5.1) indicates that the *NF* of the cascaded stages is mainly determined by the first stage if it provides sufficient gain (G_1). Thus, an extra low noise amplifier added before the active BPF can help to lower the total effective *NF*. The desirable LNA can also facilitate a single-ended to differential conversion as the proposed active BPFs are in differential configuration. The LNA presented in [105] achieves output balancing and noise canceling simultaneously. To integrate this LNA into the active BPF design, the

interface matching should be carefully dealt with.

The noise performance can also be improved in the OTA design. Different noise canceling techniques can be investigated, such as [78], [106]-[108]. However, the extra loading effects and power consumption should be considered and the final solution is dependent on the system requirements.

Nonlinearity

The nonlinearity of the active BPFs can be further optimized in the OTA level. The first technique that can be investigated is the source-degeneration topology [109]. A simple schematic of the source degeneration is shown in Figure 5.1..

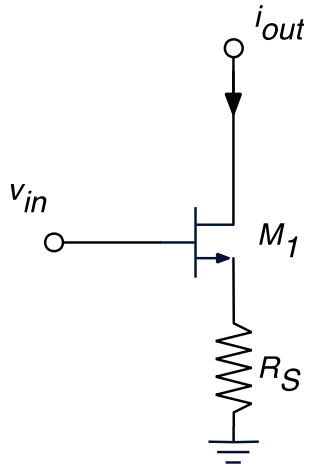

Figure 5.1. Simplified schematic of source degeneration.

The effective transconductance G_m of Figure 5.1 is

$$G_m = \frac{g_m}{1 + g_m R_s} \tag{5.2}$$

where g_m is the transconductance of the transistor M_1. Given the condition that $g_m R_S >> 1$, the effective transconductance can be simplified as

$$G_m = \frac{1}{R_s} \tag{5.3}$$

The effective transconductance is thus not related by the nonlinear transistor but the source degenerated resistor R_S. The major drawback of the resistor based source degeneration is the small effective transconductance. Moreover, the fixed resistance value eliminates the electrical tunability of the transconductance [109]. Alternatively, the source degeneration component can also be a transistor. Improved performance is thus achieved [109], [110].

Another approach to improve the nonlinearity of the OTA is the feed-forward technique. In this approach, the bias distortion induced by the large input signal is compensated by the input signal itself. The side effects of the feed-forward technique are the additional power consumption and size [111].

Providing Gain

It is attractive, for the active BPFs, to obtain signal amplification through their active configurations. The instinct idea comes to the mind is to use different values of transconductances in the gyrator cell. Preliminary simulations have shown that the gyrator cell can provide amplification when the transconductances in the forward and backward paths are different. This phenomenon can be applied in the active inductor or gyrator-resonator design to realize active BPFs with gain. However, the reciprocity of the resulted components can be traded. As a result, this technique would be studied in more detail and its application should be based on the system requirements.

Power Consumption

The pure active realization of the active BPFs also makes them more flexible in real operations. For example, in a pulsed system, the BPF can be turned on only when the pulse is passing through and turned off when there is no signal transmission. Proper design in the system level can result in a more power efficient transceiver.

5.2.2 TTDs

Optimization of TTDs Together with Antenna Array

As the key component in the phased array system, the true-time-delay based phase shifter should be packaged and integrated with real antennas to evaluate their performance. The most challenging part can be the interface of the phase shifter between its preceding/succeeding components. As the group delay of the whole signal path can be easily distorted when the reflection happens at those interfaces. Careful optimizations are thus needed in the integration process.

Flatting Insertion Loss across Frequency

It is also beneficial for the TTDs to have flat insertion loss across the frequency. Due to the frequency dependent loss in the delay cell like ATLs and APNs, the insertion loss increases with the frequency. For the trombone topology, one approach to reduce this effect is to introduce the frequency dependent tapping

transconductor. A simple possible structure is shown

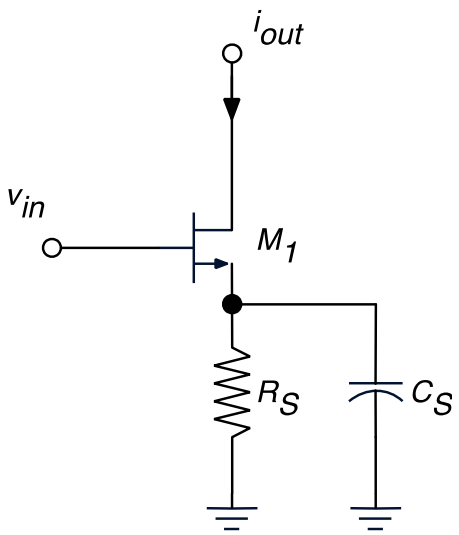

Figure 5.2. Frequency dependent transconductor using source degeneration.

The effective transconductance of Figure 5.2 can be given as

$$G_m = \frac{g_m}{1 + g_m(R_S // \frac{1}{j\omega C_S})} \tag{5.4}$$

In the low frequencies, the capacitor can be regarded as open and the effective transconductance is $\frac{1}{R_S}$. In the high frequencies, the capacitor can be considered as short and there is little source degeneration effect. The effective transconductance is thus g_m. The overall amplitude of the transconductance is then increasing from $\frac{1}{R_S}$ to g_m along with the frequency. However, this technique should be further investigated because the insertion phase needs to be carefully considered not to distort the final group delay.

Insertion Loss Compensation

The insertion loss of the TTDs can be compensated by amplifiers. In order not to deteriorate the achieved bandwidth of the TTDs, the main design challenge of the amplifiers would be the ultra-wide bandwidth.

One option is to use distributed amplifiers as they have demonstrated large bandwidth in the literature [112]-[114]. The parasitic constraints of the CMOS can be alleviated by special techniques like negative capacitance [115]. The noise performance of the distributed amplifier can also be improved [116]. Another design consideration is the group delay distortion introduced by the distributed amplifier, especially when cascaded configurations are used to boost the gain [117]. Although the distributed amplifier usually have a relatively flat delay response, special attentions are still required [118].

Another option is to introduce power or voltage amplifications into individual switching bocks. It is difficult to achieve amplification for the trombone structure TTDs in CMOS due to the stringent constraints of the input capacitance of the tapping amplifier [4]. A cascaded tapping amplifier may alleviate this issue. The trade-off would be the bandwidth because of the internal nodes [80].

New System Architecture

New architectures for the TTD based phased array system can be investigated. Some novel TTD systems have presented interesting results in the literature.

For example, as shown in [38], the novel path sharing configuration helps to reduce the chip area for integrated circuits. And the architecture proposed in [119] supports multi-beam applications. These examples inspire the author to investigate different structures for the TTD based phased array systems.

In the end, there are other building blocks, like LNA, VCO, and pulse-generator etc., need investigation for a full phased array transceiver.

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