TUNNELING FIELD-EFFECT TRANSISTORS FOR
LOW POWER LOGIC: DESIGN, SIMULATION, AND
TECHNOLOGY DEMONSTRATION

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NATIONAL UNIVERSITY OF SINGAPORE
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Declaration

I hereby declare that the thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.

Yang Yue
30 Aug. 2013
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Abstract

As complementary metal-oxide-semiconductor (CMOS) is aggressively being scaled down, it faces the fundamental limitation that the subthreshold swing ($S$) cannot be further reduced below 60 mV/decade at room temperature. Recently, a group of novel devices with the super-steep $S$ aroused great interests in the research community as it can potentially replace the metal-oxide-semiconductor field effect transistor (MOSFET) for low power applications. Among the device candidates, the tunneling field effect transistor (TFET) is the most promising one due to its excellent switching characteristics and the good compatibility with the current MOSFET platform. One of the technical challenges of the state-of-the-art TFET technology is the low drive current which may hinder its widespread application. Silicon (Si) has a relatively large bandgap, leading to a low band-to-band tunneling (BTBT) rate and low drive current for Si TFETs. Therefore, novel structure designs and materials are need advance the TFET technology to achieve high drive current. In this thesis, comprehensive simulation and experiment works were performed for drive current enhancement of TFETs. Several technology options, including enlarging tunneling region, improving source junction abruptness, and introducing small bandgap material as the substrate, were explored. The main flow of the thesis is as follows.

A detailed simulation study on TFET gate capacitances was performed to gain an in-depth understanding of the capacitance-voltage behavior of TFET. This is important for TFET circuit design. It was observed that the gate capacitance of TFET is asymmetrically partitioned into gate-to-drain and
gate-to-source capacitance. To improve the drive current of TFET, three different techniques were attempted in this thesis work. Firstly, double-gate TFETs with different shapes of extended source were investigated by simulation. By extending source region into the body under the gate, the tunneling area is enlarged, leading to an increase in tunneling current. Better uniformity of the high electric field along the source/channel interface is obtained in TFET with extended source, leading to an improvement of $S$. Secondly, integration of silicon-carbon (Si:C) source into n-type TFETs was performed experimentally. The effective suppression of boron diffusion due to the presence of substitutional carbon at the source side leads to abrupt junction, resulting in reduction of $S$ and enhancement of $I_{on}$. Lastly and the most importantly, we employed germanium-tin (GeSn) alloy, which has a smaller bandgap as compared to Ge, as a novel substrate material for high performance TFET application. The world’s first planar Ge0.958Sn0.042 p-type TFET was experimentally demonstrated by utilizing a gate-first sub-400 °C fabrication process. A relatively high drive current was achieved, which is attributed to the enhanced direct BTBT and the high hole mobility in GeSn channel. The low thermal budget of device fabrication process helps to form an abrupt source tunneling junction and thus enhance the tunneling current.
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Summary of recent reports on (a) drive current and (b) minimum point $S$ of nTFETs and pTFETs.

Key points for realizing a high performance TFET.

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**Fig. 4.4.** (a) Schematic showing device structure of DG Ge\(_{1-x}\)Sn\(_x\) TFET. (b) Band diagram near the surface along X-axis of Ge\(_{0.95}\)Sn\(_{0.05}\) TFET at \( V_{GS} = V_{DS} = 0.3 \text{ V} \). Since \( E_{c,L} \) is

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xvi
lower than $E_{c,T}$, the tunneling distance from $E_v$ at the source side to $E_{c,L}$ in the channel $w_T^{ind}$ (denoted by gray arrow) is shorter than that from $E_v$ at the source side to $E_{c,T}$ in the channel $w_T^{dir}$ (denoted by black arrow). (c) Band diagram near the surface along $X$-axis of Ge$_{0.86}$Sn$_{0.14}$ TFET at $V_{GS} = V_{DS} = 0.3$ V. Since $E_{c,T}$ is lower than $E_{c,L}$, $w_T^{dir}$ is shorter than $w_T^{ind}$. 

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**Fig. 4.5.** Spatial distributions of (a) $G^{ind}_{BTBT}$, (b) $G^{dir}_{BTBT}$ and (c) $G^{tot}_{BTBT}$ for Ge$_{0.95}$Sn$_{0.05}$ TFET at $V_{GS} = V_{DS} = 0.3$ V. As the double-gate device is symmetrical about a mirror line at $Y = 12.5$ nm, only the upper half body ($0 < Y < 12.5$nm) is shown. 

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**Fig. 4.6.** Spatial distributions of (a) $G^{ind}_{BTBT}$, (b) $G^{dir}_{BTBT}$ and (c) $G^{tot}_{BTBT}$ for Ge$_{0.86}$Sn$_{0.14}$ TFET at $V_{GS} = V_{DS} = 0.3$ V. As the double-gate device is symmetrical about a mirror line at $Y = 12.5$ nm, only the upper half body ($0 < Y < 12.5$nm) is shown. The magnitude of $G^{tot}_{BTBT}$ for Ge$_{0.86}$Sn$_{0.14}$ TFET is larger than that for Ge$_{0.95}$Sn$_{0.05}$ TFET shown in Fig. 4.5(c). 

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**Fig. 4.7.** (a) Simulated $I_{DS} - V_{GS}$ for Ge$_{0.95}$Sn$_{0.05}$ TFET. $V_{onset_{ind}}$ is lower than $V_{onset_{dir}}$ since $E_{g,L}$ is smaller than $E_{g,T}$. As $V_{GS}$ is larger than $V_{onset_{ind}}$, BTBT from $E_v$ at source side to $E_{c,L}$ occurs. However, at $V_{GS} > V_{onset_{dir}}$, BTBT from $E_v$ to $E_{c,T}$ dominates the tunneling current. (b) Simulated $I_{DS} - V_{GS}$ for Ge$_{0.86}$Sn$_{0.14}$ TFET. $V_{onset_{dir}}$ is lower than $V_{onset_{ind}}$ since $E_{g,T}$ is smaller than $E_{g,L}$. As $V_{GS} > V_{onset_{dir}}$, BTBT occurs from $E_v$ at source side to $E_{c,L}$ and dominates the drive current once $V_{GS}$ reaches $V_{onset_{dir}}$. 

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**Fig. 4.8.** A set of $I_{DS} - V_{GS}$ curves of Ge$_{1-x}$Sn$_x$ TFETs with $x$ ranging from 0 to 0.2. The drive current of Ge$_{1-x}$Sn$_x$ TFETs increases with Sn composition at a fixed $V_{GS}$ due to the reduction of minimum bandgap. 

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**Fig. 4.9.** A set of point $S$ versus $I_{DS}$ for Ge$_{1-x}$Sn$_x$ TFETs with $x$ ranging from 0 to 0.2. It can be observed that $S$ is reduced with Sn composition. The maximum $I_{DS}$ with sub-60 mV/decade $S$ becomes higher as Sn composition increases. 

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**Fig. 4.10.** $I_{off}$ versus $I_{on}$ of Ge$_{1-x}$Sn$_x$ TFETs with $x = 0.00$, 0.05, 0.11, and 0.17 at a supply voltage of 0.3 V. For a given $I_{off}$, $V_{off}$ is $V_{GS}$ when $I_{DS}$ equals to the $I_{off}$. $I_{on}$ is extracted at $V_{GS} - V_{off} = V_{DS} = 0.3$ V. For a fixed $I_{off}$, $I_{on}$ of Ge$_{1-x}$Sn$_x$ TFETs with $x > 0.11$ is higher than that of Ge TFET. 

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**Fig. 5.1.** (a) Schematic of a conventional planar TFET with p$^+$-p-n$^+$ structure. (b) Schematic of planar TFET with p$^+$-n$^+$-p$^+$ structure.
structure. (c) Illustration of dopant profile (acceptor concentration $N_a$) along A-A’ in (a). (d) Illustration of dopant profiles (acceptor concentration $N_a$ and donor concentration $N_d$) along B-B’ in (b). (e) Band diagram illustrating the band-to-band tunneling of electrons along A-A’ in (a). (f) Band diagram illustrating the band-to-band tunneling of electrons along B-B’ in (b). The additional n$^+$ pocket adjacent to the p$^+$ source leads to a more abrupt tunneling junction, reduces BTBT barrier width $w_T$, and thus enhances BTBT of electrons compared with conventional p$^+$$^-$p$^-$n$^+$ TFET.

Fig. 5.2. Schematic of silicon-carbon (Si:C) source TFET with p$^+$$^-n^+$$^-p^-$n$^+$ structure.

Fig. 5.3. Schematic illustration of suppressed boron diffusion in Si:C. Since the diffusion of boron depends on the interstitial density, and there are less interstitial sites in Si:C, the boron diffusion in Si:C is suppressed [129]. More abrupt p$^+$ junction can be formed by using Si:C source than Si source.

Fig. 5.4. (a) Fabrication process for p$^+$$^-n^+$$^-p^-$n$^+$ TFET with Si:C source. (b) Key steps to form p$^+$$^-n^+$$^-p^-$n$^+$ device structure. By implanting carbon cluster ions (C$_7$H$_7^+$) followed by boron cluster ions (B$_{18}$H$_{22}^+$) followed by annealing, the p$^+$ Si:C source was formed.

Fig. 5.5. (a) Transmission electron microscopy (TEM) image of the TaN/Al$_2$O$_3$ gate stack in fabricated Si:C source TFET with p$^+$$^-n^+$$^-p^-$n$^+$ structure. (b) C-V measurement result of a capacitor (200 µm × 200 µm) fabricated in parallel. The equivalent oxide thickness (EOT) was extracted to be about 3 nm based on the capacitance values at gate bias of -3 V.

Fig. 5.6. (a) Cross-sectional TEM image of the Si:C region at the source side of a fabricated TFET. (b) The zoomed-in view of the source junction highlighted by the square in (a). Good crystalline quality is achieved after annealing by RTA.

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Fig. 6.13. Measured $I_{DS}$-$V_{DS}$ curves of the same device in Fig. 6.12 at various gate voltages. $I_{DS}$ of 27 µA/µm was obtained at $V_{GS} = V_{DS} = -2$ V and $I_{DS}$ of 2.6 µA/µm was obtained at $V_{GS} = V_{DS} = -1$ V.  

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## List of Symbols

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<thead>
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<th>Symbol</th>
<th>Description</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_i$</td>
<td>Area of node $i$ in a mesh for device simulation ($i$ is node index)</td>
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</tr>
<tr>
<td>$C_D$</td>
<td>Depletion capacitance per device width</td>
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<tr>
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<td>Conduction band offset at heterojunction</td>
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</tr>
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<tr>
<td>$E_v$</td>
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</table>
\(E_{\text{v, front}}\)  Intercept between the valence band surface and a constant energy plane  eV
\(E_{\text{v, offset}}\)  Valence band offset at heterojunction  eV
\(E_g\)  Bandgap  eV
\(E_{g,L}\)  Bandgap at \(L\)-point  eV
\(E_{g,\Gamma}\)  Bandgap at \(\Gamma\)-point  eV
\(\xi\)  Electric field  V/m
\(\varepsilon_0\)  Permittivity of vacuum  F/m
\(\varepsilon_{ox}\)  Relative permittivity of SiO\(_2\)
\(f_c\)  Fermi-Dirac distribution of electrons in the conduction band
\(f_v\)  Fermi-Dirac distribution of electrons in the valence band
\(G\)  Generation rate of carriers  \(\text{cm}^{-3}\cdot\text{s}^{-1}\)
\(G_{\text{BTBT}}\)  Band-to-band tunneling generation rate  \(\text{cm}^{-3}\cdot\text{s}^{-1}\)
\(G_{\text{BTBT}}^{\text{dir}}\)  Band-to-band tunneling generation rate for electrons tunneling from valence band at \(\Gamma\)-point to conduction band at \(\Gamma\)-point  \(\text{cm}^{-3}\cdot\text{s}^{-1}\)
\(G_{\text{BTBT}}^{\text{ind}}\)  Band-to-band tunneling generation rate for electrons tunneling from valence band at \(\Gamma\)-point to conduction band at other than \(\Gamma\)-point  \(\text{cm}^{-3}\cdot\text{s}^{-1}\)
\(g_c\)  Density-of-states in the conduction band
\(g_v\)  Density-of-states in the valence band
\(h\)  Planck’s constant  eV\(\cdot\)s
\(I_{\text{DS}}\)  Drive-to-source current per device width  A/\(\mu\)m
\(I_{\text{GS}}\)  Gate-to-source current per device width  A/\(\mu\)m
\(I_{\text{on}}\)  On state current per device width  A/\(\mu\)m
\(I_{\text{off}}\)  Off state current per device width  A/\(\mu\)m
\(J_n\)  Electron current density  A/cm\(^2\)
\(J_p\)  Hole current density  A/cm\(^2\)
\(J_{pi}\)  Current densities at source-channel interface
\(k\)  Boltzmann constant  eV/K
\(\kappa\)  Imaginary part of the electron wave vector in the forbidden bandgap  1/m
\(L_{\text{extend}}\)  Extension length of the source into the channel  nm
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<th>Symbol</th>
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<td>$N_{c,\Gamma}$</td>
<td>Effective density of states for electrons in $\Gamma$-valley of conduction band</td>
<td>cm$^{-3}$</td>
</tr>
<tr>
<td>$N_{c,L}$</td>
<td>Effective density of states for electrons in $L$-valley of conduction band</td>
<td>cm$^{-3}$</td>
</tr>
<tr>
<td>$N_D$</td>
<td>Donor concentration</td>
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</tr>
<tr>
<td>$N_{inv}$</td>
<td>Inversion carrier density</td>
<td>cm$^2$</td>
</tr>
<tr>
<td>$N_{TA}$</td>
<td>Occupation number for transverse acoustic phonon</td>
<td>cm$^{-3}$</td>
</tr>
<tr>
<td>$N_v$</td>
<td>Effective density of states for holes in valence band</td>
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</tr>
<tr>
<td>$n$</td>
<td>Electron concentration</td>
<td>cm$^{-3}$</td>
</tr>
<tr>
<td>$n_\Gamma$</td>
<td>Electron concentration in the $\Gamma$-valley</td>
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</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
<td>Unit</td>
</tr>
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<tr>
<td>$n_e$</td>
<td>Electron concentration at the ending node of a tunneling path</td>
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</tr>
<tr>
<td>$n_i$</td>
<td>Intrinsic carrier concentration</td>
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<td>Hole concentration</td>
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<td>Electronic charge</td>
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<tr>
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<td>Inversion charge</td>
<td>C/m</td>
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<td>$\gamma_1$</td>
<td>Luttinger parameter</td>
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<tr>
<td>$\gamma_3$</td>
<td>Luttinger parameter</td>
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<tr>
<td>$R$</td>
<td>Recombination rate of carriers</td>
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<td>$R_{sh}$</td>
<td>Sheet resistance</td>
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<tr>
<td>$S$</td>
<td>Subthreshold swing</td>
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<td>$S_{min}$</td>
<td>Minimum point swing</td>
<td>mV/decade</td>
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<tr>
<td>$S_{ave}$</td>
<td>Average swing</td>
<td>mV/decade</td>
</tr>
<tr>
<td>$T$</td>
<td>Temperature</td>
<td>Kelvin or °C</td>
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<tr>
<td>$\tau$</td>
<td>Intrinsic switching delay</td>
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<tr>
<td>$T_{body}$</td>
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<tr>
<td>$T_{gate}$</td>
<td>Gate height</td>
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<tr>
<td>$T_{OX}$</td>
<td>Equivalent oxide thickness</td>
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<tr>
<td>$T_{tunnel}$</td>
<td>Tunneling probability</td>
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<td>$T_{dir}$</td>
<td>Tunneling probability of electron from valence band at Γ-point to conduction band at Γ-point</td>
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<tr>
<td>$T_{ind}$</td>
<td>Tunneling probability of electron from valence band at Γ-point to conduction band at other than Γ-point</td>
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<td>$U$</td>
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<tr>
<td>$V_{FB}$</td>
<td>Flatband voltage</td>
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<td>$V_D$</td>
<td>Drain voltage</td>
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<td>$V_{DD}$</td>
<td>Supply voltage</td>
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<td>$V_{DS}$</td>
<td>Drain-to-source voltage (V_D - V_S)</td>
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<td>$V_G$</td>
<td>Gate voltage</td>
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<td>Symbol</td>
<td>Description</td>
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<td>$V_{GD}$</td>
<td>Gate-to-drain voltage ($V_G - V_D$)</td>
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<tr>
<td>$V_{GS}$</td>
<td>Gate-to-source voltage ($V_G - V_S$)</td>
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</tr>
<tr>
<td>$V_{onset}$</td>
<td>The onset gate voltage of band-to-band tunneling occurs from $I_{DS} - V_{GS}$ curve</td>
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<tr>
<td>$V_{off}$</td>
<td>The gate voltage when $I_{DS}$ equals to $I_{off}$</td>
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<tr>
<td>$V_{onset,dir}$</td>
<td>The Gate voltage at which the onset of direct BTBT occurs</td>
<td>V</td>
</tr>
<tr>
<td>$V_{onset,ind}$</td>
<td>The Gate voltage at which the onset of indirect BTBT occurs</td>
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<tr>
<td>$V_S$</td>
<td>Source voltage</td>
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<tr>
<td>$V_{TH}$</td>
<td>Threshold voltage</td>
<td>V</td>
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<td>$V_{th,inv}$</td>
<td>Value of $V_{GD}$ when inversion occurs in the channel of a TFET</td>
<td>V</td>
</tr>
<tr>
<td>$W$</td>
<td>Gate width</td>
<td>μm</td>
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<td>$W_p$</td>
<td>The width of a tunnel path</td>
<td>nm</td>
</tr>
<tr>
<td>$w_T$</td>
<td>Width of tunnel path</td>
<td>nm</td>
</tr>
<tr>
<td>$w_T^{dir}$</td>
<td>Width of tunnel path for direct BTBT</td>
<td>nm</td>
</tr>
<tr>
<td>$w_T^{ind}$</td>
<td>Width of tunnel path for indirect BTBT</td>
<td>nm</td>
</tr>
<tr>
<td>$\rho$</td>
<td>Mass density</td>
<td>kg/m$^3$</td>
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<td>$\Phi_M$</td>
<td>Work function of metal gate</td>
<td>eV</td>
</tr>
<tr>
<td>$\mu_{eff,h}$</td>
<td>Effective hole mobility</td>
<td>cm$^2$/V·s</td>
</tr>
<tr>
<td>$\mu_n$</td>
<td>Electron mobility</td>
<td>cm$^2$/V·s</td>
</tr>
<tr>
<td>$\mu_p$</td>
<td>Hole mobility</td>
<td>cm$^2$/V·s</td>
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# List of Abbreviations

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
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<tbody>
<tr>
<td>2D</td>
<td>Two-dimensional</td>
</tr>
<tr>
<td>Al&lt;sub&gt;2&lt;/sub&gt;O&lt;sub&gt;3&lt;/sub&gt;</td>
<td>Aluminum oxide</td>
</tr>
<tr>
<td>ALD</td>
<td>Atomic layer deposition</td>
</tr>
<tr>
<td>As</td>
<td>Arsenic</td>
</tr>
<tr>
<td>BF&lt;sub&gt;2&lt;/sub&gt;</td>
<td>Boron difluoride</td>
</tr>
<tr>
<td>BTBT</td>
<td>Band-to-band tunneling</td>
</tr>
<tr>
<td>C-V</td>
<td>Capacitance-voltage</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary metal-oxide-semiconductor</td>
</tr>
<tr>
<td>E-k</td>
<td>Energy-momentum</td>
</tr>
<tr>
<td>EOT</td>
<td>Equivalent silicon oxide thickness</td>
</tr>
<tr>
<td>EPM</td>
<td>Empirical pseudopotential method</td>
</tr>
<tr>
<td>DG</td>
<td>Double-gate</td>
</tr>
<tr>
<td>DOS</td>
<td>Density-of-states</td>
</tr>
<tr>
<td>Ge</td>
<td>Germanium</td>
</tr>
<tr>
<td>GeSn</td>
<td>Germanium-tin</td>
</tr>
<tr>
<td>GSS</td>
<td>General-purpose Semiconductor Simulator</td>
</tr>
<tr>
<td>H&lt;sub&gt;2&lt;/sub&gt;SO&lt;sub&gt;4&lt;/sub&gt;</td>
<td>Sulfuric acid</td>
</tr>
<tr>
<td>HF</td>
<td>Diluted hydrofluoric</td>
</tr>
<tr>
<td>HfO&lt;sub&gt;2&lt;/sub&gt;</td>
<td>Hafnium oxide</td>
</tr>
<tr>
<td>HRXRD</td>
<td>High-resolution X-ray Diffraction</td>
</tr>
<tr>
<td>I-V</td>
<td>Current-voltage</td>
</tr>
<tr>
<td>InAs</td>
<td>Indium arsenide</td>
</tr>
<tr>
<td>InGaAs</td>
<td>Indium gallium arsenide</td>
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<tr>
<td>MOSFET</td>
<td>Metal-oxide-semiconductor field effect transistor</td>
</tr>
<tr>
<td>Ni</td>
<td>Nickel</td>
</tr>
<tr>
<td>Ni(GeSn)</td>
<td>Stanogermanide</td>
</tr>
<tr>
<td>nMOSFET</td>
<td>N-channel metal-oxide-semiconductor field effect transistor</td>
</tr>
<tr>
<td>nTFET</td>
<td>N-channel tunneling field effect transistor</td>
</tr>
<tr>
<td>pMOSFET</td>
<td>P-channel metal-oxide-semiconductor field effect transistor</td>
</tr>
<tr>
<td>P</td>
<td>Phosphorus</td>
</tr>
<tr>
<td>PR</td>
<td>Photoresist</td>
</tr>
<tr>
<td>pTFET</td>
<td>P-channel tunneling field effect transistor</td>
</tr>
<tr>
<td>TCAD</td>
<td>Technology computer-aided design</td>
</tr>
<tr>
<td>TEM</td>
<td>Transmission electron microscopy</td>
</tr>
<tr>
<td>TFET</td>
<td>Tunneling field effect transistor</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Description</td>
</tr>
<tr>
<td>--------------</td>
<td>-------------</td>
</tr>
<tr>
<td>$R_p$</td>
<td>Projected range</td>
</tr>
<tr>
<td>RTA</td>
<td>Rapid thermal annealing</td>
</tr>
<tr>
<td>SG</td>
<td>Single-gate</td>
</tr>
<tr>
<td>Si</td>
<td>Silicon</td>
</tr>
<tr>
<td>Sb</td>
<td>Antimony</td>
</tr>
<tr>
<td>Si:C</td>
<td>Silicon-carbon</td>
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<tr>
<td>Si$_2$H$_6$</td>
<td>Disilane</td>
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<tr>
<td>SF$_6$</td>
<td>Diluted hydrofluoric</td>
</tr>
<tr>
<td>SiGe</td>
<td>Silicon-germanium</td>
</tr>
<tr>
<td>SIMS</td>
<td>Secondary ion mass spectrum</td>
</tr>
<tr>
<td>SiO$_2$</td>
<td>Silicon oxide</td>
</tr>
<tr>
<td>SOI</td>
<td>Silicon-on-insulator</td>
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<tr>
<td>SPE</td>
<td>Solid phase epitaxy</td>
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<tr>
<td>SRH</td>
<td>Shockley-Read-Hall</td>
</tr>
<tr>
<td>TaN</td>
<td>Tantalum nitride</td>
</tr>
<tr>
<td>TEM</td>
<td>Transmission electron microscopy</td>
</tr>
<tr>
<td>UHVCVD</td>
<td>Ultra-high-vacuum chemical vapor deposition</td>
</tr>
<tr>
<td>WKB</td>
<td>Wentzel-Kramers-Brillouin</td>
</tr>
<tr>
<td>XRD</td>
<td>X-ray Diffraction</td>
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Chapter 1

Introduction

1.1 Background

1.1.1 Fundamental Limits of CMOS Scaling

For the past half century, the complementary metal-oxide-semiconductor (CMOS) technology has a tremendously rapid development [1] with the number of transistors per chip is approximately doubled every two years. This trend is described by Moore’s law [2]-[3], being made possible by continued scaling-down of the device dimensions and the supply voltage $V_{DD}$ (Fig. 1.1). Transistor or device scaling results in higher packing density, reduced cost per function, and increased circuit speed. Over the last decade, CMOS technology entered into the sub-100 nm regime, and the extremely scaled transistors were realized by incorporating strained silicon (Si) channel (beyond 90 nm technology node) and high-k/metal gate (beyond 45 nm technology node) [4]-[5]. Most recently, transistors at 22 nm technology node are realized by mass production using the tri-gate FinFET structure by Intel corporation [6].

However, as CMOS transistors are scaled down beyond the 22 nm technology node, immense challenges are faced to maintain the historical pace of performance scaling. The increase in the drive current, which is required for faster switching speed at low $V_{DD}$, comes with a price of an
Fig. 1.1. The scaling of transistor follows the Moore’s Law. (a) The physical gate length shrinks with technology node. (b) Supply voltage $V_{DD}$ continues to scale down. However, as the technology node goes beyond 90 nm, a very significant delay in $V_{DD}$ scaling is observed. Static power takes up more power consumption, and it becomes an issue for CMOS scaling [7]. The circle symbols present the $V_{DD}$ scaling trend predicted by ITRS 1995, while the triangles present the updated trend by ITRS 2011, where a delay of $V_{DD}$ scaling is expected.

exponential increase in the off-state current ($I_{off}$), which leads to a large standby or static power dissipation [7][Fig. 1.1(b)]. This is essentially due to the fundamental limit for the subthreshold swing $S$ of a MOSFET, which cannot be lower than 60 mV/decade at room temperature.

$S$ is defined as the change in gate voltage ($V_{GS}$) needed to induce a change in drain current ($I_{DS}$) by one order of magnitude in the subthreshold regime, where $V_{GS}$ is smaller than threshold voltage $V_{TH}$. $S$ is given by [8]

$$S = \ln 10 \frac{kT}{q} \left( \frac{C_{ox} + C_D}{C_{ox}} \right),$$

where $k$ is the Boltzmann’s constant, $T$ is the absolute temperature, $q$ is the charge of an electron, $C_{ox}$ is the gate oxide capacitance, and $C_D$ is the depletion capacitance. In a well-designed transistor, $C_{ox}$ dominates over all other capacitances, and thus $S$ has the minimum value of $\ln 10 \cdot kT/q = 60$
nMOSFET:

![Schematic of nMOSFET](image)

**Fig. 1.2.** (a) Schematic of a conventional MOS transistor. Here, we take the n-channel MOSFET as an example. (b) The change in energy band diagram along the source to drain direction as $V_{GS}$ increases in a MOSFET with fixed $V_{DS}$. Fermi distribution of carriers in energy scale $n(E)$ at the source determines the lower limit of subthreshold swing $S$ in a MOSFET, which is 60 mV/decade at room temperature. The blue arrows indicate the changing direction of band diagrams as $V_{GS}$ increases.

mV/decade at room temperature in a MOSFET [Fig. 1.2]. The physical insight of this $S$ limitation is that the rise of $I_{DS}$ is determined by the Fermi distribution of carriers at the source side [Fig. 1.2(b)], assuming that the gate has full control of the channel potential. As $V_{DD}$ decreases with technology scaling, which is required to reduce the power consumption, $V_{TH}$ will have to be reduced in order to maintain a high $I_{on}$ for a high switching speed. However, the $V_{TH}$ cannot be reduced much lower than about ~0.2 V, otherwise $I_{off}$ will increase correspondingly due to the fundamental limitation of $S$ [Fig. 1.3(a)]. In addition, aggressive scaling of MOSFET has resulted in short channel effects, leading to additional degradation of $S$. The scaling of $V_{DD}$ faces fundamental difficulty due to the working mechanism of MOSFET, which will delay $V_{DD}$ scaling as predicted by recent ITRS updates [triangular points in Fig. 1.1(b)].
At the end of CMOS scaling, there is a strong need to explore alternative novel devices, which could have steeper $S$ (less than 60 mV/decade at room temperature), to overcome the fundamental limitation of MOSFET for future logic applications [Fig. 1.3(b)].

1.1.2 Alternative Device Candidates with Steep Subthreshold Swing

Alternative devices with entirely new working mechanisms are desired to overcome the non-scalability of $S$ in the conventional MOSFET. Both industry and academia have put efforts in exploring alternative devices with steep $S$, such as the impact-ionization metal-oxide-semiconductor (IMOS) transistor [9]-[10], the tunneling field-effect transistor (TFET) [11]-[75], the feedback transistors [76], and the ferroelectric FET [77]-[78].

The IMOS employs avalanche breakdown or impact ionization by high electric field in reverse biased p-i-n diode to obtain very steep $S$. Despite the steep $S$ and excellent $I_{on}/I_{off}$ [9]-[10], IMOS requires a high reverse voltage at
the source side to provide very high electric field to trigger avalanche breakdown (source voltage ~5 V for n-type IMOS), which consumes more power and is a concern in IC design. In addition, an IMOS suffers from rapid device degradation due to hot carrier damage, which leads to severe carrier trapping, creation of interface states and gate leakage over time. The feedback transistor [76] employs forward biased p⁺-i-n⁺ diode with intrinsic channel region partially gated (denoted as source or drain offset region). The gate voltage initiates an positive feedback loop as carriers transport between the source and drain terminals: electrons drift from n⁺ source to p⁺ drain with some of them accumulate at the potential well at the drain offset, reducing the energy barrier for holes and enabling holes to flow into the channel; while, as holes are drifting towards n⁺ source side, some of them will accumulate in the potential well at source offset and the potential barrier for electron injection is reduced, causing more electrons to be injected from n⁺ source to p⁺ drain. Although S can be reduced in feedback transistor, the main drawback is the high static power consumption since the p⁺-i-n⁺ diode is working in forward biased mode and the off-state current is high. Ferroelectric FETs make use of ferroelectric dielectric to provide a negative capacitance which results in a step-in transformation of the channel potential to the gate voltage, thus sub-60 mV/decade S could be achieved [77]-[78]. The additional ferroelectric mechanism due to the electric dipole movement causes an additional delay. In addition, the interface state will also pose problem in its real fabrication.

Different from the above device schemes, a TFET exploits the gate-controlled band-to-band tunneling (BTBT) quantum mechanism to achieve very steep S with a gated p-i-n configuration. Recently, TFETs attracted a lot
of research attentions. Many theoretical investigations [11]-[40] and experimental demonstrations [41]-[75] were reported in the literature. The TFET is considered as one of the most promising candidates with steep $S$ to realize electronics at significantly reduced $V_{DD}$. Up to now, realization of TFETs with sub-60 mV/decade $S$ with various device designs have been reported [48]-[51],[53],[56],[61]. Tremendous research efforts have been made to realize high performance TFET including the fundamental study, device design, and fabrication optimization. This dissertation will primarily focus on the development of TFET technology in terms of device simulation and process development.

1.2 Device Physics of TFET

1.2.1 BTBT Theory

BTBT is a quantum phenomenon in which electrons from the valence band ($E_v$) tunnel through the forbidden energy gap to the conduction band ($E_c$) with certain tunneling probability ($T_{tunnel}$), leaving holes in the valence band.

![Fig. 1.4](image)

Fig. 1.4. (a) Band diagram of a reverse biased p$^+/n^+$ diode, where electron band-to-band tunneling (BTBT) occurs. $E_{fp}$ is the quasi Fermi level in p$^+$ region, while $E_{fn}$ is the quasi Fermi level in n$^+$ region. (b) The tunneling barrier of the p$^+/n^+$ diode in (a) can be approximated by a triangle potential barrier [82].
[Fig. 1.4(a)]. The potential barrier seen by the tunneling electrons can be approximated as a triangle [Fig. 1.4(b)], and the tunneling probability $T_{tunnel}$ has an expression with Wentzel-Kramers-Brillouin (WKB) [79]-[81] approximation as [82],[83]

$$T_{tunnel} = e^{-2w_T \sqrt{\frac{2m^*_r[U(x)-E]}{\hbar}} dx} \approx e^{-4q\frac{2m^*_rE_g^{1/2}}{3\hbar^2}}$$ (for triangle potential barrier), \hspace{1cm} (1.2)

where $w_T$ is the tunneling width, $m^*_r$ is the reduced tunneling mass, $U(x)$ is the potential energy, $\hbar$ is the reduced Planck constant, $E_g$ is the material band gap, and $\zeta$ is the uniform electrical field if triangle potential barrier is assumed. It should be noted that the smaller $w_T$, $E_g$ and $m^*_r$ are, the higher $T_{tunnel}$ becomes.

For a fixed material, $E_g$ and $m^*_r$ are fixed, and $w_T$ is an indicator of $T_{tunnel}$. BTBT could occur only if $T_{tunnel}$ is high enough and there are enough electrons at the starting side under $E_v$ [left side in Fig. 1.4(a)] and enough empty states at the ending side above $E_c$ [right side in Fig. 1.4(a)]. The BTBT generation rate $G_{BTBT}$ is obtained as [82]

$$G_{BTBT} \propto \int_{E_v}^{E_c} [f_v(E) - f_c(E)] g_c(E) g_v(E) T_{tunnel} \cdot dE ,$$ \hspace{1cm} (1.3)

where $f_v(E)$ and $f_c(E)$ are the Fermi-Dirac distribution functions, and $g_c(E)$ and $g_v(E)$ are the density-of-states in the conduction band and the valence band, respectively. According to Eqs. (1.2) and (1.3), in order to get a high tunneling current, a small $w_T$ is desirable, which requires abrupt doping profile at tunneling junction. In addition, material with a small $m^*_r$ and a narrow $E_g$ or tunneling favorable heterojunction is preferred for TFET applications.
1.2.2 Working Mechanism of TFET

A TFET is basically a gated p⁺-i-n⁺ diode, where “i” region (either the intrinsic or lightly doped semiconductor) is the channel. An n-channel TFET (nTFET) is a gated p⁺-p-n⁺ diode as illustrated in Fig. 1.5(a), while a p-channel TFET (pTFET) is a gated n⁺-n+p⁺ diode. The gate bias is used to modulate the channel potential of a TFET, and thus to control the BTBT at the interface between the source and the channel [Fig. 1.5(b) and (c)]. The TFET is switched off at low $V_{GS}$ due to the appearance of a bandgap which cuts off the Fermi tail of carrier concentrations [Fig. 1.5(b)]. Therefore, $I_{off}$ is very low and limited by the junction leakage which includes both the drift current and the Shockley-Read-Hall (SRH) generation. In addition, if the junction at the drain side is abrupt, drain side BTBT could occur at off-state, which also contributes to $I_{off}$ of a TFET. At on-state with high $V_{GS}$ and $V_{DS}$, the $I_{DS}$ of a TFET is the tunneling current contributed by the source-side BTBT [Fig. 1.5(c)].

Fig. 1.5.  (a) Schematic of an n-channel TFET (nTFET) with the gated p⁺-p-n⁺ configuration.  (b) Off-state and (c) on-state energy band diagrams extracted from the source to drain direction near the channel surface. The low leakage current at the off-state is due to the bandgap cutting off the Fermi tail of carrier concentrations [see Fig. 1.3 (b) for Fermi distribution of carrier concentrations $n(E)$]. At on-state, the band-to-band tunneling of electrons from the p⁺ source to the lightly p-type doped channel is enabled by a positive gate bias.
Transfer characteristics ($I_{DS}-V_{GS}$) of a typical Si TFET with sub-60 mV/decade $S$ are shown in Fig. 1.6 (a). For a fixed $V_{DS}$, as $V_{GS}$ increases, $E_c$ in the channel is lowered and the inversion layer is formed in the surface of the channel. Thus, the electron tunneling width (from $E_v$ in the source to $E_c$ in the channel) becomes narrower, and $I_{DS}$ increases correspondingly. As $V_{GS}$ keeps increasing, $I_{DS}$ continually increases but with a progressively reducing slope, which is due to the constraint of voltage drop at tunneling junction by $V_{DS}$ [Fig. 1.6 (a)]. Fig. 1.6 (b) shows the corresponding output characteristics ($I_{DS}-V_{DS}$) of the Si TFET. At low $V_{DS}$, $I_{DS}$ depends on $V_{DS}$ and it saturates with a decreasing $V_{GD}$ ($V_{GD} = V_{GS}-V_{DS}$) when the inversion layer is pinched off [22],[84].


1.3 Development of TFET Technology

The concept of tunneling based transistor came out in the 1980’s. S. Banerjee [41] and T. Baba [42] proposed the initial gate controlled tunnel transistors in 1987 and 1992, respectively. Si surface tunnel transistor (STT) was demonstrated by W. M. Reddick in 1995 [43], while in 2000, W. Hansch fabricated a vertical Si TFET with highly abrupt tunnel junctions achieved by MBE growth [44]. In 2004, K. K. Bhuwalka reported a vertical TFET employing a δp+ doped SiGe layer adjacent to the source tunneling junction, and the improvements in $I_{DS}$ and $S$ were obtained [45]. In the same year, J. Appenzeller demonstrated carbon-nanotube TFET with sub-60 mV/decade $S$ [46]. However, the reported $I_{DS}$-$V_{GS}$ curve is not as smooth as the normal transfer characteristics. Afterwards, plenty of experimental demonstrations using Si [47],[50],[52],[56],[57],[61],[66],[72], strained SiGe [48],[68], and Ge [49],[67] material systems were reported for both nTFETs and pTFETs. At the same time, a lot of simulation studies were also performed to explore the physical insights [11],[17],[23]-[29],[31],[33]-[39] and optimize the device design for better performance of TFETs [12]-[15],[18]-[21],[30],[32],[34]-[37],[39]. Recently, TFETs with small bandgap materials such as III-V compounds [54],[63]-[65],[69]-[71], TFET with hetero tunneling junction [50],[53],[55],[60],[62],[69]-[70],[73]-[74], and devices with multi-gate device structure [51]-[52],[57],[61],[63]-[66],[70] were demonstrated. More attentions were given to the TFETs with new materials and new structures due to their higher BTBT generation rate and improved device performance as compared with conventional planar Si TFETs. A summary of recent reports on drive current and $S$ of both nTFETs and pTFETs are shown in Fig. 1.7.
Fig. 1.7. Summary of recent reports on (a) drive current and (b) minimum point S of nTFETs and pTFETs.

Although some of the reported TFETs achieved $S$ less than 60 mV/decade, in most of the case, the extremely small $S$ only appears at very low current level. Therefore, current TFET technology is still far from being a realistic alternative to replace state-of-the-art CMOS for future logic applications. More research efforts are required to further improve the TFET performance, especially the on-state current ($I_{on}$). In order to achieve a high $I_{on}$ and a sub-60 mV/decade $S$ at the same time, some key points need to be considered in TFET realization. These are shown in Fig. 1.8 and will be discussed as follows.
1.3.1 Junction Engineering

According to the BTBT working mechanism, $I_{on}$ of a TFET is determined by abruptness of the source tunneling junction. In order to achieve a high $I_{on}$, a very abrupt source junction is needed to increase the BTBT rate. Currently, several solutions are being proposed. Dopant segregation can be used to achieve abrupt tunneling junction at the source-channel interface [56]. The profile of boron in Si could be controlled using laser anneal dopant activation [66]. In addition, using heterojunction with type II staggered band alignment can reduce the energy difference between $E_v$ in the source and $E_c$ in the channel, thereby decreasing the tunneling width and leads to an enhancement of the tunneling current [21],[50],[53],[55],[60],[62],[69]-[70],[73]-[74]. Strain engineering could also enhance the performance of TFET by splitting the energy bands to reduce the tunneling width further [26],[37]. At the drain side of a TFET, a gradual drain junction or gate to drain offset is desired to suppress drain-side BTBT, and thus to maintain a low $I_{off}$ [40]. Moreover, efficient defects removal at both the source and the drain
junctions is desired to reduce the SRH and thereby lowering the junction leakage current when a TFET is at off-state.

1.3.2 Material Engineering

In order to achieve high $I_{on}$, small bandgap materials such as Ge and III-V compounds are preferred because of the large BTBT rate when TFET is switched on. In the meantime, materials with direct bandgap are also desired since direct BTBT has a smaller $m^*$, thus, a higher tunneling probability compared to the indirect BTBT, like the BTBT in Si. In addition, the mobilities of the carriers in the channel inversion layer, i.e. electrons in nTFET and holes in pTFET, are also important. Fortunately, the materials with small bandgaps (such as InGaAs [54],[64], InAs [63],[74] and Ge[48],[53]) could have relatively high carrier mobility at the same time, thus the application of these materials in TFET is quite promising.

1.3.3 Structure Engineering

Similar to the case in MOSFET, employment of ultra-thin body substrates and multi-gate structures such as nanowire FET[51]-[52],[61],[63],[66], could result in better gate modulation of TFETs, enhancing BTBT, improving the tunneling current, and reducing the leakage current. Besides the engineering in gate structure and body thickness, source tunneling junction geometry is also very important. The source tunneling junction could be vertical, like the case in a vertical TFET [43],[44],[53],[61],[69],[73], where the advantages of in situ doping technique could be used to realize a very steep dopant profiles at source-channel interface. The source tunneling
junction could also be extended into the body of a TFET by a novel structural design to enlarge the tunneling area, leading to an enhancement of device performance [17].

1.3.4 Gate Stack Engineering

Since the TFET working mechanism is gate modulated BTBT, the gate control over the channel surface is an important factor determining the device performance. Gate stack with good interface quality is desirable. In order to achieve a high $I_{on}$ of TFET, small bandgap materials, such as III-V and Ge, are investigated as mentioned above. In this case, proper high-k material should be chosen and special passivation techniques are needed for different substrate materials.

1.4 Objectives of Research

The objectives of this dissertation are to propose or demonstrate various advanced techniques for TFETs by considering the optimization schemes described in the previous section. To completely understand the electrical characteristics of TFETs, the study on TFET capacitance-voltage ($C-V$) behavior is carried out. The main focus of this thesis is on exploring methods to improve TFET performance in terms of $I_{on}$. For Si TFETs, performance enhancement could be obtained by either enlarging area of tunneling region or improving tunneling junction abruptness. Novel device structure with special source geometry is to be designed to gain the tunneling region enlargement. Silicon-carbon is to be implemented to achieve an abrupt boron profile in Si at the source side, in order to enhance BTBT in Si TFET.
A more efficient way to enhance the TFET performance is to use a small band gap material as the substrate, such as GeSn, and its applications in both nTFET and pTFET need further theoretical assessment and experimental demonstration. The results of these research works will provide technology options for high performance TFET for the future logic devices.

1.5 Thesis Organization

This thesis includes 7 Chapters. Chapter 1 gives a brief introduction to the background and the objectives of this thesis. Chapters 2 through 4 document device design and simulation results, while Chapters 5 and 6 document experimental results.

In Chapter 2, the dependence of TFET gate capacitances on terminal voltages was studied by simulation. The total gate capacitance of TFET is asymmetrically partitioned into gate-to-drain ($C_{GD}$) and gate-to-source ($C_{GS}$) capacitance components when the inversion layer is formed. A compact model of TFET gate capacitance was developed.

In Chapter 3, the impact of extended source structures in double-gate TFETs was investigated by simulation. In the on-state, extended source structures increase the tunneling area, leading to an increase in the BTBT current and an improvement in $I_{on}$ and $S$. The benefits from extended source design are more obvious for TFET with a hetero-tunneling junction, such as the Ge-source Si-body TFETs.

In Chapter 4, a novel substrate material germanium-tin (GeSn), which has a small bandgap, was explored for nTFETs by the non-local Empirical
Pseudopotential Method (EPM) calculation and TCAD simulation. By increasing Sn composition from 0 to 0.2, GeSn transits from indirect bandgap to direct bandgap material, and $I_{on}$ of GeSn TFETs is increased due to the higher direct BTBT rate. In addition, the maximum $I_{DS}$ with sub-60 mV/decade $S$ becomes higher with increasing Sn composition, which is preferred for TFET application.

In Chapter 5, silicon-carbon (Si:C) source was incorporated into Si TFETs with a p$^+$-n$^+$.p-n$^+$ structure. A reduction in $S$ and an enhancement in $I_{on}$ are achieved due to the effective suppression of boron diffusion with the presence of substitutional carbon at the source side of the devices. The abrupt boron profile leads to an abrupt tunneling junction and thus enhances BTBT of electrons. In addition, the induced tensile strain reduces the bandgap at tunneling junction, which also helps to improve the drive current.

In Chapter 6, the first GeSn pTFET was realized using a gate-first process. Decent device characteristics was obtained, which is due to the enhanced direct BTBT and the high hole mobility in GeSn channel. The low thermal budget of the device fabrication process helps to form abrupt source tunneling junction to enhance the BTBT of electrons.

Finally, the main contributions of this thesis and suggestions for future work are summarized in Chapter 7.
Chapter 2

Gate Capacitance in Tunneling Field-Effect Transistors: Simulation Study

2.1 Introduction

Due to the gate controlled band-to-band tunneling (BTBT) mechanism, a tunnel field effect transistor (TFET) is expected to have superior current-voltage ($I$-$V$) characteristics in terms of high on-state/off-state current ratio ($I_{on}/I_{off}$) and steep subthreshold swing $S$. TFET is a promising candidate to realize electronics at low supply voltage $V_{DD}$ [11]-[75]. In order to use TFETs in integrated circuits, the switching behavior of a TFET needs to be investigated in detail. Besides $I$-$V$ characteristics, the gate capacitance is a crucial determinant of device switching speed, since the intrinsic switching delay $\tau$ is given by [1]

$$\tau = C_{GG} \cdot \frac{V_{DD}}{I_{on}},$$  \hspace{1cm} (2.1)

where $C_{GG}$ is the total gate capacitance per device width in inversion. A deep understanding of TFET gate capacitance and its components will be very important for determining the speed performance of TFETs.

The gate capacitance of a TFET can be quite different from that of a metal-oxide-semiconductor field effect transistor (MOSFET), as the TFET has a different working mechanism. There is little or no investigation on TFET gate capacitance and its components. The distributions of TFET gate capacitance components are not well studied yet. In this Chapter, we report a
systematic analysis of gate capacitance components in a planar Si TFET [85],[86]. The dependence of capacitances on terminal voltages and device geometry are investigated in detail using a physics-based technology computer-aided design (TCAD) simulator [84]. A compact TFET gate capacitance model comprising parasitic capacitance components and inversion capacitance is built. The impact of parasitic capacitance components on the total gate capacitance of TFET is discussed. Methods to reduce the parasitic capacitance components by drain dopant profile engineering are also discussed.

2.2 Numerical Simulation

2.2.1 Simulation Methodology

Device simulation was performed using our in-house two-dimensional (2D) TCAD simulator which implements a physics-based non-local BTBT algorithm [84]. This algorithm is implemented based on an open source TCAD device simulator named General-purpose Semiconductor Simulator (GSS) [87]. There is a commercially supported version by Congenda [88]. A brief description of our non-local BTBT algorithm implementation will be given in the following part, while more details are documented in Ref. [84].

The algorithm automatically identifies the tunneling paths, and for each tunneling path, the tunneling probability $T_{\text{tunnel}}$ is obtained based on Wentzel-Kramers-Brillouin (WKB) method [79]-[81]:

$$T_{\text{tunnel}} = e^{-2\kappa |\phi|_{r}}$$

with

$$\kappa = \frac{2\pi}{h} \sqrt{2m^{*}[U(r) - E]}$$

(2.1)
where $E$ is carrier energy, $\kappa$ is the imaginary part of the electron wave vector in the forbidden bandgap, $h$ is Planck’s constant, $m^*_r$ is the tunneling reduced mass (for Si, $m^*_r = 0.28m_0$, where $m_0$ is free electron mass), and $U(r) - E$ is the barrier height at position $r$.

![Diagram](image)

**Fig. 2.1.** (a) and (b) show the band diagram of a tunneling junction visualized in 3D with different viewing angles. Energy scale is in the vertical direction. One tunneling path is highlighted in red. $dE$ is small energy step, $W_p$ is the width of a tunneling path, $E_{c\text{, front}}$ the intercept between a constant energy plane and the conduction band $E_c$ surface, and $E_{v\text{, front}}$ the intercept between the a constant energy plane and a valence band $E_v$.  (c) Flow chart illustrating our non-local algorithm of calculating BTBT current for TFET application.
BTBT carrier generation rate \( G_{BTBT} \) is calculated based on the tunneling paths [Fig. 2.1(a) and (b)]:

\[
G_{BTBT} = \int_{E_{v,\text{min}}}^{E_{v,\text{max}}} \frac{4\pi \cdot q m^*_\text{DOS}}{h^3} kT \frac{n_v p_v - n_i^2}{(n_v + n_i)(p_v + n_i)} W_p \cdot T_{\text{tunnel}} \cdot dE,
\]  \hspace{1cm} (2.2)

where \( q \) is electron charge, \( m^*_\text{DOS} \) is electron density-of-state effective mass, \( k \) is Boltzmann constant, \( T \) is temperature in Kelvin, \( p_v \) is the hole concentration at the starting node of tunneling at \( E_{v,\text{front}} \) (the intercept between a constant energy plane and the valence band \( E_v \) surface at the source side), \( n_v \) is the electron concentration at the ending node at \( E_{c,\text{front}} \) (the intercept between a constant a constant energy plane and the conduction band \( E_c \) surface in the channel region), \( n_i \) is the intrinsic carrier concentration, and \( W_p \) is the width of a tunnel path [Fig. 2.1(b)]. The integration in Eq. (2.2) is performed from the minimum \( E_c (E_{c,\text{min}}) \) to the maximum \( E_v (E_{v,\text{max}}) \).

\( G_{BTBT} \) is then captured in the current continuity equations [Eqs. (2.3) and (2.4)]. The current continuity equations and Poisson equation [Eq. (2.5)] are self-consistently solved using Newton’s iteration method.

\[
\frac{\partial n}{\partial t} = \frac{1}{q} \nabla \cdot J_n - [R - (G + G_{BTBT})] \hspace{1cm} (2.3)
\]

\[
\frac{\partial p}{\partial t} = -\frac{1}{q} \nabla \cdot J_p - [R - (G + G_{BTBT})] \hspace{1cm} (2.4)
\]

\[
\nabla \cdot \varepsilon \nabla \Psi = -q( p - n + N_D - N_A) \hspace{1cm} (2.5)
\]

where \( G \) and \( R \) are generation and recombination rate of carriers, respectively, \( J_n \) and \( J_p \) are current density of electrons and holes, respectively, \( \Psi \) is the electrostatic potential, \( p \) is hole concentration, \( n \) is electron concentration,
and \( N_D \) and \( N_A \) are concentrations of donors and acceptors, respectively, assuming donors and acceptors are fully ionized. \( J_n \) and \( J_p \) are calculated as

\[
J_n = q\mu_n n E_n + qD_n \nabla n
\]

(2.6)

\[
J_p = q\mu_p p E_p - qD_p \nabla p
\]

(2.7)

where \( \mu_n \) is electron mobility, \( \mu_p \) is hole mobility, \( E_n \) and \( E_p \) are the electrical field applied to electrons and holes, respectively, and \( D_n \) and \( D_p \) are the electron and hole diffusivities, respectively. The calculation flow is summarized in Fig. 2.1(c). The algorithm is designed to be robust and the converged electrical results are checked for mesh grid independence [84].

2.2.2 Device Structure

Single-gate (SG) n-channel silicon-on-insulator (SOI) TFET with a structure shown in Fig. 2.2(a) was simulated. The p\(^+\) source is doped at 2\times10^{20} \text{ cm}^{-3} with a doping gradient of 2 nm/decade, and the n\(^+\) drain is doped at 1\times10^{20} \text{ cm}^{-3} with a doping gradient of 5 nm/decade, i.e. gradual drain doping [Fig. 2.2(b)]. The p-type channel doping is 1\times10^{16} \text{ cm}^{-3} and the body thickness \( T_{\text{body}} \) is 20 nm. The equivalent silicon oxide thickness (EOT or \( T_{\text{OX}} \)) is 0.8 nm. Metal gate is used with a work function of 4.05 eV, a gate height \( T_{\text{gate}} \) of 50 nm, and a gate length \( L_G \) of 50 nm.
Fig. 2.2. (a) Device structure of simulated SG TFET. (b) Impurity doping profiles of acceptors ($N_A$) and donors ($N_D$) underneath the gate [along $A$-$A'$ in (a)]. Zero in the horizontal axis refers to the location of left gate edge. $\Delta L_s$ and $\Delta L_d$ are the extension length of p-type and n-type region into the channel, respectively, overlapping with the gate. (c) Energy band diagrams underneath the gate [along horizontal cutline $A$-$A'$ in (a)] with $V_{DS} = 1$ V at $V_{GS} = 1$ V (solid line) and 0 V (dashed line). (d) Energy band diagrams from the gate to the channel [along vertical cutline $B$-$B'$ in (a)] with $V_{DS} = 1$ V at $V_{GS} = 1$ V (solid line) and 0 V (dashed line). Zero in the vertical axis refers to the interface between gate dielectric and channel.

The TFET was biased with various $V_D$ and $V_G$ ranging from 0 to 1 V, and the source terminal is grounded ($V_S = 0$ V). In this study, TFET is considered as switched on (at on-state) with $V_{DS} = 1$ V and $V_{GS} = 1$ V, and it is at off-state with $V_{DS} = 1$ V and $V_{GS} = 0$ V. The band diagrams for on-state (dashed lines) and off-state (solid lines) along horizontal [A-A’ in Fig. 2.2(a)] and vertical directions [B-B’ in Fig. 2.2(a)] are shown in Fig. 2.2 (c) and (d), respectively. When 1 V gate voltage is applied, the conduction band ($E_c$) and valence band ($E_v$) in the channel bend down, enabling the band-to-band tunneling of electrons from p$^+$ source to the channel. An nMOSFET with the...
same simulation parameters and dimensions as nTFET is also simulated; the nMOSFET has a source that is heavily n’ doped.

2.2.3 Extraction of Gate Capacitances

The 2D TCAD simulator can output spatial distributions of carrier concentrations. The gate charge ($Q_G$) can be obtained by integrating the charges over all the nodes (the total number of nodes is denoted as $n_G$) within the gate region by

$$Q_G = \sum_i (n + N_A - p - N_D) \cdot A_i,$$

where $N_D$ and $N_A$ are concentrations for donors and acceptors, respectively, and $n$ and $p$ are concentrations for electrons and holes, respectively, and $A_i$ is the area of node $i$, with $i = 1, 2, 3 \ldots n_G$. The simulator treats all impurities as being fully ionized. The gate capacitances, gate-to-drain capacitance ($C_{GD}$), gate-to-source capacitance ($C_{GS}$), and total gate capacitance ($C_{GG}$) were extracted by computing the change in $Q_G$ with respect to a small change in a terminal voltage (5 mV) at each bias. Specifically, $C_{GD}$, $C_{GS}$, and $C_{GG}$ are extracted as

$$C_{GD} = \frac{\partial Q_G}{\partial V_D} \bigg|_{V_D, V_G},$$

$$C_{GS} = \frac{\partial Q_G}{\partial V_S} \bigg|_{V_S, V_G},$$

$$C_{GG} = \frac{\partial Q_G}{\partial V_G} \bigg|_{V_G, V_D}. $$
For SOI device, \( C_{GG} \) is partitioned by \( C_{GD} \) and \( C_{GS} \) i.e. \( C_{GG} = C_{GD} + C_{GS} \). In addition, gate oxide capacitance \( C_{ox} \) is calculated as \( C_{ox} = \varepsilon_0 \cdot L_G / T_{ox} \), where \( \varepsilon_0 \) is vacuum permittivity and \( \varepsilon_ox \) is the relative permittivity of silicon oxide (SiO₂).

2.2.4 **Capacitance-Voltage (C-V) Characteristics of TFET**

The extracted \( C_{GD} \) and \( C_{GS} \) in nTFET and nMOSFET with various \( V_{GS} \) at \( V_{DS} = 1 \) V are shown in Fig. 2.3(a). It can be observed that for \( V_{DS} = 1 \) V and \( V_{GS} > 0.9 \) V \( C_{GD} \) and \( C_{GS} \) in nMOSFET are equal and are half of \( C_{ox} \).

![Figure 2.3](image)

**Fig. 2.3.** (a) \( C_{GD} \) and \( C_{GS} \) in nTFET and nMOSFET are extracted with various \( V_{GS} \) at \( V_{DS} = 1 \) V. Compared with nMOSFET, the asymmetric partitioning of gate capacitances \( C_{GS} \) and \( C_{GD} \) is observed in an nTFET. This is related to a key difference in inversion charge distribution in TFET and MOSFET. The nMOSFET is not optimized and has a threshold voltage of -0.15 V. (b) Under inversion bias (high \( V_{GS} \)), the electron inversion layer is formed in the channel of nTFET, and it connects to the n⁺ drain. (c) Under inversion bias (high \( V_{GS} \)), the electron inversion layer is formed in the channel of nMOSFET. The electron inversion layer connects to both n⁺ source and n⁺ drain.
while $C_{GD}$ in nTFET is much larger than $C_{GS}$. It should be noted that the nMOSFET is not optimized and has a threshold voltage of -0.15 V. When sufficient $V_{GS}$ is applied, the inversion layer is formed in the channel, and the partitioning of $C_{GG}$ in a TFET is significantly different from that in a MOSFET. This is fundamentally due to the difference in the inversion charge $Q_{inv}$ distribution between TFET and MOSFET, which is caused by their different device structures. An nMOSFET has a symmetric n$^+$-p-n$^+$ structure. It is well known that when an nMOSFET operates in the linear region [$V_{GS} > 0.9$ V with $V_{DS} = 1$ V in Fig. 2.3(a)], both source and drain regions are connected to the electron inversion layer as illustrated in Fig. 2.3(c), and gate capacitance is symmetrically partitioned between the source and the drain, leading to $C_{GD} \approx C_{GS} \approx C_{GG}/2$. In the saturation region [$0 < V_{GS} < 0.9$ V with $V_{DS} = 1$ V in Fig. 2.3(a)], $C_{GS} \approx 2/3\cdot C_{GG}$, and $C_{GD} \approx 0$ for a MOSFET. On the other hand, an nTFET has an asymmetric p$^+$-p-n$^+$ structure. When an nTFET is switched on, the electron inversion layer formed in the channel connects to the n$^+$ drain as illustrated in Fig. 2.3(b). The magnitudes of $C_{GD}$ and $C_{GS}$ are not equal, and $C_{GD}$ constitutes a larger fraction of total gate capacitance.

In order to have a clear view of how the inversion carriers distribute in TFET, the 2D distribution contours of electron concentration $n$ are plotted for $V_{GS} = V_{DS} = 0$ V, $V_{GS} = 1$ V with $V_{DS} = 0$ V, and $V_{GS} = V_{DS} = 1$ V in Fig. 2.4. Comparing Fig. 2.4 (a) and (b), it can be observed that as $V_{GS}$ increases from 0...
Fig. 2.4. Two-dimensional distribution contours of electron concentration \( n \) in the substrate of nTFET when (a) \( V_{GS} = 0 \) V and \( V_{DS} = 0 \) V, (b) \( V_{GS} = 1 \) V and \( V_{DS} = 0 \) V, and (c) \( V_{GS} = V_{DS} = 1 \) V.

V to 1 V, the electron inversion layer with high electron concentration (\( n = 1 \times 10^{20} \text{ cm}^{-3} \)) is formed in the channel of nTFET. Comparing Fig. 2.4 (b) and (c), it can be observed that as \( V_{DS} \) increases from 0 V to 1 V with fixed high \( V_{GS} (V_{GS} = 1 \) V), the electron inversion layer pinches off at the source side [22].

A complete set of \( C_{GD} \) and \( C_{GS} \) in nTFET at various \( V_{GS} \) and \( V_{DS} \) is extracted, and \( C_{GD} \) and \( C_{GS} \) versus \( V_{GS} \) are shown in Fig 2.5(a) and (b), respectively. For low \( V_{DS} \), such as \( V_{DS} = 0 \) V (white square in Fig. 2.5) or 0.2 V (yellow triangle in Fig. 2.5), before inversion occurs \( |V_{GS} = 0 \) V or negative
Fig. 2.5. (a) and (b) show $C_{GD}$ and $C_{GS}$ as functions of $V_{GS}$ with various $V_{DS}$, respectively. (c) $C_{GD}$, $C_{GS}$ and $C_{GG}$ versus $V_{GD}$, where $V_{GD} = V_{GS} - V_{DS}$ with and $V_s = 0$ V, at various biases in nTFET. In comparison with $C_{GS}$, $C_{GD}$ has a stronger dependence on $V_{GD}$. Fringing capacitance at gate sidewall was also captured in the simulation. The height of the gate $T_{gate}$ is 50 nm.

in Fig. 2.5 (a) and (b)], $C_{GD}$ or $C_{GS}$ comprises parasitic capacitance components, therefore they have small magnitudes. When electron inversion layer starts to form underneath the gate dielectric [$V_{GS} > 0$ V for $V_{DS} = 0$--0.2 V in Fig. 2.5 (a) and (b)], $C_{GD}$ increase and it is dominated by the inversion capacitance between gate and inversion layer $C_{GD,inv}$. To analysis full set of $C_{GD}$ and $C_{GS}$ at various $V_{DS}$ and $V_{GS}$, a clear trend can be observed from the plots of $C_{GD}$, $C_{GS}$ and $C_{GG}$ versus $V_{GD}$ in Fig. 2.5 (c). At a fixed $V_{DS}$, the inversion layer starts to form in the channel of TFET around where $V_{GS} > V_{DS}$, and therefore $C_{GD}$ increases with $V_{GD}$ [Fig. 2.5 (c)] due to the increase of $C_{GD,inv}$ with $V_{GD}$. This can also be observed in $C_{GD}$ - $V_{GS}$ plot along any curve with fixed $V_{DS}$ in Fig. 2.5 (a). For a given $V_{GS}$ ($V_{GS}$ high enough to form
Fig. 2.6. Inversion layer length $L_{inv}$ extracted from TCAD simulation at various $V_{GS}$ and $V_{DS}$. $L_{inv}$ decreases with increasing $V_{DS}$. The arrows indicate the direction of increasing $V_{DS}$ from 0 V to 1 V in steps of 0.2 V.

electron inversion layer), increasing $V_{DS}$ pinches the inversion layer off at the source side [22], leading to a reduction in $C_{GD,inv}$ or $C_{GD}$ with decreasing $V_{GD}$ [Fig. 2.5 (c)]. This can also be observed in Fig. 2.5 (a) along a vertical line from up to bottom. On the contrary, inversion layer pinch-off occurs at the drain side in a MOSFET. $C_{GS}$ versus $V_{GS}$ and $C_{GS}$ versus $V_{GD}$ are shown in Fig. 2.5(b) and (c), respectively. $C_{GS}$ consists of parasitic capacitances. It is smaller than $C_{GD}$ under inversion bias, and is less dependent on $V_{GD}$. $C_{GS}$ drops slightly with increasing $V_{GD}$ [Fig. 2.5(c)] due to the screening of gate-to-source capacitive coupling by the inversion layer. We extracted the length of inversion layer $L_{inv}$ in nTFET, which is measured from the drain-channel junction to the point in the channel where the electron concentration in the inversion layer is equal to the channel doping concentration ($1\times10^{16}$ cm$^{-3}$). $L_{inv}$ versus $V_{GS}$ is shown in Fig. 2.6, and it shows that $L_{inv}$ is controlled by $V_{GD}$. Increasing $V_{GD}$ lengthens $L_{inv}$ until it saturates. $C_{GD,inv}$ follows a similar trend.
2.3 TFET Gate Capacitance Components and Modeling

2.3.1 Fringing Capacitance and Overlap Capacitance

Based on the understanding of physical insight and the values of gate capacitance components from TCAD numerical simulation in Section 2.2.3, a TFET gate capacitance model is built [Fig. 2.7(a)]. The expressions used for the parasitic capacitances are similar to those of MOSFETs [89],[90]. We have

\[
    C_{GD} = C_{of} + C_{dif} + C_{dov} + C_{GD,inv},
\]

\[
    C_{GS} = C_{of} + C_{sif},
\]

as illustrated in Fig. 2.7(a), where \( C_{of} \) is the outer fringing capacitance, \( C_{dov} \) is

![Equivalent circuit used for compact modeling of gate capacitance components in a TFET.](image)

**Fig. 2.7.** (a) Equivalent circuit used for compact modeling of gate capacitance components in a TFET. \( C_{GD} = C_{of} + C_{dif} + C_{dov} + C_{GD,inv} \) and \( C_{GS} = C_{of} + C_{sif} \). (b) Inversion layer length \( L_{inv} \) extracted from TCAD simulation (diamonds) and from compact model (lines) at various \( V_{GS} \) and \( V_{DS} \). \( L_{inv} \) decreases with increasing \( V_{DS} \). The arrows indicate direction of increasing \( V_{DS} \) from 0 V to 1 V in steps of 0.2 V.
the drain overlap capacitance. $C_{\text{dif}}$ and $C_{\text{sif}}$ are the inner fringing capacitances at the drain side and source side, respectively. $C_{\text{of}}$ is given by [89]

$$C_{\text{of}} = (2\varepsilon_{\text{ox}}\varepsilon_0 / \pi) \cdot \ln\left(1 + T_{\text{gate}} / T_{\text{ox}}\right). \tag{2.14}$$

$C_{\text{dov}}$ is given by $C_{\text{ox}} L_{\text{dov}} A(V_{GD})$ where $C_{\text{ox}}$ is the gate oxide capacitance in unit area, $L_{\text{dov}}$ is the overlap length on the drain side, and $A(V_{GD}) = 1/(1 - \lambda V_{GD})$ for $V_{GD} < V_{\text{th,inv}}$ and unity for $V_{GD} \geq V_{\text{th,inv}}$. $\lambda$ is set to be 0.3 in this work to achieve a good fit. $V_{\text{th,inv}}$ is the $V_{GD}$ at which inversion occurs, when $V_{GD} \geq V_{\text{th,inv}}$, $L_{\text{inv}} > 0$. $C_{\text{dif}}$ and $C_{\text{sif}}$ are given by [89],[90]

$$C_{\text{sif}} = \begin{cases} \left(\frac{e_0^2}{\varepsilon_{\text{ox}}^2} \right) e^{-\frac{(V_{GD}-V_{\text{th,inv}})(\varphi_f/2)}{\varepsilon_{\text{ox}}^2}} & \text{for } V_{GD} < V_{\text{th,inv}} \\ \frac{e_0^2}{\varepsilon_{\text{ox}}^2} & \text{for } V_{GD} \geq V_{\text{th,inv}} \end{cases} \tag{2.15}$$

$$C_{\text{dif}} = \begin{cases} \left(\frac{e_0^2}{\varepsilon_{\text{ox}}^2} \right) e^{-\frac{(V_{GD}-V_{\text{th,inv}})(\varphi_f/2)}{\varepsilon_{\text{ox}}^2}} & \text{for } V_{GD} < V_{\text{th,inv}} \\ \frac{e_0^2}{\varepsilon_{\text{ox}}^2} & \text{for } V_{GD} \geq V_{\text{th,inv}} \end{cases} \tag{2.16}$$

with

$$C_{\text{sif, max}} = \frac{1}{6} \frac{e^2}{\varepsilon_{\text{ox}}} \ln\left[1 + \frac{\Delta L_s}{T_{\text{ox}}} \sin\left(\frac{\pi}{2} \frac{\varepsilon_{\text{ox}}}{\varepsilon_{\text{si}}} \right)\right], \tag{2.17}$$

$$C_{\text{dif, max}} = \frac{1}{6} \frac{e^2}{\varepsilon_{\text{ox}}} \ln\left[1 + \frac{\Delta L_d}{T_{\text{ox}}} \sin\left(\frac{\pi}{2} \frac{\varepsilon_{\text{ox}}}{\varepsilon_{\text{si}}} \right)\right], \tag{2.18}$$

where $\Delta L_s$ and $\Delta L_d$ are the extension length of p-type and n-type region into the channel, respectively, overlapping with the gate [Fig. 2.2(b)], and $\varphi_f$ is channel Fermi potential. The source overlap capacitance is negligible in this TFET design. The quantum capacitance $C_Q$ in Si is large ($> 30 \times C_{\text{ox}}$ in this study), and is therefore neglected. It should be noted that $C_Q$ should be taken into account when it is comparable with $C_{\text{ox}}$, e.g. in TFETs employing carbon nanotube or graphene [91],[92].
2.3.2 Inversion Capacitance

The inversion capacitance $C_{GD,\text{inv}}$ is obtained by differentiating $Q_{\text{inv}}$ with respect to $V_G$ [93], i.e. $C_{GD,\text{inv}} = C_{ox}L_{\text{inv}} = \partial Q_{\text{inv}} / \partial V_G$, with

$$Q_{\text{inv}} = C_{ox} \cdot L_{\text{active}} \left[ V_{gsteff,cv} - 0.5A_{\text{bulk}}V_{cveff} + \frac{A_{\text{bulk}}V_{cveff}^2}{12(V_{gsteff,cv} - 0.5A_{\text{bulk}}V_{cveff})} \right],$$

where $L_{\text{active}}$ is the effective gate length, $A_{\text{bulk}}$ is body effect factor, and $V_{gsteff,cv}$ and $V_{cveff}$ are smoothening functions for $(V_{GD} - V_{th,\text{inv}})$ and effective $V_{DS}$, respectively [93]. The inversion charge $Q_{\text{inv}}$ is entirely partitioned to the drain to capture the charge distribution in the TFET.

Fig. 2.8. $C_{GD}$ and $C_{GS}$ obtained from TCAD (diamonds) and from compact model (lines). The arrows indicate direction of increasing $V_{DS}$ from 0 V to 1 V in steps of 0.2 V. Good agreement between TCAD data and compact model is achieved.
The gate capacitance model achieves reasonably good agreement with TCAD numerical simulation as shown in Fig. 2.8. All the components in the model are physical, and the model describes the dependence of $C_{GD}$ and $C_{GS}$ on terminal voltages very well. It should be noted the smoothening functions affect the shape of $C_{GD}$ curves, and may be further tweaked for better fitting.

### 2.4 Reduction of Gate-to-Drain Capacitance

$C_{GD}$ is the Miller capacitance of an nTFET, and its value is important for analysis of circuits containing TFETs. Next, we investigate the impact of gate material on $C_{GD}$. $C_{GD}$ in nTFETs with metal gate and n$^+$ poly-Si gate are compared at $V_{DS} = 0$ V and 1 V in Fig. 2.9. $C_{GD}$ is dominated by

![Fig. 2.9.](image)

TCAD simulated $C_{GD}/C_{ox}$ for TFETs with gradual drain doping profiles and metal gate (solid squares) with work function of 4.05 eV or n$^+$ poly-Si gate (open squares). Solid lines are for $V_{DS} = 1$ V, and short dashed lines are for $V_{DS} = 0$ V. TFET with poly-Si gate has a lower $C_{GD}$ than the one with metal gate in the inversion region (high $V_{GD}$) due to the depletion in poly-Si gate.
inversion capacitance for high $V_{GD}$ (right portion of Fig. 2.9), and a TFET with poly-Si gate has a lower $C_{GD}$ than the one with metal gate due to additional depletion capacitance in poly-Si gate when high $V_{GS}$ is applied.

To further improve the TFET switching speed, parasitic capacitances should be reduced. The main parasitic capacitance components in a TFET with a gradual drain junction [structure (1) in Fig. 2.10] are the fringing capacitances ($C_{sif}, C_{dif}, C_{of}$) and the overlap capacitance ($C_{dov}$). By varying the position of the drain-channel junction with respect to the gate edge, e.g. by controlling the drain dopant profile, $C_{dov}$ and $C_{of}$ can be adjusted. Two approaches for reducing parasitic capacitance are considered: Use of abrupt drain doping [structure (2) in Fig. 2.10] and offset drain [structure (3) in Fig. 2.10]. Before inversion occurs, i.e. at negative or low $V_{GD}$, $C_{GD}$ is dominated by parasitic capacitances. The parasitic capacitance components of $C_{GD}$ can be reduced by using an abrupt drain junction instead of a gradual drain junction as shown in Fig. 2.10.

Shifting or offsetting the gradual drain profile with a doping gradient of 5 nm/decade by 20 nm, i.e. comparing structures in (1) and (3), can also give a significant reduction in parasitic capacitance. However, it should be noted that the drain offset also increases the drain resistance and reduces $I_{on}$. A more detailed study of its effect on switching speed may be investigated in the future.
Fig. 2.10. TCAD simulation results showing the difference in $C_{GD}/C_{ox}$ for various TFET structures with metal gate: (1) TFET with gradual drain doping profile, (2) TFET with abrupt drain doping profile; (3) TFET with offset drain having a gradual doping profile. Solid lines are for $V_{DS} = 1$ V, and short dashed lines are for $V_{DS} = 0$ V.

In the on-state, reducing $L_G$ gives a smaller $L_{inv}$ and a smaller $C_{GD,inv}$. When $L_G$ is reduced from 50 nm to 25 nm, $C_{GD}$ is significantly reduced in the inversion region without appreciable change in $I_{on}$, as shown in Fig. 2.11. $L_G$ scaling for TFET should reduce the intrinsic delay $\tau$ Eq. (2.1)] in addition to circuit density.
Fig. 2.11. Comparison of simulated (a) $C_{GD}$-$V_{GS}$ (solid symbols, left axis) and (b) $I_{DS}$-$V_{GS}$ (open symbols, right axis) curves for TFETs with gate length of 50 nm (square) and 25 nm (triangle). The metal gate has a work function of 4.05 eV.

2.5 Conclusions

The dependence of TFET gate capacitances on terminal voltages was studied using a physics-based TCAD simulator. Different from MOSFET, when inversion layer is formed in the channel, the total gate capacitance $C_{GG}$ of TFET is asymmetrically partitioned into $C_{GD}$ and $C_{GS}$, and this is a special feature of TFET and can be used to verify the TFET device structure in experimental work (to be discussed in Section 6.4.3). $C_{GD}$ is much larger than $C_{GS}$, and it is the dominating component of $C_{GG}$. The capacitance components in $C_{GD}$ and $C_{GS}$ are decoupled at various biases, and their impact on total gate capacitance was discussed. The compact model of TFET gate capacitance was
developed, and good agreement with TCAD data was achieved. $C_{GD}$ can be reduced through design optimization for the drain dopant profile, and by scaling of the gate length.
Chapter 3

Tunneling Field-Effect Transistors with Extended Source Structures: Simulation Study

3.1 Introduction

Tunneling field-effect transistors (TFETs) with sub-60 mV/decade subthreshold swing $S$ have been demonstrated experimentally, but achieving on-state current $I_{on}$ comparable with state-of-the-art complementary metal oxide semiconductor (CMOS) is challenging [45]-[74]. Research efforts have been devoted to improve $I_{on}$. $I_{on}$ in TFETs can be significantly enhanced by tuning the band alignment between the source and channel via bandgap engineering [16],[21],[30],[36],[48],[50],[53]-[55],[62]-[65]. With incorporation of small bandgap materials such as germanium and III-V compounds at the source side [64],[65], the formation of a well-designed heterojunction at the source-channel edge could reduce the tunneling barrier width and could therefore increase the band-to-band tunneling (BTBT) rate and $I_{on}$ in TFETs as mentioned in Chapter 1. In addition, by adopting the multi-gate device architecture and high-$k$ metal gate stack, the BTBT rate in TFETs could be further increased by improving the electrostatic control of the gate over the channel [12],[15],[18],[57],[45].
Geometry optimization of TFET has also been investigated through simulations [12]-[15],[18]-[21],[30],[32],[34]-[37],[39]. The spatial profile of the source, or the shape of the source in a TFET cross-section, can be designed or customized to affect the electric field distribution in the tunneling region, thereby enhancing $I_{on}$. Designs, such as extended source structures, have been proposed [17],[56].

In this Chapter, we report a detailed simulation study of various designs of extended source structure in an n-channel double-gate (DG) TFET to enhance the drive current [94],[95]. The extended $p^+$ source may comprise the same material as the body, such as Ge source in a Ge body TFET. The extended source may also comprise a material different from the body, such as Ge source in a Si body TFET. Different source shapes were investigated, and the device physics is discussed. By employing an extended source structure (Fig. 3.1), the $p^+$ source region extends into the middle of the body under the gate. When the device is in on-state, high electric field $\xi$ extends along the $p^+$ junction edge and many short tunneling paths are formed, therefore boosting $I_{on}$. The degree of on-state current enhancement depends on the shape of the extended source structure, which affects the distribution and magnitude of the high $\xi$-field at the source junction region.
3.2 Device Structure and Methodology

Device simulation was performed using our in-house two-dimensional (2D) technology computer-aided design (TCAD) simulator which implements a physics-based non-local BTBT algorithm [84]. The algorithm automatically identifies the tunneling paths in a device structure using a 2D extension of Wentzel–Kramers–Brillouin (WKB) method [79]-[81]. The calculation of BTBT carrier generation rate \( G_{BTBT} \) is based on the tunneling probability and carrier concentrations at the starting and ending nodes of the tunneling paths, and the generation rate is then captured in the current continuity equations. The current continuity and Poisson equations are self-consistently solved using the Newton’s iteration method. The details of the algorithm implementation have been discussed in Chapter 2. The algorithm is designed to be robust and the converged electrical results are checked for mesh grid independence [84].

The TFET structure investigated in this work is a double-gated \( p^+-p^-\)-\( n^+ \) diode with an abrupt source-channel \( (p^+-p^-) \) junction. The key parameters used are listed in Table 3.1.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source Doping ( N_A )</td>
<td>( 1\times10^{20} ) cm(^{-3} ) (n-type)</td>
</tr>
<tr>
<td>Drain Doping ( N_D )</td>
<td>( 1\times10^{19} ) cm(^{-3} ) (n-type)</td>
</tr>
<tr>
<td>Body Doping ( N_{body} )</td>
<td>( 5\times10^{16} ) cm(^{-3} ) (p-type)</td>
</tr>
<tr>
<td>Gate Length ( L_G )</td>
<td>50 nm</td>
</tr>
<tr>
<td>Body Thickness ( T_{body} )</td>
<td>20 nm</td>
</tr>
<tr>
<td>Gate Work Function ( \Phi_M )</td>
<td>4.11 eV</td>
</tr>
<tr>
<td>Equivalent Silicon Oxide Thickness ( EOT )</td>
<td>0.8 nm</td>
</tr>
</tbody>
</table>
For analysis of electrical characteristics, the off-state current $I_{off}$ is defined to be the drain current $I_{DS}$ at $V_{DS} = 0.7$ V and $V_{GS} = 0$ V while $I_{on}$ is defined at $V_{DS} = V_{GS} = 0.7$ V. The average subthreshold swing $S$ (also denoted as ‘Average S’) is obtained from a section of the $I_{DS}$-$V_{GS}$ curve where $I_{DS}$ varies from $10^{-12}$ A/µm to $10^{-6}$ A/µm.

### 3.3 Simulation of TFETs with Extended Source

#### 3.3.1 Ge TFET with Wedge-Shaped Extended Source

![Cross-sections](image)

**Fig. 3.1.** Cross-sections of (a) control double-gate Ge TFET and (b) double-gate Ge TFET with wedge-shaped extended source. As indicated, $L_{extend}$ is the distance the source region extends from the gate edge into the channel. $E_{f, source}$ refers to the Fermi level at source side. $E_c$ surface, $E_v$ surface, and $E_{f, source}$ plane for the devices in (a) and (b) are plotted in (c) and (d), respectively. The energy band diagrams were obtained at $V_{DS} = V_{GS} = 0.7$ V. In (b) and (d), $L_{extend} = 10$ nm.
The structures of control Ge TFET and Ge TFET with wedge-shaped extended source are illustrated in Fig. 3.1(a) and (b), respectively. In Fig. 3.1(b), the amount of extension of the wedge-shaped source into the channel is denoted as $L_{\text{extend}}$. By default, $L_{\text{extend}}$ is set to be 10 nm. The source is grounded. In the on-state ($V_{\text{DS}} = V_{\text{GS}} = 0.7$ V), the 2D surface plots of energy band diagram are shown in Fig. 3.1(c) and (d) for the control Ge TFET and the Ge TFET with wedge-shaped extended source, respectively. The source side Fermi level $E_{\text{f, source}}$ is used as an energy reference, where energy $E$ is 0 eV. Valence electrons below $E_{\text{f, source}}$ in the source side are available for BTBT if the tunneling distance is short enough, e.g. much less than 20 nm.

In the following discussion, the intercept between a constant energy plane ($E$ plane) and the conduction band $E_c$ surface is a curve denoted by $E_{c, \text{front}}$, and the intercept between the $E$ plane and a valence band $E_v$ surface is a curve denoted by $E_{v, \text{front}}$ as shown in Fig. 3.1(c) and (d). The separation between the $E_{c, \text{front}}$ and $E_{v, \text{front}}$ curves determines the tunneling distance on this $E$ plane. At an energy level $E = E_{\text{f, source}}$, the separation between $E_{c, \text{front}}$ and $E_{v, \text{front}}$ in the control Ge TFET [Fig. 3.1(a)] is generally larger than 5 nm except in the regions near the surface of the body where the dominant tunneling areas are found [Fig. 3.1(c)]. In the Ge TFET with wedge-shaped extended source [Fig. 3.1(b)], the tunneling distance in the middle of the body region is significantly reduced [Fig. 3.1(d)] as compared to that in the control device and the separation between $E_{c, \text{front}}$ and $E_{v, \text{front}}$ is generally closer. As a result, it is expected that BTBT will be enhanced in the Ge TFET with wedge-shaped extended source as compared with the control Ge TFET.
Fig. 3.2. Electric field $\xi$ distribution near source-channel junction in (a) control Ge TFET and (b) Ge TFET with wedge-shaped extended source at $V_{DS} = V_{GS} = 0.7$ V. In both devices, the electric field is highest at the source-channel junction near the gate edge, decreasing towards the middle of the body. In the region where $5 \text{ nm} < y < 15 \text{ nm}$, the $E_c = E_{f,source}$ curve is nearer to the $E_v = E_{f,source}$ curve in the device with wedge-shaped extended source, indicating that tunneling path is shortened. This contributes to the enhancement of tunneling current. In (b), $L_{\text{extend}} = 10 \text{ nm}$. 
Region with high $\xi$-field and low $G_{BTBT}$

Region with high $\xi$-field and low $G_{BTBT}$

**Fig. 3.3.** BTBT generation rate contours and tunneling paths ($V_{DS} = V_{GS} = 0.7$ V) are shown for (a) control Ge TFET and (b) Ge TFET with wedge-shaped extended source. The tunneling paths plotted are the dominant tunneling paths that contribute to 40% of the total current, while other paths with small contributions are not shown. The gray lines indicate the source-channel edges. In (b), $L_{extend} = 10$ nm.

The distributions of $\xi$-field magnitude and $G_{BTBT}$ near the source-channel junction in the on-state ($V_{DS} = V_{GS} = 0.7$ V) are compared in Fig. 3.2 and Fig. 3.3, respectively. Electric field directing from $p^-$ to $p^+$ region determines the amount of band bending from the source to the channel. When the band bending is larger than the Ge bandgap $E_{g,Ge}$ within a small distance (a few nm), significant BTBT occurs. In other words, the high $G_{BTBT}$ (more than $10^{30}$ cm$^{-3}$s$^{-1}$) should appear only when the band bending or the integral of $\xi$-
field along a short tunneling path exceeds $E_{g,Ge}$. In the control device, high $\xi$-field above 1.5 MV/cm appears within a small region at the source-channel junction within 5 nm underneath the gates [Fig. 3.2(a)]. The tunneling paths are therefore located within 5 nm underneath the gates [Fig. 3.3(a)]. On the other hand, for the Ge TFET with wedge-shaped extended source, an extensive high $\xi$-field region is observed along source-channel edge as shown in Fig. 3.2(b). As a result, dense and spatially distributed tunneling paths can be found in the high $\xi$-field region [Fig. 3.3(b)]. The high $\xi$-field region is distributed along $p^+-p^-$ junction, leading to a larger region available for electrons to tunnel from source to channel. The total tunneling current is therefore increased at the on-state for the Ge TFET with wedge-shaped extended source.

It should be noted that in both devices, there are some regions with high $\xi$-field but low $G_{BTBT}$, and such regions are typically located at the surface of channel near the gate edges (Fig. 3.3). These are regions where the band bending is less than $E_{g,Ge}$ and no tunneling paths exist, although $\xi$-field is high. From consideration of physics in BTBT, the existence of these spatial regions with high $\xi$-field but low $G_{BTBT}$ is expected. However, they cannot be captured in earlier TCAD simulations based on the local Kane’s model [83]. The local Kane’s model treats the BTBT carrier generation rate as a function of local $\xi$-field, and places the generated electron-hole pairs at each spatial point where the local generation rate was calculated. This is not physically accurate since BTBT is a nonlocal process.
Fig. 3.4. For both control Ge TFET and Ge TFET with wedge-shaped extended source, the device bodies are each partitioned into 20 horizontal strips with equal width of 1 nm. For each strip, the average current densities $J_{pi}$ at source-channel edge under various $V_{GS}$ bias are extracted. The $J_{pi}-V_{GS}$ plots for control Ge TFET and Ge TFET with wedge-shaped extended source are shown in (a) and (b), respectively.

To further investigate the electrical characteristics of the Ge TFET with wedge-shaped extended source compared with the control Ge TFET, the bodies of both devices are partitioned into many horizontal strips with equal width $\Delta w$ of 1 nm (Fig. 3.4). In each strip, indexed by $i$, the average hole current density ($J_{pi}$) at the source-channel edge as a function of $V_{GS}$ in low $V_{GS}$ region ($V_{GS} < 0.16$ V) is obtained. Note that $I_{DS} = \sum_i J_{pi} \cdot \Delta w$, where $i = 1, 2,$
As the device is symmetrical about a mirror line at \( y = 10 \) nm, only the strips in the top half of the device are considered, i.e. \( i = 1, 2, 3 \ldots 10 \). \( J_{pi} - V_{GS} \) curves for control Ge TFET and Ge TFET with wedge-shaped extended source are plotted in Fig. 3.4(a) and (b), respectively.

We define \( V_{G0i} \) as the \( V_{GS} \) at which the point swing is a minimum \( (S_{min}) \) for a \( J_{pi} - V_{GS} \) curve. The distribution of \( V_{G0i} \) and corresponding \( S_{min} \) for various strips in control Ge TFET and Ge TFET with wedge-shaped extended source are presented in Fig. 3.5. Compared with the control device, the

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**Fig. 3.5.** (a) \( V_{G0i} \) is defined as the \( V_{GS} \) where minimum point \( S \) \( (S_{min}) \) is located for each \( J_{pi} \). The distribution of \( V_{G0i} \) in Ge TFET with wedge-shaped extended source is tighter than that of the control device. (b) Cumulative distributions of \( S_{min} \) for each \( J_{pi} \) in control Ge TFET and Ge TFET with wedge-shaped extended source are compared. \( S_{min} \) in Ge TFET with wedge-shaped extended source is more uniform than that of the control device.
standard derivation of $V_{GOi}$ in Ge TFET with wedge-shaped extended source is smaller [Fig. 3.5(a)], indicating that current densities in many of the strips rise sharply at around the same $V_{GS}$. In addition, the values of $S_{min}$ for each strip are almost the same for the Ge TFET with wedge-shaped source, as shown by the cumulative plot of $S_{min}$ in Fig. 3.5(b). From Fig. 3.4 and 3.5, it is observed that the current density along source-channel edge is more uniform in the Ge TFET with wedge-shaped extended source, and its components ($J_{pi}$) rise in a more concerted manner as $V_{GS}$ increases, as compared with the control device. This is due to the improved uniformity of $\xi$-field at source-channel junction, and BTBT therefore occurs uniformly at almost the same $V_{GS}$ in the TFET with wedge-shaped extended source [Fig. 3.2(b)]. As a result, the extended source design improves the subthreshold swing.

Fig. 3.6 reveals the impact of the extended source design on $I_{DS}$-$V_{GS}$ characteristics. $I_{on}$ is increased, and $S$ is reduced slightly with adoption of the

![Graph](image)

**Fig. 3.6.** $I_{DS}$-$V_{GS}$ curves for Ge TFET with wedge-shaped extended source (solid lines) and control Ge TFET (dashed lines).
Fig. 3.7. Comparison of $I_{DS}$-$V_{GS}$ characteristics of wedge-source Ge TFETs with increasing $L_{extend}$ ($L_{extend} = 5$ nm, 10 nm, 15 nm).

extended source structure. $I_{off}$ is not substantially affected. The impact of varying $L_{extend}$ on $I_{DS}$-$V_{GS}$ characteristics of Ge TFET with wedge-shaped extended source is investigated next.

A set of $I_{DS}$-$V_{GS}$ curves for TFETs with $L_{extend}$ of 5, 10, and 15 nm is shown in Fig. 3.7. It is observed that all TFETs with wedge-shaped source show higher $I_{on}$ and steeper $S$ as compared to the control TFETs, with $I_{off}$ being unchanged. The larger tunneling area introduced by the extended or wedge-shaped source increases the volume-integrated tunneling rate, leading to higher $I_{on}$ as compared with the control TFET. The variation of $I_{on}$ and average swing $S_{ave}$ with $L_{extend}$ is illustrated in Fig. 3.8, showing that increasing $L_{extend}$ improves both $I_{on}$ and $S_{ave}$.
Fig. 3.8.  (a) $I_{on}$ and $I_{on}/I_{off}$ are improved as $L_{extend}$ increases (from 0 to 15 nm) in Ge TFET with wedge-shaped extended source. (b) Average swing $S_{ave}$ is reduced as $L_{extend}$ increases (from 0 to 15 nm) in Ge TFET with wedge-shaped extended source. $S_{ave}$ is the average subthreshold swing obtained from a section of the $I_{DS}$-$V_{GS}$ curve where $I_{DS}$ varies from $10^{-12}$ A/µm to $10^{-6}$ A/µm.

3.3.2 TFETs with Wedge-Shaped Ge Source and Si Body

The Ge-Si heterojunction has been investigated as a source-channel junction in TFETs [14],[53],[55],[27]. In this Section, the Ge-Si heterojunction is employed in TFETs with an extended-source design, and the device performance is evaluated. Fig. 3.9(a) shows the structure of a TFET with wedge-shaped Ge source and Si body, which will be used in the following simulation study.
(a) The schematic of double-gate TFET with Ge wedge-shaped source and Si body. Along the surface cutline (A-A’) near source-channel interface, the doping profile and hole concentration are shown in (b), while the band diagrams of Ge-Si heterojunction are shown in (c) at $V_{DS} = 0.7$ V and $V_{GS} = 0$ V. The large valence band offset ($E_{v_{offset}}$) at the Ge-Si heterojunction improves the off state leakage. The conduction band offset ($E_{c_{offset}}$) reduces the band-to-band tunneling width, leading to $I_{on}$ enhancement.

The device parameters are the same as the ones in Table 3.1 except the gate work function, which was adjusted so that $I_{DS}$ rises at the same $V_{GS}$ as the all-Ge TFET with extended source in the previous Section. The profiles of acceptor doping concentration $N_A$ and hole concentration near the source-channel edge (along A-A’) in Fig. 3.9(b) illustrate the box-like abrupt source junction. The energy band alignment between $p^+$ Ge and $p^-$ Si is shown in Fig. 3.9(c). Between Ge and Si, the valence band offset $E_{v_{offset}}$ is $\sim 0.5$ eV and the conduction band offset $E_{c_{offset}}$ is 0.05 eV.
For TFETs designed with wedge-shaped extended source ($L_{\text{extend}} = 10$ nm), $I_{DS}-V_{GS}$ characteristics are compared with those of all-Ge TFET and TFET with Ge source and Si body (Ge-Si TFET). The gate work function ($\Phi_M$) used in Ge-Si TFET was adjusted so that the devices roughly turn on at the same $V_{GS}$. Therefore, $\Phi_M = 4.3$ eV is used for the Ge-Si TFET in this plot. By employing Ge-Si heterojunction, $I_{on}$ and $I_{on}/I_{off}$ ratio are enhanced and $S_{ave}$ is reduced.

TFET with wedge-shaped Ge source and Si body was simulated and shown in Fig. 3.10 (gray dash-dot line). The tunneling current in a TFET with Ge source and Si body is higher than that in an all-Ge TFET at on-state. This is related to the band bending or $\xi$-field at the Ge-Si heterojunction. At a fixed $V_{GS}$ and $V_{DS}$, $E_c$ in TFET with Ge source and Si body bends more in the channel region adjacent to the source as compared with that in all-Ge TFETs ($E_{c,\text{all-Ge}}$) [Fig. 3.9 (c)]. This is mainly due to the additional $E_{c,\text{offset}}$ (0.05 eV) at Ge-Si interface as well as the smaller permittivity of Si channel compared with Ge channel. Therefore, the electron tunneling barrier width at the Ge-Si
heterojunction is smaller than that in the all-Ge source-channel junction, leading to a higher $I_{on}$ in TFET with Ge source and Si body [27].

For a fairer comparison, the gate work function ($\Phi_M$) used in the TFET with Ge source and Si body was adjusted so that turn-on behavior of the $I_{DS}$-$V_{GS}$ curve roughly matches that of the all-Ge TFET. We define $V_{onset}$ to be the maximum gate voltage in the off-state leakage floor region of the $I_{DS}$-$V_{GS}$ curve, i.e. the onset of $V_{GS}$ where $I_{DS}$ starts to rise. $V_{onset}$ for the devices are matched in Fig. 3.10. The TFET with wedge-shaped Ge source and Si body has an adjusted $\Phi_M$ of 4.3 eV. In all the following Ge-Si TFET simulations, device parameters are the same as the ones in Table 3.1 except that $\Phi_M = 4.3$ eV was used. By incorporating the Ge-Si heterojunction as the source-channel junction in TFET with extended source, $I_{off}$ is reduced about 2 orders of magnitude as compared with the all-Ge TFET (Fig. 3.10), and is in the same order of magnitude as the $I_{off}$ in an all-Si TFET. The $I_{off}$ reduction is related to the large band gap of Si in the channel and in the drain, which effectively suppresses both drain-side BTBT and the thermal carrier generation in the subthreshold regime.

Fig. 3.11 shows a set of $I_{DS}$-$V_{GS}$ curves for TFETs with Si body and Ge source having $L_{extend}$ of 5, 10, and 15 nm. It is observed that $I_{on}$ increases with increasing $L_{extend}$. The enhancement of $I_{on}$ with $L_{extend}$ in TFETs with Ge source and Si body is more pronounced than that in all-Ge TFETs. Up to 93% $I_{on}$ enhancement ($\Delta I_{on}$) can be achieved by increasing $L_{extend}$ from 0 to 15 nm.
Fig. 3.11. $I_{\text{on}}$ in TFET with Ge wedge-shaped source and Si body is improved as $L_{\text{extend}}$ increases from 0 to 15 nm in step of 5 nm. $I_{\text{on}}$ enhancement due to the source extension is more obvious in Ge-Si TFET than in all-Ge TFET. For $L_{\text{extend}} = 15$ nm, $I_{\text{on}}$ increases by 93% in Ge-Si TFET, while $\Delta I_{\text{on}}$ is 72% in all-Ge TFET.

It should be noted that, in reality, the strain is introduced at Ge-Si heterojunction, which is not considered in this simulation. Even higher $I_{\text{on}}$ is expected if the strain effect at the Ge-Si interface is taken into account. This is because the strain splits conduction and valence bands, and causes a smaller energy difference between $E_v$ in Ge and $E_c$ in Si. This leads to a smaller BTBT barrier, and therefore higher tunneling current in the on-state (Fig. 3.12).
Fig. 3.12. Illustration of band diagrams of Ge-Si heterojunction as source-channel junction in a TFET. Strain-free Ge-Si band alignment is illustrated in (a). The band diagram shown in (b) takes strain effect into account. The compressive strain in Ge splits $E_v$ into light hole (LH), heavy hole (HH), and spin-orbit split-off bands, and the tensile strain in Si splits $E_c$ into $\Delta 2$ and $\Delta 4$, causing the reduction in BTBT barrier and leading to higher $I_{on}$ of TFET.

3.4 Analysis of Extended Source with Different Shapes

Besides the wedge-shaped source, another two types of extended source structures, namely arc-shaped and squarish shaped extended sources, are also investigated. Fig. 3.13 illustrates the structures of DG TFET with Si body and different shapes of Ge extended source. The corresponding $I_{DS}-V_{GS}$ characteristics are compared in Fig. 3.14, while $I_{on}$ and $S_{av}$ are summarized in Fig. 3.15.
Fig. 3.13. Band-to-band generation rate contours are plotted for Ge-Si TFETs with three different shapes of extended Ge source with $L_{\text{extend}} = 10$ nm: (a) arc-shape, (b) wedge-shape, and (c) square-shape, in the on-state ($V_{DS} = V_{GS} = 0.7$ V). The location of BTBT depends on the shape of the extended sources, and therefore device performance is affected.

A TFET with Si body and arc-shaped Ge source can be realized experimentally by a recess etch at the source side followed by an epitaxial growth of Ge with in situ $p^+$ doping. As compared with Ge-Si TFETs with other source shapes, it has a smaller $I_{on}$ enhancement over the control. In a TFET with Si body and arc-shaped Ge source, the $p^+$ source region only extends slightly into the channel region, and the source-channel region with high $\xi$-field is not substantially expanded as compared with the control device. The increase in the tunneling area is small as observed in Fig. 3.13(a). This explains the small improvement in $I_{on}$ (Fig. 3.14).
Fig. 3.14. \( I_{DS} - V_{GS} \) characteristics of TFETs with Si body and three different shapes of Ge extended sources: arc-shape, wedge-shape and squarish-shape. The shape of Ge extended source has an impact on device output characteristics.

In a TFET with Si body and wedge-shaped Ge source, which extends further into the middle of the body or channel region as compared with the arc-shaped source, a more substantial enhancement in \( I_{on} \) and \( S \) can be observed (Fig. 3.14 and 3.15). The wedge-shaped source structure can be realized by an advanced etch technique to form an \( \Sigma \)-shaped recess, followed by selective epitaxy of the source material. This source recess etch and epitaxy process have been developed for p-channel MOSFETs [96],[97]. Among the three source designs considered in Fig. 3.13, TFET with Si body and squarish Ge extended source gives the largest \( I_{on} \) and smallest \( S_{ave} \).
Fig. 3.15. Summary of $I_{on}$ enhancement and $S_{ave}$ reduction in TFETs with Si body and three different shapes of Ge extended sources: arc-shape, wedge-shape and squarish-shape. Among the three devices, TFET with Si body and squarish Ge source has highest $I_{on}$ (~0.8 mA/µm) and the smallest $S_{ave}$. $S_{ave}$ is the average subthreshold swing obtained from a section of the $I_{DS}$-$V_{GS}$ curve where $I_{DS}$ varies from $10^{-12}$ A/µm to $10^{-6}$ A/µm.

The squarish Ge extended source design features a source-channel heterojunction that is parallel to the gate dielectric interface. This leads to a large region with high $\xi$-field that is very uniformly distributed. In addition, the corners in the squarish source structure also lead to high $\xi$-field and contribute to the large tunneling current. The TFET with Si body and squarish Ge extended source gives a drive current of more than 0.8 mA/µm at $V_{DS} = V_{GS} = 0.7$ V and an $I_{on}/I_{off}$ ratio of around 11 orders of magnitude.
3.5 Conclusion

The impact of extended source structures in DG all-Ge and Ge-Si TFETs were investigated in detail using a 2D TCAD simulation tool. In the on-state, extended source structures increase the tunneling area, increase the total band-to-band generation current and boost $I_{on}$. In addition, an extended source structure also improves $S$ slightly, due to the better uniformity of the high $\tilde{\varsigma}$-field at the source-channel junction. For TFET with Si body and Ge extended source, device performance is further improved in terms of $I_{on}$ and $S$. The larger the $L_{extend}$, the larger the improvement in $I_{on}$ and $S$. Three different extended source shapes were investigated: wedge-shape, arc-shape and squarish shape. TFET with squarish Ge source and Si body outperformed the other designs studied in this work, giving a drive current of more than 0.8 mA/µm at $V_{DS} = V_{GS} = 0.7$ V and an $I_{on}/I_{off}$ ratio of around 11 orders of magnitude. The extended source design is effective in boosting $I_{on}$ of TFET, and it could also be applied in multi-gate TFETs with other channel materials such as III-V compound semiconductors.
Chapter 4

Simulation Study on Germanium-Tin N-Channel Tunneling Field-Effect Transistor: Simulation Study

4.1 Introduction

Tunneling field-effect transistors (TFETs) with subthreshold swing ($S$) below 60 mV/decade have been demonstrated experimentally [48]-[51],[53],[56],[61], but achieving on-state current $I_{on}$ comparable with that of state-of-the-art high-performance complementary metal-oxide semiconductor (CMOS) is challenging. There have been many research efforts directed at improving $I_{on}$ of TFETs, and one effective approach employs bandgap engineering. Materials with smaller bandgaps, such as germanium (Ge), indium gallium arsenide (InGaAs) and indium arsenide (InAs), have been used in the tunneling regions of TFETs to boost $I_{on}$ [49], [54],[63]-[65], [67], [69]-[71]. In addition, direct BTBT is preferred for TFET operation, as tunneling of electrons from valence band ($E_v$) to conduction band at Γ-point ($E_{c,\Gamma}$) without a change in momentum gives rise to a higher $I_{on}$ than indirect BTBT [38],[98],[99]. Therefore, a direct bandgap material is desired for use in TFET device design.
Besides III-V compound semiconductors, germanium-tin alloy (Ge$_{1-x}$Sn$_x$) has emerged as a promising material to realize a direct and small bandgap through tuning the Sn composition $x$ [100]-[119]. Moreover, as a group IV material, Ge$_{1-x}$Sn$_x$ may be more process compatible or more easily integrated with silicon-based CMOS technology as compared to III-V compound semiconductors. These considerations make Ge$_{1-x}$Sn$_x$ an attractive material for TFET device design.

In this work, the device physics of Ge$_{1-x}$Sn$_x$ n-channel TFETs with $x$ varying from 0 to 0.2 is investigated. Based on electronic band structures calculated by non-local Empirical Pseudopotential Method (EPM), the BTBT related material parameters of Ge$_{1-x}$Sn$_x$ alloys are obtained. Two-dimensional (2D) technology computer-aided design (TCAD) simulation study on Ge$_{1-x}$Sn$_x$ TFET is also performed for the first time. The objective is to examine the potential of high quality Ge$_{1-x}$Sn$_x$ with high Sn composition, which may be realized in the future, for application in TFETs. Both the direct BTBT from $E_v$ to $E_{c,\Gamma}$ and the indirect BTBT from $E_v$ to conduction band at $L$-point ($E_{c,L}$) are calculated, which are denoted by “direct $\Gamma$ - $\Gamma$ BTBT” and “indirect $\Gamma$ - $L$ BTBT,” respectively. Simulation results show that by employing Ge$_{1-x}$Sn$_x$ in TFETs, an enhancement in drive current and $S$, as compared with Ge TFET, can be achieved.

4.2 Extraction and Calculation of Material Parameters

The band structures of Ge$_{1-x}$Sn$_x$ alloys have been studied both theoretically [100]-[106] and experimentally [107]-[119], and the transistor fabrication has been demonstrated [120]-[123]. The reported Sn
Fig. 4.1. (a) Composition dependence of Ge$_{1-x}$Sn$_x$ bandgap at Γ-valley ($E_{g,\Gamma}$) and $L$-valley ($E_{g,L}$) for Ge$_{1-x}$Sn$_x$ alloy. Symbols are experimental data and the lines are obtained from EPM calculations. For Ge$_{1-x}$Sn$_x$ alloys with Sn composition $x$ below 0.11, the conduction band minimum is at $L$-point, and the alloy is an indirect bandgap material. For $x$ higher than 0.11, Ge$_{1-x}$Sn$_x$ is a direct bandgap material since the conduction band minimum is located at Γ-point. (b) Full band $E$-$k$ dispersion for Ge and Ge$_{0.89}$Sn$_{0.11}$. As Sn composition increases, Ge$_{1-x}$Sn$_x$ alloy transits from indirect to direct bandgap at around $x = 0.11$. The differences in bandgaps at Γ-point and $L$-point are highlighted as $\Delta E_{g,\Gamma}$ and $\Delta E_{g,L}$.

The compositional dependence of bandgaps at Γ and $L$-point, denoted as $E_{g,\Gamma}$ and $E_{g,L}$, respectively, is shown in Fig. 4.1(a). The crossover from indirect-to-direct bandgap occurs at $x = 0.06 \sim 0.11$ [116]-[119]. In this work, the crossover from indirect bandgap is assumed to be at $x = 0.11$ according to Ref. [118]. Based on the values of $E_{g,L}$ and $E_{g,\Gamma}$ from Ref. [118], the form factors used in non-local-EPM [124] were adjusted to reproduce the full band structures of Ge$_{1-x}$Sn$_x$. The details of the calibration and the EPM calculation are documented in Ref. [125]. Due to the introduction of Sn, $E_{g,\Gamma}$ and $E_{g,L}$ of
Ge$_{1-x}$Sn$_x$ decrease as Sn composition increases [See Fig. 4.1(a)]. By varying $x$ from 0 to 0.2, the bandgap reduction at $\Gamma$-point ($\Delta E_{g,\Gamma}$) is more pronounced than that at $L$-point ($\Delta E_{g,L}$), causing Ge$_{1-x}$Sn$_x$ alloy to become a direct bandgap material when $x$ is 0.11 or larger. This can be observed from a comparison between the full band structures of Ge and Ge$_{0.89}$Sn$_{0.11}$, as shown in Fig. 4.1(b).

In order to perform a simulation of the electrical characteristics of Ge$_{1-x}$Sn$_x$ TFETs, material parameters of Ge$_{1-x}$Sn$_x$ such as density-of-states (DOS) effective masses of electrons and holes, intrinsic carrier concentrations, and tunneling reduced masses are needed. These parameters can be calculated based on the effective masses extracted from the full band energy-momentum ($E$-$k$) plots obtained by EPM [125].

The electron effective masses (transverse effective mass $m^*_{e,t}$ and longitudinal effective mass $m^*_{e,l}$ in $L$-valley, isotropic effective mass $m^*_{e,\Gamma}$ in $\Gamma$-valley) and hole effective masses (heavy hole effective mass $m^*_{hh}$ and light hole effective mass $m^*_{lh}$) are extracted directly from the band edges using a parabolic line fit. The electron DOS effective masses at $\Gamma$-valley and $L$-valley ($m^*_{DOS,\Gamma}$ and $m^*_{DOS,L}$, respectively) are calculated as $m^*_{DOS,\Gamma} = m^*_{e,\Gamma}$ and

$$m^*_{DOS,L} = 4^{2/3}(m^*_{e,t})^{2/3}(m^*_{e,l})^{1/3}.$$  

The values of $m^*_{DOS,\Gamma}$ and $m^*_{DOS,L}$ for Ge$_{1-x}$Sn$_x$ with $x$ ranging from 0 to 0.2 are presented in Fig. 4.2(a). $m^*_{DOS,\Gamma}$ becomes smaller with Sn composition $x$, while $m^*_{DOS,L}$ shows negligible dependence on Sn composition. For valence band, Luttinger parameters $\gamma_1$, $\gamma_2$, and $\gamma_3$ are also fitted from full band $E$-$k$ by EPM [125]. The hole DOS effective mass $m^*_{DOS,h}$ is calculated based on spherical averaged heavy hole ($m^*_{hh}$) and light
hole (\( m_{LH}^{*} \)) effective masses as \( m_{DOS,h}^{*} = \left( m_{HH}^{*} \right)^{3/2} + \left( m_{LH}^{*} \right)^{3/2} \), where \( m_{HH}^{*} / m_0 = [\gamma_1 (1-\mu)]^{-1} \) and \( m_{LH}^{*} / m_0 = [\gamma_1 (1+\mu)]^{-1} \) with \( \mu = (6\gamma_3 + 4\gamma_2) / 5\gamma_1 \) [126].

The intrinsic carrier concentration \( n_i \) is given by

\[
n_i = N_{C,L} \cdot e^{-\frac{E_{c,L} - E_i}{kT}} + N_{C,\Gamma} \cdot e^{-\frac{E_{c,\Gamma} - E_i}{kT}} = N_V \cdot e^{-\frac{E_E - E_i}{kT}}, \tag{4.1}
\]

where \( E_i \) is intrinsic Fermi level, \( N_{C,L} \) is the effective density of states for electrons in \( L \)-valley with \( N_{C,L} = 2(2\pi \cdot m_{DOS,L}^* kT / h^2)^{3/2} \), \( N_{C,\Gamma} \) is the effective density of states for electrons in \( \Gamma \)-valley with \( N_{C,\Gamma} = 2(2\pi \cdot m_{DOS,\Gamma}^* kT / h^2)^{3/2} \), \( N_V \) is the effective density of states for holes in valence band with \( N_V = 2(2\pi \cdot m_{DOS,h}^* kT / h^2)^{3/2} \), \( k \) is the Boltzmann constant, \( T \) is temperature in degrees Kelvin, and \( h \) is the Planck’s constant. Therefore, \( n_i \) can be rewritten as

\[
n_i = N_V^{1/2} \left( N_{C,L} \cdot e^{-\frac{E_{c,L} - E_i}{kT}} + N_{C,\Gamma} \cdot e^{-\frac{E_{c,\Gamma} - E_i}{kT}} \right)^{1/2}. \tag{4.2}
\]

The ratio of the electron concentration \( n_L \) at the \( L \)-valley to the electron concentration \( n_\Gamma \) at the \( \Gamma \)-valley in Ge\(_{1-x}\)Sn\(_x\) alloy is therefore:

\[
\frac{n_L}{n_\Gamma} = \frac{N_{C,L} \cdot e^{-\frac{E_{c,L} - E_i}{kT}}}{N_{C,\Gamma} \cdot e^{-\frac{E_{c,\Gamma} - E_i}{kT}}} = \frac{N_{C,L}}{N_{C,\Gamma}} \cdot e^{-\frac{E_{c,L} - E_{c,\Gamma}}{kT}}. \tag{4.3}
\]

The values of \( n_i \) and the ratio \( n_L / n_\Gamma \) at various Sn compositions are shown in Fig. 4.2(a) and (b), respectively. The increase of \( n_i \) with \( x \) is mainly
due to the decrease of $E_{g,L}$ and $E_{g,\Gamma}$ with increasing Sn composition. It should be noted that the electron population at $L$-valley is a few orders of magnitude larger than that at $\Gamma$-valley for $0 \leq x \leq 0.2$. The larger electron population at $L$-valley is due to the larger DOS electron effective mass. The electron occupation ratio $n_L / n_{\Gamma}$ decreases as $x$ increases, which is consistent with Ref. [106].

The tunneling reduced mass $m_t^*$ is an important material parameter in the calculation of BTBT current. For Ge$_{1-x}$Sn$_x$ TFET, both direct $\Gamma - \Gamma$ and indirect $\Gamma - L$ BTBT current components need to be calculated. Direct

![Graph](image)

**Fig. 4.2.** (a) The DOS electron effective mass in the $L$-valley ($m_{DOS,L}^*$) is larger than the one in the $\Gamma$-valley ($m_{DOS,\Gamma}^*$) for Ge$_{1-x}$Sn$_x$ alloys with various $x$. (b) The intrinsic carrier concentration and electron occupation ratio versus Sn composition. For Ge$_{1-x}$Sn$_x$ with $x > 0.11$, although the conduction band minimum at the $\Gamma$-valley is lower than the one at the $L$-valley, there are more electrons in $L$-valley than $\Gamma$-valley.
tunneling reduced mass \( m_{r,\Gamma}^* \) and indirect tunneling reduced mass \( m_{r,L}^* \) are obtained using [18],[38],[83]

\[
m_{r,\Gamma}^* = \frac{(m_{e,\Gamma}^* \times m_{lh}^*)}{(m_{e,\Gamma}^* + m_{lh}^*)},
\]

and

\[
m_{r,L}^* = \frac{(m_{e,L}^* \times m_{lh}^*)}{(m_{e,L}^* + m_{lh}^*)},
\]

respectively. The dependence of \( m_{r,\Gamma}^* \) and \( m_{r,L}^* \) on Sn composition is shown in Fig. 4.3. \( m_{r,\Gamma}^* \) is smaller than \( m_{r,L}^* \) at the same Sn composition. As discussed later, this contributes to a larger probability of direct \( \Gamma - \Gamma \) BTBT as compared with indirect \( \Gamma - L \) BTBT. It is also found that both \( m_{r,\Gamma}^* \) and \( m_{r,L}^* \) decrease with increasing Sn composition.

![Graph showing the decrease in tunneling reduced mass with increasing Sn composition.](image)

**Fig. 4.3.** Tunneling reduced masses for \( \Gamma - \Gamma \) BTBT \( (m_{r,\Gamma}^*)\) and \( \Gamma - L \) BTBT \( (m_{r,L}^*)\) decrease as Sn composition \( x \) increases.
Table 4.1: Summary of material parameters used in TCAD simulation.

<table>
<thead>
<tr>
<th>$x$</th>
<th>$E_{g,t}$</th>
<th>$E_{g,l}$</th>
<th>Bandgap (eV)</th>
<th>Relative Permittivity</th>
<th>Mass Density (kg/cm$^3$)</th>
<th>Electron DOS Mass ($m_0$)</th>
<th>Hole DOS Mass ($m_0$)</th>
<th>Tunneling Reduced Mass ($m_0$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.00</td>
<td>0.660</td>
<td>0.800</td>
<td>16.00</td>
<td>5.330</td>
<td>0.600</td>
<td>0.041</td>
<td>0.370</td>
<td>0.0224</td>
</tr>
<tr>
<td>0.05</td>
<td>0.573</td>
<td>0.648</td>
<td>16.40</td>
<td>5.352</td>
<td>0.598</td>
<td>0.036</td>
<td>0.366</td>
<td>0.0191</td>
</tr>
<tr>
<td>0.08</td>
<td>0.524</td>
<td>0.561</td>
<td>16.64</td>
<td>5.365</td>
<td>0.598</td>
<td>0.032</td>
<td>0.361</td>
<td>0.0172</td>
</tr>
<tr>
<td>0.11</td>
<td>0.477</td>
<td>0.477</td>
<td>16.88</td>
<td>5.377</td>
<td>0.597</td>
<td>0.029</td>
<td>0.358</td>
<td>0.0152</td>
</tr>
<tr>
<td>0.14</td>
<td>0.433</td>
<td>0.397</td>
<td>17.12</td>
<td>5.391</td>
<td>0.596</td>
<td>0.025</td>
<td>0.356</td>
<td>0.0132</td>
</tr>
<tr>
<td>0.17</td>
<td>0.390</td>
<td>0.318</td>
<td>17.36</td>
<td>5.404</td>
<td>0.597</td>
<td>0.021</td>
<td>0.351</td>
<td>0.0111</td>
</tr>
<tr>
<td>0.20</td>
<td>0.351</td>
<td>0.247</td>
<td>17.60</td>
<td>5.417</td>
<td>0.596</td>
<td>0.017</td>
<td>0.349</td>
<td>0.0091</td>
</tr>
</tbody>
</table>

Other material parameters such as relative permittivity and mass density, are calculated by linear interpolation between the values of Ge and Sn. The electron affinity of Ge$_{1-x}$Sn$_x$ is assumed to be 4.05 eV. The Ge$_{1-x}$Sn$_x$ material parameters used in this work are summarized in Table 3.1.

4.3 Simulation Methodology

The simulation of Ge$_{1-x}$Sn$_x$ TFETs was performed using our in-house 2D-TCAD simulator which implements a physics-based non-local BTBT algorithm [84]. The algorithm automatically identifies the tunneling paths using a 2D extension of Wentzel–Kramers–Brillouin method [79]-[81], and
the tunneling probability along each path is obtained by integration. The calculation of BTBT carrier generation rate is based on the tunneling probability, and the electron concentration at the starting nodes and the concentration of empty states at the ending nodes of the tunneling paths. The generation rate is then captured in the current continuity equation. The current continuity and Poisson equations are self-consistently solved using Newton’s iteration method. The algorithm is designed to be robust, and the converged electrical results have been shown to be mesh grid independent [84]. During the TCAD device simulation, both direct $\Gamma - \Gamma$ BTBT and indirect $\Gamma - L$ BTBT were considered simultaneously.

The direct $\Gamma - \Gamma$ BTBT generation rate ($G_{\text{dir} BTBT}$) is obtained by an integration in energy scale of the BTBT generation rate for all the tunneling paths. The generation rate contributed by each tunneling path is calculated based on the direct tunneling probability ($T_{\text{tunnel dir}}$) and carrier concentrations at the starting and ending nodes of the tunneling path [84]:

$$G_{\text{dir} BTBT} = \int_{E_c,\Gamma}^{E_v,\Gamma} \frac{4\pi m^*_{\text{DOS,\Gamma}} kT}{h^3} \frac{n_e p_v - n_v^2}{(n_e+n_v)(p_v+n_v)} W_p \cdot T_{\text{tunnel dir}} \cdot dE, \quad (4.6)$$

$$T_{\text{tunnel dir}} = e^{(-2|\kappa|d)\tau}, \text{ with } \kappa = \frac{2\pi}{h} \sqrt{2m^*_{\text{DOS,\Gamma}}} \left[U(r) - E\right], \quad (4.7)$$

where $E$ is carrier energy, $W_p$ is the width of tunnel path, $p_v$ is the hole concentration at the starting node of tunneling at $E = E_v$ at source side, $n_e$ is the electron concentration at the ending node at $E = E_{c,\Gamma}$ in the channel region, $\kappa$ is the imaginary part of the electron wave vector in the forbidden bandgap, and $U(r) - E$ is the barrier height at position $r$. The integration in Eq. (4.6) is performed from the minimum $E_{c,\Gamma}$ ($E_{c,\Gamma_{\text{min}}}$) to the maximum $E_v$ ($E_{v,\text{max}}$).
The indirect $\Gamma - L$ BTBT is a phonon-assisted tunneling process, which involves a change in carrier momentum from $\Gamma$-point to $L$-point. The indirect BTBT process has to involve phonon for momentum conservation, and the BTBT generation rate is reduced by an attenuating pre-factor [99]. The attenuating pre-factor $\alpha_{ph}$ is used to capture the reduction in BTBT generation rate due to the phonon scattering effect. In this work, we take the ratio of direct BTBT generation rate to indirect BTBT generation rate from Kane’s model to obtain $\alpha_{ph}$ [38],[127]:

$$\alpha_{ph} = \frac{(1 + 2N_{TA})D_{TA}^2}{\rho \cdot \epsilon_{TA}} \left[ \frac{9}{2^{1/4}} \cdot h^{1/4} \left( \frac{m^*_p \cdot m^*_n \cdot m^*_D \cdot \text{DOS}_L}{m^*_{r,L}} \right)^{3} \right]^{1/2} \left( \frac{q\zeta}{\epsilon_{TA}} \right)^{1/2},$$

(4.8)

where mass density $\rho$ and acoustic phonon energy $\epsilon_{TA}$ are calculated by linear interpolation between Ge and Sn, $N_{TA}$ is phonon occupation number and expressed as $1/(e^{\epsilon_{TA}/kT} - 1)$, $D_{TA}$ is constant deformation potential, and the value for Ge, $8 \times 10^{-9}$ eV/m, is used [38], $q$ is the charge of an electron, and $\zeta$ is average electric field over the length of the tunneling path. Note that only transverse acoustic phonons are taken into account since they contribute most in the phonon-assisted BTBT due to their highest occupation number and the smallest phonon energy [38],[128].

Therefore, $G_{BTBT}^{ind}$ is calculated using

$$G_{BTBT}^{ind} = \int_{E_{c,L,min}}^{E_{c,L,max}} \alpha_{ph} \frac{4\pi q\epsilon_{TA}^2 kT}{h^3} \frac{n_c p_v - n_l^2}{(n_c + n_l)(p_v + n_l)} W_p \cdot T_{tunnel}^{ind} \cdot dE,$$

(4.9)

$$T_{tunnel}^{ind} = e^{(-2||k_\parallel E||)}, \text{ with } \kappa = \frac{2\pi}{h} \sqrt{2m^*_c \gamma U(r) - E},$$

(4.10)

where $T_{tunnel}^{ind}$ is the indirect tunneling probability. The integration in Eq. (4.9) is performed from the minimum $E_{c,L} (E_{c,L,min})$ to $E_{v,max}$. In Ge, $G_{BTBT}^{ind}$ is around...
2 orders of magnitude lower than $G_{BTBT}^{dir}$ for electric field in the order of a few MV/cm, which agrees with previous simulation work [29],[38].

The device structure and key parameters of the simulated double-gate (DG) Ge$_{1-x}$Sn$_x$ (001) n-channel TFET are shown in Fig. 4.4(a). It should be noted that the quantum confinement is not taken into account due to the constraint of our simulator. In this work, a body thickness larger than the Bohr radius of Ge was used, and quantum effects may be neglected.

It should be noted the state-of-the-art Ge$_{1-x}$Sn$_x$ material with high Sn concentration (e.g. $x > 0.10$) is not defect-free at present. Further improvements in growth technology and material quality may be expected in the future. The GeSn material in this work is assumed to be free of bulk defects or traps. Thus, trap-assisted tunneling is not considered in the device simulation, and we are effectively examining the upper bound of the electrical performance of Ge$_{1-x}$Sn$_x$ TFETs. In the presence of traps, the off-state leakage current and subthreshold swing would be substantially higher due to trap-assisted tunneling.

4.4 Analysis and Discussion

4.4.1 Ge$_{1-x}$Sn$_x$ TFET with High and Low Sn Composition

Device simulation of Ge$_{1-x}$Sn$_x$ TFET with various Sn compositions was performed using the device structure shown in Fig. 4.4(a). Ge$_{1-x}$Sn$_x$ TFETs with Sn composition of 0.05 and 0.14 are studied, which represent the cases of using indirect and direct bandgap materials, respectively. Fig. 4.4(b) and (c)
Fig. 4.4. (a) Schematic showing device structure of DG Ge$_{1-x}$Sn$_x$ TFET. (b) Band diagram near the surface along X-axis of Ge$_{0.95}$Sn$_{0.05}$ TFET at $V_{GS} = V_{DS} = 0.3$ V. Since $E_{c,L}$ is lower than $E_{c,\Gamma}$, the tunneling distance from $E_v$ at the source side to $E_{c,L}$ in the channel $w_T^{ind}$ (denoted by gray arrow) is shorter than that from $E_v$ at the source side to $E_{c,\Gamma}$ in the channel $w_T^{dir}$ (denoted by black arrow). (c) Band diagram near the surface along X-axis of Ge$_{0.86}$Sn$_{0.14}$ TFET at $V_{GS} = V_{DS} = 0.3$ V. Since $E_{c,\Gamma}$ is lower than $E_{c,L}$, $w_T^{dir}$ is shorter than $w_T^{ind}$.

show the band diagrams of Ge$_{0.95}$Sn$_{0.05}$ and Ge$_{0.86}$Sn$_{0.14}$ TFETs near the surface along X-axis at $V_{GS} = V_{DS} = 0.3$ V. For Ge$_{0.95}$Sn$_{0.05}$ TFET, $E_{c,L}$ is lower than $E_{c,\Gamma}$, and the tunneling distance from $E_v$ at the source side to $E_{c,L}$ in the channel $w_T^{ind}$ is shorter than that from $E_v$ at the source side to $E_{c,\Gamma}$ in the channel $w_T^{dir}$. On the other hand, for Ge$_{0.86}$Sn$_{0.14}$ TFET, $E_{c,\Gamma}$ is lower than $E_{c,L}$, causing a smaller $w_T^{dir}$ than $w_T^{ind}$.
Figs. 4.5 and 4.6 show the spatial distribution of $G_{BTBT}^{ind}$, $G_{BTBT}^{dir}$, and total generation BTBT rate $G_{BTBT}^{tot}$ for Ge$_{0.95}$Sn$_{0.05}$ and Ge$_{0.86}$Sn$_{0.14}$ TFETs, respectively, at $V_{GS} = V_{DS} = 0.3$ V. $G_{BTBT}^{tot}$ is extracted when both direct and indirect BTBT models are turned on. For Ge$_{0.95}$Sn$_{0.05}$ TFET, the contour plots of $G_{BTBT}^{ind}$ and $G_{BTBT}^{dir}$ are shown in Fig. 4.5(a) and (b), respectively. By comparing Fig. 4.5(a) and (b), we observe that the magnitude of $G_{BTBT}^{dir}$ is larger than $G_{BTBT}^{ind}$ due to the higher tunneling probability of direct $\Gamma - \Gamma$ BTBT. $G_{BTBT}^{tot}$ equals to the sum of the indirect $\Gamma - L$ ($G_{BTBT}^{ind}$) and direct $\Gamma - \Gamma$ BTBT ($G_{BTBT}^{dir}$) components [Fig. 4.5(c)]. It is found that $G_{BTBT}^{dir}$ is the dominant component in $G_{BTBT}^{tot}$ at the given bias. Fig. 4.6(a) and (b) show the $G_{BTBT}^{ind}$ and $G_{BTBT}^{dir}$, respectively, for Ge$_{0.86}$Sn$_{0.14}$ TFET. Ge$_{0.86}$Sn$_{0.14}$ is direct bandgap material with $E_{c,\Gamma}$ lower than $E_{c,L}$. $G_{BTBT}^{tot}$ is dominated by $\Gamma - \Gamma$ BTBT component for Ge$_{0.86}$Sn$_{0.14}$ TFET [Fig. 4.6(c)], which is the same as the case of Ge$_{0.95}$Sn$_{0.05}$ TFET. Comparing Fig. 4.5(c) and Fig. 4.6(c), we can observe that under the same bias condition, the magnitude of $G_{BTBT}^{tot}$ for Ge$_{0.86}$Sn$_{0.14}$ TFET is larger than that for Ge$_{0.95}$Sn$_{0.05}$ TFET. This is mainly due to the enhanced $G_{BTBT}^{dir}$ caused by the smaller $E_{c,\Gamma}$ when Sn composition is higher.
**Fig. 4.5.** Spatial distributions of (a) $G_{\text{BTBT}}^{\text{ind}}$, (b) $G_{\text{BTBT}}^{\text{dir}}$ and (c) $G_{\text{BTBT}}^{\text{tot}}$ for Ge$_{0.95}$Sn$_{0.05}$ TFET at $V_{\text{GS}} = V_{\text{DS}} = 0.3$ V. As the double-gate device is symmetrical about a mirror line at $Y = 12.5$ nm, only the upper half body ($0 < Y < 12.5$ nm) is shown.
Fig. 4.6. Spatial distributions of (a) $G_{\text{BTBT}}^{\text{ind}}$, (b) $G_{\text{BTBT}}^{\text{dir}}$ and (c) $G_{\text{BTBT}}^{\text{tot}}$ for Ge$_{0.86}$Sn$_{0.14}$ TFET at $V_{GS} = V_{DS} = 0.3$ V. As the double-gate device is symmetrical about a mirror line at $Y = 12.5$ nm, only the upper half body ($0 < Y < 12.5$nm) is shown. The magnitude of $G_{\text{BTBT}}^{\text{tot}}$ for Ge$_{0.86}$Sn$_{0.14}$ TFET is larger than that for Ge$_{0.95}$Sn$_{0.05}$ TFET shown in Fig. 4.5(c).

4.4.2 Electrical Characteristics of GeSn TFET

The simulated $I_{DS} - V_{GS}$ curves for Ge$_{0.95}$Sn$_{0.05}$ and Ge$_{0.86}$Sn$_{0.14}$ TFETs with direct $\Gamma - \Gamma$ and indirect $\Gamma - L$ tunneling current components are plotted in Fig. 4.7. For Ge$_{0.95}$Sn$_{0.05}$ TFET, the voltage $V_{\text{onset, ind}}$ at which the onset of indirect $\Gamma - L$ BTBT occurs is lower than the voltage $V_{\text{onset, dir}}$ at which the
onset of direct $\Gamma - \Gamma$ BTBT occurs as shown in Fig. 4.7(a). This is due to the smaller value of $E_{g,l}$ as compared with $E_{g,\Gamma}$. Therefore, indirect BTBT current dominates the total current for $V_{\text{onset\_ind}} < V_{GS} < V_{\text{onset\_dir}}$. For $V_{GS} > V_{\text{onset\_dir}}$, both indirect and direct BTBT take place, and the direct $\Gamma - \Gamma$ BTBT dominates the total current due to $G_{\text{BTBT}}^\text{dir}$ being larger than $G_{\text{BTBT}}^\text{ind}$. On the other hand, for Ge$_{0.86}$Sn$_{0.14}$ TFET [Fig. 4.7(b)], $E_{c,\Gamma}$ is lower than $E_{c,l}$, $V_{\text{onset\_dir}}$ is lower than $V_{\text{onset\_ind}}$, and the direct BTBT dominates the total tunneling current for $V_{GS} > V_{\text{onset\_dir}}$.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{Fig4.7.png}
\caption{(a) Simulated $I_{DS}$ - $V_{GS}$ for Ge$_{0.95}$Sn$_{0.05}$ TFET. $V_{\text{onset\_ind}}$ is lower than $V_{\text{onset\_dir}}$ since $E_{g,l}$ is smaller than $E_{g,\Gamma}$. As $V_{GS}$ is larger than $V_{\text{onset\_ind}}$, BTBT from $E_V$ at source side to $E_{c,l}$ occurs. However, at $V_{GS} > V_{\text{onset\_dir}}$, BTBT from $E_V$ to $E_{c,\Gamma}$ dominates the tunneling current. (b) Simulated $I_{DS}$ - $V_{GS}$ for Ge$_{0.86}$Sn$_{0.14}$ TFET. $V_{\text{onset\_dir}}$ is lower than $V_{\text{onset\_ind}}$ since $E_{g,\Gamma}$ is smaller than $E_{g,l}$. As $V_{GS} > V_{\text{onset\_dir}}$, BTBT occurs from $E_v$ at source side to $E_{c,\Gamma}$ and dominates the drive current once $V_{GS}$ reaches $V_{\text{onset\_dir}}$.}
\end{figure}
For Ge$_{1-x}$Sn$_x$ TFETs with both direct and indirect $E_G$, simulations indicate that the direct $\Gamma - \Gamma$ BTBT contributes more to the total drive current once it occurs ($V_{GS} > V_{onset,dir}$) due to the larger value of $G^{dir}_{BTBT}$ in direct $\Gamma - \Gamma$ BTBT compared with $G^{ind}_{BTBT}$ in indirect $\Gamma - L$ BTBT. This is due to the higher tunneling probability for direct BTBT than indirect BTBT.

Fig. 4.8 shows the $I_{DS}$ - $V_{GS}$ characteristics of Ge$_{1-x}$Sn$_x$ TFETs with $x$ ranging from 0 to 0.2. The drive current of Ge$_{1-x}$Sn$_x$ TFETs increases with Sn composition at a fixed $V_{GS}$. The $V_{GS}$ at which the tunneling current rises steeply in Fig. 4.8 reduces
with increasing Sn composition, and this is related to the bandgap reduction. It is also observed that the leakage floor of Ge$_{1-x}$Sn$_x$ TFETs increases with Sn composition. The leakage floor is determined by the leakage current of reverse biased p-i-n junction, which is higher for a smaller bandgap.

$S$ obtained at each $V_{GS}$ is defined to be $dV_{GS}/d(\log I_{DS})$ and may also be referred to as Point $S$. Point $S$ versus $I_{DS}$ curves for Ge$_{1-x}$Sn$_x$ TFETs with $x$ ranging from 0 to 0.2 are plotted in Fig. 4.9. By incorporation Sn into Ge, $S$ of TFET is improved significantly. The reduction of $S$ values is more obvious for Ge$_{1-x}$Sn$_x$.

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**Fig. 4.9.** A set of point $S$ versus $I_{DS}$ for Ge$_{1-x}$Sn$_x$ TFETs with $x$ ranging from 0 to 0.2. It can be observed that $S$ is reduced with Sn composition. The maximum $I_{DS}$ with sub-60 mV/decade $S$ becomes higher as Sn composition increases.
TFETs with direct bandgap ($x = 0.11, 0.14, 0.17, \text{ and } 0.2$). More importantly, the maximum $I_{DS}$ with sub-60 mV/decade $S$ becomes higher as Sn composition increases. The improvement of $S$ characteristics for Ge$_{1-x}$Sn$_x$ TFETs is due to the following reasons. Firstly, as $x$ is larger than 0.11, Ge$_{1-x}$Sn$_x$ becomes a direct bandgap material, and $I_{DS}$ is dominated by direct BTBT. Direct BTBT results in a steeper $S$ in comparison with indirect BTBT (Fig. 4.7). Secondly, the reduction in bandgap of Ge$_{1-x}$Sn$_x$ causes enhanced $I_{DS}$ as $x$ increases, leading to the improvement of $S$ especially at high current level. For Ge$_{0.8}$Sn$_{0.2}$ TFET, sub-60 mV/decade $S$ is achieved at $I_{DS}$ of around 8 μA/μm.

Fig. 4.10 depicts $I_{off}$ versus $I_{on}$ characteristics for Ge$_{1-x}$Sn$_x$ TFETs with $x = 0.00, 0.05, 0.11, \text{ and } 0.17$. For a given $I_{off}$, which is varied from $10^{-12}$ to $10^{-5}$ A/μm, $V_{off}$ is $V_{GS}$ when $I_{DS}$ equals to $I_{off}$, and $I_{on}$ is extracted at $V_{GS} - V_{off} = V_{DS} = 0.3$ V. When Ge$_{1-x}$Sn$_x$ becomes direct bandgap with $x$ higher than 0.11, for a given $I_{off}$, Ge$_{1-x}$Sn$_x$ TFETs demonstrate higher $I_{on}$ and $I_{on}/I_{off}$ compared to Ge TFET. For $I_{off} = 1$ nA/μm, $I_{on}$ of 0.095 mA/μm and $I_{on}/I_{off}$ of $\sim 10^5$ are achieved in Ge$_{0.89}$Sn$_{0.11}$ TFET. It should be noted that $I_{on}$ of Ge$_{1-x}$Sn$_x$ TFETs show less sensitivity to $I_{off}$ than that of Ge TFET. This is attributed to the improved $S$ characteristics of Ge$_{1-x}$Sn$_x$ TFETs as compared to Ge device.
**Fig. 4.10.** $I_{off}$ versus $I_{on}$ of Ge$_{1-x}$Sn$_x$ TFETs with $x = 0.00, 0.05, 0.11,$ and $0.17$ at a supply voltage of 0.3 V. For a given $I_{off}$, $V_{off}$ is $V_{GS}$ when $I_{DS}$ equals to the $I_{off}$. $I_{on}$ is extracted at $V_{GS} - V_{off} = V_{DS} = 0.3$ V. For a fixed $I_{off}$, $I_{on}$ of Ge$_{1-x}$Sn$_x$ TFETs with $x > 0.11$ is higher than that of Ge TFET.

### 4.5 Conclusion

In this Chapter, we performed a detailed simulation study of Ge$_{1-x}$Sn$_x$ n-channel TFETs with Sn composition varying from 0 to 0.2. The material parameters were extracted from full band structure by EPM calculations, which were subsequently imported to TCAD for device simulation. By increasing Sn composition, $I_{on}$ of Ge$_{1-x}$Sn$_x$ TFETs is increased due to the higher direct BTBT rate which relates to the reduction in $E_g$. In addition, the maximum $I_{DS}$ with sub-60 mV/decade $S$ becomes higher with increasing Sn composition. For Ge$_{0.8}$Sn$_{0.2}$ TFET, sub-60 mV/decade $S$ is achieved at $I_{DS}$ of…
~8 μA/μm. For a given $I_{\text{off}}$, $I_{\text{on}}$ of Ge$_{1-x}$Sn$_x$ TFETs with $x$ higher than 0.11 is higher than those of Ge TFET at a supply voltage of 0.3 V.
Chapter 5

Tunneling Field-Effect Transistors with Silicon-Carbon Source Tunneling Junction: Experimental Demonstration

5.1 Introduction

Conventional planar silicon (Si) p⁺-p-n⁺ (p⁺-i-n⁺) tunneling field-effect transistors (TFETs) generally suffer from low on-state current $I_{on}$ [47],[49],[52],[56],[57],[61],[66],[72]. This is due to the large bandgap of Si and gradual tunneling junction at the source-channel interface caused by large lateral diffusion of dopants. Reducing the band-to-band tunneling (BTBT) barrier width $w_T$ is required to obtain good TFET performance, and can be achieved by employing materials with narrow bandgap, strain engineering, or with abrupt source junction [45],[48]-[50],[54]-[55],[62]-[71]. Recently, a TFET with p⁺-n⁺-p-n⁺ structure (Fig. 5.1) was proposed and simulated, and it incorporated an additional n⁺ pocket adjacent to the p⁺ source [20]. The TFET with this new design has a steeper doping profile at the tunnel junction compared to the conventional p⁺-p-n⁺ TFET, and thus can achieve a higher $I_{on}$. Planar p⁺-n⁺-p-n⁺ Si TFET was later demonstrated experimentally by adding a source dopant profile steepening implant step, and an enhancement in drive current was reported [58], [59]. However, in order for TFET to be considered as a next generation device, further improvement in $I_{on}$ is needed.
In this Chapter, we use silicon-carbon (Si:C) as the source material of $p^+\cdot n^-\cdot p^+\cdot n^+$ Si TFETs, and the device structure is shown in Fig. 5.2. Si:C/Si heterojunction is employed in order to improve tunneling current as discussed in Chapter 3. More importantly, the diffusion of boron in Si depends on the
interstitial density, the substitutional carbon atoms in Si:C can consume the interstitial sites and thus lead to a suppression of the boron diffusion \[129\]. A schematic illustration of the carbon-induced boron diffusion suppression is shown in Fig. 5.3. Therefore, abrupt p⁺ junction is easier to be formed in Si:C than in Si, which is preferred.

\[
\text{Si:C Source p⁺-n⁺-p-n⁺-TFET}
\]

\[\text{Fig. 5.2.  Schematic of silicon-carbon (Si:C) source TFET with p⁺-n⁺-p-n⁺ structure.}\]

\[
\text{Fig. 5.3.  Schematic illustration of suppressed boron diffusion in Si:C. Since the diffusion of boron depends on the interstitial density, and there are less interstitial sites in Si:C, the boron diffusion in Si:C is suppressed \[129\]. More abrupt p⁺ junction can be formed by using Si:C source than Si source.}\]
as source tunneling junction for TFETs. We demonstrate the Si:C source TFETs with p⁺-n⁺-p-n⁺ structure for the first time. The Si:C source was implemented by carbon-boron cluster co-implant. The performance enhancement of Si:C source p⁺-n⁺-p-n⁺ TFET compared with all-Si p⁺-n⁺-p-n⁺ TFET is investigated.

5.2 Device Fabrication

N-channel p⁺-n⁺-p-n⁺ TFETs were fabricated on 6 inch p-type (100) Si wafers with a resistivity of 4–8 Ω·cm. Gate-first process was used and the process steps are shown in Fig. 5.4(a). Active regions were defined by patterned silicon dioxide SiO₂ (400 nm). About 5 nm aluminum oxide (Al₂O₃) was deposited by atomic layer deposition (ALD), and sputter deposition of 100 nm tantalum nitride (TaN) was performed subsequently. The gate definition was done by chlorine-based dry etch. Arsenic ion (As⁺) implant was performed at an energy of 20 keV and a dose of 6×10¹⁴ cm⁻² to form the n⁺ drain and n⁺ pocket. Rapid thermal annealing (RTA) was then carried out at 1000 ºC for 1 minute for n-type dopant activation and defect removal. The drain was formed before the source to achieve a gradual drain doping profile to suppress gate-drain gate capacitance as discussed in Chapter 2. This was followed by sequential carbon cluster (C₇H₇⁺) and boron cluster ion (B₁₈H₂₂⁺) implantation performed by SemEquip [Fig. 5.4(b)]. Implantation energy of 4.5 keV with an effective carbon dose of 2×10¹⁵ atoms/cm² was used for C₇H₇⁺ implant, and the peak atomic percentage of carbon is 1.44%.
Control devices were prepared without Carbon co-implant step.

(a) Process Flow

- Active Region Patterning (p-Si)
- TaN/Al₂O₃ Deposition
- Gate Definition

(b) N⁺ Implant + Activation

- As⁺ Implant + Activation
- C7H₇⁺ Implant (Self-Amorphization) (4.5 keV, dose of 2×10¹⁵ cm⁻²)
- B₁₈H₂₂⁺ Implant (0.8 keV, dose of 2×10¹⁵ cm⁻²)

RTA for Si:C Epitaxy and Source Dopant Activation (700 °C, 20 s)

Si:C

(b) N⁺ Implant + Activation

- As⁺ Implant + Activation
- C7H₇⁺ Implant (Self-Amorphization) (4.5 keV, dose of 2×10¹⁵ cm⁻²)
- B₁₈H₂₂⁺ Implant (0.8 keV, dose of 2×10¹⁵ cm⁻²)

Fig. 5.4. (a) Fabrication process for p⁺-n⁻-p⁺ TFET with Si:C source. (b) Key steps to form p⁺-n⁻-p⁻ device structure. By implanting carbon cluster ions (C₇H₇⁺) followed by boron cluster ions (B₁₈H₂₂⁺) followed by annealing, the p⁺ Si:C source was formed.

Implantation energy of 0.8 keV with an effective boron dose of 2×10¹⁵ atoms/cm² was used for B₁₈H₂₂⁺ implant. The C₇H₇⁺ are implanted deeper than B₁₈H₂₂⁺ to sufficiently suppress boron diffusion. The main advantage of carbon clusters implantation is the self-amorphization, which provides better implant uniformity. In parallel, all-silicon control devices were prepared without the C₇H₇⁺ implant step. Finally, Si:C formation and p⁺-source activation were performed in a single annealing step using RTA. Several RTA recipes were attempted, and an optimal condition of 700 °C for 20 s was used.
Fig. 5.5. (a) Transmission electron microscopy (TEM) image of the TaN/Al₂O₃ gate stack in fabricated Si:C source TFET with p⁺-n⁺-p-n⁺ structure. (b) C-V measurement result of a capacitor (200 μm × 200 μm) fabricated in parallel. The equivalent oxide thickness (EOT) was extracted to be about 3 nm based on the capacitance values at gate bias of -3 V.

5.3 Results and Discussions

5.3.1 Gate Stack Characterization

The TaN/Al₂O₃ gate stack on Si substrate was inspected by transmission electron microscopy (TEM) as shown in Fig. 5.5(a). The physical thickness of Al₂O₃ is about 5.6 nm, and good interface quality between Al₂O₃ and Si is observed. Capacitors with dimensions of 200 μm × 200 μm were also fabricated in parallel with Si:C source TFETs. Capacitance-voltage (C-V) measurement was performed at a frequency of 100 kHz [Fig. 5.5(b)], and the equivalent oxide thickness (EOT) of around 3 nm was extracted from the capacitance at gate bias of -3 V.
Fig. 5.6. (a) Cross-sectional TEM image of the Si:C region at the source side of a fabricated TFET. (b) The zoomed-in view of the source junction highlighted by the square in (a). Good crystalline quality is achieved after annealing by RTA.

5.3.2 Characterization of Si:C Source

TEM images shown in Fig. 5.6 reveals that Si:C with good crystalline quality was formed at the source side after the RTA step at 700 °C for 20 s. The high-resolution X-ray Diffraction (HRXRD) measurement was performed on a blanket Si sample, which received the same carbon and boron cluster ion implantations followed by the same RTA. The XRD result is shown in Fig. 5.7. According to the carbon implant energy which is 4.5 keV, the projected range ($R_p$) of carbon is 17 nm and the as-formed Si:C layer thickness is around 20 nm. According to the two-dimensional (2D) XRD mapping result of the Si:C sample with a similar carbon implant condition in Ref. [130], the Si:C layer in our experiment can be considered as fully strained. The fitted curve obtained by simulation (red dash-dotted line) in Fig. 5.7 indicates that the substitutional carbon composition is up to 1.5% assuming that the Si:C layer is
Fig. 5.7. HRXRD curve obtained from Si:C formed on Si (100), showing the Si:C (004) peak. Assuming that the Si:C is fully strained, the carbon composition is 1.5%.

Fig. 5.8. Lateral strain $\varepsilon_{xx}$ (%) distribution at Si:C/Si interface by finite element simulation. Si:C ($\text{Si}_{0.985}\text{C}_{0.015}$) is under tensile strain, leading to a reduction in the bandgap of Si:C. The positive sign indicates tensile strain, while the negative sign is for compressive strain.

fully strained. Since carbon atomic percentage of about 1.44 % is predicted based on the implant condition, this XRD fitting result implies that all the carbon atoms that implanted into Si are mostly at substitutional sites after the
RTA. As the substitutional carbon atoms can function as sinks for Si interstitials [129], the high substitutional carbon concentration (up to 1.5%) in our sample should be sufficient to have an impact on the reduction of Si interstitials.

In addition, the high concentration of substitutional carbon will lead to a smaller lattice constant of Si:C (for Si_{0.985}C_{0.015}, the lattice constant is estimated as 5.395 Å [131]) as compared with that of Si (5.431 Å). The strain profile at Si:C/Si interface was calculated by finite element simulation with a structure similar to the source region in our fabricated device and the results are shown in Fig. 5.8. From the simulation results, it is found that the tensile strain (~0.2 %) is induced near the top surface of the Si:C region. This strain is transferred from the horizontal Si:C/Si interface below. The surface of Si is also under tensile strain (~0.35 %). This is due to the compressive strain in the vertical direction introduced by Si:C with small lattice constant than Si. The induced tensile strain, in both Si:C and Si, splits the conduction band into two subbands (Δ_2 and Δ_4) [132], leading to a reduction in bandgap. The narrow bandgap reduces the energy barrier width \( w_T \) for band-to-band tunneling of electrons and thus increases tunneling current.

To investigate the impact of carbon co-implant on boron distribution, secondary ion mass spectrum (SIMS) analysis was performed on the blanket Si sample with carbon and boron co-implant. The boron profile in the sample with boron implant only was also characterized by SIMS for comparison. Both of the samples were annealed at 700 °C for 20 s by RTA. The SIMS profiles shown in Fig. 5.9 reveal that a more abrupt boron profile is obtained in Si:C.
Fig. 5.9. Secondary ion mass spectrum (SIMS) results for boron (red squares) and carbon (blue squares) profiles in Si:C sample and boron profile (black line) in Si sample. The samples are after 700 °C 20 s anneal. The boron profile is slightly more abrupt in Si:C as compared with that in Si.

Based on the SIMS data, process simulation was performed to investigate 2D doping profiles near the source tunneling junction by TSUPREM-4 [133]. Fig. 5.10(a)-(c) show the simulated active arsenic ($N_d$), active boron ($N_a$) and net dopant ($N_d-N_a$ and $N_a-N_d$) concentration contours at the source side of the p$^+$-n$^+$-p-n$^+$ TFET. Fig. 5.11(d) shows doping profiles in the lateral direction from the source to the channel near the surface. The n$^+$ pocket compensates the p$^+$ dopants near the channel surface for a very small distance (less than 10 nm), leading to a more abrupt p$^$/p tunneling junction compared with conventional p$^+$/p TFET [Fig. 5.10(d)].
Fig. 5.10. Simulated (a) active arsenic ($N_d$), (b) active boron ($N_a$), and (c) net dopant ($N_a-N_d$ and $N_d-N_a$) concentration contours at the source side of the p$^+$-n-p$^+$-n$^+$ TFET. (d) shows doping profiles in the lateral direction near the channel surface along dark yellow cutline in (c).

5.3.3 Electrical Results

The $I_{DS}$-$V_{GS}$ characteristics of a typical Si:C source TFET ($L_G = 2 \mu$m and $W = 6 \mu$m) and an all-silicon control device with the same dimensions are shown in Fig. 5.11. The drive current is enhanced and subthreshold swing $S$ is significantly improved due to increased BTBT rate for Si:C source TFET as compared with all-silicon device. This relates to the smaller bandgap of tensile strained Si:C/Si at the
tunneling junction and steeper boron profile obtained by incorporating Si:C at source side of TFETs. At \( V_{DS} = V_{GS} = 2 \text{ V} \), \( I_{DS} \) of 3.87 \( \mu \text{A}/\mu \text{m} \) is achieved in Si:C source TFET, which is about 40\% higher than that in all-silicon control device (2.76 \( \mu \text{A}/\mu \text{m} \)). Extracted from \( I_{DS}-V_{GS} \) curve at \( V_{DS} = 0.5 \text{ V} \), the minimum point swing \( S_{min} \) of 95 mV/decade is achieved in Si:C source TFET, and it is 41 mV/decade smaller than that in control device. The average swing \( S_{ave} \) is extracted with \( I_{DS} \) ranging from \( 10^{-9} \) to \( 10^{-8} \) \( \mu \text{A}/\mu \text{m} \). \( S_{ave} \) of 115 mV/decade is achieved in Si:C source TFET, and it is 34 mV/decade smaller than that in control device.

The leakage floor is defined as the plateau of \( I_{DS} \) with very low \( V_{GS} \), which is insufficient to turn on the BTBT (such as \( V_{GS} < 0.5 \text{ V} \) in Fig. 5.11). The leakage floor of Si:C source TFET is about 1 order of magnitude lower than that of all-Si control device. This is attributed to the high crystalline quality at source tunneling junction within Si:C. The Si:C source TFET

**Fig. 5.11.** \( I_{DS}-V_{DS} \) curves of Si:C source TFET and all-silicon control TFET. A higher drive current is achieved by employing Si:C source.
received additional carbon implant step, which is deeper than subsequent boron implant, leading to pre-amorphization before boron implant. After recrystallization by RTA, the end of range (EOR) defects will appear near the Si:C/Si interface of Si:C source TFET. It should be noted that the EOR defects are not located in the p⁺ tunneling junction region. (The EOR defects are more than 20 nm deep below the surface according to the implant condition.) On the other hand, in all-Si control device, the EOR defects locate within the p⁺ tunneling junction and distribute near to the surface (about 5 nm below the surface according to the implant condition), leading to high leakage floor as well as $S$ degradation.

$I_{DS}$-$V_{DS}$ characteristics of the Si:C source TFET are compared with those of the all-silicon control device in Fig. 5.12. The drive current in Si:C source TFET is higher as compared with that of control device due to higher tunneling rate.

![Fig. 5.12.](image)

$V_{GS} = 0.2 \sim 2$ V in steps of 0.2 V

$V_{DS}$ curves of Si:C source TFET, compared with all-silicon control TFET, which is without carbon co-implantation. The higher drive current is achieved by employing Si:C source.
The statistical plot of $S_{\text{min}}$ in Si:C source TFETs and all-Si control devices are shown in Fig. 5.13(a), and Fig. 5.13(b) shows the statistical distribution of $S_{\text{ave}}$. All the devices measured are with same dimensions. For each measured device, $S_{\text{min}}$ and $S_{\text{ave}}$ are extracted from $I_{DS}$-$V_{GS}$ curve with $V_{DS}$ = 0.5 V. Compared with control devices, Si:C source TFETs have smaller $S_{\text{min}}$ and $S_{\text{ave}}$. The median of $S_{\text{min}}$ and $S_{\text{ave}}$ are reduced by 47 mV/decade and 43 mV/decade, respectively.

The cumulative plots of $I_{\text{on}}$ and $I_{\text{off}}$ are shown in Fig. 5.14 and 5.15, respectively. $V_{TH}$ is defined by the constant current method as the $V_{GS}$ where $I_{DS}$ reaches $10^{-8}$ A/μm. $I_{\text{on}}$ is defined as the $I_{DS}$ at $V_{DS}$ = 1.5 V and $V_{GS} = V_{TH} + 1$ V, and $I_{\text{off}}$ is extracted at $V_{DS}$ = 1.5 V and $V_{GS} = V_{TH} - 0.5$ V. The cumulative

![Image](image_url)

**Fig. 5.13.** Statistical plots of (a) minimum point swing $S_{\text{min}}$ and (b) $S_{\text{ave}}$, which is the average swing with $I_{DS}$ ranging from $10^{-9}$ to $10^{-8}$ μA/μm. For each measured device, $S_{\text{min}}$ and $S_{\text{ave}}$ are extracted from $I_{DS}$-$V_{GS}$ curve with $V_{DS}$ = 0.5 V. It can be observed that Si:C source p$^+$-n$^*$-p-n$^+$ TFETs achieve steeper swing. Compared with control devices, the median of $S_{\text{min}}$ and $S_{\text{ave}}$ are reduced by 47 mV/decade and 43 mV/decade, respectively. It should be noted that some control devices have leakage floor current larger than $10^{-9}$ μA/μm, so $S_{\text{ave}}$ cannot be calculated for those devices. Therefore, there are less points for control devices in (b).
Fig. 5.14. Cumulative probability plot of $I_{on}$ for Si:C source TFETs and all-silicon TFETs. $V_{TH}$ is defined as the $V_{GS}$ where $I_{DS}$ reaches $10^{-8}$ A/$\mu$m. $I_{on}$ is defined as the $I_{DS}$ at $V_{DS} = 1.5$ V and $V_{GS} = V_{TH} + 1$ V. The $I_{on}$ values in Si:C source TFET are around 2 times larger than those of the control devices. The median $I_{on}$ is enhanced by $\sim 85\%$ as compared with that of the control devices.

Fig. 5.15. Cumulative probability plot of $I_{off}$ for Si:C source TFETs and all-silicon control devices. $I_{off}$ is extracted at $V_{DS} = 1.5$ V and $V_{GS} = V_{TH} - 0.5$ V. The $I_{off}$ is reduced in Si:C source TFETs. The median $I_{off}$ is reduced by $\sim 70\%$ as compared with that of the control devices.
plots of $I_{on}$ in Fig. 5.14 shows that $I_{on}$ in Si:C source TFETs are higher than that of the control devices, and the median $I_{on}$ is enhanced by ~85%. The median $I_{off}$ is reduced in Si:C source TFETs by around 70% compared with that in control devices as shown in Fig. 5.15.

5.3.4 Impact of Channel Orientations

We also studied the dependence of device performance on channel orientations. Si:C source p$^+$-n$^+$-p-n$^+$ TFETs with <100> and <110> channel orientations were fabricated together. The $I_{DS}$-$V_{GS}$ characteristics of devices with these two orientations are compared in Fig. 5.16. $I_{on}$ in device with <100> channel orientation is twice as high as that in devices with <110> channel. The statistical box plots of $I_{on}$ are shown in Fig. 5.17. The median $I_{on}$ in devices with <100> channel orientation is improved about 50% as compared with devices with <110> channel orientation. The $I_{on}$ improvement may be related to the smaller boron diffusion coefficient in <100> direction than <110> direction [134]. This will lead to a more abrupt p$^+$ source junction to increase the band-to-band tunneling rate.
Fig. 5.16.  $I_{DS}$-$V_{GS}$ for Si:C source TFETs with channel in <100> and <110> orientations. The $I_{on}$ is higher for devices with <100> channel orientation, which is probably due to less boron diffusion along <100> direction.

Fig. 5.17.  Statistical box plot of $I_{on}$ for Si:C source TFETs with channel in <100> and <110> directions. The $I_{on}$ is higher for <100> channel devices, which could be due to less boron diffusion along <100> direction.
### 5.3.5 Two-step Source Annealing

A two-step annealing scheme was carried out to further improve the performance of Si:C source TFETs. The two-step annealing consists of a low temperature solid phase epitaxy (SPE) and a high temperature dopant activation. The conditions of the two annealing steps are 600 °C for 2 minutes and 700 °C for 20 s, respectively. The optimized annealing step is highlighted in the process flow shown in Fig. 5.18. The purpose is to perform low temperature SPE with long duration to obtain good crystalline quality and remove defects in Si:C region before the high temperature dopant activation step. As a result, the diffusion of boron could be suppressed further.

The transfer characteristics of Si:C source TFET with two-step source annealing (SPE+RTA) were measured. The $S_{\text{min}}$ and $S_{\text{ave}}$ are extracted in the same way as defined before. The cumulative plots for $S_{\text{min}}$ and $S_{\text{ave}}$ are

![Process Flow Diagram](image.png)

**Fig. 5.18.** Process flow for two-step source annealing for Si:C source p⁺-n⁺-p⁻ TFET.
Fig. 5.19. Statistical plots of (a) $S_{\text{min}}$ and (b) $S_{\text{ave}}$ for Si:C source p$^+$-n$^+$-p-n$^+$ TFETs with single step and two-step annealing. $S_{\text{ave}}$ is defined the average swing with $I_{\text{DS}}$ ranging from $10^{-9}$ to $10^{-8}$ $\mu$A/\mu m. Both $S_{\text{min}}$ and $S_{\text{ave}}$ are improved due to the additional SPE step.

compared with previous devices (Fig. 5.13) and the results are shown in Fig. 5.19. It is observed that after two-step source annealing, both $S_{\text{min}}$ and $S_{\text{ave}}$ are improved. The median values of $S_{\text{min}}$ and $S_{\text{ave}}$ is reduced by 4.3 mV/decade and 6.2 mV/decade, respectively. The enhancement in $S$ relates to the reduction of defects at tunneling junction by the additional SPE step. The presence of defects degrades $S$ of a TFET due to trap-assisted BTBT. Si:C source TFETs after SPE +RTA have less defects leading to less trap-assisted BTBT and therefore has better $S$ compared with the devices receiving single RTA. However, no obvious $I_{\text{on}}$ enhancement is observed, indicating the two-step annealing process with current recipe may not have large impact on boron diffusion. Future process optimization should be done to achieve better boron diffusion control meanwhile reduce more defects at the tunneling junction of TFETs.
Table 5.1. Summary the increment of $I_{on}$ ($\Delta I_{on}$), reduction of $I_{off}$ ($\Delta I_{off}$), and reduction in $S_{min}$ ($\Delta S_{min}$) and $S_{ave}$ ($\Delta S_{ave}$) for Si:C source TFETs as compared with all-Si control devices. The calculation is based on the median value of statistical data.

<table>
<thead>
<tr>
<th></th>
<th>$\Delta I_{on}$ (↑)</th>
<th>$\Delta I_{off}$ (↓)</th>
<th>$\Delta S_{min}$ (↓)</th>
<th>$\Delta S_{ave}$ (↓)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si:C Source</td>
<td>85%</td>
<td>70%</td>
<td>47 mV/decade</td>
<td>43 mV/decade</td>
</tr>
<tr>
<td>Channel Rotated from</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>&lt;110&gt; to &lt;100&gt;</td>
<td>50%</td>
<td>Not Observed</td>
<td>Not Observed</td>
<td>Not Observed</td>
</tr>
<tr>
<td>2-step Annealing</td>
<td>Not Observed</td>
<td>Not Observed</td>
<td>4.3 mV/decade</td>
<td>6.2 mV/decade</td>
</tr>
<tr>
<td>(SPE+RTA)</td>
<td></td>
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</tbody>
</table>

5.4 Conclusion

Lateral n-channel Si:C source TFETs with p$^+$-n$^+$-p-n$^+$ structure were demonstrated using carbon cluster (C$_7$H$_7^+$) and boron cluster (B$_{18}$H$_{22}^+$) co-implantation. Reduction in $S$ (the median of $S_{min}$ is reduced by 47 mV/decade and $S_{ave}$ is reduced by 43 mV/decade) and enhancement in $I_{on}$ (the median $I_{on}$ is increased by ~ 85%) are achieved as summarized in Table 5.1. This could be attributed to the effective suppression of boron diffusion due to the presence of substitutional carbon at the source side of the devices. The abrupt boron profile leads to abrupt tunneling junction and thus enhances BTBT of electrons. In addition, the induced tensile strain reduces the bandgap in both Si:C and Si near the surface. This also helps to reduce the energy barrier width of BTBT and thus increase the electron tunneling probability. The impact of channel orientation was also investigated. It is observed that device
with <100> channel direction has higher $I_{on}$, which may relate to the smaller boron diffusivity coefficient in <100> direction. Two-step annealing process was performed to improve the $S$ of Si:C source p$^+$-n$^+$-p-n$^+$ TFETs further by reducing the defects at the source tunneling junction.
Chapter 6

Germanium-Tin (GeSn) P-channel Tunneling Field-Effect Transistor: Simulation and Experimental Demonstration

6.1 Introduction

It was reported that the conventional silicon (Si) based tunneling field-effect transistors (TFETs) suffer from low on-state current ($I_{on}$), in the range of $0.01 \text{ to } 1 \mu A/\mu m$ for $|V_{DS}|$ and $|V_{GS}| \approx 1 \text{ V}$ [47],[49],[56],[57],[59],[61],[66],[72]. Research efforts have been focused on small bandgap ($E_g$) materials to boost the drive current. For n-channel TFETs (nTFETs), III-V compound semiconductors, such as InGaAs, have been exploited as source and channel materials for achieving high drive current due to the direct band-to-band tunneling (BTBT) and high electron mobility [54],[64],[65]. However, current p-channel TFETs (pTFETs) mainly employ group IV materials, such as Si, Ge, and SiGe [49],[56],[57],[66]-[68], and more research efforts are needed to further improve the drive current. While III-V materials, like InGaAs, have high BTBT rate due to direct bandgaps, their hole mobilities are generally low, which can lead to high channel resistance. SiGe or Ge has high hole mobility
and might be promising for pTFET application, but the BTBT is indirect, limiting the tunneling current. In addition, forming a good n$^+$ junction in Ge is difficult due to the low solubilities and large diffusivity coefficients of n-type dopants, such as phosphorus (P), arsenic (As) and antimony (Sb) [135],[136]. Moreover, the n-type dopants require high activation temperature in Ge [137],[138], leading to a gradual or non-abrupt n$^+$ junction, which is not preferred for pTFET application. GeSn alloy is a promising material candidate for pTFET application as it has small and direct bandgap (as discussed in Chapter 4), as well as the high hole mobility. In addition, as a group IV material, GeSn has good process compatibility with Si technology, and it is very attractive from the cost point of view. Table 6.1 compares advantages and disadvantage of III-V, SiGe and GeSn as source and channel materials for pTFETs.

In this Chapter, we explore GeSn alloy as the active layer for pTFETs and report the first demonstration of lateral GeSn pTFET. The incorporation of Sn into Ge shifts the Γ valley down, thus increasing direct BTBT rate and enabling a high on-state current. Furthermore, n-type dopant activation temperature can be reduced in GeSn (less than 400 °C) as compared to Ge [120],[122],[139]. Thus, the dopant diffusion is suppressed, leading to a high

Table 6.1. Comparison of III-V, SiGe, and GeSn for pTFET application.

<table>
<thead>
<tr>
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<th>III-V</th>
<th>SiGe</th>
<th>GeSn</th>
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<tbody>
<tr>
<td>Small $E_g$</td>
<td>√</td>
<td>×</td>
<td>√</td>
</tr>
<tr>
<td>Direct BTBT</td>
<td>√</td>
<td>×</td>
<td>√</td>
</tr>
<tr>
<td>High hole mobility</td>
<td>×</td>
<td>√</td>
<td>√</td>
</tr>
<tr>
<td>Abrupt n$^+$ junction</td>
<td>×</td>
<td>×</td>
<td>√</td>
</tr>
<tr>
<td>High gate interface quality</td>
<td>×</td>
<td>√</td>
<td>√</td>
</tr>
<tr>
<td>Easy integration on Si</td>
<td>×</td>
<td>√</td>
<td>√</td>
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</table>
quality n+ GeSn tunneling junction.

In addition, GeSn has higher hole mobility than Ge, and thus reduces the channel resistance of pTFET [120]. The fabrication details of GeSn pTFETs will be discussed in the following sections and the performance of the GeSn pTFETs will be assessed as well.

6.2 Device Design Considerations and Simulations

Single-gate lateral Ge$_{1-x}$Sn$_x$ pTFETs with $x$ of 0, 0.04, 0.08, and 0.12 were simulated by our in-house two-dimensional (2D) technology computer-aided design (TCAD) simulator, which implements a physics-based non-local BTBT algorithm [84]. Ge$_{1-x}$Sn$_x$ material parameters were extracted from full band $E$-$k$ dispersion by non-local Empirical Pseudopotential Method (EPM)

![Figure 6.1](image_url)

**Fig. 6.1.** (a) Schematic of simulated lateral single-gate Ge$_{1-x}$Sn$_x$ pTFET. (b) List of device dimensions and simulation parameters. (c) Band diagrams along X-direction at 0.1 nm below the surface of Ge$_{0.96}$Sn$_{0.04}$ pTFET. The drain bias $V_{DS}$ is -0.6 V in the simulation. The gate bias $V_{GS}$ is 0 V for grey lines and -0.6 V for black lines, respectively.
calculation [125], and the details are documented in Chapter 4. The device structure of simulated Ge$_{1-x}$Sn$_{x}$ pTFET is illustrated in Fig. 6.1(a), and the simulation parameters are listed in Fig. 6.1(b). It should be noted that the bandgap of Ge$_{1-x}$Sn$_{x}$ alloy is small (< 0.66 eV) and is tunable by Sn composition $x$. It was reported that when $x < 0.11$ the conduction band minimum is at $L$-point, while for $x \geq 0.11$, the conduction band minimum is at $\Gamma$-point, and GeSn alloy transits to a direct bandgap material [118]. In this simulation, the BTBT of electrons from valence band ($E_v$) to both the conduction band minimum at $L$-point ($E_{c,L}$) and $\Gamma$-point ($E_{c,\Gamma}$) will be considered. For example, the simulated band diagrams of Ge$_{0.96}$Sn$_{0.04}$ pTFET at on-state ($V_{DS} = -0.6$ V and $V_{GS} = -0.6$ V) and off-state ($V_{DS} = -0.6$ V and $V_{GS} = 0$ V) are shown in Fig. 6.1(c), where $E_{c,L}$ is lower than $E_{c,\Gamma}$. It should be noted that when Sn composition $x$ is larger than 0.11, the band diagrams will be different that $E_{c,\Gamma}$ becomes lower than $E_{c,L}$. The BTBT generation rate is different in this case and its impact on $I$-$V$ characteristics will be discussed next.

The $I_{DS}$-$V_{GS}$ characteristics for Ge$_{1-x}$Sn$_{x}$ pTFET with various Sn compositions ($x = 0, 0.04, 0.08, 0.12$) are calculated and shown in Fig. 6.2. In Ge$_{1-x}$Sn$_{x}$ alloy with $x < 0.11$, $E_{c,L}$ is lower than $E_{c,\Gamma}$, thus the onset gate voltage of indirect $\Gamma$ - $L$ BTBT is smaller than that of direct $\Gamma$ - $\Gamma$ BTBT. However, direct $\Gamma$ - $\Gamma$ BTBT has a higher tunneling probability than the indirect $\Gamma$ - $L$ BTBT. Thus, the current contributed by direct $\Gamma$ - $\Gamma$ BTBT is much higher than that by $\Gamma$ - $L$ BTBT, and it is dominant in total drain current of Ge$_{1-x}$Sn$_{x}$ TFET ($x < 0.11$). On the other hand, for Ge$_{1-x}$Sn$_{x}$ TFET with $x \geq 0.11$, the onset gate voltage of direct $\Gamma$ - $\Gamma$ BTBT is smaller than that of indirect $\Gamma$ - $L$.  

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Fig. 6.2. Simulated $I_{DS}$-$V_{GS}$ characteristics of Ge, Ge$_{0.96}$Sn$_{0.04}$, Ge$_{0.92}$Sn$_{0.08}$, and Ge$_{0.88}$Sn$_{0.12}$ pTFETs at $V_{DS} = -0.6$ V. $I_{DS}$ increases significantly with increasing Sn composition $x$.

Thus, the $\Gamma$ - $\Gamma$ BTBT tunneling current dominants the drain current over the whole range of $V_{GS}$. The $I_{DS}$-$V_{GS}$ curve for Ge$_{1-x}$Sn$_{x}$ pTFET with $x = 0.12$ therefore shows a steeper swing as compared with others with $x < 0.11$ in Fig. 6.2. More details for the direct and indirect tunneling current components in Ge$_{1-x}$Sn$_{x}$ TFET with various $x$ can be found in Chapter 4. Besides the above observation, it is also noted that Ge$_{1-x}$Sn$_{x}$ pTFET with $x \geq 0.11$ has higher total drain current than devices with $x < 0.11$, which relates to the reduction of bandgap in Ge$_{1-x}$Sn$_{x}$ with increasing $x$. However, the leakage floor of Ge$_{1-x}$Sn$_{x}$ pTFET increases with larger $x$. The leakage floor is defined as the plateau of $I_{DS}$ with very low $V_{GS}$ that insufficient to turn on the BTBT. This relates to the increase in thermal generation current due to the reduction in bandgap of Ge$_{1-x}$Sn$_{x}$ with larger $x$. 

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Fig. 6.3. (a) Point-swing versus $I_{DS}$ for Ge, Ge$_{0.96}$Sn$_{0.04}$, Ge$_{0.92}$Sn$_{0.08}$, and Ge$_{0.88}$Sn$_{0.12}$ pTFETs extracted from corresponding $I_{DS}$-$V_{GS}$ curves in Fig. 6.2. $I_{sub60}$ is defined as the maximum $I_{DS}$ with point-swing of sub-60 mV/decade. (b) $I_{sub60}$ tends to be higher with increasing Sn composition $x$, and the average swing $S_{ave}$ becomes smaller with increasing $x$. $S_{ave}$ is the average subthreshold swing obtained from a section of the $I_{DS}$-$V_{GS}$ curve where $I_{DS}$ varies from $10^{-10}$ A/µm to $10^{-6}$ A/µm.

Point-swing refers to the slope obtained at a specific $V_{GS}$ bias in an $I_{DS}$-$V_{GS}$ curve. Point-swing versus $I_{DS}$ for Ge$_{1-x}$Sn$_x$ pTFET with various $x$ are extracted from $I_{DS}$-$V_{GS}$ curves in Fig. 6.2 and are shown in Fig. 6.3(a). We define $I_{sub60}$ as the maximum $I_{DS}$ with point-swing less than 60 mV/decade. In addition, the average swing $S_{ave}$ is obtained from a section of the $I_{DS}$-$V_{GS}$ curve where $I_{DS}$ varies from $10^{-10}$ A/µm to $10^{-6}$ A/µm. It should be noted that $I_{DS}$ for the definition of $S_{ave}$ starts from $10^{-10}$ A/µm, which is different from Chapter 3 ($I_{DS}$ varies from $10^{-12}$ A/µm to $10^{-6}$ A/µm) due to high leakage floor for Ge$_{1-x}$Sn$_x$ pTFET with high Sn composition. $I_{sub60}$ and $S_{ave}$ versus Sn composition $x$ are plotted in Fig. 6.3(b). It can be observed that as $x$ increases, $I_{sub60}$ tends to be higher, indicating sub-60 mV/decade point-swing can be achieved at a higher drain current level. This is preferred by TFET application as discussed.
in Chapter 1. In Ge$_{0.88}$Sn$_{0.12}$ pTFET, point-swing keeps below 60 mV/decade with $I_{DS}$ up to 1.7 $\mu$A/\(\mu\)m. In addition, the $S_{ave}$ becomes smaller as $x$ increases [Fig. 6.3(b)]. These mainly relate to the smaller onset voltage of the direct $\Gamma$-$\Gamma$ BTBT, as well as the reduced bandgap with increasing Sn composition.

For analysis of electrical characteristics, the off-state current $I_{off}$ is fixed at 0.1 nA/\(\mu\)m, and $V_{off}$ is defined as the $V_{GS}$ where $I_{DS} = I_{off}$. $I_{on}$ with a certain $V_{DD}$ window is then defined to be the drain current $I_{DS}$ at $V_{DS} = V_{GS} - V_{off} = V_{DD}$. The $I_{DS}$-$V_{GS}$ for Ge$_{1-x}$Sn$_x$ pTFET with $x = 0, 0.04, 0.08, 0.12$ are calculated at different $V_{DS}$ ($V_{DS} = -0.2$ V, -0.4 V, and -0.6 V) as shown in Fig. 6.4. Distribution of $I_{on}$ at various $V_{DD}$ windows, ranging from 0.2 V to 0.6 V, and Sn compositions ($x = 0 ~ 0.14$) is shown in Fig. 6.5. $I_{on}$ above 300 $\mu$A/\(\mu\)m is achieved at $V_{DD} = 0.6$ V by Ge$_{0.86}$Sn$_{0.14}$ pTFET.

**Fig. 6.4.** Simulated $I_{DS}$-$V_{GS}$ of Ge, Ge$_{0.96}$Sn$_{0.04}$, Ge$_{0.92}$Sn$_{0.08}$, and Ge$_{0.88}$Sn$_{0.12}$ pTFETs at (a) $V_{DS} = -0.2$ V, (b) $V_{DS} = -0.4$ V, and (c) $V_{DS} = -0.6$ V.
**Fig. 6.5.** Contour plot of $I_{on}$ at various $V_{DD}$ windows (-0.2 V ~ -0.6 V) and Sn compositions (0 ~ 0.14) for a fixed $I_{off}$ of 0.1 nA/μm. $I_{on}$ above 300 μA/μm is achieved at $V_{DD} = -0.6$ V in Ge$_{0.86}$Sn$_{0.14}$ pTFET (top-right corner of the plot).

### 6.3 GeSn pTFET Fabrication

The GeSn pTFETs were fabricated on epitaxial GeSn layer on 4-inch n-type (100) Ge wafers. The thickness of the GeSn layer is about 146 nm, as indicated by the transmission electron microscopy (TEM) image in Fig. 6.6(a). It can also be observed that the GeSn film has perfect crystalline structure and the good interface between GeSn and Ge is achieved. We performed the high resolution X-ray diffraction (XRD) measurement, and the well-defined GeSn peak is observed, indicating that high quality GeSn film with 4.2% substitutional Sn is grown on the Ge substrate [Fig. 6.6(b)].
Fig. 6.6. (a) Transmission electron microscopy (TEM) image showing ~146 nm GeSn epitaxially grown on Ge. Perfect GeSn crystalline structure is observed in high resolution TEM image below, and good GeSn/Ge interface is obtained. (b) X-ray diffraction (XRD) curve indicates that a high quality Ge$_{0.958}$Sn$_{0.042}$ layer is grown on Ge substrate.

Fig. 6.7 shows the process flow for realizing GeSn pTFETs. Phosphorus well implant was performed at energy of 20 keV and a dose of 5×10$^{14}$ cm$^{-2}$. Dopant activation was then carried out at 450 ºC for 3 minutes by rapid thermal anneal (RTA) to form the lightly doped n-type GeSn body. After pre-gate cleaning by diluted hydrofluoric acid (HF:H$_2$O = 1:100), the samples were loaded into an ultra-high-vacuum chemical vapor deposition (UHVCVD) tool. Native oxide was removed by sulfur hexafluoride (SF$_6$) plasma etching, and low temperature disilane (Si$_2$H$_6$) surface passivation was then carried out at 370 ºC for 90 minutes with a flow rate of 10 sccm. The hafnium oxide (HfO$_2$) gate dielectric was then formed by atomic layer deposition (ALD) and a 100 nm-thick tantalum nitride (TaN) film was deposited by sputter subsequently. The gate patterns were defined by
Fig. 6.7. (a) Key process steps for fabricating GeSn pTFET. (b) Low-temperature Si$_2$H$_6$ surface passivation was performed before high-k and metal gate deposition. (c) BF$_2^+$ implantation was performed in the drain region with an energy of 35 keV and a dose of $2 \times 10^{15}$ cm$^{-2}$. (d) P$^+$ implantation was performed in the source region with an energy of 8 keV and a dose of $4 \times 10^{15}$ cm$^{-2}$. (e) Source and drain were activated together at 400 °C for 5 minutes. Ni(GeSn) contact were formed afterwards.

chlorine-based dry etching. Next, boron difluoride ion (BF$_2^+$) implant was performed in the drain region with an energy of 35 keV and a dose of $2\times10^{15}$ cm$^{-2}$. The phosphorus ion (P$^+$) implantation was performed for the source formation, and the implant condition is with an energy of 8 keV and a dose of $4\times10^{15}$ cm$^{-2}$. Source and drain were activated together at 400 °C for 5 minutes by RTA. Sputter deposition of 10 nm nickel (Ni) was performed and followed by a 350 °C anneal for 30 s to form the nickel stanogermanide Ni(GeSn) contacts. Selective wet etch was done by concentrated sulfuric acid (H$_2$SO$_4$) to remove excessive Ni to complete the device fabrication. The top-view
scanning electron microscope (SEM) image of a fabricated GeSn pTFET is shown in Fig. 6.8(a).

The GeSn pMOSFETs were fabricated on the same wafer with GeSn pTFETs for the purpose of characterization (to be discussed in the next Section). The pMOSFETs received BF$_2^+$ implant in both source and drain sides and were capped by photoresist (PR) during P$^+$ implant.

6.4 Results and Discussion

6.4.1 Gate Stack Characterization

TEM inspection was performed to characterize the gate stack of GeSn pTFETs. The TEM image in Fig. 6.8(b) shows the TaN/HfO$_2$/SiO$_2$/Si stack formed on epitaxially grown GeSn layer on Ge substrate. High resolution TEM in Fig. 6.8(c) shows the zoomed-in view of TaN/HfO$_2$ stack on Si$_2$H$_6$ passivated GeSn channel. The physical thickness of HfO$_2$ is around 4.2 nm. The Si passivation layer is partially oxidized, and good quality SiO$_2$/Si interfacial layer is formed after the Si$_2$H$_6$ surface passivation step. The effective hole mobilities $\mu_{eff,h}$ of 300 cm$^2$/V·s at inversion carrier density $N_{inv}$ of 4×10$^{12}$ cm$^{-2}$ and $\mu_{eff,h}$ of 240 cm$^2$/V·s at $N_{inv}$ of 1×10$^{13}$ cm$^{-2}$ in GeSn channel are extracted from pMOSFETs fabricated in parallel. This confirms that a high quality of GeSn channel and a good interface between HfO$_2$ and Si-passivated GeSn channel were achieved.
Fig. 6.8. (a) Top-view scanning electron microscope (SEM) image of a fabricated GeSn pTFET with actual gate length of 4µm. (b) TEM image shows TaN/HfO$_2$ gate stack on a GeSn layer epitaxially grown on Ge. (c) Zoom-in view of TaN/HfO$_2$ stack on Si$_3$H$_6$ passivated GeSn channel as indicated by the square in (b). It can be observed that the Si passivation layer (the bright layer between HfO$_2$ and GeSn channel) could be partially oxidized. The physical thickness of HfO$_2$ is around 4.2 nm.

6.4.2 $N^+$ GeSn Source Formation

The sheet resistance $R_{sh}$ of phosphorus-doped Ge and GeSn blanket samples after 400 °C annealing were measured and compared as shown in Fig. 6.9. Lower $R_{sh}$ is achieved by phosphorus-doped GeSn sample annealed at 400 °C for 5 minutes compared with the Ge sample, which went through the same phosphorus implant and was annealed at 400 °C for 30 minutes. The mean value of $R_{sh}$ in GeSn is ~ 54 % smaller than that in Ge.
Fig. 6.9. Sheet resistance $R_{Sh}$ of phosphorus doped Ge and GeSn after 400 °C activation. Lower $R_{Sh}$ is achieved in GeSn as compared with that in Ge. Better phosphorus activation is achieved in GeSn as compared with Ge at low temperature, i.e. 400 °C.

Considering the larger junction depth in Ge due to longer annealing time, the resistivity in GeSn is even lower than what we get from Fig. 6.9. This implies a higher electron concentration in GeSn, and thus an enhanced phosphorus activation in GeSn at a relatively low temperature (400 °C). The enhanced phosphorus activation is probably due to the passivation of vacancies in Ge lattice with the presence of Sn atoms. More details can be found in Ref. [139].

To study the contact formation and the dopant profile in the n$^+$ source side of GeSn pTFET, secondary ion mass spectrometry (SIMS) analysis was performed and the concentration profiles for Ge, Sn, Ni and P are shown in Fig. 6.10(a). The cross-sectional TEM image for the source side of a device
Fig. 6.10. (a) Secondary ion mass spectrometry (SIMS) profiles of Ge, Sn, Ni and P along vertical direction in n$^+$ source region of GeSn pTFET as indicated by the red dash line in the inset. About 20 nm heavily n-type doped (P concentration above $1 \times 10^{20}$ cm$^{-3}$) GeSn layer is observed underneath Ni(GeSn). (b) Cross-sectional TEM image at n$^+$ source side of a fabricated GeSn pTFET.

is also shown in Fig. 6.10(b). Underneath Ni(GeSn), about 20 nm phosphorus-rich GeSn layer (P concentration above $1 \times 10^{20}$ cm$^{-3}$) is formed, which is the heavily n-type doped source region for GeSn pTFET.

6.4.3 Capacitance-Voltage (C-V) Characteristics of GeSn pTFETs

Agilent 4284A Precision LCR Meter with resolution of 0.01 fF was used for high frequency capacitance-voltage (C-V) measurement. For total gate capacitance $C_{GG}$ measurement, ‘Hi’ terminal was connected to the gate, ‘Lo’ terminal was connected to both the source and the drain, and the body was grounded. For gate-to-source capacitance $C_{GS}$ (gate-to-drain capacitance
$C_{GD}$ measurement, ‘Hi’ terminal was connected to the gate, ‘Lo’ terminal was connected to the source (drain), and both of body and drain (source) were grounded.

The $C-V$ characteristics ($C_{GD}$, $C_{GS}$, $C_{GG}$ versus gate bias $V_G$) for a pTFET and a pMOSFET with the same dimensions ($L_G = 20 \, \mu m$, $W = 200 \, \mu m$) were measured at a frequency of 100 kHz as shown in Fig. 6.11. In a pTFET, the gate capacitance $C_{GG}$ is asymmetrically partitioned into $C_{GS}$ and $C_{GD}$, which is a typical feature of TFET as mentioned in Chapter 2. For $V_{DS} = 0 \, V$, the magnitude of $C_{GD}$ is larger than that of

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**Fig. 6.11.**  (a) Measured gate capacitance $C_{GG}$, $C_{GD}$, and $C_{GS}$ of a fabricated GeSn pTFET. TFET features are observed: $C_{GG}$ is mainly contributed from $C_{GD}$ at high $|V_G|$. (b) Measured gate capacitance $C_{GG}$, $C_{GD}$, and $C_{GS}$ of a GeSn pMOSFET. The magnitudes of $C_{GD}$ and $C_{GS}$ are very close, and both of them are about half of $C_{GG}$. 

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when \(|V_G|\) is higher than 0.2 V, and \(C_{GD}\) almost dominates the \(C_{GG}\) with even higher \(|V_G|\) (> 0.5 V) [Fig. 6.11(a)]. This is attributed to the asymmetric n⁺-n-p⁺ structure of a pTFET. When sufficient \(|V_G|\) is applied, hole inversion layer is formed in the channel, which only connects to p⁺ drain side. Thus, the whole inversion capacitance is included in \(C_{GD}\). In the contrary, in a pMOSFET, at \(V_{DS} = 0\) V, the magnitudes of \(C_{GS}\) and \(C_{GD}\) are equal, and are about half of \(C_{GG}\) [Fig. 6.11(b)]. This is due to the symmetric structure of pMOSFET. When uniform hole inversion layer is formed in the channel with sufficient \(|V_G|\), \(C_{GG}\) is equally partitioned into \(C_{GD}\) and \(C_{GS}\).

From the \(C-V\) analysis above, we can confirm that n⁺-n-p⁺ structure was formed in the as-fabricated GeSn pTFETs.

### 6.4.4 Current-Voltage (I-V) Characteristics of GeSn pTFETs

The transfer characteristics (\(I_{DS}-V_{GS}\)) of a typical GeSn pTFET with a gate length (\(L_G\)) of 4 \(\mu\)m are shown in Fig. 6.12. In this device, for \(V_{DS} = -1\) V, \(I_{DS}\) of 22 \(\mu\)A/\(\mu\)m is achieved at \(V_{GS} = -2\) V, and for \(V_{DS} = -0.3\) V, \(I_{DS}\) of 6.3 \(\mu\)A/\(\mu\)m is achieved at \(V_{GS} = -2\) V. The minimum point-swing \(S_{min}\) of this device is \(~ 330\) mV/decade for \(V_{DS} = -0.05\) V. The output characteristics (\(I_{DS}-V_{DS}\)) curves at various gate voltages of the same device are shown in Fig. 6.13. \(I_{DS}\) of 27 \(\mu\)A/\(\mu\)m was obtained at \(V_{GS} = V_{DS} = -2\) V, and \(I_{DS}\) of 2.6 \(\mu\)A/\(\mu\)m was obtained at \(V_{GS} = V_{DS} = -1\) V.
Fig. 6.12. Measured $I_{DS}$-$V_{GS}$ curves of a Ge$_{0.958}$Sn$_{0.042}$ pTFET with self-aligned Ni(GeSn) contacts. Decent transfer characteristics are observed.

Fig. 6.13. Measured $I_{DS}$-$V_{DS}$ curves of the same device in Fig. 6.12 at various gate voltages. $I_{DS}$ of 27 µA/µm was obtained at $V_{GS} = V_{DS} = -2$ V and $I_{DS}$ of 2.6 µA/µm was obtained at $V_{GS} = V_{DS} = -1$ V.

Fig. 6.14 shows the cumulative distribution of $I_{DS}$ extracted at $V_{GS} = V_{DS} = -2$ V for the devices with a fixed $L_G$ of 4 µm. The median value of 23
μA/μm, and a maximum value of 29 μA/μm is obtained for $I_{DS}$ at $V_{GS} = V_{DS} = -2$ V. $I_{DS}$ at $V_{GS} = V_{DS} = -2$ V for GeSn pTFETs with various gate lengths $L_G$ is shown in Fig. 6.15. It is observed that $I_{DS}$ at $V_{GS} = V_{DS} = -2$ V increases with the scaling of $L_G$ which is less than 7 μm. This indicates that the channel resistance has an important impact on $I_{DS}$ at $V_{GS} = V_{DS} = -2$ V. With further scaling of $L_G$, higher drain current could be achieved in a GeSn pTFET.

**Fig. 6.14.** Cumulative probability plot of $I_{DS}$ at $V_{DS} = V_{GS} = -2.0$ V for Ge$_{0.958}$Sn$_{0.042}$ pFETs with $L_G$ of 4 μm. The highest drive current is 29 μA/μm and median one is about 23 μA/μm.
Fig. 6.15. Plot of $I_{DS}$ at $V_{DS} = V_{GS} = -2.0$ V for Ge$_{0.958}$Sn$_{0.042}$ pTFETs with various $L_G$. For devices with gate length $L_G$ less than 7 μm, the drain current increases with decreasing $L_G$.

6.4.5 Low Temperature Measurement

Low temperature characteristics of GeSn pTFETs were investigated. $I_{DS}-V_{GS}$ transfer characteristics of a GeSn pTFET with $L_G = 11$ μm was measured at various temperatures ranging from 200 to 280 K in steps of 20 K as shown in Fig. 6.16. For $V_{DS} = -0.05$ V, the leakage floor is lowered with decreasing temperature, while for $V_{DS} = -1$ V, $I_{DS}$ is much less dependent on temperature. Figs. 6.17 (a) and (b) are Arrhenius plots of $\ln(I_{DS}/T^{3/2})$ versus $1/kT$ for $V_{DS} = -0.05$ V and $V_{DS} = -1$ V, respectively. The $I_{DS}$ is extracted at $V_{GS} = 0.1$ V, which is the leakage floor current. For $V_{DS} = -0.05$ V, the slope of the linear fitted line is 0.31 eV, which is about the half bandgap of Ge$_{0.958}$Sn$_{0.042}$ (0.587 eV) as shown in Fig. 6.17(a). This indicates that the leakage floor for $V_{DS} = -0.05$ V is dominated by the Shockley-Read-Hall (SRH)
Fig. 6.16. $I_{DS}$-$V_{GS}$ transfer characteristics of a TFET with $L_G/W = 10\mu m/100\mu m$ at different temperatures. $S$ is improved with reduction of the leakage floor.

generation current. SRH-dominated leakage current is a function of the intrinsic carrier concentration $n_i$ that has the temperature dependence as [140]:

$$n_i = \sqrt{N_e N_h} \exp \left[ -\frac{E_g}{2kT} \right] \propto A \cdot T^{3/2} \exp \left[ -\frac{E_g}{2kT} \right],$$ (6.1)

where $N_e$ and $N_h$ are effective density of states of electrons and holes, respectively, $k$ is the Boltzmann constant, $T$ is temperature in degrees Kelvin, and $A$ is a constant. It should be noted that SRH generation current depends on deep level trap density. In order to reduce this leakage current level of GeSn pTFET, process such as source/drain implant and activation should be optimized to reduce the defects at source/drain junctions more efficiently. On the other hand, for $V_{DS} = -1$ V, the slope of the linear fitted line is close to 0 eV
SRH is dominant
\[ \text{Slope} = 0.31 \text{ eV} \]
\[ \sim E_g/2 \text{ of Ge}_{0.958}\text{Sn}_{0.042} \]

\[ \ln\left(\frac{I_{DS}}{T^{3/2}}\right), \text{where } I_{DS} \text{ at } V_{GS} = 0.1 \text{ V} \]
\[ \frac{1}{kT} \text{ (eV}^{-1}) \]
\[ V_{DS} = -0.05 \text{ V, } V_{GS} = 0.1 \text{ V} \]

(b) Arrhenius plot of \( \ln(I_{DS}/T^{3/2}) \) versus \( 1/kT \) for \( V_{DS} = -1 \text{ V} \). The \( I_{DS} \) is extracted at \( V_{GS} = 0.1 \text{ V} \). The slope of the fitted line is close to 0 eV. This indicates the dominant mechanism of leakage current at high \( V_{DS} \) (-1 V) is BTBT at the drain side.

As shown in Fig. 6.17(b). In addition, \( I_{DS} \) at low \( V_{GS} \) (such as \( V_{GS} > -0.2 \text{ V} \) in Fig. 6.16) is dependent on \( V_{GS} \) at \( V_{DS} = -1 \text{ V} \). These two features indicate that, for \( V_{DS} \) as high as -1 V, the dominant mechanism of leakage current is the BTBT at the drain side. Therefore, optimization of drain side, such as the drain doping concentration engineering or gate-to-drain underlap is needed to suppress drain side BTBT current.
Temperature dependence of $I_{DS}$ with $V_{GS} = -1.5$ V, -2 V, and -2.5 V was extracted and shown in Fig. 6.18. The temperature dependence of $I_{DS}$ is determined by two factors: hole mobility and BTBT rate. When temperature decreases, mobility increases due to less phonon scattering. However, BTBT rate is reduced with decreasing temperature since the increase of $E_g$ leads to a larger barrier width for the BTBT of electrons. For $T \geq 240$ K, $I_{DS}$ increases with decreasing temperature, which indicates that the hole mobility in the device channel has a larger impact on the drain current as compared with BTBT. This also explains the scaling property of $I_{DS}$ at room temperature in Fig. 6.15. While for $T < 240$ K, BTBT is the dominant mechanism, leading to an overall trend of decreasing $I_{DS}$ with decreasing temperature.

The temperature dependence of $I_{on}$ is another typical feature of TFET, which is distinguished from MOSFETs [23]. In MOSFETs, the drain current is dominant by mobility, which decreases with increasing temperature. The
temperature dependence of $I_{DS}$ shown in Fig. 6.18 also helps to confirm the realization of $n^+\text{-}n\text{-}p^+$ structures in GeSn pTFETs.

6.4.6 Benchmark and Device Optimization

We compare the drive current of our GeSn pTFETs with those of reported pTFETs in the literatures, as shown in Table 6.2. Long channel GeSn devices ($L_G \geq 4 \mu$m) demonstrate much higher $I_{on}$ than the reported Si and Ge pTFETs [49],[56],[57],[67], and [68]. This is due to the high tunneling current at the GeSn $n^+$ tunneling junction and the high hole mobility in GeSn channel.

<table>
<thead>
<tr>
<th>Device Structure</th>
<th>Gate Length $L_G$</th>
<th>Supply Voltage $V_{DD}$ (V)</th>
<th>$I_{on}$ ($\mu$A/$\mu$m)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ref. [49] GOI pTFET</td>
<td>100 nm</td>
<td>$V_{DS} = -0.8$ V, $V_{GS-V_{BTBT}} = -1.0$ V</td>
<td>1</td>
</tr>
<tr>
<td>Ref. [57] Si pTFET</td>
<td>160 nm</td>
<td>-1.0 V</td>
<td>0.15</td>
</tr>
<tr>
<td>Ref. [56] Si pTFET</td>
<td>20 $\mu$m</td>
<td>-1.0 V</td>
<td>0.47</td>
</tr>
<tr>
<td>Ref. [67] Strained Ge pTFET</td>
<td>700 nm</td>
<td>$V_{DS} = -1.5$ V, $V_{GS-V_{BTBT}} = -1.0$ V</td>
<td>0.006</td>
</tr>
<tr>
<td>Ref. [68] SiGe/SOI pTFET with Raised S/D</td>
<td>200 nm</td>
<td>-1.0 V</td>
<td>7</td>
</tr>
<tr>
<td>This Work GeSn pTFET</td>
<td>4 $\mu$m</td>
<td>-1.0 V</td>
<td>4.34</td>
</tr>
</tbody>
</table>

$^\dagger$ Some publications do not provide $I_{DS}$-$V_{GS}$ curve at $V_{DS} = -1$ V, therefore we choose the $I_{DS}$-$V_{GS}$ curve with $V_{DS}$ nearest to 1 V to make the comparison. For example, we choose $V_{DS} = -0.8$ V for Ref. [49].
The GeSn pTFET, however, has lower drive current than the SiGe/SOI pTFET with raised source/drain ($L_G = 200$ nm) [68]. This is probably due to the large source/drain resistance in the GeSn device, as the p$^+$ drain side series resistance is about 5 kΩ·μm, which was obtained from the GeSn pMOSFETs fabricated in parallel. The source side resistance could be even larger, because the Fermi level pinning (near valence band) at Ni(GeSn) GeSn interface leads to a large Schottky barrier height for electrons and hence a high contact resistance. In addition, the $L_G$ of the GeSn pTFET in this work is much larger as compared with that in Ref. [68]. Further performance improvement of GeSn pTFETs can be achieved by increasing Sn composition, $L_G$ scaling, raised source/drain, and optimization of contact formation, such as selenium (Se) or sulfur (S) co-implant [141].

The subthreshold swing in fabricated GeSn pTFET is still large, which mainly due to the large leakage current floor, trap-assisted band-to-band tunneling as well as unoptimized source doping profile. In order to improve $S$, more efforts should be put into forming a defect free n$^+$/n$^-$ source tunneling junction with very abrupt doping profile, suppressing defects in all process steps, such as drain junction formation and contact formation to reduce leakage current floor. Moreover, employing heterojunction with staggered band alignment is a great solution to suppress leakage current and improve drive current at the same time.
6.5 Conclusions

We demonstrate the world’s first lateral GeSn pTFETs. Decent device characteristics in terms of on-state current were obtained. The maximum $I_{DS}$ of 4.34 $\mu$A/µm at $V_{DD} = -1$ V and 29 $\mu$A/µm at $V_{DD} = -2$ V are achieved for the Ge$_{0.958}$Sn$_{0.042}$ pTFETs with $L_G$ of 4 µm. This should be attributed to the enhanced direct $\Gamma - \Gamma$ BTBT and high hole mobility in the GeSn channel. The low thermal budget (400 °C) of device fabrication process helps to form abrupt source tunneling junction to enhance the BTBT of electrons. The device performance can be further improved by increasing Sn composition, optimizing source/drain contact formation, and scaling down $L_G$. 
Chapter 7

Conclusion and Future Work

7.1 Conclusion

Complementary metal-oxide-semiconductor (CMOS) technology is reaching its fundamental limits due to the nonscalibility of subthreshold swing ($S$). Alternative devices are desired to overcome this limitation, among which tunneling field-effect transistor (TFET) stands out as a promising candidate for future low power applications. This is because that the working mechanism in a TFET is completely different from a MOSFET, and it is based on gate-controlled quantum band-to-band tunneling (BTBT) phenomenon. Nowadays, although many experimental demonstrations of TFETs were reported, a lot of research efforts are still needed to improve the on-state current ($I_{on}$).

The objective of this thesis is to explore novel TFET device designs as well as to integrate new materials to solve the on-current problem of TFETs. Various process technologies coupled with new materials have been proposed and experimentally realized. Si:C is introduced in the source of the TFET to achieve the enhancement of $I_{on}$ as well as $S$. GeSn, as new group IV material candidate for TFET, is investigated in both nTFET and pTFET, where its small and direct bandgap benefits the BTBT rate and ultimately results in enhanced drive current. GeSn pTFETs were experimental demonstrated and
decent $I_{on}$ is achieved. The seminal contributions of this thesis are listed in next Section.

7.2 Contributions of This Thesis

7.2.1 Investigation of Gate Capacitance in TFET (Chapter 2)

In order to have a more complete understanding of the electrical behavior of TFET, a detailed simulation study on TFET gate capacitances was performed. The total gate capacitance of TFET is asymmetrically partitioned into gate-to-drain ($C_{GD}$) and gate-to-source ($C_{GS}$) capacitances. The physical insights gained were discussed and a compact model of TFET gate capacitance was built. Reduction of $C_{GD}$ is desired since it is the Miller capacitance in circuit application of TFET, and schemes for $C_{GD}$ reduction were proposed by drain engineering as well as gate length scaling.

7.2.2 Design of TFETs with Extended Source (Chapter 3)

One efficient method to improve the tunneling current in TFET is to enlarge the tunneling area by novel device structures. Double-gate TFETs with different shapes of extended source are design to improve device performance, and their electrical characteristics were studied by TCAD simulation. By extending the source region into the middle of the TFET body under the gate, the tunneling area is enlarged, leading to an increase in BTBT current and thus the $I_{on}$. $S$ is also improved due to the better uniformity of the high electric field along source/channel interface, which is also the tunneling junction. The benefit of the extended source design is more obvious in TFET with Ge/Si
hetero tunneling junction as compared with all-Ge TFET. Simulation shows that TFET with squarish Ge-source Si-body can achieve a drive current of more than 0.8 mA/µm at $V_{DD} = 0.7$ V and an $I_{on}/I_{off}$ ratio of around 11 orders of magnitude. The extended source design could also be applied in multi-gate TFETs with other channel materials such as GeSn and III-V compound semiconductors.

7.2.3 Assessment of GeSn nTFET (Chapter 4)

To improve the efficiency of BTBT in TFET, the material(s) used in the tunneling region needs to have a small bandgap. We investigated the GeSn alloy, whose bandgap is smaller than that of Ge, as a novel substrate material for high performance nTFET. GeSn nTFETs with Sn composition varying from 0 to 0.2 were simulated with help from non-local Empirical Pseudopotential Method (EPM) calculations, which capture the material properties of GeSn alloy. By increasing the Sn composition, GeSn transits from an indirect to a direct bandgap material with cross-over at Sn composition of 11%, and $I_{on}$ of GeSn TFETs is improved due to the higher direct BTBT rate. In addition, sub-60 mV/decade $S$ is achieved at higher drain current ($I_{DS}$) level with increasing Sn composition, e.g. sub-60 mV/decade $S$ is achieved at $I_{DS}$ of ~8 µA/µm in Ge$_{0.8}$Sn$_{0.2}$ TFET.

7.2.4 Demonstration of TFET with Si:C Source Tunneling Junction (Chapter 5)
Another efficient method to improve tunneling current in TFET is to use an abrupt tunneling junction. It is known that a $p^+-n^+-p-n^+$ TFET can achieve better device performance due to extremely abrupt tunneling junction. Investigation was performed by employing Si:C source in $p^+-n^+-p-n^+$ nTFETs, and the experimental result shows that further reduction in $S$ and enhancement in $I_{on}$ are achieved. This is mainly attributed to the effective suppression of boron diffusion due to the presence of substitutional carbon at the source side. Thus, the resulting abrupt boron profile leads to enhanced BTBT of electrons. In addition, the induced tensile strain due to the lattice mismatch between Si:C and Si reduces the bandgap at source tunneling junction, which also benefits the BTBT of electrons.

7.2.5 Demonstration of Planar GeSn pTFET (Chapter 6)

Due to the small direct bandgap (bandgap at Γ-point) as well as the high hole mobility, GeSn is a promising material candidate for pTFET application. We demonstrated the world’s first planar GeSn pTFETs. Decent device characteristics were obtained, and a $I_{DS}$ of 29 $\mu$A/µm at $V_{DD}$ of 2 V is achieved for the Ge$_{0.958}$Sn$_{0.042}$ pTFET with a $L_G$ of 4 µm. The respectable $I_{DS}$ is attributed to the enhanced direct BTBT and high hole mobility in the GeSn channel. The low thermal budget (400 °C) of device fabrication process helps to form abrupt source tunneling junction to enhance BTBT of electrons.
7.3 Future Work

This thesis focuses on developing techniques to solve the low $I_{on}$ problem for TFETs, which is one of key challenges of TFETs for advanced logic applications. Nevertheless, several issues have been opened up in this thesis and deserve further investigation. Some of the suggestions for future directions of TFET technology are highlighted as follows.

7.3.1 Contact Optimization of GeSn pTFET

In Chapter 6, planar GeSn pTFET was demonstrated for the first time. However, the n$^+$ source resistance is large due to the Fermi level pinning (near valence band) at Ni(GeSn)/GeSn interface, which leads to a large Schottky barrier height for electrons and thus a high contact resistance. Future work can be performed to improve GeSn pTFET performance by optimizing the source-side contact formation process, such as selenium (Se) or sulfur (S) co-implant [141], where ohmic contact could be achieved.

7.3.2 GeSn pTFET with Hetero Tunneling Junction

Although the GeSn pTFET can achieve a high $I_{on}$, it suffers from large off-state current. Future work could focus on GeSn/SiGeSn hetero junction TFET, where SiGeSn has a larger bandgap to suppress drain side BTBT as well as thermal generation current in the channel, leading to a low $I_{off}$. The compositions of Si and Sn in SiGeSn need to be carefully designed to obtain a favorable band alignment, like type II staggered heterojunction, to enhance the
tunneling probability. In addition, the impact of induced stain in GeSn/SiGeSn heterojunction on device performance needs to be further investigated. Additional efforts need to be put on the growth of good GeSn/SiGeSn heterojunction.

7.3.3 Demonstration of GeSn nTFET and its integration with GeSn pTFET

GeSn is not only a favorable material for pTFET, but also promising for nTFET application due to its small bandgap as documented in Chapter 4. Compared with III-V nTFET, which is widely researched for nTFET recently, GeSn nTFET shows advantages in process compatibility with CMOS. While the author of this thesis did not manage to demonstrate GeSn nTFETs, further work can be carried out on the fabrication of high performance GeSn nTFETs. The gate stack issue can be foreseen in GeSn nTFET fabrication since the gate stack in Ge or GeSn nMOSFET is not well developed yet. Some of the techniques, like ammonium sulfide [(NH₄)₂S] treatment [142], germanium-tin oxide (GeSnO₂) [122] or Si surface passivation [143], and Ge capping [123] could be implemented in GeSn nTFET fabrication to obtain high quality gate interface. Therefore, good gate control in the channel could be achieved, leading to efficient BTBT of electrons from the source to the channel. Furthermore, integration of GeSn pTFET and nTFET could also be explored, and many process development efforts are needed to achieve high performance in both GeSn pTFET and nTFET.
7.3.4 Demonstration of TFET with Extended Source

Chapter 3 proposed double-gate TFETs with different shapes (wedge-shape, arc-shape, and squarish shape) of extended source design by simulation. A TFET with squarish Ge source and Si body outperformed the other designs in terms of high $I_{on}$ and $I_{on}/I_{off}$. Further work could be carried out to realize vertical TFET with this structure, and the fabrication steps could include dry etching, subsequent p-type in situ epitaxy growth of Ge source, and pillar formation by etching. N-type drain implant and gate stack formation as well as contact formation could be followed to complete the vertical TFET with squarish Ge source and Si body. More works can be done for the process optimization to obtain high performance devices.

7.3.5 Further Study on Gate Capacitance in TFET

In Chapter 2, the gate capacitance in TFET was investigated by simulation. Further study such as the impact of source/drain junction lateral profiles, trade-off between the gate capacitance and tunneling resistance on TFET $C-V$ characteristics could be performed. These studies will be very useful for future device design.

7.3.6 Calibration of Band-to-band Tunneling in GeSn

As theoretical study on GeSn TFET has been carried out in Chapter 4, it could be quite interesting to calibrate the simulation of band-to-band tunneling in GeSn more accurately with experimental data. Fabrication of vertical GeSn tunneling diodes is required with full control of the doping
profiles at tunneling junctions. Low temperature measurements will be useful to characterize Esaki tunneling phenomena and further verify the doping energy levels.
References


[5] S. Natarajan, M. Armstrong, M. Bost, R. Brain, M. Brazier, C.-H. Chang, V. Chikarmane, and M. Childs, “A 32 nm logic technology featuring 2nd-generation high-k plus metal-gate transistors, enhanced channel strain and 0.171 μm² SRAM cell size in a 291 Mb array,”


[10] E.-H. Toh, G. H. Wang, L. Chan, G. Samudra, and Y.-C. Yeo, “A doublespacer I-MOS transistor with shallow source junction and lightly doped drain for reduced operating voltage and enhanced device


with vertical silicon–germanium/germanium heterostructure,”


TSUPREM-4 Version F-2011.09-0, Synopsys Incorporation, 2011.


[141] Y. Tong, G. Han, B. Liu, Y. Yang, L. Wang, W. Wang, and Y.-C. Yeo, “Ni(Ge$_{1-x}$Sn$_x$) ohmic contact formation on n-type Ge$_{1-x}$Sn$_x$ using


Appendix

List of Publications

Journal and Letter Publications


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[38] L. Wang, S. Su, W. Wang, X. Gong, Y. Yang, P. Guo, G. Zhang, C. Xue, B. Cheng, G. Han, and Y.-C. Yeo, “(NH$_4$)$_2$S passivation for high mobility germanium-tin (GeSn) p-MOSFETs,” 6th *International SiGe Technology and Device Meeting (ISTDM)*, Berkeley, CA, USA, June 4-6, 2012.


[42] P. Guo, Y. Yang, Y. Cheng, G. Han, C. K. Chia, and Y.-C. Yeo, “Tunneling field-effect transistor with novel Ge/In$_{0.53}$Ga$_{0.47}$As tunneling
junction,” 222nd Electrochemical Society Meeting, Honolulu, HI USA, Oct. 7 - 12, 2012.


[46] X. Gong, S. Su, B. Liu, L. Wang, W. Wang, Y. Yang, E. Kong, B. Cheng, G. Han, and Y.-C. Yeo, “Negative bias temperature instability study on Ge$_{0.97}$Sn$_{0.03}$P-MOSFETs with Si$_2$H$_6$ passivation and HfO$_2$ high-k and TaN metal gate,” 222nd Electrochemical Society Meeting, Honolulu, HI USA, Oct. 7 - 12, 2012.

[47] G. Han, Q. Zhou, P. Guo, W. Wang, Y. Yang, and Y.-C. Yeo, “In situ boron doped germanium (Ge:B) grown on (100), (110), and (111) silicon: Crystal orientation and B incorporation effects,” 222nd Electrochemical Society Meeting, Honolulu, HI USA, Oct. 7 - 12, 2012.


(GeSn) n-channel MOSFETs with low temperature silicon surface passivation,” *International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA)*, Hsinchu, Taiwan, Apr. 22-24, 2013.

[50] C. Zhan, W. Wang, X. Gong, P. Guo, B. Liu, Y. Yang, G. Han, and Y.-C. Yeo, “(110)-oriented germanium-tin (Ge0.97Sn0.03) p-channel MOSFETs,” *International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA)*, Hsinchu, Taiwan, Apr. 22-24, 2013.