CHARACTERIZATION AND DESIGN OF CMOS COMPONENTS FOR MICROWAVE AND MILLIMETER WAVE APPLICATIONS

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Summary

Accurate models of the on-chip active and passive components are essential for successful CMOS IC designs. This work aims to characterize important active and passive components in modern CMOS technologies for microwave and millimeter wave applications to accommodate the two trends in many practical applications: smaller technology nodes and higher operating frequencies. The thesis is mainly concerned with the noise characterization of 65nm RF n-MOSFETs, modeling of the impact of metal dummy fills on the microwave behavior of spiral inductors, and the design of line resonators and filters at 60 GHz and 77 GHz in a 0.18-μm CMOS process.

To investigate the noise properties of the nano-scale MOSFETs at microwave frequencies, the various noise sources in the MOSFETs are extracted based on an equivalent circuit from measured S-parameters and noise parameters. It is found that the intrinsic noise figure generally improves with a shorter gate length, mainly due to the reduced induced gate noise. However, the excess noise increases in the shorter channels which holds back the improvement of the intrinsic noise figure of the MOSFETs to a certain extent. Additionally, the thermal noise from the extrinsic parasitics, particularly the gate resistance which is inversely proportional to the gate length, has an increasing weight in the total MOSFET noise figure. The overall noise performance may deteriorate when the gate length reduces to below 100 nm.

In smaller CMOS technology nodes, metal dummy fills are inserted in all the metallization layers to fulfill the process metal density and uniformity requirements. They influence the passive components when the frequency increases into the mi-

crowave range. The Q-factor of the on-chip spiral inductors is shown to be degraded by the inserted metal dummy fills. By comparing the extracted model parameters based on a physics-based model from the experimental results, it is found that the main reason for the reduced Q-factor is due to the increased oxide capacitance. A methodology is proposed to update existing inductor models by modifying the oxide capacitance analytically.

The feasibility of implementing millimeter wave passive filters in standard CMOS technology is studied in this thesis. A technique to use the lowest metallization as a ground plane is exploited to reduce the losses in the silicon substrate. First, the best layer configuration for transmission lines with the ground plane in a 0.18-μm CMOS is identified by comparing the unloaded Q-factors of three viable options. Next, coupled-line bandpass filters at 60 and 77 GHz with different bandwidths are realized using $\lambda/4$ line resonators. The relationship between the center frequency insertion loss and the 3-dB bandwidth is determined experimentally. The results provide trade-off considerations for the design of the 60 GHz and 77 GHz filters in CMOS.

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CHAPTER 1

Introduction

1.1 CMOS Technology for Microwave and Millimeter Wave Applications

The rapid development and expansion of the wireless communication market has driven the wide application of radio-frequency integrated circuits (RFICs). The spectrum for most wireless applications is from the RF range to the millimeter wave range allocated as illustrated in Fig. 1.1.

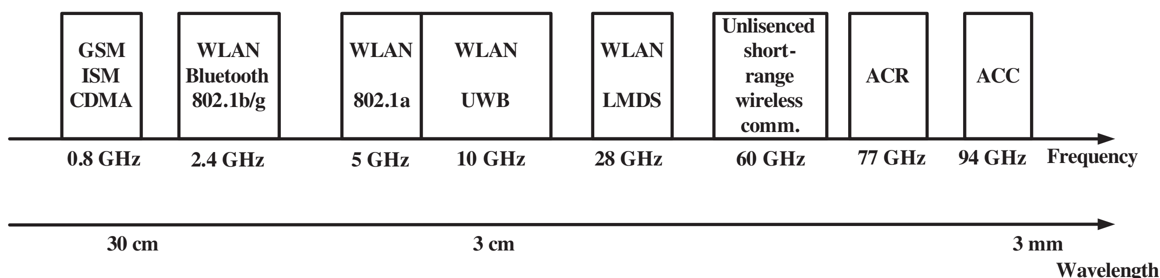


Figure 1.1: Frequency spectrum of wireless applications (after [1]).

With the growing interest in short-range broadband wireless communications in microwave and millimeter wave frequency bands, such as 22-29 GHz and 76-77 GHz for automotive radar, and 57-64 GHz for unlicensed use, for higher data rates of 100 Mbit/s to 1 Gbit/s and beyond, higher operating speeds or frequencies and lower power consumption have been become general trends for wireless electronics [2]. Advances in the semiconductor technologies for the microwave and millimeter wave ICs are highly needed to fulfill these demands.

Traditionally, microwave ICs were mostly realized in III-V technologies. GaAs or InP based field-effect transistors (MESFETs) and heterostructure field-effect transistor (HFETs) can operate at higher speeds and are superior in low noise performance because of the high mobility of the electrons. However, these technologies are costly for consumer electronics.

Silicon-based technologies have received profound interest for reasons of low cost and high yield. Between CMOS and SiGe BiCMOS technologies, CMOS is even cheaper, and more advantageous in integrating digital circuits and data storage devices on the same chip. A constant effort has been made to realize whole communication systems on a single chip to further bring down the manufacturing cost, complexity, and to improve the reliability. To this end, the integration of the RF front-end circuits in CMOS is of key importance.

Fortunately, CMOS technology is being pushed to higher operating frequencies, entering the millimeter wave range. MOSFETs with increased cutoff frequency f_T around 200 GHz have now been realized due to the downscaling of the modern CMOS technologies to the nano-scale level.

This downscaling phenomenon was first predicted by Gordon Moore in 1965: the number of transistors on an IC would double about every two years since invention [3]. This infers a scaling factor of $\sqrt{2}$ of the feature size designated by the "DRAM half-pitch" [4]. The semiconductor industry has almost kept the pace for more than 40 years. Currently in year 2009, a 32nm logical CMOS technology has been delivered by Intel on-target [5]. The scaling of CMOS technology generations in near- and long-term predicted by the International Technology Roadmap for Semiconductors (ITRS) is shown in Fig. 1.2 [1]. Note that, the smallest gate length is generally smaller than the feature size of a technology generation. For example, a 65nm CMOS can have a gate length smaller than 65 nm. Also shown in Fig. 1.2 are the increase in the peak $f_{\max}$ and peak f_T of the MOSFETs resulting

from the downscaling [1]. Many high-speed and microwave ICs are likely to be implemented in CMOS technology [6–10].

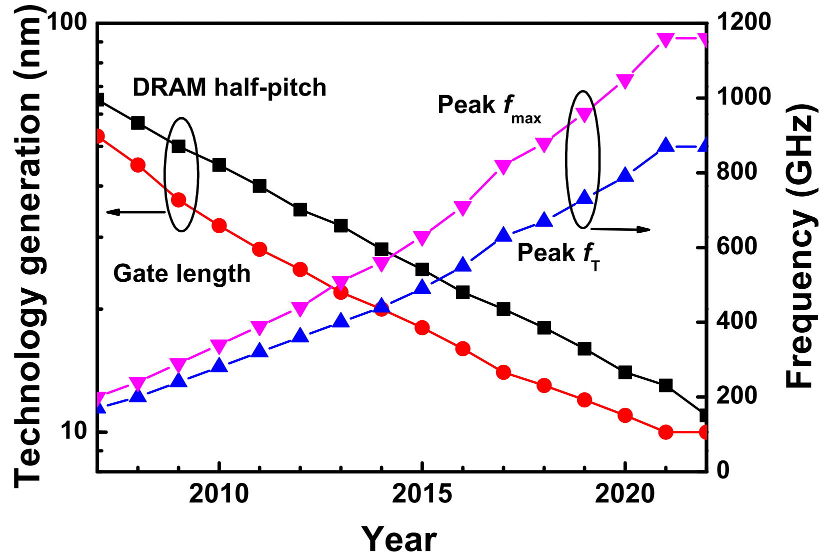


Figure 1.2: Predicted scaling of the gate length and peak $f_{\max}$ and peak f_T of CMOS technology in near- and long-term (after [1]).

1.2 CMOS Components

The success in CMOS RFIC design strongly depends on the availability of accurate models of the constituent components. New challenges are faced as the components shrink in size, and operate at higher frequencies.

1.2.1 MOSFETs

The evolution of CMOS technologies has mostly been digital-oriented. The foundries first develop the process for digital design which mainly targets higher transistor density, higher speed, and lower power dissipation. Then, modifications may be made to the process to suit mixed-signal and analog RF applications. Options such as using copper in the top metal layer, thickening the top metal layer or adding

a special device mask may be taken. Moreover, the performance of the MOSFET remains the foremost component to represent the progress of the process.

In terms of MOSFET application for RF circuits, there are three most important figure-of-merit parameters: the cutoff frequency associated with the short-circuit current gain f_T, the maximum frequency of oscillation $f_{\max}$, and the minimum noise figure $NF_{\min}$. Higher f_T and $f_{\max}$ enable higher operating frequencies of CMOS ICs with better performance. Lower $NF_{\min}$ is required to reduce the noise figure of the circuits. This is of key importance in most receiver front-end circuit design to improve the receiver sensitivity.

Although both f_T and $f_{\max}$ are almost linear to $1/L$, where L is the MOSFET gate length, as shown in Fig. 1.2, the scaling of $NF_{\min}$ with the technology node has been found more complex. First of all, the $NF_{\min}$ is a function of frequency and bias. Due to the various noise mechanisms in a MOSFET, such as flicker noise, generation-recombination noise, shot noise, and thermal noise, the overall noise behavior of the MOSFET depends on the operation region, and the operating frequency. Moreover, different noise sources may have different scaling properties. Finally, $NF_{\min}$ has a complex relationship with the various noise sources through small-signal parameters. Hence, accurate modeling the noise performance of the MOSFETs is extremely important.

Compact MOSFET models have been developed over the years. The most popular one is the industry standard BSIM series MOSFET models developed by the research group from UC Berkeley with a current version of BSIM4 [11]. The BSIM4 model predicts the DC, small-signal, and noise behavior based on a large number of parameters (more than 300), including model parameters and process parameters provided by the foundries. High accuracy of fitting the model parameters to different technologies is one of the main challenges.

Noise performance for smaller MOSFETs or at higher frequencies is still dif-

ficult to predict due to the various short-channel effects, exacerbated substrate noises, and non-quasi-static effects [12]. Experimental verification of the commercial models has been reported. Deviations of the measured noise performance in subthreshold region with the BSIM4 model predictions were reported in [13]. In [14], it was found that additional gate noise sources were added to the BSIM4 model in order to fit the experimental results.

The weakness of BSIM4 model in the weak to moderate inversion regions is because it is based on a threshold voltage formulation which inherently lacks of physical solutions in these regions [15]. The surface potential based formulation is a better approach to solve this problem. However, a major drawback of the models is that the surface potential is formulated by an implicit relation and thus, requires an iterative solution.

As the technology node continues to reduce, and the operating speed of the MOSFETs increases into the microwave and millimeter wave regime, accurate compact models to predict the DC, small-signal, and noise behavior of the MOSFETs for a broad range of bias conditions and operating frequencies are more urgently demanded.

1.2.2 Passive Components

Integrating passive components is imperative to realize high-performance low-cost system-on-chips. On-chip passive components include resistors, capacitors, inductors, and transmission lines. They are frequently used in designing matching networks, resonance circuits, filters, and antennas. As the operating frequency increases into the microwave regime, the intrinsic and substrate parasitics of the passives play a key role in the overall circuit behavior.

Resistors, capacitors, inductors are all lumped components which are usually much smaller than the operating wavelength and have relatively lower quality

factors than distributed components. The resistors and capacitors are beyond the scope of this thesis and are introduced very briefly here.

Resistors are typically used in bias circuits. A precise resistor is implemented using the doped polysilicon in CMOS salicide process which has a low sensitivity to voltage changes and temperature variations. Important characteristics of polysilicon resistors include the interface resistance, sheet resistance, and the process deviation of the polysilicon resistor width [16]. Integrated capacitors in CMOS usually take the forms of metal-insulator-metal (MIM) or MOS capacitors. A MOS capacitor which is formed between poly-silicon layer and N-well layer provides larger capacitance value per unit area, however, such capacitor has a larger capacitance variation. The Q-factor of the capacitors becomes more critical at millimeter wave frequencies [17].

Inductors play a vital role in CMOS RFICs. They are widely used in microwave integrated circuits including oscillators, low noise amplifiers and matching networks. The Q-factor is an important measure of the inductors which determines the overall performance of the circuits. For instance, in VCO design, inductors with a high Q-factor are required to achieve a low phase noise. Over the decades, enormous efforts have been devoted to the modeling of on-chip inductors at microwave frequencies. Compact parasitic models have been proposed to characterize high frequency effects such as the skin effect, proximity effect, and substrate losses [18–20]. However, the inductor models need to be updated with the progress in CMOS technology. Examples include using copper instead of aluminum as the interconnect layers and inserting the metal dummy fills to meet the uniform metal density requirement on all the interconnect layers. The inductor models must be able to take into account the influence of these metal dummy fills on the microwave performance of the inductors.

As the operating frequency enters the millimeter wave regime, wavelengths

become comparable to on-chip component dimensions. As a result, transmission lines are more widely used in both narrow-band and broad-band circuit design [7, 21]. They can realize small and accurate inductances and thus replace lumped inductors to achieve resonance at higher frequencies [22]. They can realize a broad range of impedance and are widely utilized in matching circuits [23]. To achieve high performance of the circuits, dedicated efforts have been made in the design of low loss transmission lines. Several viable transmission line structures in standard CMOS have been studied. Types of transmission lines can be implemented in CMOS process, such as a simple transmission line on the SiO_2-Si substrate, a CPW line consisting of a conductor and a pair of ground planes on the same plane, and a microstrip-like transmission line with a signal line and a ground plane in between the signal line and the silicon substrate. These transmission lines support different electromagnetic modes and have applications in the circuit.

1.3 Motivation, Scope, and Thesis Organization

The aim of this thesis is to characterize and design the on-chip components in order to cater for the two trends in the progress of CMOS technology and its applications: smaller technology nodes and the increased operating frequency.

More specifically, the problems defined in this research are listed below.

1. For MOSFETs in a 65nm CMOS technology, the microwave noise properties of the MOSFETs biased in the weak to moderate inversion regions have not been fully characterized.

2. The insertion of the metal dummy fills required in advanced CMOS process influences the microwave performance of spiral inductors, and thus the inductor models need to be updated to take into account the impact of the metal dummy fills;

3. To push the integration level as high as possible, on-chip millimeter wave bandpass filters are desired. Integrating the filters in standard CMOS was restricted by the considerable losses in the lossy silicon substrate (typical resistivity about 10 Ω-cm).

The main objectives of this research are:

1. to extract the various noise sources in short channel MOSFETs, to examine the contribution of the respective noise sources, and to investigate the scaling behavior of MOSFET noise parameters with reduced gate length;
2. to characterize the influence of the floating metal dummy fills on the microwave behavior of on-wafer spiral inductors, and to develop a methodology for designers to update the existing models of the conventional on-chip inductors to account for the effects of dummy fills;
3. to identify an optimum configuration in a standard CMOS for millimeter wave line resonator with the highest Q-factor; to design coupled line millimeter wave bandpass filters with various bandwidth, to determine the relationship of the center frequency insertion loss and the 3-dB bandwidth of the filters for the adopted CMOS process.

All of the research work presented in this thesis is based on or verified by experimental results. As a basis, the on-wafer measurements and de-embedding techniques for S-parameters and noise parameter measurements are discussed in chapter 2.

Chapter 3 presents the microwave noise characterization of MOSFETs with scaled gate lengths from 60 nm to 240 nm biased in weak to moderate inversion regions. A methodology for noise source extraction and breakdown based on measured noise parameters is demonstrated. The contributions of various noise

sources to the noise figure of the MOSFET are quantified. The results highlight the important noise sources as the gate length reduces.

Chapter 4 presents the characterization of the influence of the metal dummy fills on the performance of spiral inductors up to 40 GHz, and proposes an approach to update the existing compact models by accounting for the effects. In chapters 5 and 6, a systematic study of millimeter wave line resonators and the design of bandpass filters at 60 and 77 GHz in a standard CMOS is demonstrated. Options to further improve the millimeter wave performance of the on-chip filters will be discussed.

The thesis concludes with Chapter 7, which summarizes the main contributions of the thesis and proposes directions for future research.

1.4 List of Publications

Journal Papers

- L. Nan, Y.-Z. Xiong, K. Mouthaan, A. Issaoun, J. Shi, and B.-L. Ooi, "A Thru-Short Method for Noise De-Embedding of MOSFETs," *Microwave and Optical Technology Letters*, vol. 51, no. 5, pp. 1379-1382, Mar 2009.

- L. Nan, K. Mouthaan, Y.-Z. Xiong, J. Shi, S. C. Rustagi, and B.-L. Ooi, "Design of 60- and 77-GHz Narrow-Bandpass Filters in CMOS Technology," *IEEE Transactions on Circuits and Systems II*, vol. 55, no. 8, pp.738-742, Aug. 2008.

- L. Nan, K. Mouthaan, Y.-Z. Xiong, J. Shi, S. C. Rustagi, J. Brinkoff, and B.-L. Ooi, "CMOS Bandpass Filters for 77 GHz Automotive Radar Systems," *Microwave and Optical Technology Letters*, vol. 50, no. 11, pp. 2934-2937, Nov. 2008.

- J. Shi, Y.-Z. Xiong, K. Kang, L. Nan, F. Lin, "RF Noise of 65nm MOSFETs in Weak to Moderate Inversion Regions," *IEEE Electron Device Letters*, vol. 30, no. 2, pp. 185-188, Feb. 2009.

- K. Kang, L. Nan, S. C. Rustagi, K. Mouthaan, J. Shi, R. Kumar, W.-Y. Yin, and L.-W. Li, "A Wideband Scalable and SPICE-Compatible Model for On-Chip Interconnects Up to 110 GHz," *IEEE Transaction on Microwave Theory and Technology*, vol. 56, no. 4, pp. 942-951, Aril 2008.

- Y.-Z. Xiong, J. Shi, L. Nan, and F. Lin, "Gate Substrate Effect on RF CMOS Device Noise," *Electronics Letters*, vol. 43, no. 24. November 2007.

- Y.-Z. Xiong, A. Issaoun, L. Nan, J. Shi, and K. Mouthaan, "Simplified RF Noise De-embedding Method for On-Wafer CMOS FET," *Electronics Letters*, vol. 43, no. 18, pp. 1000-1001, August 2007.

Conference Papers

- L. Nan, K. Mouthaan, Y.-Z. Xiong, J. Shi, S. C. Rustagi, J. Brinkoff, and B.-L. Ooi, "60 GHz Bandpass Filters with Small and Large Bandwidths Using Thin Film Coupled Microstrip in 0.18-μm CMOS," in *2008 Asia-Pacific Microwave Conference (APMC)*, Hong Kong and Macau, Dec. 16-20, 2008.

- L. Nan, K. Mouthaan, Y.-Z. Xiong, J. Shi, S. C. Rustagi, and B.-L. Ooi, "Unloaded Q-Factors of Thin Film Microstrip Resonators in 0.18-μm CMOS for Millimeter Wave Applications," in *2008 Asia-Pacific Microwave Conference (APMC)*, Hong Kong and Macau, Dec. 16-20, 2008.

- L. Nan, K. Mouthaan, Y.-Z. Xiong, J. Shi, S. C. Rustagi, and B.-L. Ooi, "Improved Microwave Modeling of CMOS Spiral Inductors with Metal Dummy

Fills," in *the 10th Electronics Packaging Technology Conference (EPTC) 2008*, Singapore, Dec. 9-12, 2008.

- L. Nan, K. Mouthaan, Y.-Z. Xiong, J. Shi, S. C. Rustagi, and B.-L. Ooi, "Impact of Metal Dummy Fills on the Performance of CMOS Inductors," in *IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC) 2007*, Taiwan, Dec. 20-22, 2007.

- L. Nan, K. Mouthaan, Y.-Z. Xiong, J. Shi, S. C. Rustagi, and B.-L. Ooi, "Experimental Characterization of the Effect of Metal Dummy Fills on Spiral Inductors," in *Radio Frequency Integrated Circuits (RFIC) Symposium 2007*, Hawaii, Honolulu, 3-5 June, 2007.

CHAPTER 2

On-Wafer Measurements and De-embedding

2.1 Introduction

For microwave and millimeter wave IC designs, accurate and robust component models are required for simulations. The first challenge that a modeling engineer faces in developing such models is to obtain accurate measurement data of device test-structures. At microwave frequencies, the accuracy of on-wafer calibration and parasitic deembedding techniques is still an extremely important issue for device characterization and modeling.

In this work, the on-wafer measurement system and calibration techniques will be introduced. Next, various de-embdding methods will be discussed. Three sets of experimental data applying these methods will be shown to further demonstrate the suitability of the methods for different applications.

2.2 S-Parameter Measurements

2.2.1 S-Parameters

S-parameters are fundamental for characterizing linear two-port networks at microwave frequencies. They measure traveling waves rather than total voltages and currents. The S-parameters are defined in relation to the reflected and incident

power waves at each of the network ports as

$$b_1 = S_{11}a_1 + S_{12}a_2$$
$$b_2 = S_{21}a_1 + S_{22}a_2 \tag{2.1}$$

where the waves a_n and b_n are the root-mean-square (rms) voltages $V_{in,n}$ of the incident and reflected waves at port n ($n = 1, 2$) respectively normalized with a characteristic impedance Z_0 (usually 50 Ω):

$$a_1 = \frac{V_{in,1}}{\sqrt{Z_0}} \quad a_2 = \frac{V_{in,2}}{\sqrt{Z_0}}$$
$$b_1 = \frac{V_{out,1}}{\sqrt{Z_0}} \quad b_2 = \frac{V_{out,2}}{\sqrt{Z_0}} \tag{2.2}$$

The parameters S_{11} and S_{22} are the reflection coefficients with the opposite port terminated in Z_0 . The parameters S_{12} and S_{21} are the forward and reverse transmission coefficients respectively.

2.2.2 Vector Network Analyzer

The S-parameters of passive and active networks can be measured with a vector network analyzer (VNA), which is usually a two-channel receiver designed to measure the amplitude and phase of the transmitted and reflected wave quantities from the network [24].

Fig. 2.1 shows the key elements of a VNA [25]. The RF source is coupled to the device-under-test (DUT) by forward and reverse switches and directional couplers. The forward and reverse waves at the test ports are down-converted to IF sections for further digital processing and display.

On-wafer measurements are performed with a VNA combined with probes. Before proceeding to the measurement of the test structures, a calibration procedure is required to define the reference planes at the probe tips. Imperfections of the measurement system from the VNA itself, cable losses, and probe losses and reflections, beyond the reference planes must be corrected and removed [26]. Accurate calibrations are important to ensure reliable subsequent on-wafer measurements.

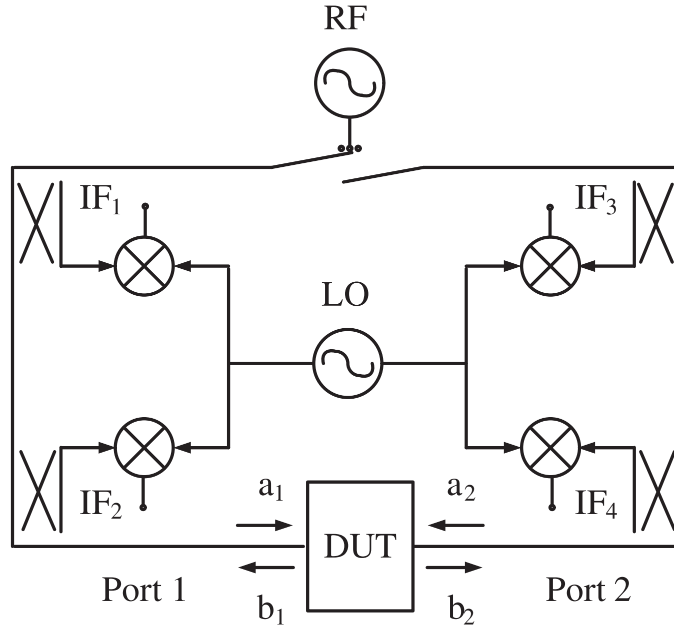


Figure 2.1: Block diagram of a vector network analyzer (VNA).

The main idea of calibration is to model and remove the system imperfections by measuring standards with known or partly known characteristics. The standards can include short-circuit, open-circuit, 50 Ω loads and through lines fabricated on a separate impedance standard substrate (ISS). Open-circuit can also be realized by raising the probes in air above the wafer by at least 250 μm [26].

The required standards depend on the calibration method employed. There are a number of calibration methods available. Most commonly used ones are SOLT, SOLR, LRM, LRRM, and TRL. These calibration algorithms have their own advantages and limitations in practice. Proper choice of the method is needed, and the verification of calibration results is important [25].

With SOLT (short-open-load-thru) and SOLR (short-open-load-reflect) methods, exact parasitic inductances and capacitances of the standard must be known. Main problems with this kind of methods include difficulties in determining the parasitics of the standards, and that variations in the parasitic descriptions greatly degrade the accuracy. Since the variations of the inductive and capacitive para-

sitics are more severe at higher frequencies, these methods are more suited for lower frequency measurements (below 20 GHz) [26].

LRM (line-reflect-match) and LRRM (line-reflect-reflect-match) methods are more advanced. Only the resistance of the match needs to be known, which can be obtained accurately at DC [27]. Thus they are more suitable for broadband measurements. The LRRM method has an additional advantage over the LRM method: it avoids discrepancies between the load reactances seen by the port-1 and port-2 probes by adopting two reflections (short and open). These methods are normally implemented in WinCal software unlike those accessible in the VNA such as SOLT and SOLR.

In this work, we use the LRRM calibration in most of the experiments, especially for those at millimeter waver frequencies.

2.3 Noise Parameter Measurements

Noise factor (the noise factor in dB is called noise figure and is denoted by *NF*) is a measure of the degradation in the signal-to-noise (SNR) ratio between the input and output of the component. The noise factor F of any noisy linear two-port network can be represented by:

$$F = F_{\min} + \frac{R_n}{G_s}|Y_s - Y_{opt}|^2 \tag{2.3}$$

where $F_{\min}$ is the minimum noise factor, R_n is the equivalent noise resistance, G_s is the source admittance and Y_{opt} is the optimum source admittance which results in the $F_{\min}$. Note that the noise factor defined here assumes that the input noise is at the standard noise temperature of $T_0 = 290$K.

To characterize the noise performance of a MOSFET, usually four parameters needed to be measured: $F_{\min}$, R_n and the complex Y_{opt}. The on-wafer noise measurement system is quite complex, and a simplified illustration is shown in Fig.

2.2 [28].

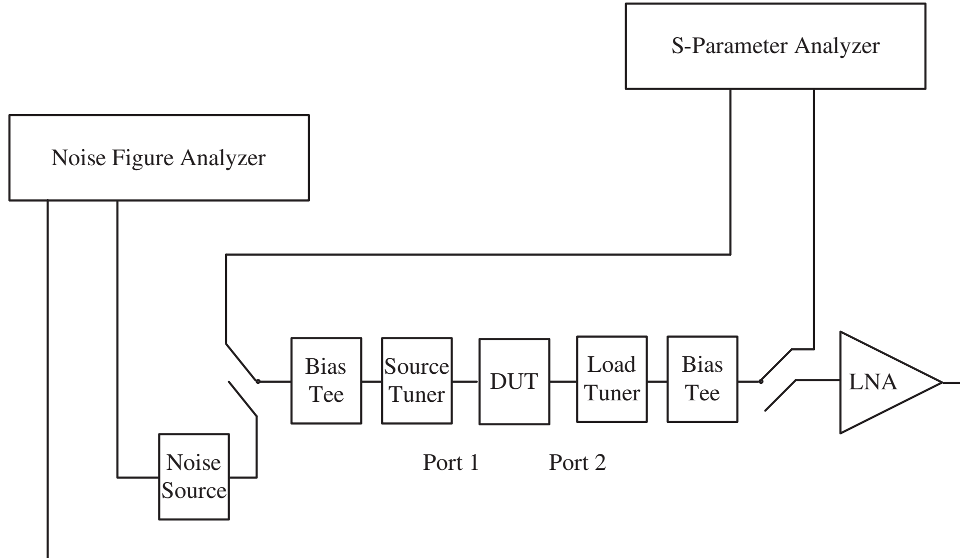


Figure 2.2: System setup for S-parameter and noise and on-wafer measurements.

It includes solid-state (or mechanical) tuners, a vector network analyzer (VNA) system, a noise figure analyzer, a microwave probe station and other peripheral devices such as a personal computer. In theory, the four noise parameters ($F_{\min}$, R_n and the complex Y_{opt}) can be calculated by measuring four noise factors corresponding to four different source impedances provided by the source tuner [29]. To ensure better accuracy, usually more impedance points are measured and then optimization techniques for minimizing different error functions are used to obtain these four noise parameters. Calibration for the whole system is extremely important. Reflection coefficient calibration of the system using the VNA and noise calibration of the noise source and noise meter are both need. The accuracy is usually verified by measuring a “thru” line which ideally leads to 0 dB noise figure over the frequency band.

2.4 De-embedding Techniques

Measurements for the test structures can be carried out after calibrating the measurement system using the ISS standards. It should be noted that if the transition from probe to the test-structure is much different from the transition from probe to the standard, for example when the test structure is on a lossy substrate like silicon, the pad parasitics must be further removed.

In addition the device under test (DUT) is typically embedded with interconnections from the ports of the DUT where the desired reference planes are located, to the contact pads as shown in Fig. 2.3. Here, the DUT shows a typical common-source transistor with the source legs connected to the ground bars. The contact pads, the interconnects, and the source ground legs all influence the measured S-parameters of the test-structures. Their effects must be de-embedded from the measured raw S-parameters of the test-structures in order to obtain the the behavior of the DUT.

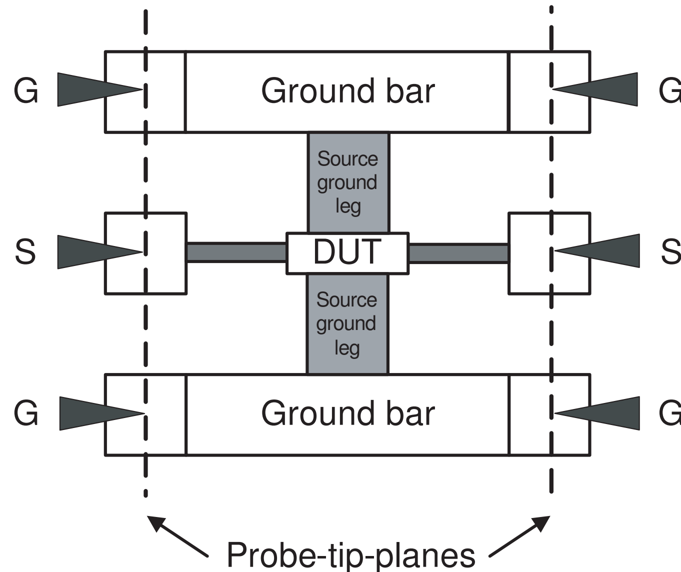


Figure 2.3: Layout of the test structure of the DUT. The measurement reference planes are located at the probe tips after calibration.

To do this, the parasitic effects beyond the DUT reference planes are determined

by fabricating and measuring additional standards on the same wafer with the DUT test-structure. These standards usually include "open", "short", and "thru". This section provides an overview of some commonly used de-embedding techniques. Improvements or alternatives are made to the existing methods.

2.4.1 Pad De-embedding

This is the simplest method, which only determines the parasitics for the contact pads. It assumes that the parasitics associated with the pads are shunt admittances in parallel with the DUT [30]. The required extra on-wafer standard is an "open" structure as shown in Fig. 2.4(a). The parasitic model of the DUT test-structure assumed in the method is shown in Fig 2.4(b). The Y elements stand for the frequency-dependent shunt parasitics which can be found in the on-wafer "open" standard.

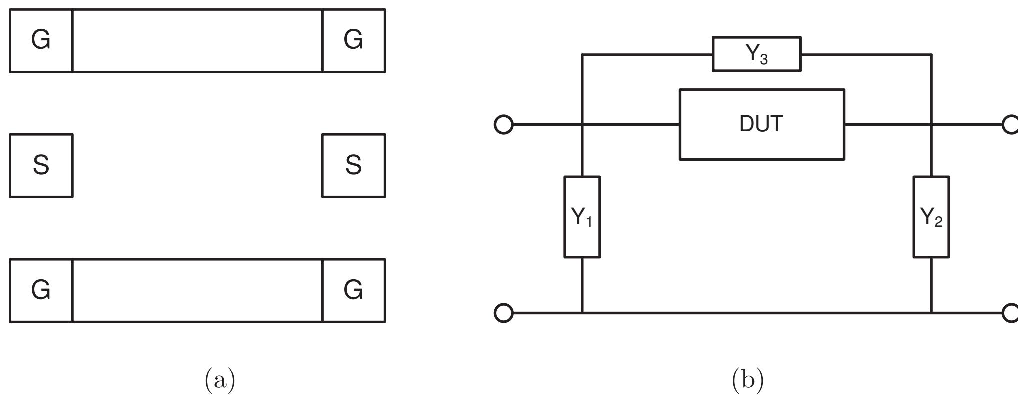


Figure 2.4: (a) Layout of an "open" standard. (b) The parasitic model of the DUT test-structure in a pad de-embedding method.

The Y-parameters of the DUT are easily found from:

$$[Y]_{DUT} = [Y]_{meas} - [Y]_{open}, \tag{2.4}$$

where $[Y]_{meas}$ are the measured raw Y-parameters of the test-structure, and $[Y]_{open}$ the measured Y-parameters of the "open" standard.

This method is only applicable for the cases where the series parasitics of the interconnects are negligible. Moreover, interconnects in CMOS technology are typically realized using aluminum traces while the ISS uses gold for the metallization, and therefore the contact resistance increases when the probes are lifted from the ISS onto the CMOS chip. Failure to consider this additional series contact resistance can introduce a significant error [31].

2.4.2 "Thru" De-embedding

This method further considers the series resistances and inductances of the interconnects in addition to the shunt parasitics of the pads. In this method, the interconnects on both sides of the DUT are designed with the same length of $L/2$ and the pads are the same as shown in Fig. 2.5(a). The required "thru" standard is designed as a combination of the contact pads and the two $L/2$ long interconnects as shown in Fig. 2.5(b).

The parasitic model of the DUT test-structure is assumed in Fig. 2.5(c). The shunt Y and a series Z represent the pad and interconnects parasitics respectively. They are solved from the Y-parameters of the "thru" standard as follows

$$Y_1 = Y_{11,thru} + Y_{12,thru} \tag{2.5a}$$

$$Z_1 = -Y_{12,thru} \tag{2.5b}$$

Based on the cascade network of the test-structure, the DUT can be solved by ABCD-matrix from

$$\begin{pmatrix} A & B \\ C & D \end{pmatrix}_{DUT} = \begin{pmatrix} 1 & Z_1 \\ Y_1 & 1+Y_1Z_1 \end{pmatrix}^{-1} \begin{pmatrix} a & b \\ c & d \end{pmatrix}_{meas} \begin{pmatrix} 1+Y_1Z_1 & Z_1 \\ Y_1 & 1 \end{pmatrix}^{-1} \tag{2.6}$$

where $\begin{pmatrix} A & B \\ C & D \end{pmatrix}_{meas}$ is the ABCD-matrix converted from the measured S-parameters of the test-structures.

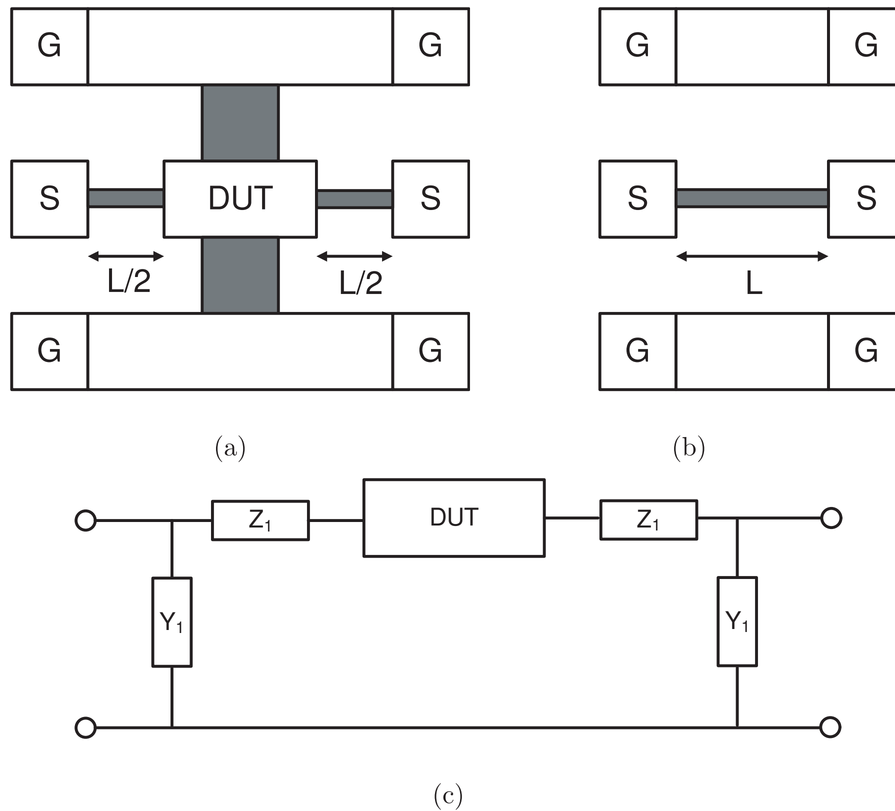


Figure 2.5: (a) Layout of the DUT test-structure. (b) Layout of a “thru” standard. (c) The parasitic model of the DUT test-structure in a “thru” de-embedding method.

Improved “thru” method

The conventional model of the “thru” may have problems at higher frequencies when the shunt parasitics of the interconnect such as substrate losses start to play. Hence, an improved model is proposed to account for these shunt parasitics by an additional admittance (Y_2) as illustrated in Fig 2.6.

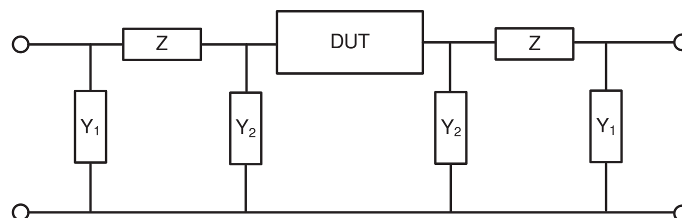


Figure 2.6: The parasitic model of the DUT test-structure in an improved “thru” de-embedding method.

Since three unknowns (Y_1, Y_2 and Z) are involved, one more condition needs to be given in order to get the solutions. For this purpose, a scaling factor k between Y_1 and Y_2 is pre-assumed, i.e., $Y_1 = kY_2$. This assumption is reasonable in the sense that the contact pad and interconnect can be treated as two transmission lines with different widths, and the shunt impedance is approximately proportional with the area of the transmission line. Thus the half-thru matrix can be obtained as

$$\begin{cases} a_1 = 1 + kx \\ b_1 = \frac{B}{2a} \\ c_1 = \frac{C}{2d} \\ d_1 = 1 + x \end{cases}, \text{ where } \mathrm{x} = \frac{\sqrt{(\mathrm{k}+1)^2 - 4\mathrm{k}(1-\mathrm{t})} - (\mathrm{k}+1)}{2\mathrm{k}} \text{ and } \mathrm{t} = \frac{\mathrm{A}^{\mathrm{thru}} + 1}{2} \tag{2.7}$$

It can be seen that the k factor restricts the relationship between a_1 and d_1 as

$$\frac{a_1 - 1}{d_1 - 1} = k \tag{2.8}$$

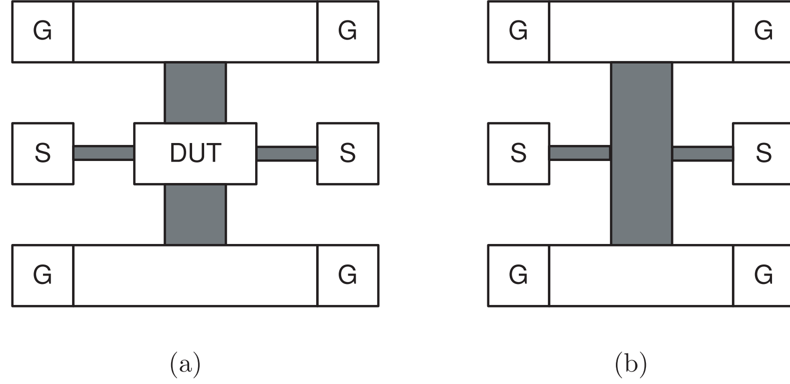
Given a one-degree of freedom of choosing the k factor, Eq. (2.7) can be solved and leading to the final de-embedding step:

$$\begin{pmatrix} A & B \\ C & D \end{pmatrix}_{DUT} = \begin{pmatrix} a_1 & b_1 \\ c_1 & d_1 \end{pmatrix}^{-1} \begin{pmatrix} a & b \\ c & d \end{pmatrix}_{meas} \begin{pmatrix} a_2 & b_2 \\ c_2 & d_2 \end{pmatrix}^{-1} \tag{2.9}$$

When $k = 0$, it reduces to the conventional model case where Y_2 does not exist.

2.4.3 "Open-Short" De-embedding

This method, referred to as two step de-embedding, measures two extra on-wafer standard: an"open" and a "short". The two-step de-embedding approach was originally envisioned for the high-frequency characterization of bipolar transistors [32]. The layouts of the DUT and the corresponding "short" are shown in Fig. 2.7 respectively.



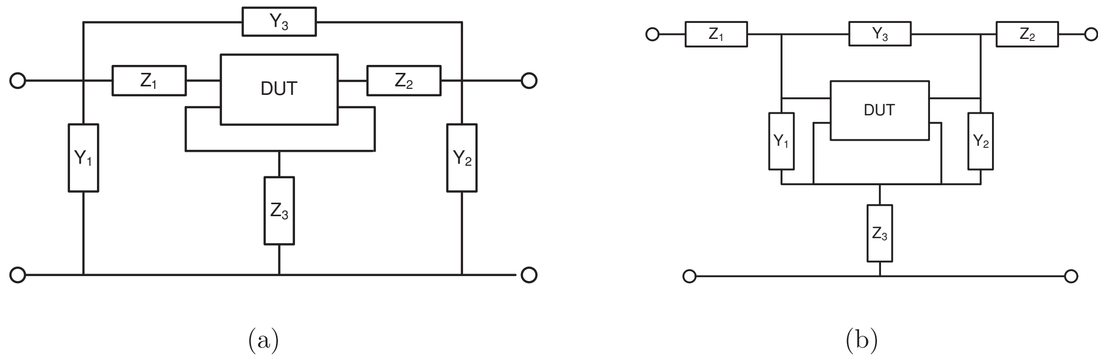
(a) (b)

Figure 2.7: (a) Layout of a DUT containing a transistor with the source connected to ground bars. (b) Layout of the "short" standard.

In addition to the shunt parasitics represented by the "open" as discussed in Fig. 2.4(b), the series parasitics introduced by the interconnects are modeled by the "short". Depending on how the shunt and series parasitics are connected in the model of the "short", two schemes are developed based on the same "open" and "short" standards. The well-known method "open-short" assumes a model as shown in Fig 2.8(a). The Y-parameters of the DUT are determined by:

$$[Y]_{DUT} = (([Y]_{meas} - [Y]_{open})^{-1} - ([Y]_{short} - [Y]_{open})^{-1})^{-1}, \tag{2.10}$$

where $[Y]_{short}$ is the measured Y-parameters of the "short" standard.



(a) (b)

Figure 2.8: The parasitic model of the DUT test-structure (a) in an "open-short" de-embedding scheme and (b) in a "short-open" scheme.

An alternative scheme which switches the order of the series impedance and parallel admittance as in the "open-short" method is the "short-open" de-embedding.

The model of the "short" in this method is shown in Fig. 2.8(b). The solution to $[Y]_{DUT}$ is:

$$[Y]_{DUT} = ([Z]_{meas} - [Z]_{short})^{-1} - ([Z]_{open} - [Z]_{short})^{-1} \tag{2.11}$$

The choice between these two schemes depends on the distribution of series and shunt parasitics of the "short" structure.

2.4.4 Three-Step De-embedding

A more comprehensive de-embedding method was proposed in [33]. In this method, four additional structures are needed, "open", "thru", "short1" and "short2" as shown in Fig 2.9.

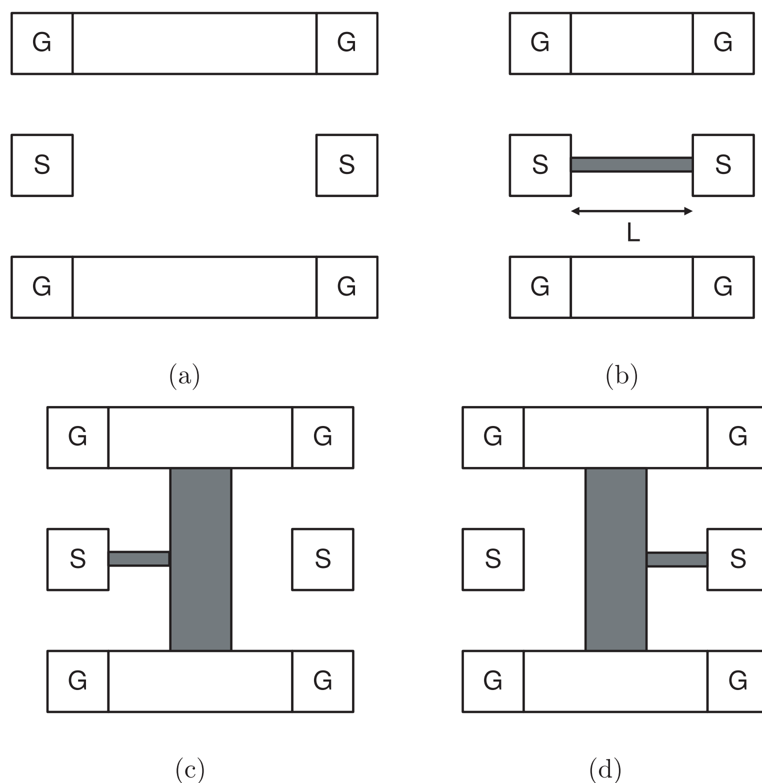


Figure 2.9: Layout of (a) "open", (b) "thru", (c) "short1", and (d) "short2".

The equivalent circuit of the test-structure with the parasitic elements is shown in Fig 2.10. Y_1 and Y_2 represent the capacitive coupling between pads and substrate while Y_3 reflects the coupling between the two ports of the DUT. The series

elements Z_1, Z_2 and Z_3 represent the impedance of the pads and the interconnects.

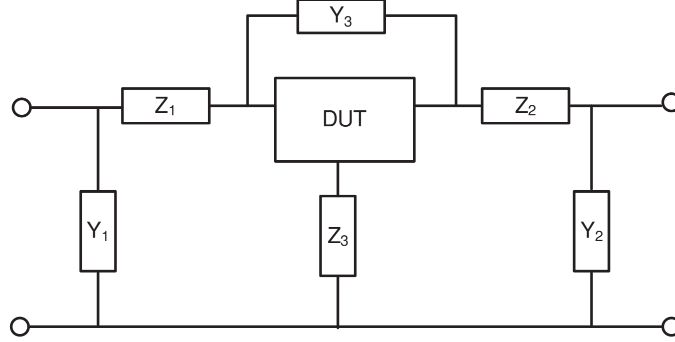


Figure 2.10: The parasitic model of the DUT test-structure in a three-step de-embedding method.

The Y and Z elements are solved from the "open", "thru", and "shorts" as below:

$$Y_1 = Y_{11,open} + Y_{12,open} \tag{2.12a}$$

$$Y_2 = Y_{22,open} + Y_{12,open} \tag{2.12b}$$

$$Y_3 = -Y_{12,open} \tag{2.12c}$$

$$Z_1 = \frac{1}{2}\left(\frac{1}{Y_{11,short1}} - \frac{1}{Y_{22,short2}} - \frac{1}{Y_{12,thru}}\right) \tag{2.12d}$$

$$Z_2 = \frac{1}{2}\left(-\frac{1}{Y_{11,short1}} + \frac{1}{Y_{22,short2}} - \frac{1}{Y_{12,thru}}\right) \tag{2.12e}$$

$$Z_1 = \frac{1}{2}\left(\frac{1}{Y_{11,short1}} + \frac{1}{Y_{22,short2}} - \frac{1}{Y_{12,thru}}\right) \tag{2.12f}$$

The de-embedding procedure is summarized in the following three steps [33]:

1. Subtract Y_1 and Y_2 from $[Y]_{meas}$, resulting in $[Y]'$.

2. Convert $[Y]'$ to Z-parameters $[Z]'$. Subtract Z_1, Y_2 and Z_3 from $[Z]'$, resulting in $[Z]''$.

3. Convert $[Z]''$ to Z-parameters $[Y]''$. Subtract Y_3 from $[Y]''$, and obtain the Y-parameters of the DUT $[Y]_{DUT}$.

This method is the most complete one considering all the parasitics associated with the pads, interconnects, and the source ground legs. However, good accuracy is achieved at the cost of computation complexity and the consumed wafer area for the additional standards.

2.4.5 "Thru-Short" De-embedding

The proposed "thru-short" method is similar to the "open-short" method but uses different standards and a different algorithm [34]. The parasitic model of the test-structure is shown in Fig. 2.11.

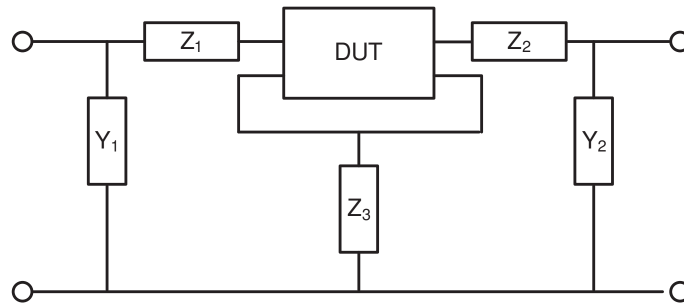


Figure 2.11: The parasitic model of the DUT test-structure in a "thru-short" de-embedding method.

The series parasitics Z_1 and shunt parasitics Y_1 are modeled by the "thru" standard, while the shunt Z_s represents the parasitic effects from the source ground legs of the transistor, and is modeled by the "short" standard. To extract Z_3, Y_1 and Z_1 must be removed from "short" first. The de-embedding steps of this method are summarized as follow:

1. Subtract Y_1 and Y_2 from $[Y]_{meas}$, , resulting in $[Y]'$.

2. Convert $[Y]'$ to Z-parameters $[Z]'$. Subtract Z_1, Y_2 and Z_3 from $[Z]'$, resulting in $[Z]''$.

3. Convert $[Z]''$ to Z-parameters $[Y]''$. Subtract Y_3 from $[Y]''$, and obtain the Y-parameters of the DUT $[Y]_{DUT}$.

2.5 Results and Discussions

To verify the various methods, three cases are studied: S-parameter de-embedding for transmission lines, S-parameter de-embedding for source grounded transistors, and noise parameter de-embedding for source grounded transistors.

2.5.1 Case 1: S-Parameter De-embedding for Two-Port Transmission Lines

A group of on-chip transmission lines with a width of 10 μm, lengths ranging from 100 μm up to 1000 μm were fabricated in a commercial 0.18 μm CMOS process. The technology consists of six metallization layers, and the transmission lines are placed on the top layer. The structure of the transmission lines is illustrated in Fig. 2.12. Measurements were performed using the Anritsu W3700 broadband VNA for 110 GHz, SUSS semi-auto probe station and Cascade infinity G-S-G probes. The system was calibrated to the probe-tip-planes using a LRRM calibration method.

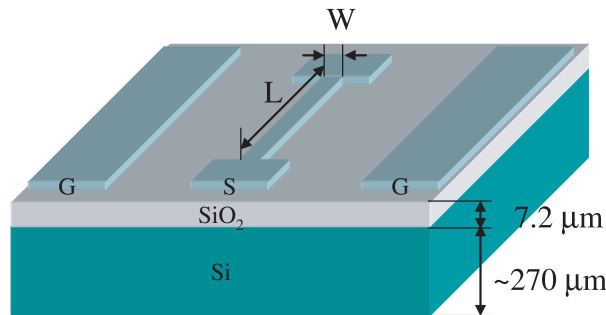


Figure 2.12: The structure of the transmission lines fabricated in a 0.18-μm CMOS technology.

Here, consider a test-structure of a transmission line with a length of 1000 μm. The contact pads used as square metal of 30×30 μm^2. The "thru" standard

is a 200 μm long transmission line with contact pads. After de-embedding, the intrinsic DUT is a 800 μm long and 10 μm wide transmission line. This DUT is also simulated in Momentum as a reference.

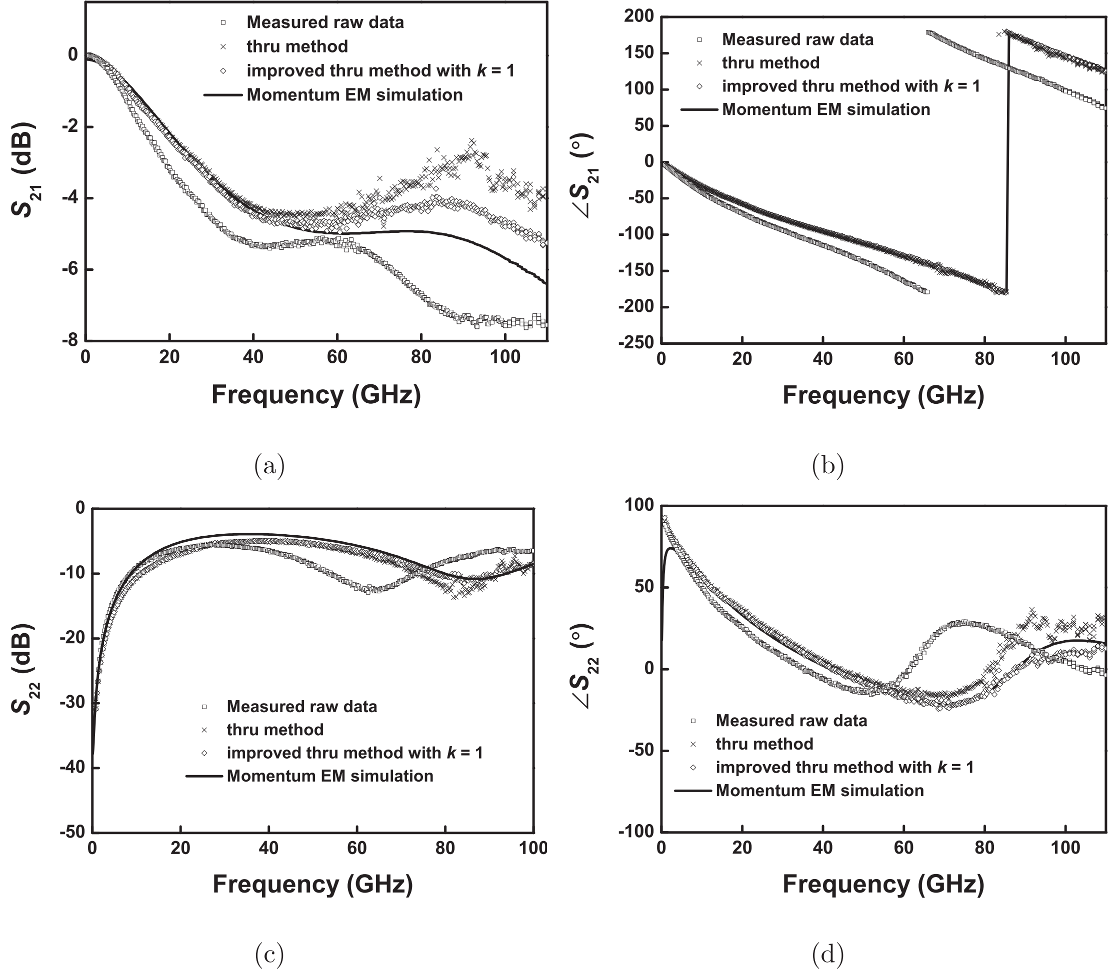


Figure 2.13: De-embedded S-parameters for a 800 μm long and 10 μm wide transmission line using different de-embedding methods. Momentum EM simulation results are also shown.

The “thru” method and the improved “thru” method with $k = 1$ are compared in Fig. 2.13. Momentum EM simulations are used as a reference. It shows that both methods calibrate $\angle S_{21}$ correctly shown in Fig. 2.13 (b). The improved “thru” method with $k = 1$ produces better results mainly in $|S_{21}|$ and $\angle S_{22}$. When the frequency is higher than 60 GHz, the improved “thru” method also has certain deviation in $|S_{21}|$ compared to the Momentum simulations. More experiments are

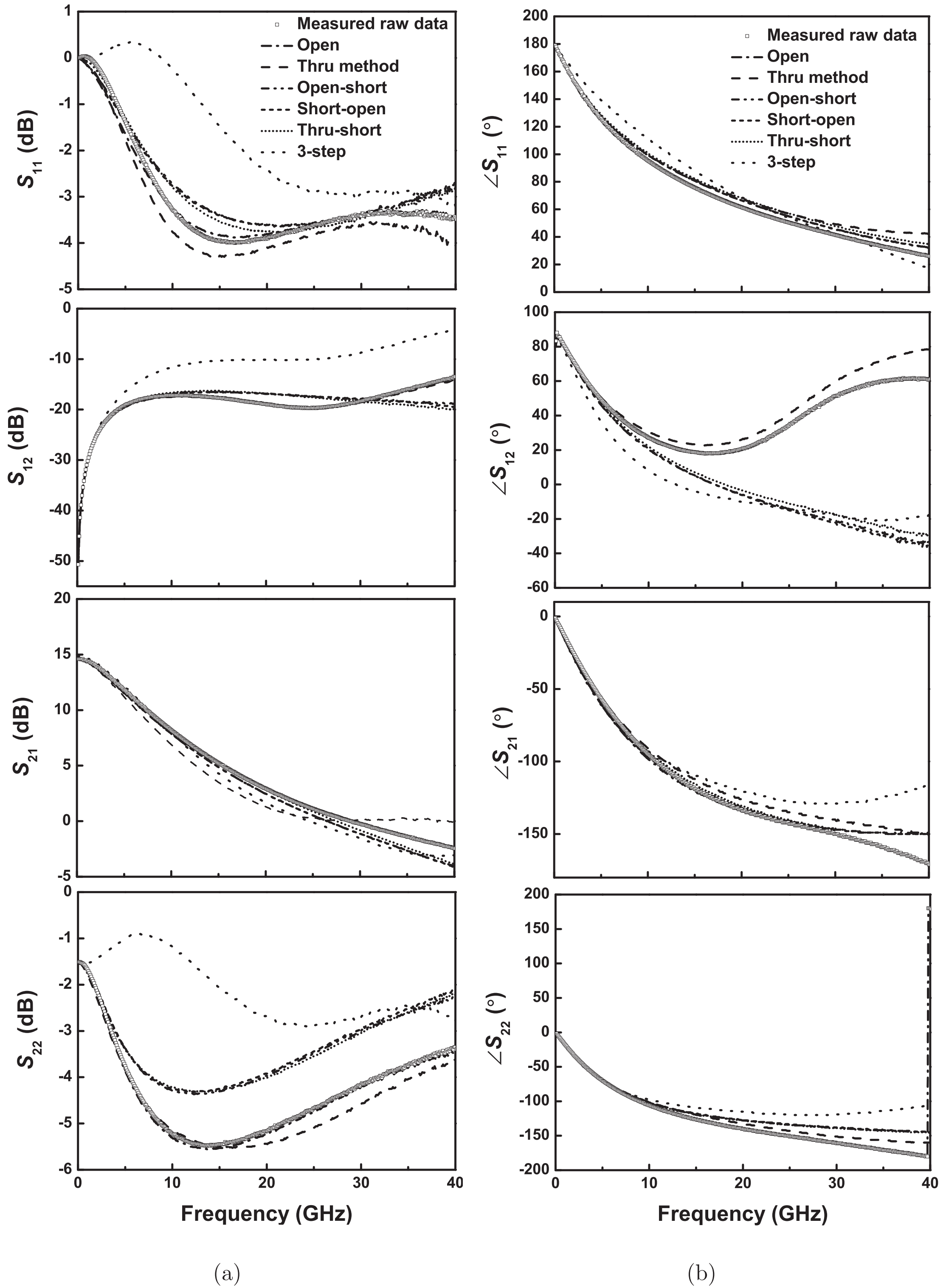
performed with varying the DUT line lengths, and similar results are observed.

2.5.2 Case 2: S-Parameter De-embedding for Source Grounded Transistors

In this case, the S-parameter de-embedding is performed on a MOSFET with its source terminal connected to ground by the "source ground legs". Compared to the two-port passives, the source ground legs further introduce parasitics to the intrinsic FET. The main purpose of this case is thus to show the effects of the source ground legs on the S-parameter de-embedding.

A 16-finger MOSFET with a unit gate width of 5 μm was used as a test-structure. The MOSFET was biased with $V_G = 0.7$ V and $V_D = 1.8$ V. On-wafer standards were also fabricated including a "open", a "thru", and two "shorts". Fig. 2.14 shows the de-embedding results using the open-short, three-step, thru, and thru-short de-embedding methods.

From the comparison, it is shown that for lower frequency applications, all methods except the pad de-embedding method lead to similar results, i.e., the dominant parasitics from the contact pads and the interconnects have been removed. The "thru-short" method is an alternative method to the widely used "open-short" method. They produce similar results. The three-step method does not show advantages in the accuracy in the conducted experiments of this work. Other than complexity, it may even cause deviations from the physical predictions such as $|S_{11}|$ and $|S_{22}|$ shown in Fig. 2.14. The difference between the three-step method and the "open-short" method mainly lies in the capacitive coupling element Y_3 in the equivalent circuit models shown in Fig. 2.8(a) and Fig. 2.10 respectively. The determination of how Y_3 should be connected strongly depends on the geometry of the test-structures. Above all, the coupling is more of a distributed effect than a lumped element at higher frequencies. Thus, this is is a general



(a) (b)

Figure 2.14: De-embedded S-parameters for a 16-finger MOSFET with $V_G = 0.7$ V and $V_D = 1.8$ V using different de-embedding methods.

drawback for all the lumped-element model based de-embedding methods. They all have a frequency limitation.

Effect of Source Ground Legs

The "thru" method is advantageous in simplicity and wafer-area cost efficiency. However, above 10 GHz, the limitation of the "thru" method becomes visible. Neglecting the source ground legs causes larger errors at higher frequencies. By comparing the results of the "thru" method and the "thru-short" method shown in Fig. 2.14, it shows that the two methods differ in $|S_{12}|$ and $|S_{12}|$ the most above 10 GHz, where the S-parameters are more sensitive to the effect of the source ground legs. The "thru" method results follow the raw data as if no de-embedding has been performed over the frequency range; whereas the "thru-short" method provides results as physically expected.

To examine the effect of the source ground legs, the parasitic resistance R_s and inductance L_s of the source ground legs are be extracted from the "thru-short" method and are shown in Fig. 2.15. The extracted inductance L_s is almost constant around 35 pH, while the resistance R_s is around 0.1 Ω below 20 GHz, but increases rapidly with frequency above 20 GHz. The skin effect can be used to explain this phenomenon, which implies the increasing importance of considering the effect of source ground legs at higher frequencies.

2.5.3 Case 3: Noise Parameter De-embedding for Source Grounded Transistors

Noise parameters characterize the noise behavior of the active devices, such as transistors. Through this case, the effects of the source ground legs on the nosie parameter de-embedding will be demonstrated.

Noise parameter de-embedding is performed together with the S-parameter

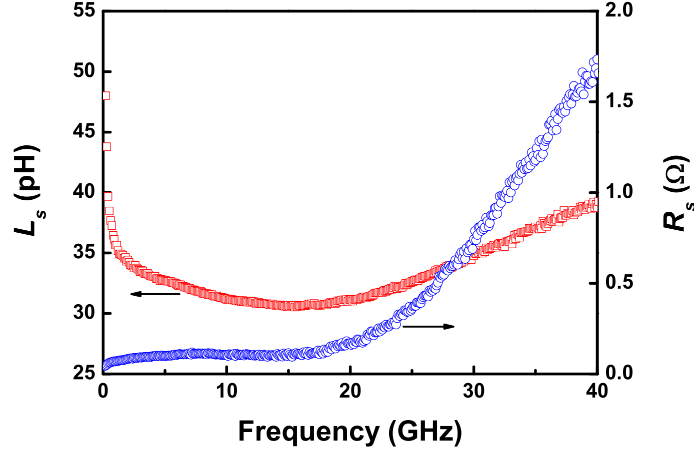


Figure 2.15: Extracted R_s and L_s of the source ground legs in the "short".

de-embedding with the assistance of noise correlation matrices [35]. Taking the "thru-short" method as an example in the noise parameter de-embedding for the device, the procedure is summarized as below: The de-embedding procedure is summarized as follows:

1. Measure the S-parameters $\left[S^{dev}\right]$, $\left[S^{thru}\right]$, and $\left[S^{short}\right]$ of the device test-structure, "thru", and "short", respectively, and the noise parameters $NF_{\min}^{DUT}$, Y_{opt}^{DUT}, and R_n^{DUT} of the DUT;

2. Solve Y_1 and Z_2 from the Y-parameters of the "thru" converted from $\left[S^{DUT}\right]$, $\left[S^{thru}\right]$ as: $Y_1 = Y_{11}^{thru} + Y_{12}^{thru} = Y_{22}^{thru} + Y_{21}^{thru}$, and $Z_2 = -(1/Y_{12}^{thru})/2 = -(1/Y_{21}^{thru})/2$;

3. Solve Z_3 from the cascaded network of the "short" from $\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & Z_2 \\ Y_1 & Y_1 Z_2 \end{bmatrix}^{-1} \left[A^{short}\right] \begin{bmatrix} Y_1 Z_2 & Z_2 \\ Y_1 & 1 \end{bmatrix}^{-1}$, where $\left[A^{short}\right]$ is the ABCD-matrix converted from $\left[S^{short}\right]$, and Z_3 is obtained as $1/C$;

4. Compute the noise correlation chain matrix $\left[C_A^{DUT}\right]$ and convert it to the

noise correlation admittance matrix $\left[C_Y^{DUT}\right]$;

5. Calculate the noise correlation matrix for Y_1, Z_2 and Z_3 elements: $[C_Y^{Y_1}] = 2kTRe\begin{bmatrix} Y_1 & 0 \\ 0 & Y_1 \end{bmatrix}$, and $[C_Z^{Z_{2,3}}] = 2kTRe\begin{bmatrix} Z_2 + Z_3 & Z_3 \\ Z_3 & Z_2 + Z_3 \end{bmatrix}$;

6. Subtract the correlation matrix of Y_1 as $[C_Y^{de_Y_1}] = [C_Y^{DUT}] - [C_Y^{Y_1}]$, and convert it to $[C_Z^{de_Y_1}]$;

7. Subtract the correlation matrix of Z_2 and Z_3: $[C_Z^{FET}] = [C_Z^{de_Y_1}] - [C_Z^{Z_{2,3}}]$;

8. Convert $[C_Z^{FET}]$ to $[C_A^{FET}]$ and compute the de-embedded noise parameters: $NF_{\min}^{FET}$, Y_{opt}^{FET}, and R_n^{FET} of the MOSFET.

The same test structure is used as in Case II for noise de-embedding. The noise parameters were measured from 2 GHz to 18 GHz by Agilent 8363B PNA and Modified Focus Microwave WinNoise system. The tested FET was biased at $V_{ds} =$ 1.8 V and $V_{gs} = 0.7$ V. Fig. 2.16 shows the noise parameters before de-embedding and after de-embedding using four methods: “open-only”, “thru-only”, “open-short”, and “thru-short”. As shown in Fig. 2.16(a), over the frequency range from 2 GHz to 18 GHz, the de-embedded noise figure from the ”open-only” method is higher than that from the other three. This extra portion is mainly due to the series parasitics of the input/output interconnection which are not considered in the “open” structure. In contrast, the “thru-only”, “open-short”, and “thru-short” methods generate similar noise figures at frequencies from 2 GHz to 12 GHz. This further indicates that these three methods are reliable for removing both the series and shunt parasitics. At frequencies higher than 12 GHz, it can be observed that both the “open-short” and the “thru-short” methods lead to close noise figures whereas the “thru-only” method gives smaller values. The deviation is attributed to the impedance of the source ground legs which are neglected in

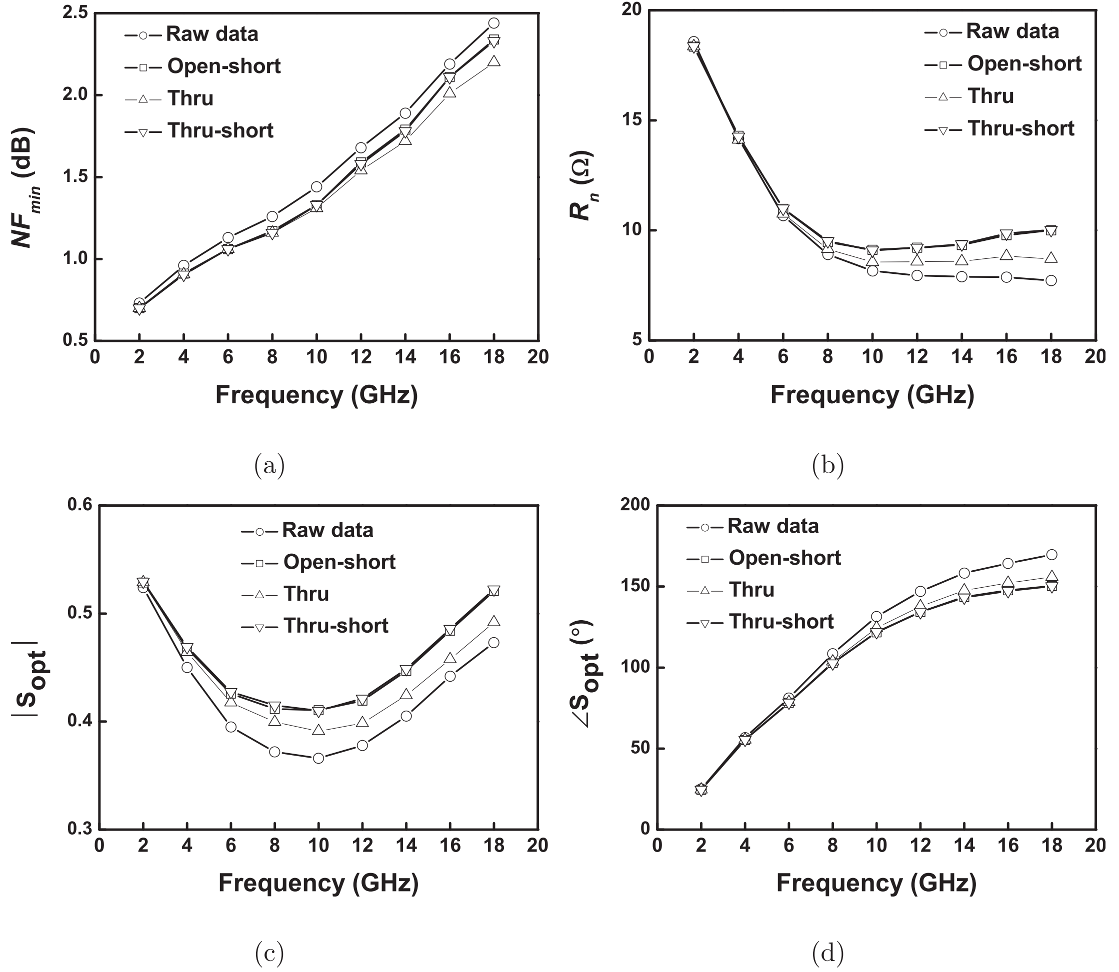


Figure 2.16: Measured and de-embedded noise-parameters for a 0.18-μm MOSFET with a total width of 80 μm biased at V_{ds} = 1.8 V and V_{gs} = 0.7 V. (a) Minimum noise figure, (b) noise resistance, (c) magnitude of optimized source reflection coefficient, and (d) phase of optimized source reflection coefficient.

the "thru-only" method. In principle, the source ground legs provide a negative feedback to the MOSFET. The output-referred noise will be reduced due to this negative feedback. Therefore, the effect of the source ground legs should be taken into account at higher frequencies, since the inductive component of Z_3 increases with frequency.

2.6 Conclusions and Recommendations

Microwave on-wafer measurements are important for developing device and component models. After calibration and measurements, de-embedding is a crucial step for obtaining the intrinsic behavior of the DUTs by removing the parasitics of the contact pads and interconnects that are required for accessing the DUTs in the test-structures. A variety of de-embedding methods are compared.

It has been found that a "thru" standard is sufficient for de-embedding the passive two-port devices accurately up to tens of GHz. A modified model of the "thru" standard accounting for the shunt parasitics of the interconnects is exploited to improve the conventional "thru" method. For reasons of accuracy, simplicity, and wafer-area efficiency, this method has been adopted for experimental characterization of the two-port passive components and circuits in this thesis.

A "thru-short" method proposed as an alternative to the widely used "open-short" method is utilized to de-embed the transistors with source connected to ground. It allows the extraction of the effective resistance and inductance of the source ground legs. Due to the skin effect and inductive effect, the source ground legs which provide a negative feedback to the transistors become more significant as frequency increases. Experimental evidence of the influence of these effects on both the S-parameters and noise parameters of the transistors is provided.

CHAPTER 3

Microwave Noise Characterization of MOSFETs

3.1 Introduction

Continuous downscaling of CMOS technologies generally pushes the MOSFET cut-off frequency f_T, which increases linearly with the inverse of the gate length [1]. The minimum noise figure $NF_{\min}$ as another important figure-of-merit of MOSFETs, however, has a more complex scaling trend as the technology advances. Noise in a MOSFET is caused by various noise mechanisms, mainly including flicker noise, generation-recombination noise, thermal noise, and shot noise. They follow different scaling rules, and have different frequency- and bias-dependencies. Additionally, the extrinsic resistive parasitics, such as in the poly-silicon gate, source and drain doping regions, contribute thermal noise to the overall $NF_{\min}$. All of these factors have to be considered in the characterization of the overall noise behavior of MOSFETs.

The noise issue becomes more critical in low voltage low power applications, such as wireless sensor networks, medical instruments, and portable devices [36], [37]. There has been growing interest to utilize the MOSFETs in weak to moderate inversion regions for such applications [38].

In contrast to the case of strong inversion region, the noise behavior of MOSFETs biased in weak and moderate regions has not yet been thoroughly studied [13], [12]. Experimental results bridging these gaps are thus important for

designers. In this chapter, microwave noise parameters of 65-nm n-MOSFETs biased in weak to moderate inversion regions are measured and characterized. The MOSFETs have scaled gate lengths ranging from 60 nm to 240 nm and the same gate width of 160 μm. The scaling behavior of the noise figure with the gate length is explained through the analysis of individual noise sources extracted based on a small-signal equivalent circuit approach. A quantification of the respective noise contributions of the noise sources is demonstrated.

3.2 Methodology

In this work, the noise modeling of the MOSFETs employs an equivalent circuit approach based on measurements. First, a noise model needs to be constructed based on physical mechanisms in a MOSFET at microwave frequencies. Most of today's MOSFETs use multifinger structures by repeating a unit gate finger. A typical cross-sectional view of a gate finger in a MOSFET is sketched in Fig. 3.1. Some of the equivalent circuit elements are also shown.

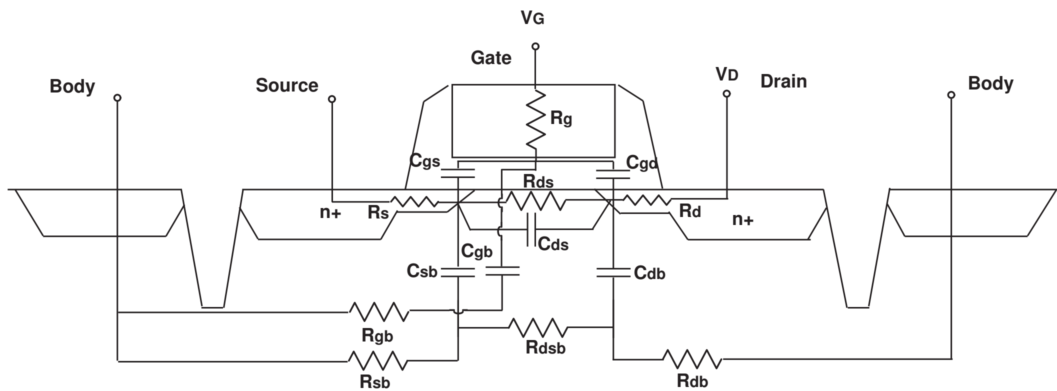


Figure 3.1: Cross-sectional view of a gate finger in a MOSFET with equivalent circuit elements.

In many applications, the source and body are tied together and connected to ground. Such a configuration is adopted in this work. A compact model to

characterize the RF and noise performance of the MOSFETs is employed here and shown in Fig. 3.2.

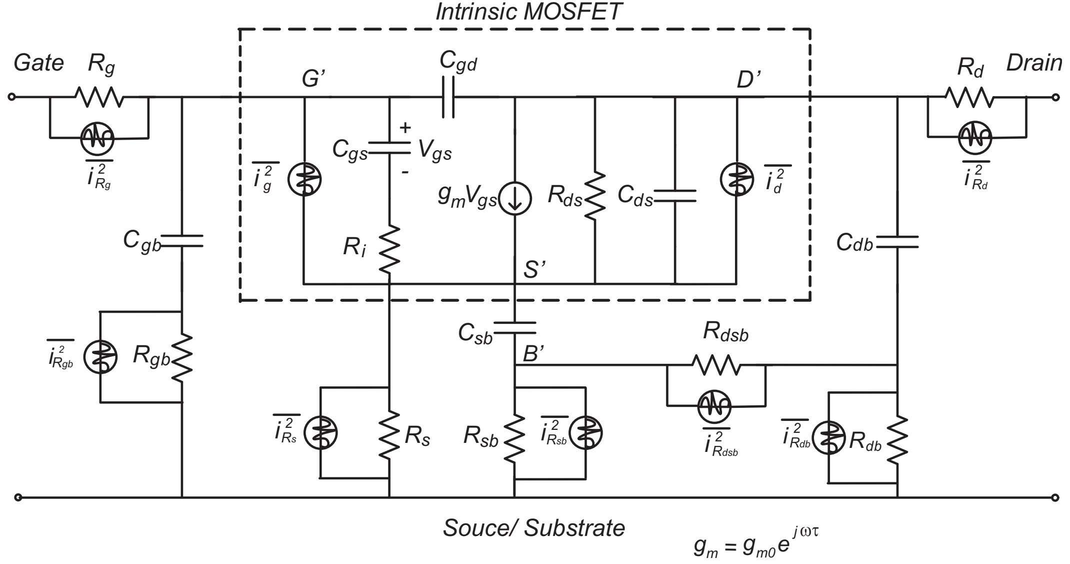


Figure 3.2: MOSFET Microwave noise model.

The boxed region represents the intrinsic part of the MOSFET, containing the elements within the inversion layer, the depletion layer, and the oxide and the gate plate between source and drain [39]. C_{gs}, C_{gd} are the intrinsic capacitances between gate and source, and gate and drain respectively. C_{ds} is the drain to source capacitance. R_{ch} is the channel conductance. When operating at microwave frequencies, the non-quasi static (NQS) effect must be taken into account. In the compact model, R_i is included in series with C_{gs}. Due to the RC delay at the gate, g_m is the gate transconductance is modified at higher frequencies as:

$$g_m = g_{m0}e^{-j\omega\tau}, \tag{3.1}$$

where τ is the transconductance delay related to R_i and the total gate capacitance $C_{gg} \approx C_{gs} \| C_{gd} \| C_{gb}$. Two noise currents $\overline{i_d^2}$ and $\overline{i_g^2}$ with a correlation coefficient C

are considered in the intrinsic MOSFET.

The extrinsic parasitic components outside the boxed region can strongly influence the RF behavior and noise behavior of the MOSFETs. R_g models the resistance of the polysilicon gate, and R_d and R_s are the resistances at drain and source terminals respectively. The substrate parasitics due to the coupling from drain to source and body terminals through the substrate are accounted for by the junction capacitances C_{sb}, C_{db}, and a π-network with three resistors R_{sb}, R_{dsb}, and R_{db} [40]. The resistances contribute thermal noise, represented by the associated noise currents in parallel with the components as shown in Fig. 3.2. The current noise of a resistor R is $4kTR\Delta f$ [41]. These extrinsic noise sources are all assumed uncorrelated.

The methodology follows these steps:

1. Measure the S-parameters and noise parameters of the MOSFET (DUT);

2. Measure the S-parameters of the on-wafer standards, such as "open", "short", and "thru";

3. De-embed both the S-parameters and noise parameters of the DUT as described in chapter 2;

4. Extract the small-signal equivalent circuit of the MOSFET as shown in Fig. 3.2 based on the de-embedded S-parameters;

5. Remove the extrinsic parasitics, which contribute thermal noise, from the de-embedded noise parameters step by step from outside to inside of the circuit. Quantify the contribution of the respective noise sources in the corresponding steps;

6. Extract the intrinsic noise sources based on the noise parameter set for the intrinsic part;

7. Analyze the noise properties of the intrinsic noise sources.

The measurement and de-embedding in steps 1 to 3 were covered in chapter 2. This chapter will focuse on steps 4 to 7 in the following sections. At each stage, important results will be shown and discussed accordingly.

3.3 Small Signal Parameter Extraction

It should be noted that, using this measurement-based modeling methodology, the obtained intrinsic noise sources are sensitive to the removal of the extrinsic components. Thus, a reliable extraction of the small signal parameters must be performed first. While there is no way to uniquely determine the component values in the model shown in Fig. 3.2, in this work, strategies such as averaging the bias-independent parameters over multiple bias conditions, and local parameter optimization are used to improve the accuracy and reliability.

An overview of the whole extraction flow is given in Fig. 3.3. Each MOSFET is measured under eight bias conditions. First of all, initial values for all the components are found through direction extraction, curve fitting or physical assumption under every bias condition. We consider the directly extracted parameters, i.e., mainly the intrinsic parameters, are the most reliable. While keeping them fixed, the remaining parameters are optimized around the initial values, which is called a local optimization. After that, the gate resistance R_g and drain resistance R_d, which are bias-independent, are averaged for each MOSFET among the values obtained for different bias conditions. This could further reduce the errors resulting from measurements. In the last step, the averaged R_g and R_d as well as the intrinsic parameters are kept fixed, and the remaining parameters are optimized again for each bias condition.

In the following subsections, the extraction strategies will be explained in detail. At the end of this section, experimental results will be shown, and the verification

of the small signal modeling will be demonstrated.

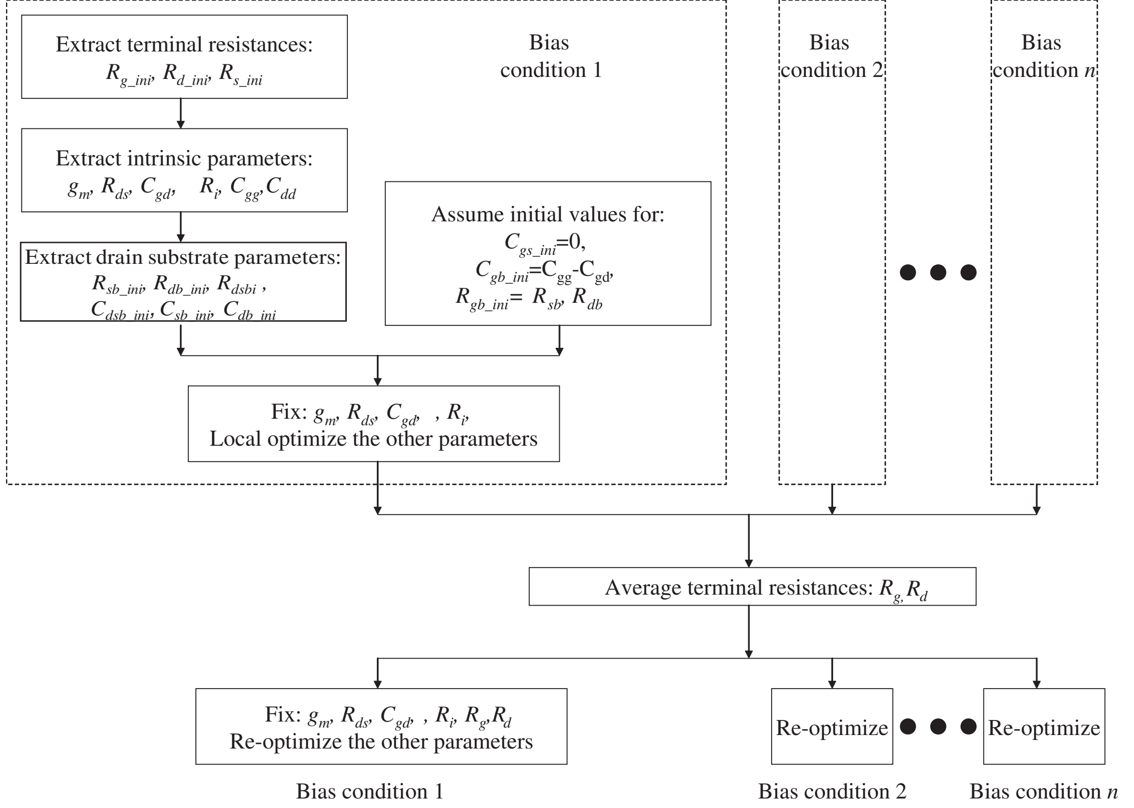


Figure 3.3: Extraction flow for the MOSFET small signal equivalent circuit shown in Figure 3.2.

3.3.1 Terminal Resistances

The terminal resistances R_g, R_d, and R_s influence the DC, RF small-signal, and noise behavior of a MOSFET, among which R_g is the most important one. Since R_g is almost bias-independent, one of the methods is to measure the MOSFETs with zero drain bias voltage so that $g_m = 0$, and the intrinsic circuit is greatly simplified [42]. In this work, the extraction uses a combination of curve fitting and averaging over different bias conditions to ensure accuracy.

R_d and R_s are the diffusion resistances, and both are slightly dependent on bias. R_d is less critical than R_s since it is in series with a very large intrinsic

output resistance R_{ds}, and the output impedance is mostly affected by the latter. Thus, R_d is also assumed bias-independent, and can be averaged among different bias conditions.

The extrinsic parameters are estimated from Z-parameters based on the following equations [43]:

$$\mathrm{Re}\left(Z_{11} - Z_{12}\right) = R_g + \frac{A_g}{\omega^2 + B} \tag{3.2}$$

$$\mathrm{Re}\left(Z_{22} - Z_{12}\right) = R_d + \frac{A_d}{\omega^2 + B} \tag{3.3}$$

$$\mathrm{Re}\left(Z_{12}\right) = R_s + \frac{A_s}{\omega^2 + B} \tag{3.4}$$

where A_g, A_d, A_s, and B are constant determined by the frequency-independent intrinsic network approximated as follows [42].

$$A_g = \frac{C_{ds}\left[g_m C_{gd} + g_{ds}\left(C_{gs} + C_{gd}\right)\right]}{\left[C_{gs}C_{ds} + C_{gs}C_{gd} + C_{gd}C_{ds}\right]^2} - \frac{g_{ds}}{C_{gs}C_{ds} + C_{gs}C_{gd} + C_{gd}C_{ds}} \tag{3.5a}$$

$$A_d = \frac{C_{gs}\left[g_m C_{gd} + g_{ds}\left(C_{gs} + C_{gd}\right)\right]}{\left[C_{gs}C_{ds} + C_{gs}C_{gd} + C_{gd}C_{ds}\right]^2} \tag{3.5b}$$

$$A_s = \frac{C_{gd}\left[g_m C_{gd} + g_{ds}\left(C_{gs} + C_{gd}\right)\right]}{\left[C_{gs}C_{ds} + C_{gs}C_{gd} + C_{gd}C_{ds}\right]^2} \tag{3.5c}$$

$$B = \left[\frac{g_m C_{gd} + g_{ds}\left(C_{gs} + C_{gd}\right)}{C_{gs}C_{ds} + C_{gs}C_{gd} + C_{gd}C_{ds}}\right]^2 \tag{3.5d}$$

In our case, since there is lack of measurement data at sufficiently high frequencies to obtain the limiting values, a curve fitting technique is used over the entire available frequency range in this work. It should be noted that the initial values assumed for A_s, A_d, A_g, and B must be within a reasonable range, and estimations based on the formulas in Eq. (4.1) can help.

3.3.2 Intrinsic Parameters

The intrinsic parameters are estimated at the low frequencies, where the gate-to-bulk and drain-to-bulk substrate networks are assumed open-circuited as shown in Fig. 3.4.

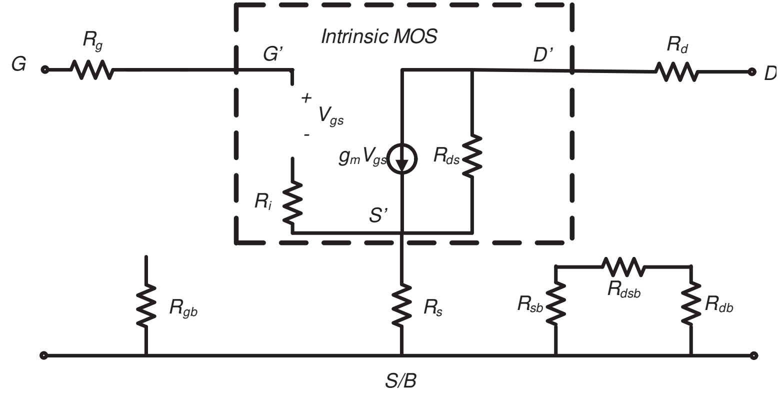


Figure 3.4: MOSFET small signal equivalent model at DC or low frequencies.

The terminal resistances resistances of R_g, R_d and R_s are removed from the Z-parameters. To facilitate the extraction, a new π-circuit mainly containing the intrinsic part is constructed in Fig. 3.5. In this circuit, the capacitances C_{gg} and C_{dd} approximate the total gate and drain capacitances respectively: $C_{gg} \approx C_{gs} + C_{gd} + C_{gb}$, and $C_{dd} \approx C_{ds} + C_{db}$ [44].

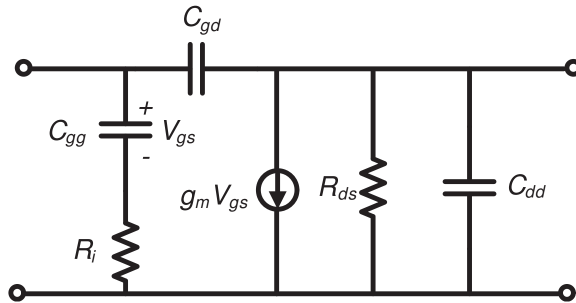


Figure 3.5: Small signal equivalent model of an intrinsic MOSFET.

To analyze this π-circuit, it is convenient to use the Y-parameters converted from the Z-parameters without R_g, R_d and R_s. The Y-parameters of the circuit

are expressed as follow [42]:

$$Y_{11}^{\text{int}} = \frac{\omega^2 C_{gs}^2 R_i}{1 + (\omega C_{gs} R_i)^2} + j\left[\frac{\omega C_{gs}}{1 + (\omega C_{gs} R_i)^2} + \omega C_{gd}\right] \tag{3.6a}$$

$$Y_{12}^{\text{int}} = -j\omega C_{gd} \tag{3.6b}$$

$$Y_{21}^{\text{int}} = \frac{g_{m0} e^{-j\omega\tau}}{1 + j\omega C_{gs} R_{gsi}} - j\omega C_{gd} \tag{3.6c}$$

$$Y_{22}^{\text{int}} = \frac{1}{R_{ds}} + j\omega\left(C_{gd} + C_{ds}\right) \tag{3.6d}$$

For a typical low-noise device, the term $(\omega C_{gs} R_i)^2$ is on the order of 0.01 around 10 GHz. It allows us to assume $(\omega C_{gs} R_i)^2 \ll 1$ and the above expressions are simplified to:

$$Y_{11}^{\text{int}} = \omega^2 C_{gs}^2 R_i + j\omega\left(C_{gs} + C_{gd}\right) \tag{3.7a}$$

$$Y_{12}^{\text{int}} = -j\omega C_{gd} \tag{3.7b}$$

$$Y_{21}^{\text{int}} = g_{m0} - j\omega\left[g_{m0}\left(\tau + C_{gs} R_i\right) + C_{gd}\right] \tag{3.7c}$$

$$Y_{22}^{\text{int}} = \frac{1}{R_{ds}} + j\omega\left(C_{gd} + C_{ds}\right). \tag{3.7d}$$

Therefore, the following elements can be directly solved from the above equations at the lower frequencies:

$$g_{m0} = \operatorname{Re}\left(Y_{21}\right)\Big|_{\omega\downarrow 0} \tag{3.8}$$

$$R_{ds} = 1/\operatorname{Re}\left(Y_{22}\right)\Big|_{\omega\downarrow 0} \tag{3.9}$$

$$C_{gd} = -\operatorname{Im}\left(Y_{12}\right)/\omega\Big|_{\omega\downarrow 0} \tag{3.10}$$

$$C_{gg} = \operatorname{Im}\left(Y_{11}\right)/\omega\Big|_{\omega\downarrow 0} \tag{3.11}$$

$$C_{dd} = \left(\operatorname{Im}\left(Y_{12}\right) + \operatorname{Im}\left(Y_{22}\right)\right)/\omega\Big|_{\omega\downarrow 0} \tag{3.12}$$

With C_{gd} extracted, the transconductance delay τ and the channel charging resistance R_i are further estimated by assuming $\tau = C_{gg} R_i$:

$$\tau = \frac{-\operatorname{Im}\left(Y_{21}\right)/\omega - C_{gd}}{2 g_{m0}} \tag{3.13}$$

$$R_i = \frac{-\text{Im}\left(Y_{21}\right)/\omega - C_{gd}}{2g_{m0}C_{gs}} \tag{3.14}$$

The gate-to-source and drain-to-source capacitances C_{gs} and C_{ds} will be determined through a local optimization to be described in section 3.3.4.

3.3.3 Drain Substrate Parameters

The extraction of the drain substrate network is based on Y'_{22} converted from the corrected Z-parameters which exclude R_d in Z_{22}:

$$Z'_{22} = Z_{22} - R_d \tag{3.15}$$

The following equation can be derived for the substrate network as illustrated in Fig. 3.6 [45]:

$$\text{Re}\left(Y_{sub}\right) = \text{Re}\left(Y'_{22}\right) - R_g(\omega C_{gd})^2 - \frac{1}{R_{ds}}, \tag{3.16a}$$

$$\text{Im}\left(Y_{sub}\right) = \text{Im}\left(Y'_{22}\right) - j\omega C_{gd}, \tag{3.16b}$$

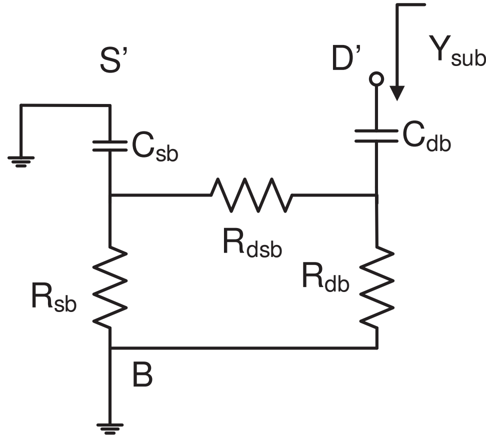


Figure 3.6: Substrate network of the small-signal equivalent circuit as shown in Figure 3.2.

Therefore, the junction capacitance and substrate resistance are obtained as

follows:

$$C_{db} = \mathrm{Im}\left(Y_{sub}\right)/\omega \tag{3.17a}$$

$$R_{sub} = \mathrm{Re}\left(Y_{sub}\right)/\mathrm{Im}(Y_{sub})^2 \tag{3.17b}$$

3.3.4 Optimization

The extrinsic parameters suffer from more uncertainty in the extraction, due to the unavailability of measurement data at sufficiently high frequencies, a gradient optimizer in ADS is used used to optimize the extrinsic parameters with most of the intrinsic parameters kept fixed as shown in Fig. 3.3 to minimize the sum of the error in the four S-parameters over the frequency range:

$$EF(S) = \frac{1}{4N_{freq}} \sum_{n=1}^{N_{freq}} \sum_{i,j=1,2} \frac{\left|S_{ij,meas}(n) - S_{ij,sim}(n)\right|^2}{\left|S_{ij,meas}(n)\right|^2} \tag{3.18}$$

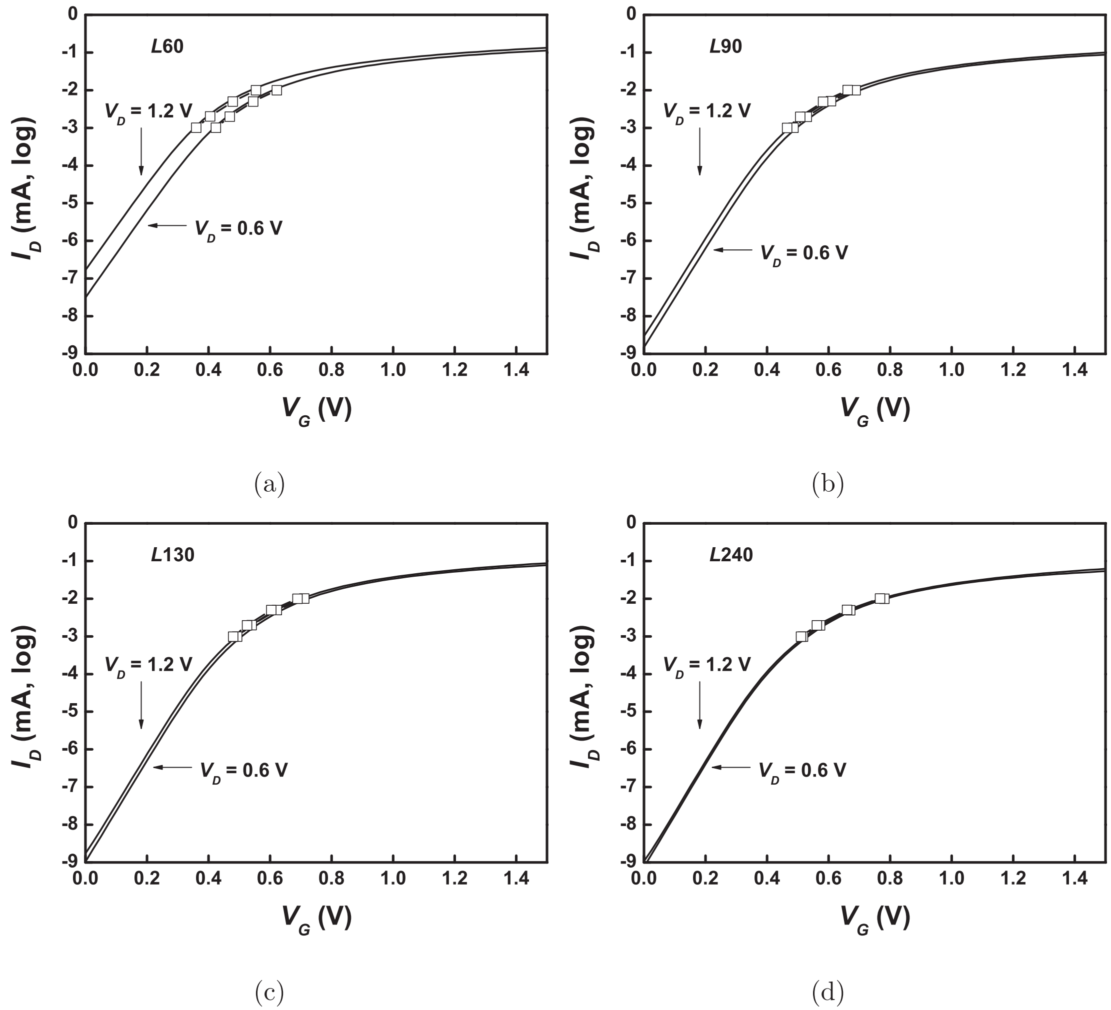
where N_{freq} is the total number of frequency points, $S_{ij,meas}(n)$ is the measured S-parameter as a function of frequency, and $S_{ij,sim}(n)$ is the simulated S-parameter of the extracted model.

If the MOSFET is measured with more than one bias condition, an average value of R_g can be obtained to improve the accuracy. With this R_g, a second round of local optimization can be run again to find the final set of parameters.

3.3.5 Experimental Results

Four MOSFETs were fabricated in a 65nm CMOS process with gate lengths of 60, 90, 130, and 240 nm, here referred to as $L60$, $L100$, $L130$, and $L240$ respectively. All the MOSFETs have 16 fingers with a unit finger width of 10 μm, which is a total width W_{tot} of 160 μm. The MOSFETs were measured as common-source structures. The MOSFETs are biased with low and high drain voltages $V_D = 0.6\ V$ and $V_D = 1.2\ V$ respectively. Gate voltages are adjusted to achieve the drain currents I_D of 1, 2, 5, and 10 mA for each MOSFET.

The bias points are shown on the DC characteristics of $\log(I_D)$ against the gate voltage V_G with two fixed V_D's for each MOSFET in Fig. 3.7. The measured bias points are mostly in the moderate inversion region, a transition region from the weak inversion region where I_D is linear with V_G to the strong inversion region where I_D exhibits an exponential behavior [46].

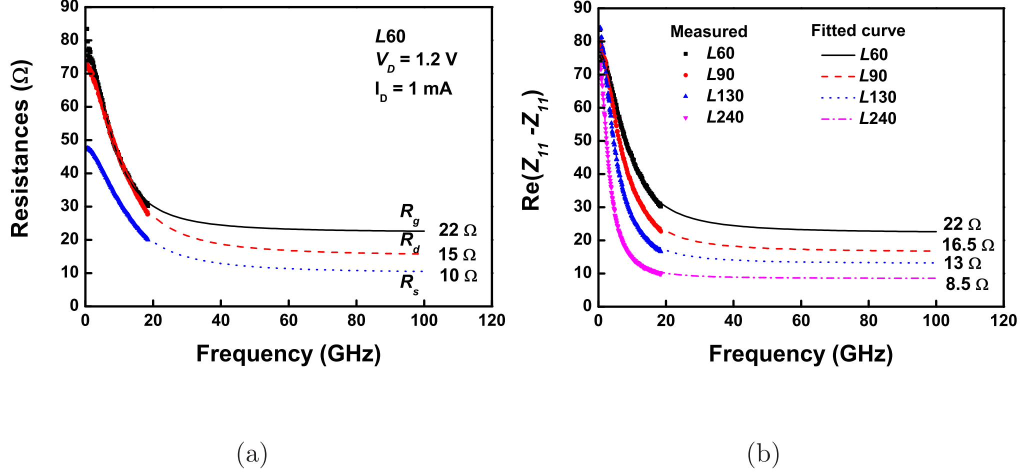


(a) (b) (c) (d)

Figure 3.7: Logarithm of I_D in mA against V_G. Symbols are measured data.

First, $L60$ is used as an example to demonstrate the extraction results. Fig. 3.8(a) shows the curves of the functions in Eq. (3.2) to (3.13) to estimate the terminal resistances of $L60$. The initial values of R_g, R_d, and R_s are obtained by curve fitting and the values are shown by extending the curves to 100 GHz. To

show the scaling of R_g with gate length, Fig. 3.8(b) shows the comparison of R_g for different gate lengths.



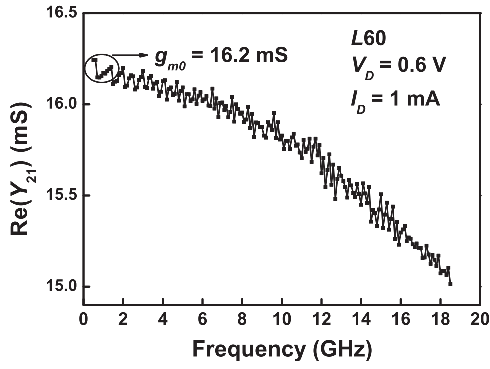
(a) (b)

Figure 3.8: Curve fitting for estimating the terminal resistances. (a) To estimate R_g, R_d, and R_s for $L60$ with $V_D = 1.2$ V and $I_D = 1$ mA. (b) To estimate R_g for the four MOSFETs. The scattered symbols are measurements up to 18.5 GHz, and the lines are the fitted curves calculated up to 100 GHz to show the values.

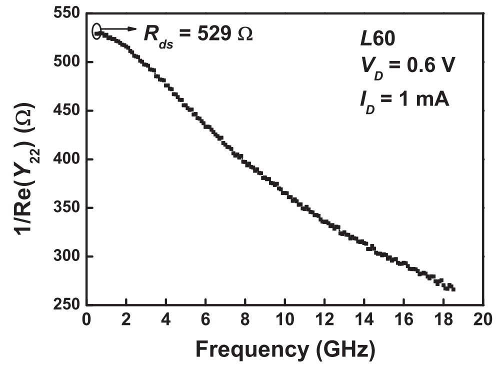
In Fig. 3.9, the functions from Eq. (3.8) to (3.11) for $L60$ with $I_D = 1$ mA and $V_D = 0.6$ V are shown for the intrinsic parameter extractions.

After the final optimization, the small-signal equivalent circuits are established for the four MOSFETs under eight bias conditions each. Table 3.1 provides the parameter values for $L60$ with $V_D = 0.6$ V and $I_D = 1$ mA. The measured and simulated S-parameters are compared in Fig. 3.10 which demonstrates good agreement.

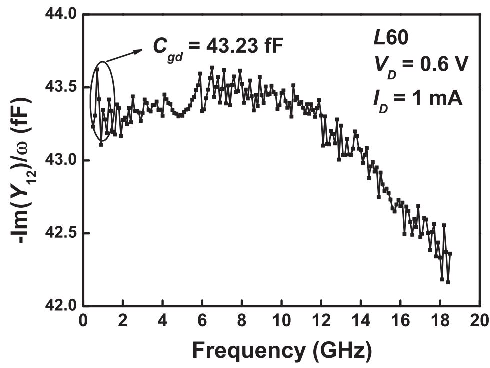
Next, some of the important parameters are summarized as a function of the scaled gate length in the following. A reduced gate length leads to an increased gate resistance reverse proportionally as plotted in Fig. 3.11(a). Fig. 3.11(b) shows the DC transconductance g_{m0} for the four MOSFETs. The dependency of g_{m0} on the gate length L is stronger under larger I_D than smaller I_D. When the gate length decreases from 240 nm to 90 nm, g_m almost increases linearly under



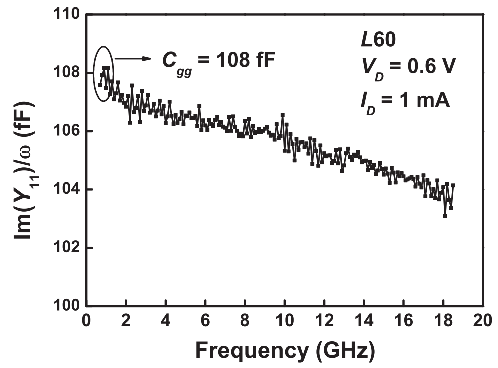
(a)



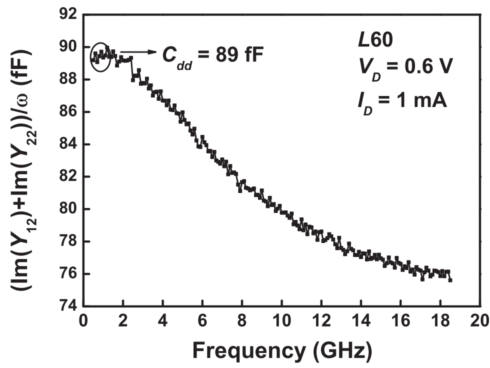
(b)



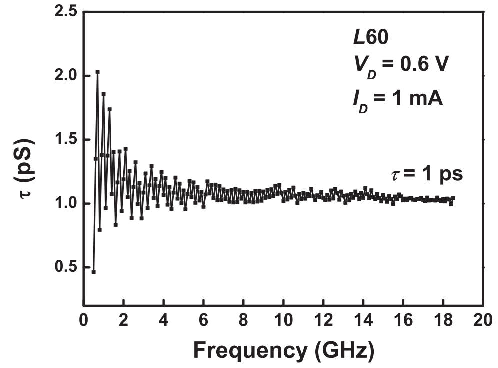
(c)



(d)



(e)



(f)

Figure 3.9: Extraction of (a) g_m, (b) R_{ds}, (c) C_{gd}, and (d) C_{gg} for $L60$ with V_D = 1.2 V and I_D = 1 mA.

Table 3.1: Model Parameters of MOSFET $L60$ with $V_D = 0.6$ V and $I_D = 1$ mA

R_g (Ω)	12.07	C_{gd} (fF)	43.23
R_d (Ω)	0.37	C_{gb} (fF)	20.87
R_s (Ω)	0. 46	C_{gs} (fF)	43.76
g_m (mS)	16.22	C_{db} (fF)	18.25
R_{ds} (Ω)	529.15	C_{ds} (fF)	62.15
R_i (Ω)	15.8	R_{gb} (Ω)	40.60
τ (ps)	1.04	R_{dsb} (Ω)	587.09
		R_{db}, R_{sb} (Ω)	45.8

all four bias conditions. Note that for the smaller drain currents of 1 mA and 2 mA, g_m of $L60$ is smaller than that of $L90$, as a result of the low gate bias (below V_T). Fig. 3.11(c) and 3.11(c) shows the gate-to-source capacitance which is linear with the gate length since the MOSFETs all have the same gate width.

Further, the cutoff frequency can be estimated from $f_T = g_m/2\pi C_{gg}$, and is shown in Fig. 3.12 as a function of L with various drain currents. The f_T is improved by the reduction of gate length due to the reduced gate capacitance. With the same drain current, a higher drain voltage leads to a higher f_T. It shows the trade-off between the power consumption and the operation speed.

3.4 Noise Source Extraction

After establishing the small signal equivalent circuit for the MOSFETs, the various noise sources can be extracted from noise parameters based on the aforementioned noise model. A general procedure of noise extraction was proposed in [47], by treating the intrinsic and extrinsic circuits as two cascaded networks. In this work, a detailed breakdown of the contribution of each individual noise source will be

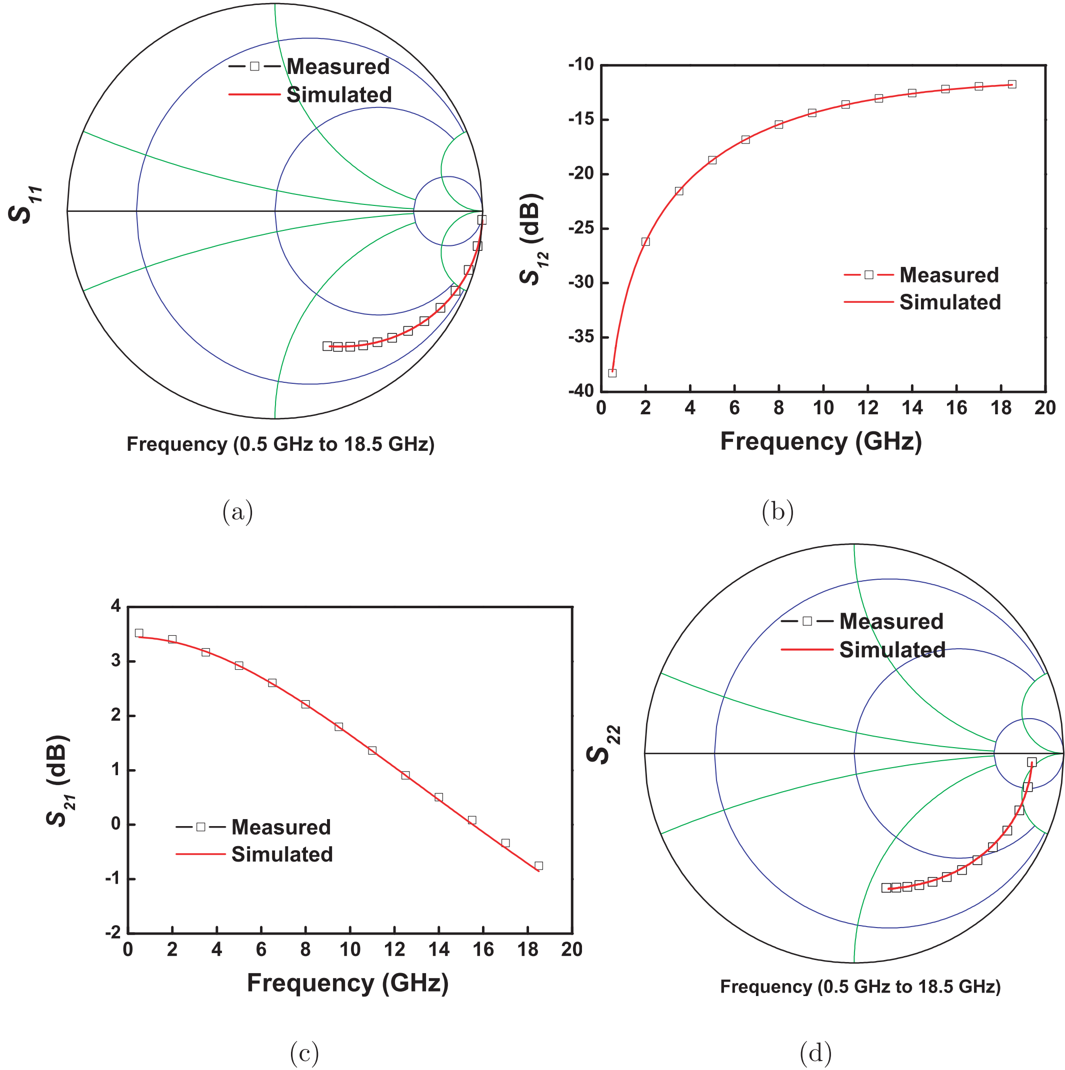


Figure 3.10: Comparison of measured and modeled S-parameters for $L60$ with V_D = 0.6 V and I_D = 1 mA.

performed. For this purpose, a step-by-step removal of the extrinsic noise sources is required. Prior to that, the complex substrate networks associated with drain and source terminals need to be separated.

3.4.1 Substrate Network Transformation

The source-to-substrate and drain-to-substrate networks of Fig. 3.2 must be transformed to facilitate the removal of extrinsic noise sources. The steps of the transformation are illustrated in Fig. 3.13. In Fig. 3.13 (a), R_s, C_{sb}, and R_{sb} form a

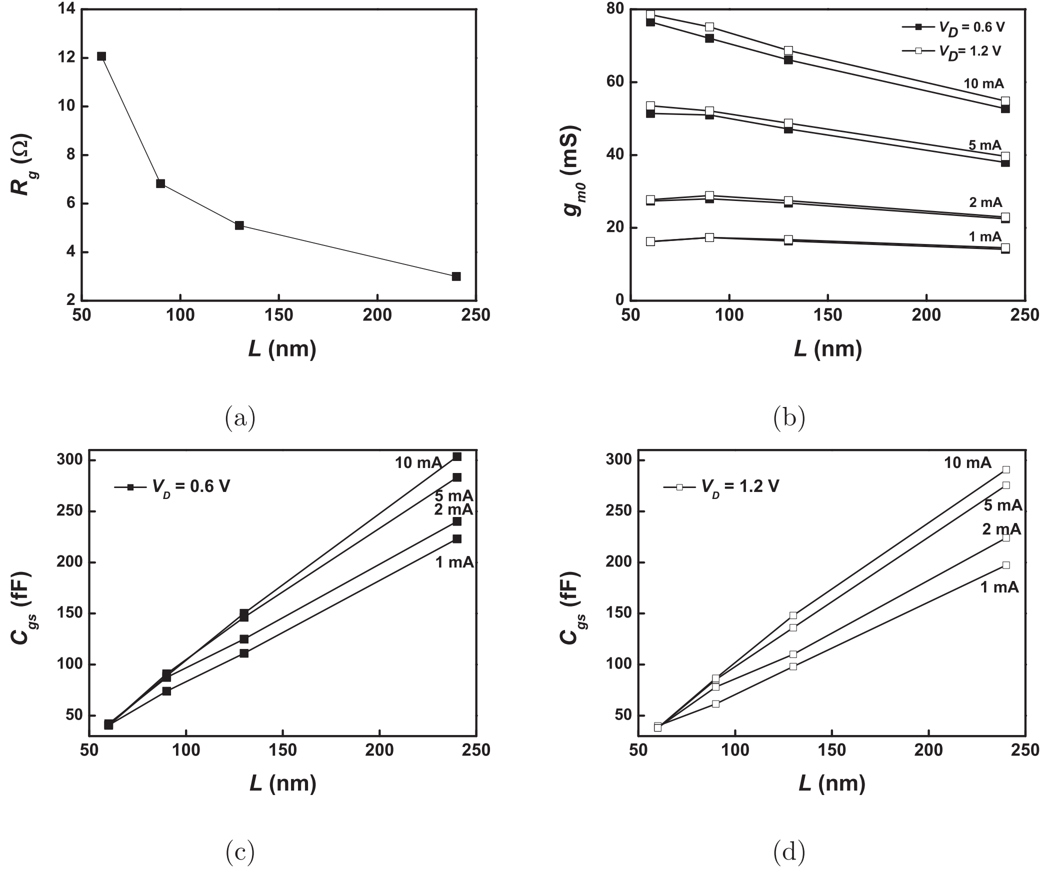


Figure 3.11: Small-signal model parameters for the MOSFETs.

Δ-network which can be converted to a Y-network consisting of R_1, R_2, and R_3 as shown in Fig. 3.13 (b). These impedance components are calculated by (3.19) to (3.21).

$$R_1 = \frac{(R_s + j\omega L_s) \times R_{sb}}{R_s + j\omega L_s + \frac{1}{j\omega C_{sb}} + R_{sb}} \tag{3.19}$$

$$R_2 = \frac{\frac{1}{j\omega C_{sb}} \times (R_s + j\omega L_s)}{R_s + j\omega L_s + \frac{1}{j\omega C_{sb}} + R_{sb}} \tag{3.20}$$

$$R_3 = \frac{R_{sb} \times \frac{1}{j\omega C_{sb}}}{R_s + j\omega L_s + \frac{1}{j\omega C_{sb}} + R_{sb}} \tag{3.21}$$

The second step from (b) to (c) is to convert the Δ-network consisting of R_1, R_{dB}, R_{dsb} and R_3 to a Y-network with the new components values computed by (3.22) to (3.24).

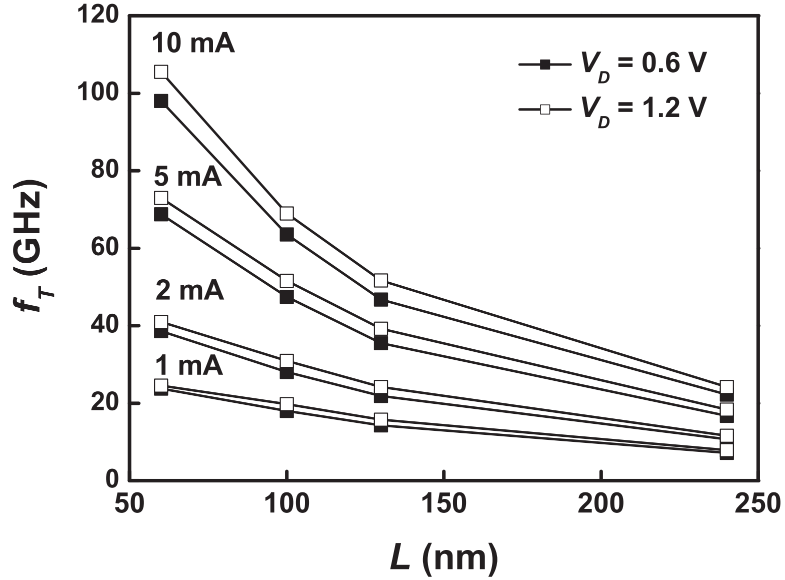


Figure 3.12: Cutoff frequency of the measured MOSFETs.

$$R_{1_2} = \frac{R_1 \times R_{db}}{R_1 + R_3 + R_{dsb} + R_{db}} \tag{3.22}$$

$$R_{2_2} = \frac{(R_3 + R_{dsb}) \times R_1}{R_1 + R_3 + R_{dsb} + R_{db}} \tag{3.23}$$

$$R_{3_2} = \frac{R_{db} \times (R_3 + R_{dsb})}{R_1 + R_3 + R_{dsb} + R_{db}} \tag{3.24}$$

Finally, the impedances associated with source, drain and substrate are given by (3.25) to (3.27).

$$Z_s = R_2 + R_{2_2} \tag{3.25}$$

$$Z_{sb} = R_{1_2} \tag{3.26}$$

$$Z_d = R_{3_2} \tag{3.27}$$

The final equivalent circuit is shown in Fig. 3.13 (e).

3.4.2 Noise Source De-embedding and Contribution Breakdown

Noise correlation matrices are used to facilitate the subtraction of the extrinsic noise sources. The noise behavior of any linear, time-invariant noisy two-port net-

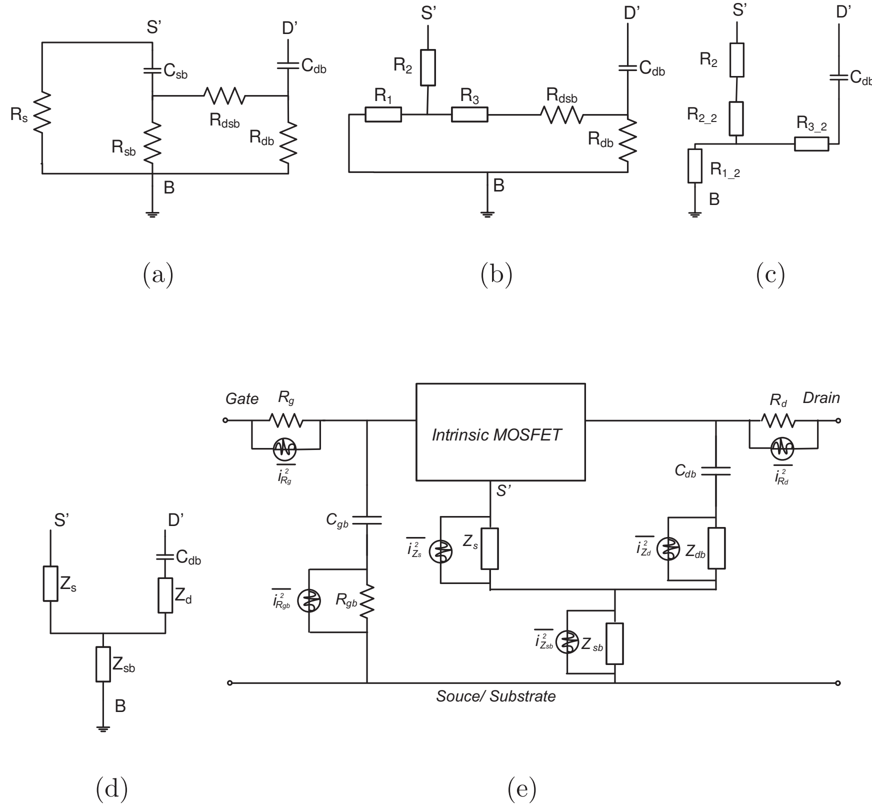


Figure 3.13: Substrate network transformation for intrinsic noise source extraction. (a)-(d) network transformantion steps. (e) final equivalent circuit.

work can be described by the noise parameters: $NF_{\min}$, R_n, and Y_{opt}, or equivalently the noise correlation chain matrix $[C_A]$. Thus, the measured noise parameters of the MOSFET can be converted to the correlation chain matrix $[C_A]_{dev}$.

After transforming the substrate network, a step by step subtraction of the extrinsic parasitics can be performed. In every step, the parasitic component is subtracted from the Y- or Z-parameters and the corresponding noise correlation matrices. If we take the excess noise factor $(F_{\min} - 1)$ as a figure of merit to weight the contributions of each noise source, the change of $(F_{\min} - 1)$ in every step represents the respective contribution of the noise source. The procedure is as follows:

1. De-embed R_g:

Convert S-parameters $[S]_{dev}$ to Z-parameters $[Z]_{dev}$, and convert $[C_A]_{dev}$ to $[C_Z]_{dev}$.

Calculate the Z-parameters and the correlation matrix of R_g and subtract from $[Z]_{dev}$ and $[C_Z]_{dev}$, resulting in $[Z]_1$ and $[C_Z]_1$.

Convert $[C_Z]_1$ to $[C_A]_1$, from which the corresponding noise parameters are solved. The minimum noise factor is $F_{\min,1}$, and the contribution of R_g (C_{R_g}) is calculated as:

$$C_{R_g} = \frac{F_{\min,dev} - F_{\min,1}}{F_{\min,dev} - 1} \times 100\% \tag{3.28}$$

Noise source de-embedding and contribution calculation of the other components is performed similarly in the following steps.

2. De-embed R_d:

   Calculate the Z-parameters and the correlation matrix of R_d and de-embed from $[Z]_1$ and $[C_Z]_1$, resulting in $[Z]_2$ and $[C_Z]_2$. Convert $[C_Z]_2$ to $[C_A]_2$, and solve for $F_{\min,2}$. The contribution of R_d in $(F_{\min,dev} - 1)$ is calculated.

3. De-embed C_{gb} and R_{gb}:

   Convert Z-parameters $[Z]_2$ to Y-parameters $[Y]_2$, and convert $[C_Z]_2$ to $[C_Y]_2$. The Y-parameters of the shunt branch R_{gb} and C_{gb} and the correlation matrix are de-embedded from $[Y]_2$ and $[C_Z]_2$, resulting in $[Y]_3$ and $[C_Y]_3$. Convert $[C_Y]_3$ to $[C_A]_3$, and solve for $F_{\min,3}$. The contribution of R_{gb} in $(F_{\min,dev} - 1)$ is calculated.

4. De-embed Z_{sb}:

   Convert Y-parameters $[Y]_3$ to Z-parameters $[Z]_3$, and convert $[C_Y]_3$ to $[C_Z]_3$. De-embed the Z-parameters and the correlation matrix of Z_{sb} from $[Z]_3$ and $[C_Z]_3$, resulting in $[Z]_4$ and $[C_Z]_4$. Convert $[C_Z]_4$ to $[C_A]_4$, and solve for $F_{\min,4}$. The contribution of Z_{sb} in $(F_{\min,dev} - 1)$ is calculated.

5. De-embed C_{db} and Z_{db}:

   Convert Z-parameters $[Z]_4$ to Y-parameters $[Y]_4$, and convert $[C_Z]_4$ to $[C_Y]_4$. De-embed the Y-parameters and the correlation matrix of the shunt branch C_{db} and Z_{db} from $[Y]_4$ and $[C_Y]_4$, resulting in $[Y]_5$ and $[C_Y]_5$. Convert $[C_Y]_5$ to $[C_A]_5$, and solve for $F_{\min,5}$. The contribution of Z_{db} in $(F_{\min,dev} - 1)$ is calculated.

6. Subtract Z_s:

   Convert Y-parameters $[Y]_5$ to Z-parameters $[Z]_5$, and convert $[C_Y]_5$ to $[C_Z]_5$. De-embed the Z-parameters and the correlation matrix of Z_s from $[Z]_5$ and $[C_Z]_5$, resulting in $[Z]_6$ and $[C_Z]_6$. Convert $[C_Z]_6$ to $[C_A]_6$, and solve for $F_{\min,6}$. The contribution of Z_s in $(F_{\min,dev} - 1)$ is calculated.

All the extrinsic parasitics have now been removed. Convert $[C_Z]_6$ to $[C_Y]_6$, and this is the correlation matrix of the intrinsic MOSFET. By representing the MSOFET intrinsic noise circuit to a noise-free network with an input and output noise current i_g and i_d as shown in Fig. 3.14, the two noise sources are directly found in the correlation matrix $[C_Y]_6$ since $[C_Y]_6 = \begin{bmatrix} \overline{i_g^2} & \overline{i_g i_d^*} \\ \overline{i_d i_g^*} & \overline{i_d^2} \end{bmatrix}$, where $\overline{i_d^2}$ and $\overline{i_g^2}$ are the gate and drain current noise respectively, and $\overline{i_g i_d^*}$ is the cross-correlation. The correlation coefficient C is defined as $C = \overline{i_g i_d^*} / \sqrt{\overline{i_d^2 i_g^2}}$.

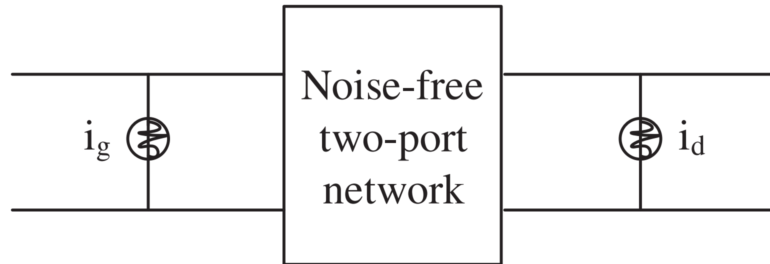


Figure 3.14: Equivalent noise circuit representation of the intrinsic MOSFET.

3.5 Noise Source Distribution

The distribution chart in Fig. 3.15 indicates the weighting of the main noise sources in $L60$ with respect to the excess noise factor ($F_{\min} - 1$) with $V_D = 0.6$ V and I_D = 1 mA. It demonstrates the increased importance of noise from the extrinsic parasitics with increased frequency, among which the gate resistance is the most significant one. Contribution from the substrate resistances is relatively minor, but also increases as frequency increases. The thermal noise contribution from the source and drain resistances are negligible since R_s and R_d are very small.

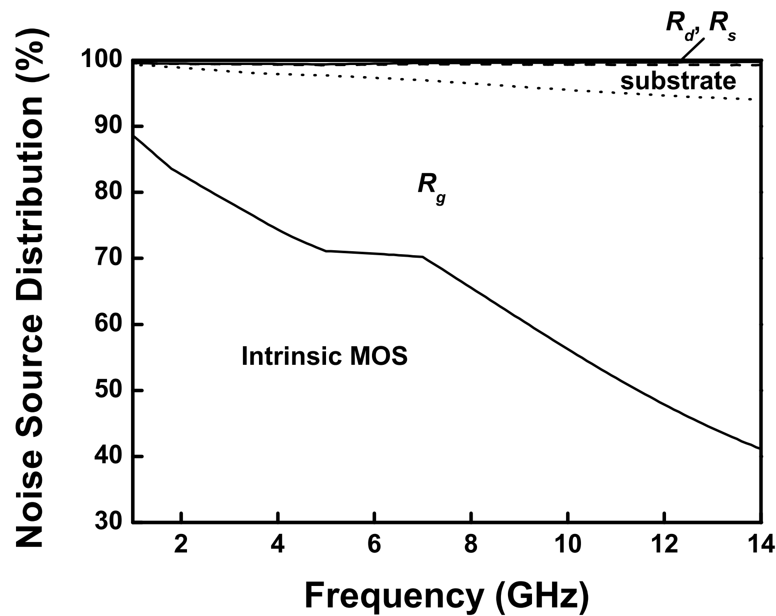


Figure 3.15: The contribution of the various noise sources in the excess noise factor ($F_{\min} - 1$) of the MOSFETs with $I_D = 0.6V$ and $I_D = 1mA$.

3.6 Intrinsic Noise Source Modeling

In this section, modeling of the intrinsic noise sources will be discussed, including drain current noise and gate current noise. The extracted data from measurements will be shown for verification.

The most important noise mechanisms in the intrinsic MOSFET include flicker noise, shot noise, and thermal noise. Since there are no correlations between different noise mechanisms, the sum of them leads to the total amount of the drain noise current and the total gate noise current respectively [48], [49].

3.6.1 Drain Current Noise

Flicker Noise

Flicker noise occurs in almost all electronic devices. It is commonly called $1/f$ noise, because its noise spectrum varies as $1/f^{\alpha}$, where the exponent α is close to unity ($\alpha = 1 \pm 0.2$) [48].

Different theories have been proposed to explain this mechanism, mainly categorized in three types: carrier number fluctuation theory (Δn) [50], mobility fluctuation theory (Δv) [51], and a unified 1/f model considering correlated carrier and mobility fluctuation [52], [49]. Although there is still controversy on the fundamentals of flicker noise, the unified model is the most modern and popular one widely employed in the commercial compact MOSFET models, such as BSIM4, MOS Model 11 [11], [53].

A general model for flicker noise is [48]:

$$\overline{i_{d,flicker}^2} = \frac{KF \cdot I_D^{AF} \Delta f}{C_{oxe} L^2 f^{EF}}, \tag{3.29}$$

where KF, AF and EF are flicker noise coefficient, flicker noise exponent and flicker noise frequency exponent respectively dependent on the device type and process conditions [12], and C_{oxe} is the per unit area gate oxide capacitance. It infers that flicker noise could get worse in smaller technology nodes, where the gate oxide thickness becomes thinner and the gate length reduces.

Thermal Noise

The thermal noise component in the drain current noise, referred to as channel thermal noise, is generated by the thermal agitation of the charge carriers (electrons in n-MOSFETs) in the channel. It is white noise. Since flicker noise decays as frequency increases, the thermal noise is the dominant noise mechanism at microwave frequencies. Modeling of channel thermal noise in MOSFETs has received much attention [45, 54]. A classical thermal noise model is given by [48]

$$\overline{i^2_{d,thermal}} = 4kTg_m\Delta f\gamma, \tag{3.30}$$

where the theoretical noise factor $\gamma = 2/3$ for long channels [48].

In the study on the channel thermal noise in the short channels, the excess thermal noise has been widely discussed, which is characterized by an increase in γ. While a value of 4 to 5 times the long channel theoretical value was reported in [55], only a small raise in γ was supported by experimental data from other groups recently [49], [56]. The excess noise was mostly attributed to the short channel effects such as channel length modulation and velocity saturation. Since it is very difficult to determine the exact noise factor for short channels theoretically due to the complexity of various short channel effects, Eq. (3.30) with $\gamma = 2/3$ is used to evaluate the channel thermal noise in this work. In section 3.7, the sensitivity of the MOSFET minimum noise figure $NF_{\min}$ on γ will be investigated.

Shot Noise

Shot noise is caused by the current flowing in the channel which is non-uniform consisting of individual electrons arriving at random times [48]. It has been shown that shot noise in MOSFETs is mainly due to the diffusion current I_{diff}, which dominates the drain current in weakly inverted channels [57]. The power spectrum density of shot noise is linear with the drain diffusion current as $\overline{i^2_{d,shot}} = 2qI_{diff}$.

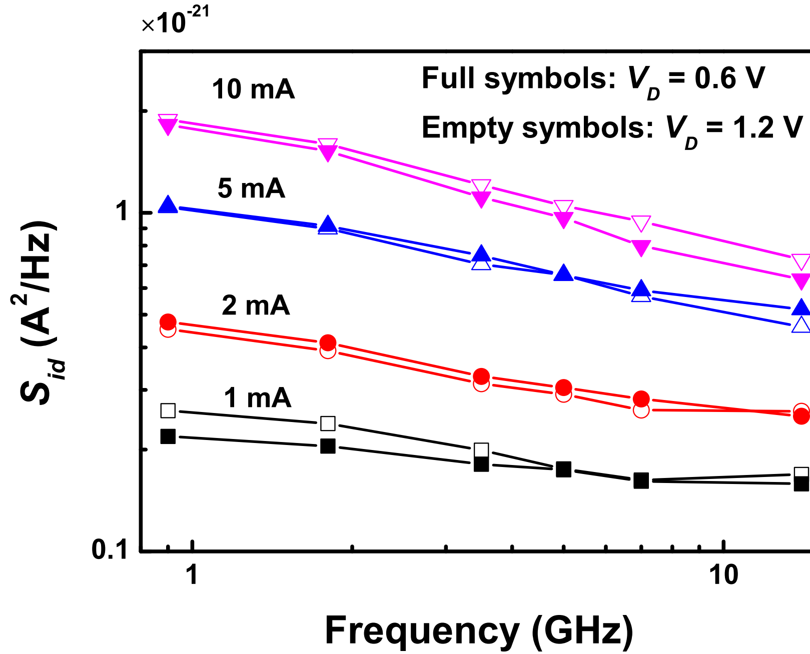


Figure 3.16: Drain noise power spectral density S_{id} for $L60$ from measurements. Full symbols are with a low drain voltage of 0.6 V, and empty symbols are with a higher voltage of 1.2 V.

Experimental Results

First we show the extracted power spectrum density (PSD) of drain current noise $S_{id} = \overline{i_d^2}/\Delta f$ for $L60$ from measurements under all bias conditions in Fig. 3.16. On a logarithmic scale, it is easy to verify that the spectrum is close to the function as $1/f$ within 10 GHz indicating the presence of flicker noise. The larger the drain current, the larger the slope, which is supported by Eq. (3.29).

Next, drain current noise at the higher frequency range is examined as a function of DC drain current. When the channel is in strong insertion, the drift current I_{drift} is the dominant component, while in weakly inverted channels the diffusion current $I_{diffusion}$ dominates. In the moderate inversion regtion, the drain current is a combination of both with a certain ratio. Diffusion current gives rise to shot noise in the channel, and drift current generally causes thermal noise [57].

Fig. 3.17 (a) to (d) shows the extracted drain noise power spectral density S_{id} at 14 GHz with $V_D = 0.6V$. Theoretical calculations of shot noise ($2qI_D$) and thermal noise ($8kTg_m/3$) are also shown for comparison. The experimental data for S_{id} of the four MOSFETs is found to be in between the shot noise and thermal noise estimations. This implies that the proportion of the two noise mechanisms in the total drain current noise. For very small currents, shot noise and thermal noise tend to converge. Since a lower gate voltage is required for shorter channels to achieve the same drain current, the ratio of the diffusion current to the total is larger. Thus, the total drain current noise is more towards shot noise. For $L240$, the total drain current noise could be almost completely modeled by thermal noise.

Fig. 3.18 shows the modeled and measured S_{id} for $L60$ with $V_D = 0.6$ V and I_D = 1 mA. Flicker noise is fitted to the lower frequncy spectrum while the thermal noise prediction is based on Eq. (3.30) with $\gamma = 2/3$.

3.6.2 Gate Current Noise

Induced Gate Noise

The induced gate noise is due to the coupling of the channel thermal noise through the gate-to-source capacitance C_{gs}. Theoretical analysis shows that the induced gate noise is [48]:

$$\overline{i^2_{g,induced}} = 4kT\frac{\omega^2 C_{gs}^2}{5g_m}\Delta f\beta \tag{3.31}$$

where $\beta = 4/3$ for long channels.

In shorter channels, it is found that β could be 3 times higher than 4/3 [49]. Note that the increase in β is more significant than in γ of the channel thermal noise as the gate length reduces. A possible reason may be due to the increased gate resistance which also impacts the induced gate noise with shorter gate lengths [49]. However, this needs further study to prove.

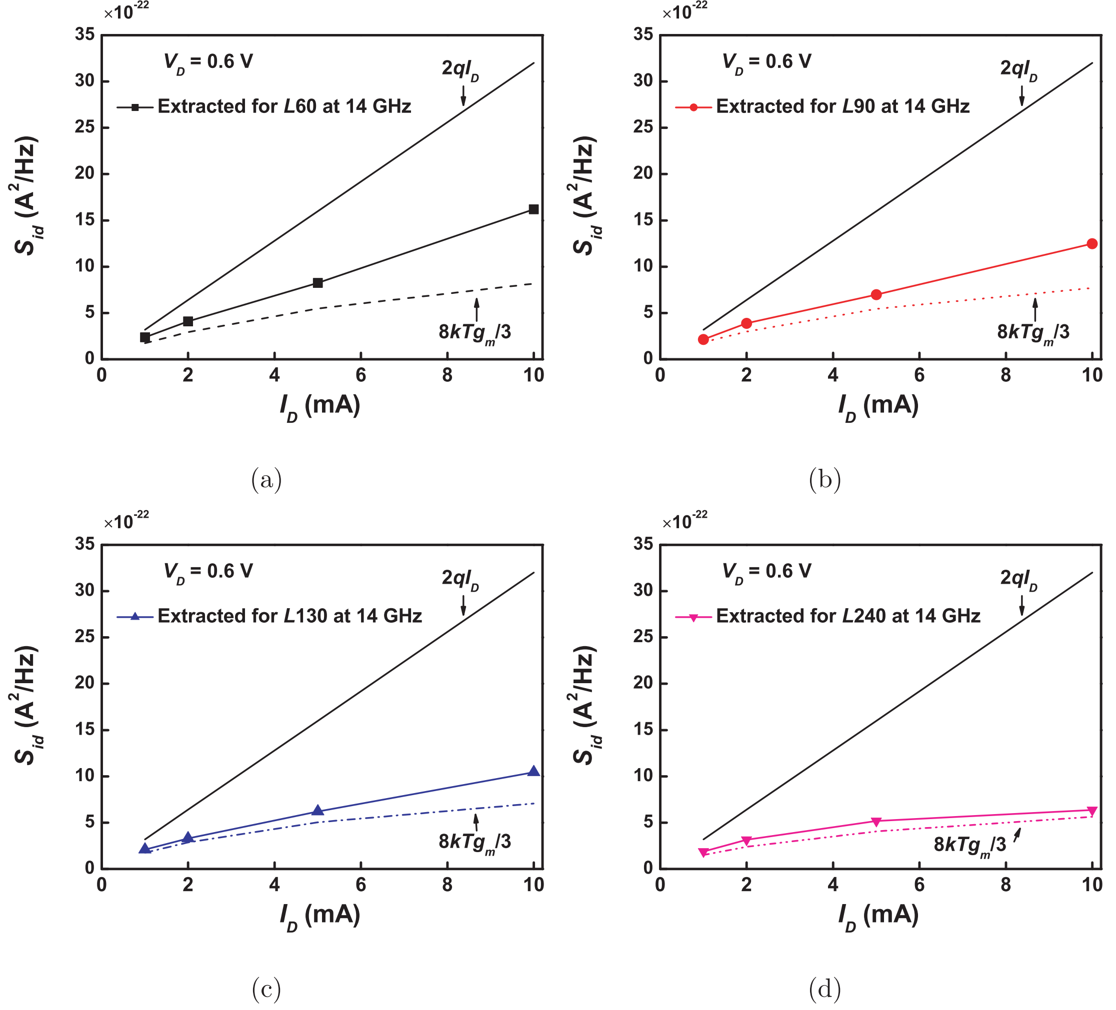


Figure 3.17: Extracted drain noise power spectral density S_{id} at 14 GHz against the DC drain current. The drain voltage is 0.6 V. Theoretical calculations of shot noise ($2qI_D$) and thermal noise ($8kTg_m/3$) are shown for comparison.

The cross-correlation power between the induced gate noise and the channel thermal noise is calculated as [48]:

$$\overline{i_g i_d^*} = \frac{2}{3} kTj\omega C_{gs} \Delta f \tag{3.32}$$

Thus, the correlation coefficient $C = \overline{i_g i_d^*} / \sqrt{\overline{i_d^2 i_g^2}}$ is purely imaginary about $j0.359$ for long channels [48].

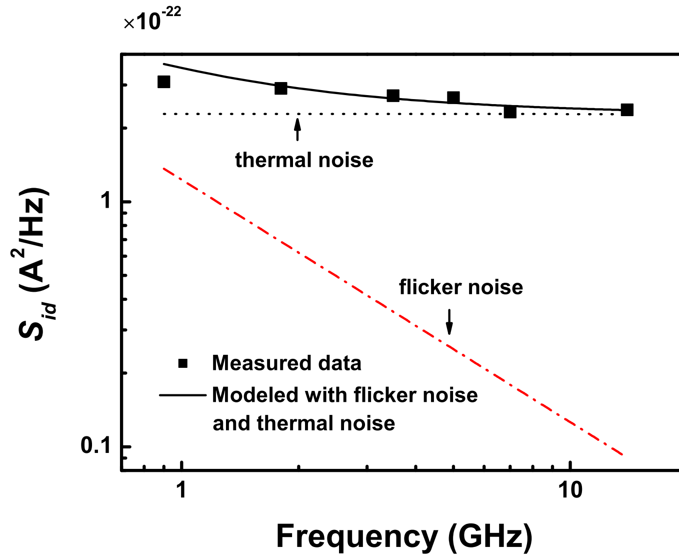


Figure 3.18: Drain noise power spectral density S_{id} of $L60$ with $V_D = 0.6$ V and $I_D = 1$ mA. Symbols are measured data. Modeled flicker noise, thermal noise, and the sum of them are also shown.

Gate Tunneling Noise

With the continuous downscaling of CMOS technologies, the gate oxide thickness is steadily reduced, which is now on the order of 2 nm in the technology node around 100 nm [1], [58]. The thin gate oxide layer exacerbates the gate quantum-mechanism direct tunneling of the carriers through the gate oxide. The gate tunneling current is one of the undesired effects in modern MOSFETs. It affects the MOSFET operation in off state and limits the applications with a high gate current. The gate tunneling current contributes to the noise performance of MOSFETs as a shot noise component [49], [59]. As a result, a white noise level $2qI_g$, where I_g is the total gate current, is added to the induced gate noise in the gate current noise spectrum.

Experimental Results

The power spectral density (PSD) of the gate current noise $S_{ig} = \overline{i_g^2}/\Delta f$ for the MOSFETs with an I_D of 1 mA is shown in Fig. 3.19. It is found that S_{ig} is dominated by the induced gate noise. The MOSFETs with longer gate lengths have a much larger S_{ig} at higher frequencies due to the larger C_{gs}. Thus, the induced gate noise has been considered a critical noise source for higher frequencies applications.

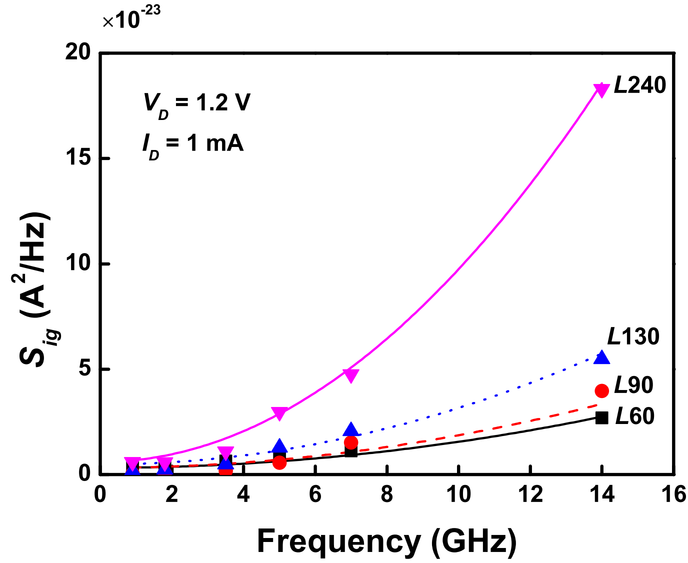


Figure 3.19: Symbols: extracted gate current noise power spectral density S_{ig} for the MOSFETs with I_D = 1 mA. Lines: modeled gate current noise taking into account the gate tunneling noise and the induced gate noise.

Long channel MOSFET noise theory predicts the correlation coefficient C to be a pure imaginary number of $0.359j$. For the short-channel MOSFETs, the accurate determination of C is limited by the measurement setup [49]. The extracted correlation coefficient C is plotted in Fig. 3.20. It shows that C generally increases with increasing gate length L and decreases with the drain current. Negative values were observed for $L60$ and also longer MOSFETs at some bias conditions.

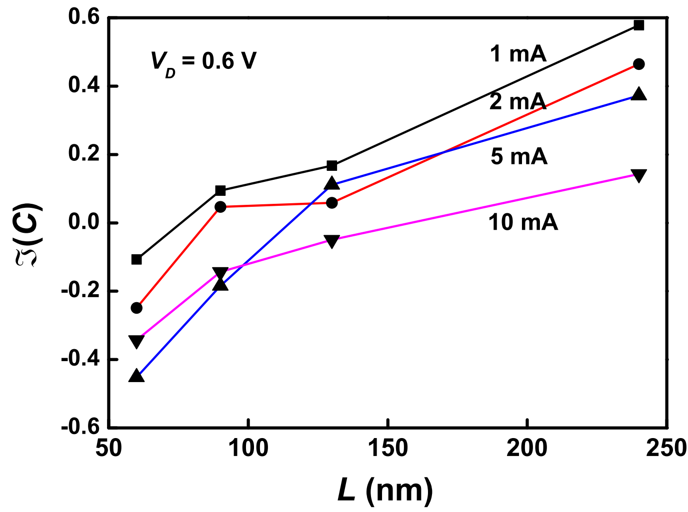


Figure 3.20: Extracted correlation coefficient for the MOSFETs with different drain currents.

3.7 Scaling of Minimum Noise Figure

It has been shown in section 3.4.2 that around 95% of the noise contribution is from the intrinsic MOSFET and the gate resistance up to 14 GHz, a simplified noise model can be used to approximate the noise performance of the MOSFETs, including only three noise sources, i.e., the intrinsic S_{id} and S_{ig} with a correlation coefficient C and R_g, as shown in Fig. 3.21.

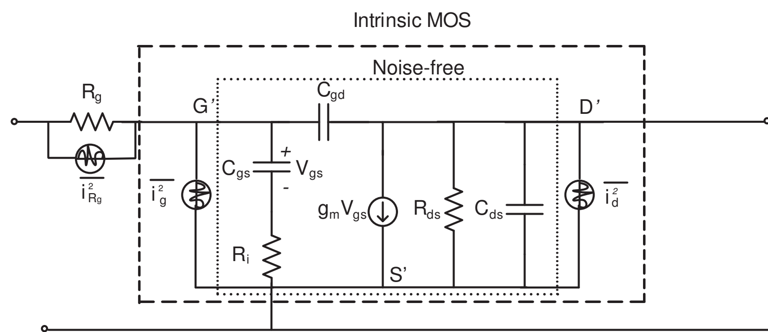


Figure 3.21: Simplified noise model for the MOSFET with three noise sources:S_{id}, S_{ig} and R_g.

3.7.1 Intrinsic Noise

First, the intrinsic noise is examined. Without incorporating R_g in the circuit shown in 3.21, the minimum noise figure can be derived as:

$$NF_{\min,int} = 1 + \frac{\sqrt{S_{id}S_{ig}}\left(\sqrt{1-C^2}\right)}{2kTg_m} \tag{3.33}$$

Suppose no new physical effects emerge as the gate length reduces, and we can assume that S_{id} remains the same for the same drain current, S_{ig} scales linearly with L^2 according to the scaling of C_{gs}, the intrinsic $NF_{\min,int}$ will decreases linearly with $1/L$ deduced from the above equation.

However, from the experimental characterization of the noise sources discussed in the previous section, three factors should be noted which deviate from the above scaling rules. The first one is flicker noise, which adds to S_{id} proportional to $1/L^2$ at lower frequencies. Further, the excess noise factors γ and β in shorter devices must be considered as the gate length scales down. Fig. 3.22 summarizes the experimental data for γ and β at different gate lengths. It can be seen that while γ does not have a large increase, β is more susceptible to the gate length.

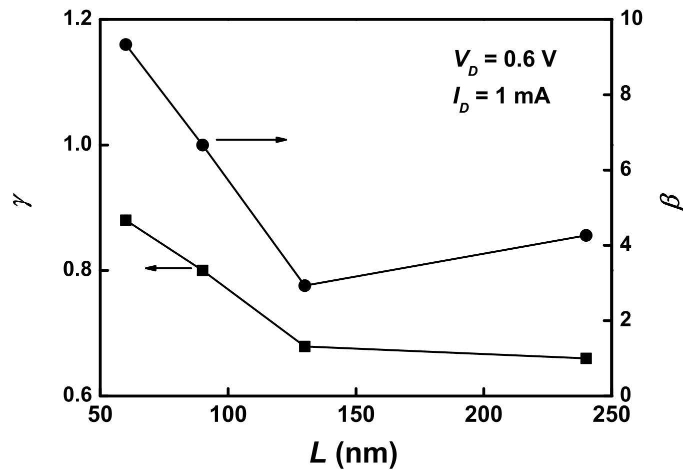
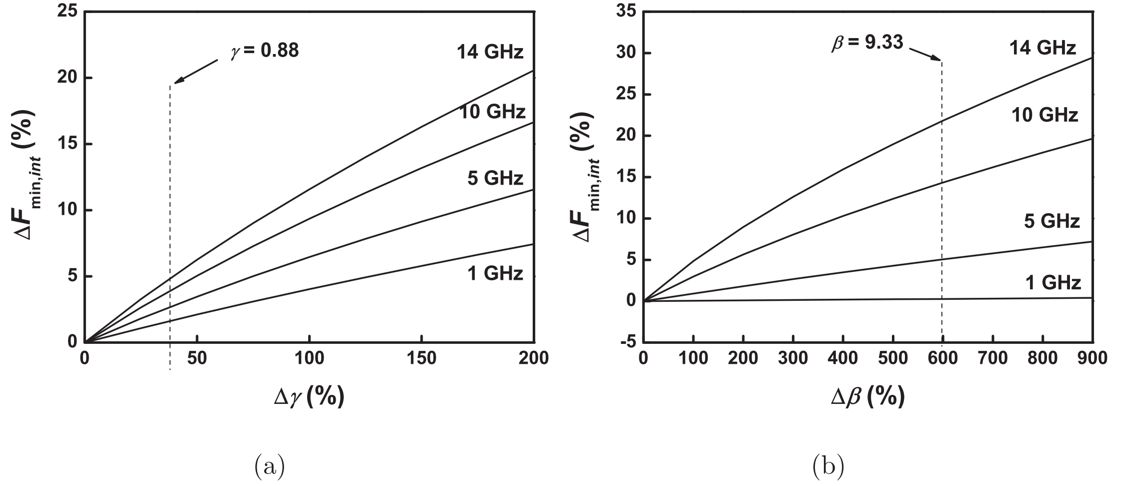


Figure 3.22: γ and β factors versus gate length with $V_D = 0.6$ V and $I_D = 1$ mA.

Here, we will examine how much the excess noise factors γ and β affect $NF_{\min,int}$. Eq. (3.33) is calculated by substituting Eq. (3.30) and (3.31) and varying γ and β respectively. A benchmark is set as $\gamma = 2/3$ and $\beta = 4/3$, and the corresponding $NF_{\min,int}$ is utilized as a reference. By increasing the γ and β, the increase in $NF_{\min,int}$ with respect to the reference is calculated for $L60$ and shown in Fig. 3.23(a) and 3.23(b) respectively. It shows that the increased γ, which leads to the excess drain thermal noise, results in an increase of $NF_{\min,int}$ by 2% to 5% in the frequency range of 1 to 14 GHz. The influence of the increase in γ on $NF_{\min,int}$ is strongly frequency-dependent. Although it remains intact below 1 GHz, $NF_{\min,int}$ is risen considerabley by 25% at 14 GHz due to the excess induced gate noise.



(a) (b)

Figure 3.23: Calculated $NF_{\min,int}$ with varying γ and β for $L60$ with $V_D = 0.6$ V and $I_D = 1$ mA.

Experimental $NF_{\min,int}$ data is obtained after de-embedding all the extrinsic noise sources as described in section 3.4.2. The data is plotted against gate length L as shown in Fig. 3.24. The decrease trend of $NF_{\min,int}$ with the downscaled gate length is changed when L reduces to 60 nm at higher frequencies. The reason is the large excess induced gate noise in the small devices, as discussed above.

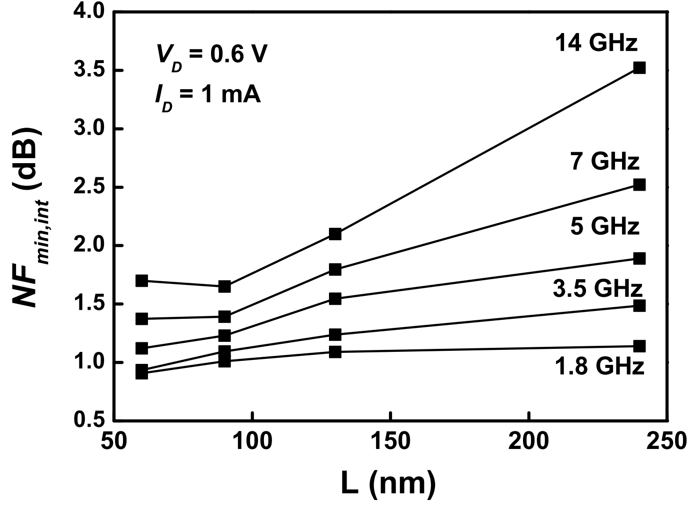


Figure 3.24: Intrinsic $NF_{\min}$ against gate length L with $V_D = 0.6$ V and $I_D = 1$ mA.

3.7.2 Extrinsic Noise

Further incorporating the contribution of R_g, $NF_{min,tot}$ of the entire MOSFET is:

$$\begin{aligned} NF_{\min,tot} &= 1 + 2\left(\frac{S_{id}R_g}{4kT}\left(\frac{\omega C_{gs}}{g_m}\right)^2 + \frac{S_{ig}R_g}{4kT}\right) \cdot \\ &+ \sqrt{\frac{S_{id}R_g(\omega C_{gs})^2}{4kT} + \frac{S_{ig}R_g}{4kT} + \frac{S_{id}S_{ig}(1-C)^2}{(4kTg_m)^2}} \end{aligned} \quad (3.34)$$

Comparing Eq. (3.34) and (3.33), two terms reflect how R_g influences $NF_{\min,tot}$: $\frac{S_{id}R_g}{4kT}\left(\frac{\omega C_{gs}}{g_m}\right)^2$ and $\frac{S_{ig}R_g}{4kT}$. It indicates that the contribution of R_g increases with frequency. As the gate length L reduces, R_g increases proportionally to $1/L$, C_{gs} increases linearly with L, and g_m is assumed to be unchanged under the same drain current, it can be found that both increase with $\gamma\omega^2 L$ and $\beta\omega^2 L$ respectively. Thus, the excess drain thermal noise and induced gate noise will further impact the total minimum noise figure $NF_{\min,tot}$ through the incorporation of R_g. This is demonstrated by the experimental data shown in Fig. 3.25. The minimum noise figure improves as the gate length reduces at lower frequencies. However, when L further reduces to 90 nm, it increases at frequencies above 5 GHz.

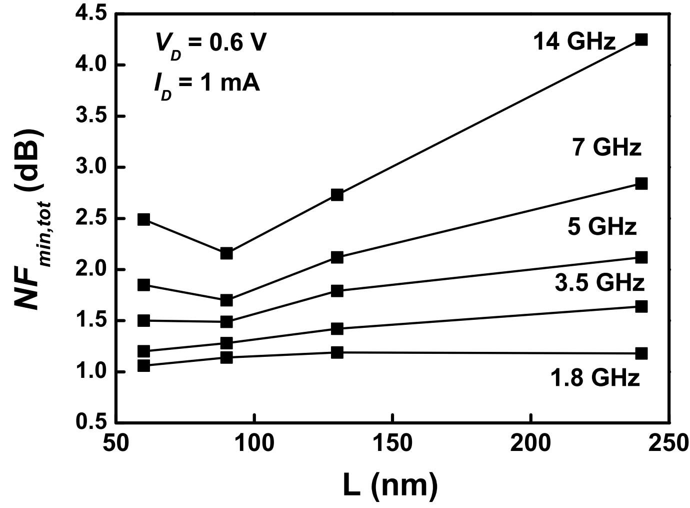


Figure 3.25: Measured $NF_{\min}$ against gate length L with $V_D = 0.6$ V and $I_D = 1$ mA.

3.8 Conclusions and Recommendations

In this chapter, the characterization of microwave noise behavior for MOSFETS with scaled gate lengths ranging from 60 to 240 nm is presented. The intrinsic and extrinsic noise sources in the MOSFETs are extracted based on a high frequency small signal equivalent circuit. The respective contribution of individual noise sources is quantified. The most dominant noise sources are in the intrinsic part and the extrinsic gate resistance. Further analysis reveals that two main factors mainly holds back the improvement of microwave noise performance of the MOSFETs as the gate length scales down, which are intrinsically the increased excess induced gate noise and extrinsically the increased gate parasitic noise. When the gate length reduces to 60 nm, the overall noise figure deteriorates especially at higher frequencies. In this case, a tradeoff between the noise performance and the cutoff frequency f_T must be made in the designs.

CHAPTER 4

Modeling of Inductors with Metal Dummy Fills

4.1 Introduction

In the development of CMOS technologies, remarkable achievements have been made in realizing downscaled MOSFETs with higher speed and lower power consumption. Along with efforts in the device process, the back-end-of-the-line (BEOL) process is also altered with a major target to reduce the RC delay of the global interconnects. For this purpose, new materials have been introduced, such as using copper instead of aluminum to reduce the ohmic resistance of the wires, and lower dielectric constant materials to reduce the per unit area capacitance [60, 61]. The use of copper requires a intermetal dielectric chemical-mechanical polishing (CMP) process step to planarize the metal layers since copper is a very soft metal mechanically [60]. However, problems such as metal dishing and erosion prone to happen in this step in blank areas which degrade the quality of the process or even cause process failure [62]. To avoid these defects, a minimum metal density is required.

The metal density is checked by adjacent “scan windows”, which can be as small as $20 \times 20\ \mu\text{m}^2$ over the whole chip to ensure a uniform density in present technologies. To meet this requirement, metal dummy fills are inserted with the on-chip circuits or components, even in small empty areas. As suggested by the manufacturers, the metal dummy fills are typically square or rectangular fill pat-

terns with a size typically between 2×2 to 4×4 μm^2. Floating dummy fills are usually favored over grounded ones since they are more flexible to place.

Although the metal dummy fills are presumably electrically inactive cells, they have considerable impact on the performance of circuits or components in the microwave regime. The increased capacitive parasitics of interconnects due to the proximity of metal dummy fills have been studied in [63] and [64]. The effect of grounded metal dummy fills under the spiral inductors has been reported in [65]. However, the placement of dummy poles does not represent a typical case. There is still a lack of good models to capture the microwave behavior of on-chip components with inserted metal dummy fills.

The aim of this chapter is to experimentally characterize the influences of floating metal dummy fills on the microwave performance of on-chip inductors, and develop a methodology for designers to update the existing models to account for the effects of dummy fills. Here we first designed and fabricated inductors with and without metal dummy fills are in a commercial 0.18-μm CMOS technology to mimic the situation in more advanced nodes. The effect of the metal dummy fills is characterized experimentally. The reasons for the deteriorated performance of the inductors due to metal dummy fills are then identified based on the equivalent circuit model. Simple but accurate methods are proposed to predict the microwave behavior of on-chip spiral inductors with metal dummy fills.

4.2 Design and Measurement of Inductor Counterparts

4.2.1 Design of Experiment

Fourteen pairs of square inductors with various layout geometries with and without metal dummy fills are designed and fabricated. Four "thru" standards are fabricated for de-embedding. Fig. 4.1 shows the whole experimental set.

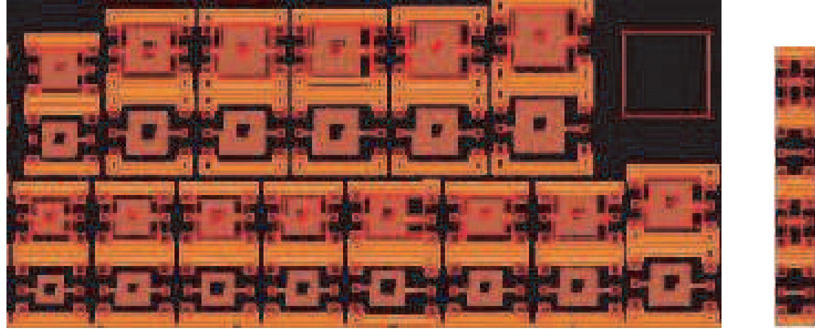


Figure 4.1: The experimental set including 14 pairs of inductors and 4 “thru” standards.

Table 4.1 lists the geometry parameters for the designed inductors. W represents the width of the spirals, S is the spacing between adjacent traces, ID is the inner diameter of the inductor and N is the number of turns.

The interconnects at both ports of the inductors are 50 μm long, and the widths are the same as the inductor trace width to avoid discontinuity. The “thru” standards have a total line length of 100 μm with the corresponding line widths of 6 μm and 10 μm respectively. Each has a counterpart with metal dummy fills.

In the test-structures with metal dummy fills, the metal dummy fills are 2×2 μm^2 in size, and repeated uniformly with a spacing of 2 μm on all metallization layers. A clearing distance around 15 μm is kept between the metal dummy fills

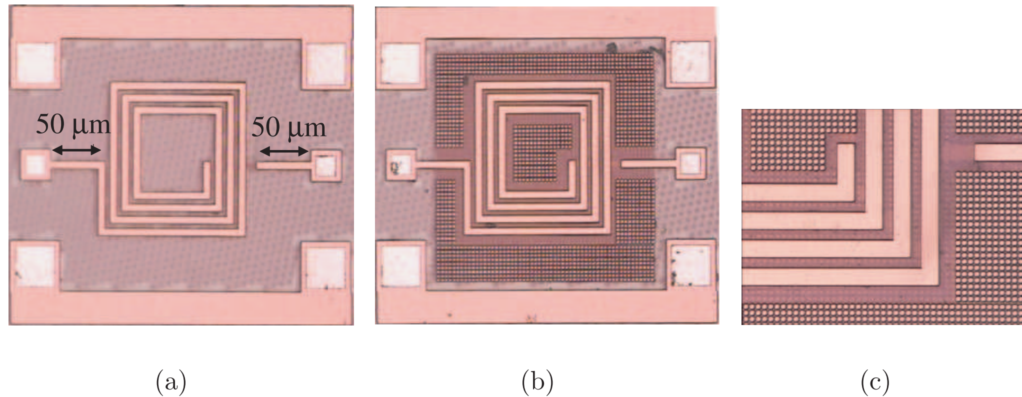
Table 4.1: Design Parameters for Inductors

W (μm)	S (μm)	ID (μm)	N
6	2,4,6	70, 86, 78	3.5, 4.5, 5.5
10	2,4,6,8	82, 66, 74, 82	3.5, 5.5

and the inductor traces on the same layer.

4.2.2 Fabrication and Measurement

A 0.18-μm CMOS technology was used to fabricate the experimental set. The technology consists of six aluminum metallization layers, and SiO_2 dielectric layers between all conductive layers. The inductors were placed on the top layer (i.e. M6) with an underpass on M4. The bulk Si has a resistivity of 10 Ω-cm. Fig 4.2 shows the microphotographs for a sample pair.



(a) (b) (c)

Figure 4.2: Microphotographs of fabricated inductors with W=6 μm, S=6 μm, ID=78 μm, and N=3.5 (a) without metal dummy fills, and (b) with metal dummy fills. (c) Regional enlarged view of (b).

Measurements were performed using the Agilent HP8510C VNA and the Cascade Microtech I40-A-GSG-100 probes. The VNA is first calibrated to the probe-tip-planes using the LRRM technique with an Impedance Standard Substrate (ISS) [26]. A "thru" de-embedding is used obtain the intrinsic behavior of the inductors as described in chapter 2.

4.3 Modeling of Inductors

This section describes the modeling of inductors with and without metal dummy fills based on de-embedded S-parameters. A widely used inductor model is a

physics-based single-π compact model shown in Fig. 4.3.

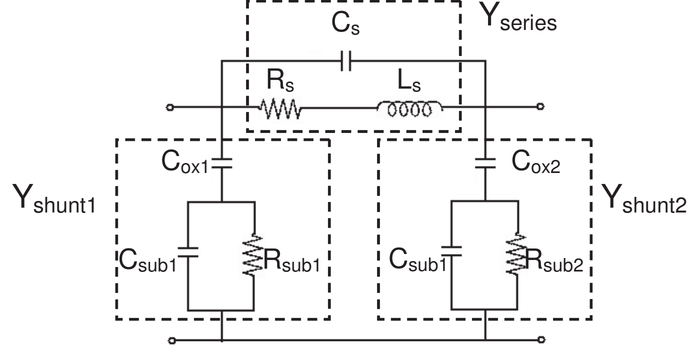


Figure 4.3: The equivalent single π-model for on-ship spiral inductors.

The model contains a series branch and two shunt branches. The series branch models the effective inductance as L_s and a parasitic resistance R_s in the metal traces, while C_s mainly represents the coupling between the two ports of the inductor through the spiral inductor and the underpass [18]. The shunt branches reflect the substrate effects, where C_{ox} is the capacitance in the oxide layer, C_{sub} is the capacitance in the substrate, and R_{sub} is the resistance due to the losses in the silicon substrate.

Reasons of using this model in this work are that it enables direct frequency-independent parameter extraction, and the impact of the metal dummy fills can be characterized by the change in the lumped elements.

The strategy of model parameter extraction is based on low-frequency and high-frequency assumptions. The procedure is demonstrated as follows. The first step is to find the Y elements in Fig. 4.3 through the Y-parameters converted from the de-embedded S-parameters:

$$Y_{series} = -Y_{12} = -Y_{21} \tag{4.1a}$$

$$Y_{shunt1} = Y_{11} + Y_{12} \tag{4.1b}$$

$$Y_{shunt2} = Y_{22} + Y_{21} \tag{4.1c}$$

At low frequencies, the input impedance of the model is dominated by the series branch and the effect of C_s is also negligible, i.e. $Z = 1/\left(Y_{series} + Y_{shunt}\right) \approx R_s + j\omega L$. Hence, R_s and L_s can be extracted from the real and imaginary part of $1/Y_{11}$ at low frequency from

$$R_s = \mathrm{Re}\left(1/Y_{11}\right) \tag{4.2}$$

and

$$L_s = \mathrm{Im}\left(1/Y_{11}\right)/\omega. \tag{4.3}$$

The values of the inductance and resistance for inductor W=6 μm, S=2 μm, ID=70 μm, and N=3.5 with and without metal dummy fills are plotted in Fig. 4.4 (a) and (b) as an example.

Extracting C_s directly from measurement is difficult since its value is usually very small. Instead, the value can be evaluated from a physical approximation using formula (15) in [18] and repeated here:

$$C_s = nW^2 \frac{\varepsilon_{ox}}{t_{ox,\mathrm{M6-M4}}} \tag{4.4}$$

where n is the number of overlap, for example, $n = 3$ for a 3.5-turn spiral, W is the line width of the inductor, and $t_{ox,\mathrm{M6-M4}}$ is the oxide thickness between the spiral in M6 and the underpass in M4.

The shunt admittance reflects the capacitance between the inductor and silicon substrate C_{ox} and the resistance and capacitance in the substrate R_{sub} and C_{sub} respectively due to the electric field penetrating into the substrate. According to their physical meanings, at lower frequencies, $R_{sub} \ll 1/\left(\omega C_{sub}\right)$, and thus Y_{shunt} is dominated by C_{ox} and R_{sub} at low frequencies. Based on this assumption, we can extract C_{ox} and R_{sub} from

$$C_{ox} = -\frac{1}{\omega \mathrm{Im}(1/Y_{shunt})}, \tag{4.5}$$

and

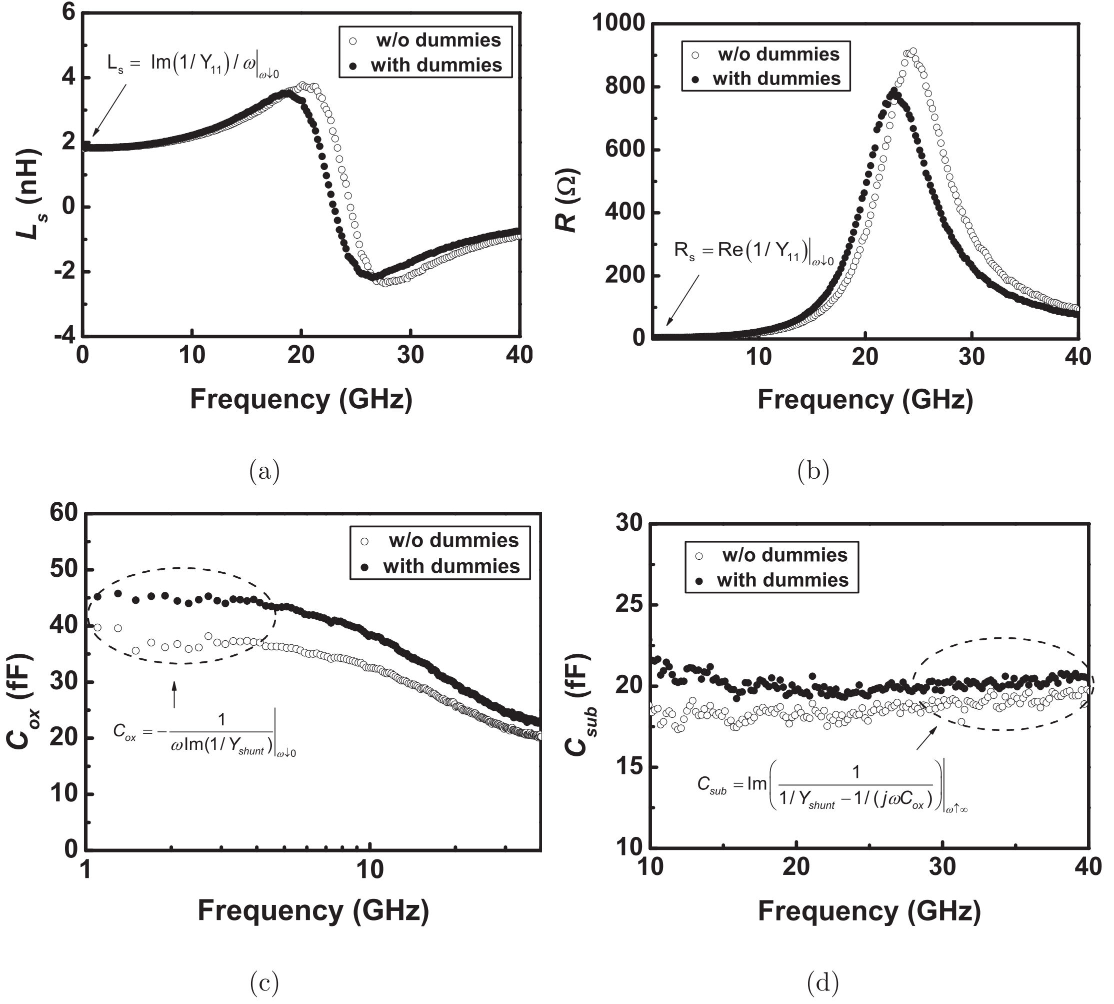


Figure 4.4: Measured (a) inductance, (b) resistance, (c) oxide capacitance, and (d) substrate capacitance for inductors with W=6 μm, S=2 μm, ID=70 μm, and N=3.5 with and without metal dummy fills.

$$R_{sub} = Re(1/Y_{shunt}). \tag{4.6}$$

Using the extracted value of C_{ox}, C_{sub} is obtained at higher frequencies from

$$C_{sub} = \mathrm{Im}\left(\frac{1}{1/Y_{shunt} - 1/(j\omega C_{ox})}\right) \tag{4.7}$$

C_{ox} and C_{sub} of inductor with W=6 μm, S=2 μm, ID=70 μm, and N=3.5 with and without metal dummy fills are plotted in Fig. 4.4 (c) and (d) respectively. It shows that C_{ox} of the inductor with dummy fills is about 20% more than that of

the inductor without dummy fills and C_{sub} is also increased slightly.

The effective Q-factor of the inductor is computed using

$$Q = -\mathrm{Im}\left(Y_{11}\right)/\mathrm{Re}\left(Y_{11}\right). \tag{4.8}$$

Measured and simulated Q-factors of the inductor with W=6 μm, S=2 μm, ID=70 μm, and N=3.5 with and without dummy fills are plotted in Fig. 4.5. The maximum Q value ($Q_{\max}$) is lowered by 7.2% and the frequency for $Q_{\max}$ ($f_{\max}$) is reduced by 800 MHz. The resonance frequency (f_{res}) is also slightly reduced. Simulated results use the model of Fig. 4.3 with the extracted parameter values. The figure demonstrates that below the first resonance frequency of 25 GHz, the model predicts the Q-factor well.

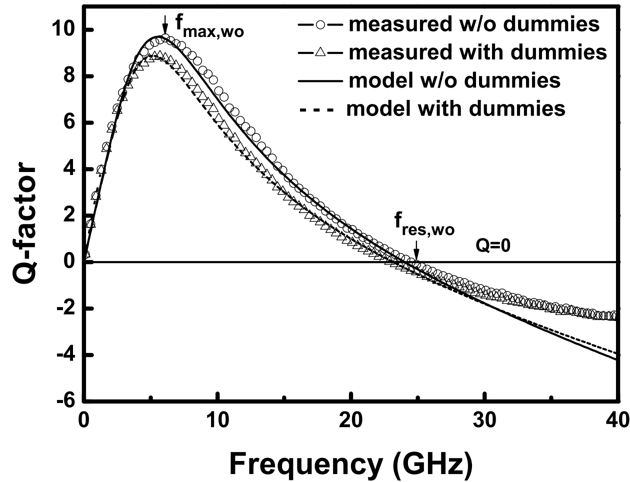


Figure 4.5: Comparison of the measured and simulated Q-factors of inductor with W=6 μm, S=2 μm, ID=70 μm, and N=3.5 with and without metal dummy fills.

4.4 Effect of Metal Dummy Fills On Inductors

The effect of the metal dummy fills on the spiral inductors are summarized in this section. The extracted equivalent model parameters as well as $Q_{\max}$, $f_{\max}$ and f_{res}

for the experimental inductors are listed in Tables 4.2 and 4.3.

From the tables, it is observed that the changes on the elements in the series branch of the model are not pronounced. The changes are less than 1% in L_s and less than 3% in R_s. However, the shunt branch elements are affected considerably. Experimental results show C_{ox} increases around 15% to 20%. C_{sub} is also increased up to 10% while R_{sub} is decreased accordingly.

The impact of the changes in C_{ox}, C_{sub} and R_{sub} on $Q_{\max}$ are examined taking the inductor with W=6 μm, S=2 μm, ID=70 μm, N=3.5 as an example. First, the extracted model parameters except C_{ox} for the inductor without metal dummy fills are kept fixed. Through varying C_{ox} from 0 (ΔC_{ox} =-100%) to double the value (ΔC_{ox}=100%), the resulting change in $Q_{\max}$ ($\Delta Q_{\max}$) is found as a function of ΔC_{ox} and is shown in Fig. 4.6(a). Similarly, the function of ΔC_{sub} and ΔR_{sub} are plotted in Fig. 4.6(b) and Fig. 4.6(c) respectively. The changes in $Q_{\max}$ caused by the changes in these three elements are found in the curves respectively. The extracted C_{ox} of the inductor with metal dummy fills is increased by 21% compared to the one without dummies. The corresponding change in $Q_{\max}$ is found at -8% in the curve, which matches the measured result well as listed in Table 4.2 and Table 4.3, while the impact of C_{sub} and R_{sub} are substantially less. This reveals that the change in $Q_{\max}$ is mainly due to the change in C_{ox}. Hence, the change in C_{ox} affects the $Q_{\max}$ most while the effect due to the changes in C_{sub} and R_{sub} is the much less significant.

4.5 Model Modification

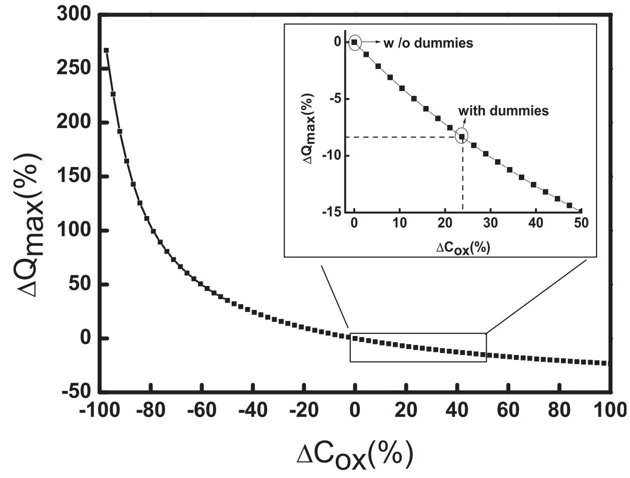
From the analysis of the sensitivity of the Q-factor to the changes in the substrate elements, ΔC_{ox} has been identified as the dominant factor of the Q-factor degradation due to the metal dummy fills. Hence, we propose to modify the conventional inductor models by updating C_{ox} taking into account the metal dummy fills.

Table 4.2: Extracted Parameter Values and Changes for Inductors with and without Metal Dummy Fills (W=6 μm)

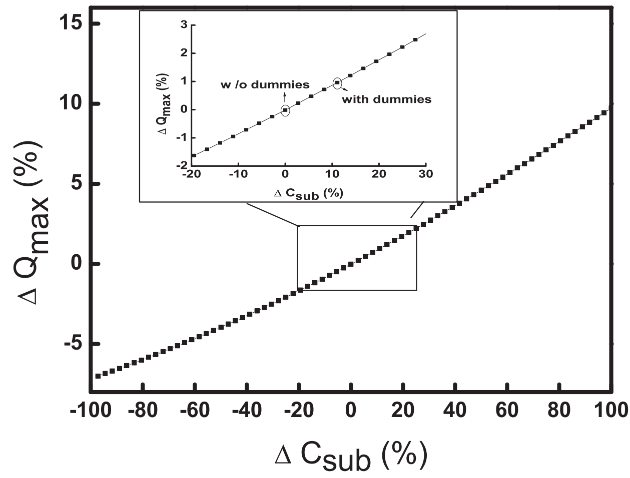
W (μm)	6													
N	3.5						4.5		5.5					
S/ID (μm)	2/70		4/86		6/78		4/66		2/70		4/86		6/78	
Dummies	no	yes	no	yes	no	yes	no	yes	no	yes	no	yes	no	yes
L_s (nH)	1.80	1.78	2.25	2.26	2.02	2.02	2.84	2.84	4.45	4.45	5.53	5.53	5.16	5.16
ΔL_s	-1.1%		-0.4%		0		0		0		0		0	
R_s (Ω)	4.25	4.26	4.3	4.4	4.2	4.3	5	5	6.4	6.5	7. 9	7.8	7.9	7.9
ΔR_s	0.2%		2.3%		2.3%		0		3.1%		-0.1%		0%	
C_{ox} (fF)	38	45	50	61	51	61	59	69	65	76	86	96	73	84
ΔC_{ox}	18%		22%		19%		17%		17%		11%		15%	
C_{sub} (fF)	18	20	23	25	24	25	20	23	30	30	26	24	25	28
ΔC_{sub}	11.1%		8.7%		4.2%		15%		0		4.3%		12%	
R_{sub} (Ω)	490	440	520	410	500	410	490	480	540	430	500	460	660	620
ΔR_{sub}	-10.2%		-10.6%		-18%		-2%		-20.3%		-8%		-12.7%	
$Q_{\max}$	9.65	8.89	9.26	8.35	9.02	8.33	8.54	7.95	8.10	7.55	7.36	7.12	7.55	7.17
$\Delta Q_{\max}$	-7.8%		-9.8%		-7.7%		-6.8%		-6.8%		-3.3%		-4.9%	
$f_{\max}$(GHz)	6.3	5.5	5.1	4.7	5.5	4.9	4.3	3.9	3.5	3.1	2.5	2.5	2.9	2.7
$\Delta f_{\max}$	-12.7%		-7.8%		-10.9%		-9.3%		-11.4%		0		-6.8%	
fres (GHz)	24.5	23.1	20.1	18.7	21.5	20.1	16.9	15.7	12.3	11.5	9.5	9.1	10.1	9.3
Δf_{res}	-5.7%		-7%		-6.5%		-7.1%		-6.5%		-4.2%		-8%	

Table 4.3: Extracted Parameter Values and Changes for Inductors with and without Metal Dummy Fills (W=10 μm)

W (μm)	10													
N	3.5								5.5					
S/ID (μm)	2/82		4/66		6/74		8/82		2/80		4/66		6/74	
Dummies	no	yes	no	yes	no	yes	no	yes	no	yes	no	yes	no	yes
L_s (nH)	2.17	2.17	1.74	1.74	1.94	1.94	2.18	2.23	5.39	5.39	4.64	4.65	5.22	5.22
ΔL_s	0		0		0		2.3%		0		2%		0	
R_s (Ω)	3.16	3.23	2.68	2.77	2.92	3.03	3.25	3.37	5.4	5.51	5.11	5.2	5.68	5.73
ΔR_s	2.2%		3.4%		3.7%		3.7%		2%		1.7%		0.9%	
C_{ox} (fF)	65	77	62	71	71	83	82	96	105	126	114	127	133	154
ΔC_{ox}	18.5%		14.5%		16.9%		17%		20%		17.2%		15.8%	
C_{sub} (fF)	28	30	26	27	31	33	35	35	28	30	28	30	24	26
ΔC_{sub}	7.1%		3.8%		6.5%		0		7.1%		7.1%		8.3%	
R_{sub} (Ω)	660	580	620	520	570	500	530	480	710	620	620	550	600	530
ΔR_{sub}	-12.1%		-16.1%		-12.3%		-9.4%		-12.7%		-11.3%		-11.7%	
$Q_{\max}$	8.9	8. 3	9.4	8.6	9.4	8.7	9.0	7.9	7.6	7.0	7.5	7.1	7.4	7.0
$\Delta Q_{\max}$	-7.8%		-8.1%		-7.5%		-13%		-7%		-6%		-5.9%	
$f_{\max}$(GHz)	4.3	3.9	5.1	4.3	4.3	4.1	4.1	3.9	2.3	2.1	2.5	2.3	2.3	2.1
$\Delta f_{\max}$	-9.3%		-15.7%		-4.7%		-4.8%		-8.7%		-8%		-8.7%	
f_{res} (GHz)	17.7	16.7	21.5	20.1	18.7	17.5	16.9	15.9	8.3	7.7	9.1	8.7	7.9	7.5
Δf_{res}	-5.6%		-6.5%		-6.4%		-5.9%		-7.2%		-4.4%		-5%	



(a)



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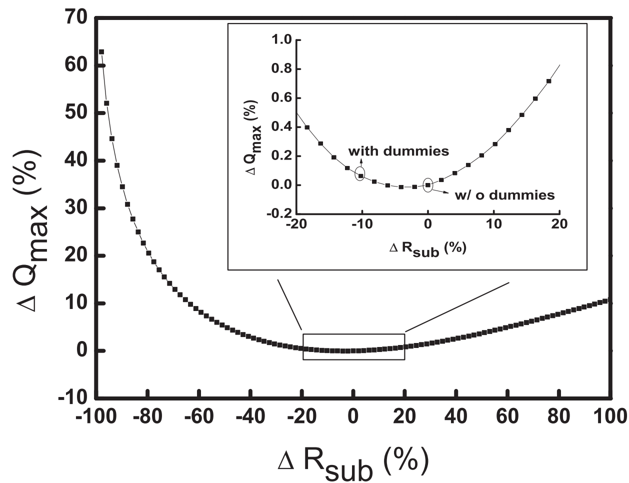


(c)

Figure 4.6: Change in $Q_{\max}$ versus the changes in (a) C_{ox}, (b) C_{sub}, and (c) R_{sub} for the inductor with W=6 μm, S=2 μm, ID=70 μm, and N=3.5.

In the following section, the effect of metal dummy fills on C_{ox} of the inductor will be analyzed using two methods.

4.5.1 Method 1: Parallel-Plate Assumption

Fig. 4.7 shows the structure of an inductor with metal dummy fills inserted underneath. Assume the metal dummy fills are with a size of $a \times a$ and a pitch size $p \times p$. The metal density by the coverage of the metal dummy fills is $\eta = a^2/p^2$.

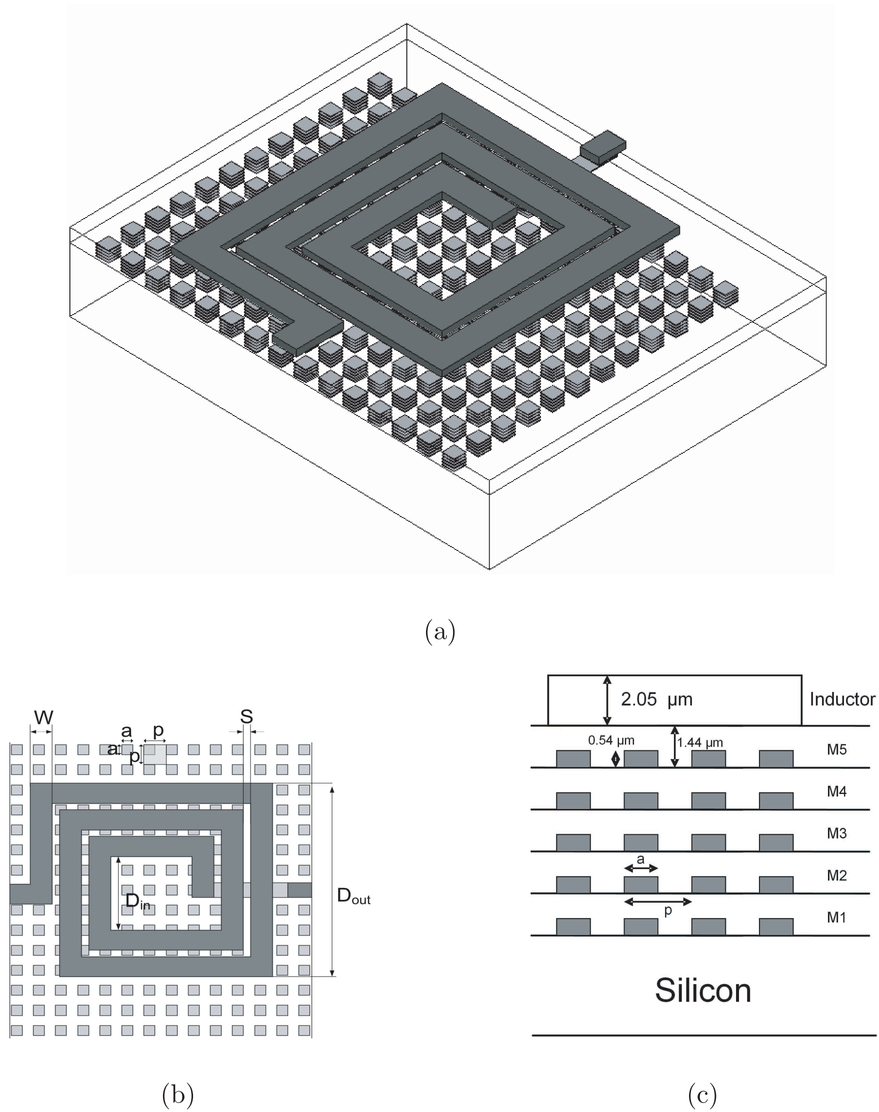


Figure 4.7: (a) 3-D view of the spiral inductor with metal dummy fills. (b) Top view. (c) Cross-sectional view of the inserted metal dummies in M1 to M5.

Based on the parallel plate assumption, the capacitance of an area of A without metal dummy fills is calculated as

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_r A}{h_{IMD}}, \tag{4.9}$$

where ϵ_r is the relative dielectric constant of the oxide layer, and h_{IMD}=7.2 μm which is the total height of the oxide layers. Considering the physical volume of the metal dummy fills, the oxide capacitance with metal dummy fills can be estimated as

$$C'_{ox} = \frac{\varepsilon_0 \varepsilon_r A(1-\eta)}{h_{IMD}} + \frac{\varepsilon_0 \varepsilon_r A \eta}{h_{eff}}, \tag{4.10}$$

where the thickness of the oxide layer h_{IMD} is reduced to h_{eff}=0.95=4.5μm due to the placement of the metal dummy fills. The second term in Eq. (4.10) is the increased capacitance due to the existence of metal dummy fills. The ratio of increase is

$$\frac{C'_{ox}}{C_{ox}} = 1 + \eta(\frac{h_{IMD}}{h_{eff}} - 1), \tag{4.11}$$

Hence, for a given process with fixed thickness of the oxide and metallization layers, the increase of C_{ox} is determined by the metal dummy density η. With a metal density of 25% on M1 to M5 in our test structures, the resulted increase in C_{ox} is 15% with the parallel-plate consideration. However, this number is slightly underestimated compared to experimental results. The reason is probably due to the fringing electric fields which are ignored at the edge of the inductors and also among the metal dummy fills.

4.5.2 Method 2: Fringing Field Consideration

In this section, C_{ox} of the inductors is modeled using an analytical formula which accounts for the fringing effects. As reported in [66], the oxide capacitance of the inductor without metal dummies can be calculated as

$$C_{ox,wo} = \varepsilon_0 \left\{ \left(\frac{\varepsilon_r A}{h_{IMD}} \right)^n + \left[0.9 \times \frac{\varepsilon_r + 1}{2} \sqrt{8\pi A_p} \right]^n \right\}^{1/n}, \tag{4.12}$$

where A is the area of the conductor of the inductor, A_p is the total area of the spiral including gaps but without the center hole, i.e., $A_p = OD^2 - ID^2$. The first term in Eq. (4.12) identifies the parallel-plate capacitance between the spiral and the silicon substrate while the second term accounts for the fringing field capacitance at the edge of spiral. The power n is taken as 1.114 [66].

Similarly, the oxide capacitance with metal dummy fills can be approximately estimated as [66]

$$\begin{aligned} C_{ox,dm} = \varepsilon_0 & \left\{ \left(\frac{\varepsilon_r A(1-\eta)}{h_{IMD}} \right)^{n'} + \left[0.9 \times \frac{\varepsilon_r + 1}{2} \sqrt{8\pi A_p (1-\eta)} \right]^{n'} \right\}^{1/n'} \\ + \varepsilon_0 & \left\{ \left(\frac{\varepsilon_r A \eta}{h_{eff}} \right)^{n'} + \left[0.9 \times \frac{\varepsilon_r + 1}{2} \sqrt{8\pi A_p \eta} \right]^{n'} \right\}^{1/n'} \end{aligned} \quad (4.13)$$

The power n' may be slightly changed due to the periodic insertion of metal dummy fills [66]. For simplicity, n' is kept as 1.114. The increase in the ratio $C_{ox,dm}/C_{ox,wo}$ is a function of the dummy density η and also depends on the geometry of the spiral inductor. The estimated increase in the ratio using Eq. (4.12) and Eq. (4.13) for the inductor samples is between 17% and 19%.

4.5.3 Update of the Compact Model

As described above, C_{ox} of the spiral inductor can be modified to account for the effect of metal dummy fills. This allows the updating of the existing compact model of inductors without metal dummy fills. To verify this, models of the inductors without metal dummy fills are back simulated with the corrected C_{ox} while keeping the other model parameters the same. Fig. 4.8 shows the comparison of the measured and predicted Q-factor using two methods for the inductor with metal dummy fills with W=6 μm, S=2 μm, ID=66 μm and N=3.5. Good agreement is observed between the predicted Q-factor using the two methods and the measured Q-factor below the self-resonance frequency.

The predicted $Q_{\max}$ and $f_{\max}$ with updated C_{ox} using the two methods are

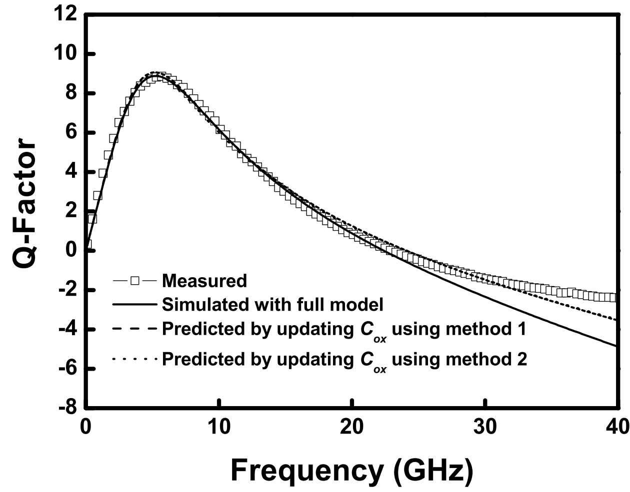


Figure 4.8: Comparison of the measured, simulated and predicted Q-factors of inductor with metal dummy fills with W=6 μm, S=2 μm, ID=70 μm, N=3.5 using two methods.

plotted in Fig. 4.9 and Fig. 4.10 against the measured results for all sample inductors with metal dummy fills. It is demonstrated that both methods can predict the performance of the inductors with metal dummy fills. Method 2 is slightly more accurate. The predicted $Q_{\max}$ is within an error of 2% and $f_{\max}$ within 8%.

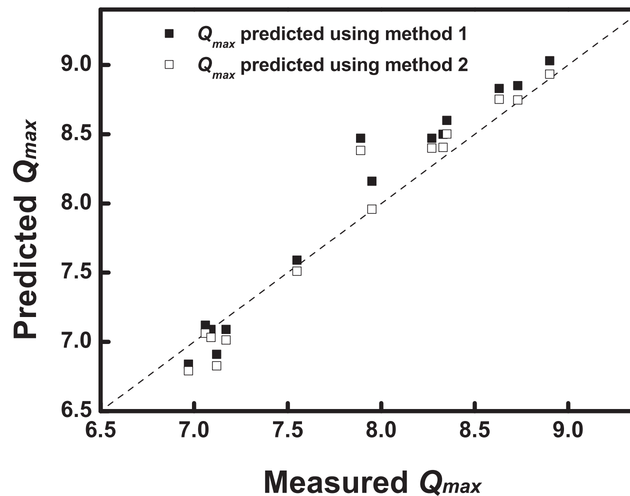


Figure 4.9: Predicted $Q_{\max}$ versus measured $Q_{\max}$ by updating C_{ox} using two methods.

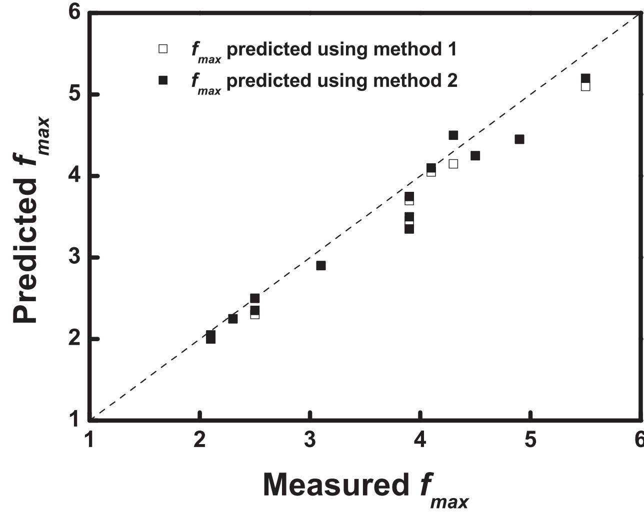


Figure 4.10: Predicted $f_{\max}$ versus measured $f_{\max}$ by updating C_{ox} using two methods.

4.6 Conclusions and Recommendations

In this chapter, a method to predict the microwave behavior of the on-chip inductors with metal dummy fills based on the conventional equivalent models is proposed. It was found that the main impact of metal dummy fills is the increase in the oxide capacitance C_{ox} which leads to a decrease in $Q_{\max}$ and $f_{\max}$. Two methods were used to analyze the change in C_{ox}: the parallel-plate method and the method to include the fringing field effects. Good agreement was achieved between the predicted and measured performance of inductors with metal dummy fills by updating C_{ox} using the two methods in the conventional models. Hence, the existing model of inductors without metal dummy fills can be fast and accurately updated to predict the performance of the inductor counterpart with metal dummy fills.

CHAPTER 5

Millimeter Wave Thin Film Microstrip Lines in CMOS

5.1 Introduction

There is a growing interest in developing millimeter wave communication systems which enable higher data rates and larger capacity of wireless networks. Several frequency bands in the millimeter wave range have been allocated by the Federal Communications Commision (FCC) for wireless communications: the unlicensed bands from 57-64 GHz for personal area high data rate communications, and the 22-29 GHz and the 76-77 GHz bands for automotive radar systems. Other potential applications are also under exploration such as millimeter wave imaging above 100 GHz.

Due to the continuous downscaling, CMOS technology is becoming a promising candidate for millimeter wave applications with its advantages of low cost for high volume production. However, major challenges still remain in realizing high quality passives due to the high losses associated with the low-resistivity silicon substrate and metallization conductor losses.

On-chip line resonators are the basic building blocks of distributed filters and matching circuits. Important characteristics of the line resonators include the resonant frequency, the characteristic impedance, and the unloaded Q-factor. In designs where low loss is of prime importance, such as filters, a high Q-factor of

the line resonators is imperative.

Several types of transmission lines can be realized in CMOS technologies. The simplest transmission line is formed by a conductor over the dielectric and the silicon substrate. As an undesired side effect, energy is coupled into the low-resistivity silicon substrate which increases the losses as frequency increases [67]. Another type is the coplanar waveguide (CPW) structure formed by a conductor and a pair of ground planes on the same plane [68]. This structure suffers less from the substrate losses because the electromagnetic fields can be mostly contained within the dielectric layer. However, the CPW configuration is not considered here due to the required additional ground connections when applying it in the parallel-coupled resonator filters as illustrated in Fig. 5.1. These ground connections are used to suppress undesired slotline modes, which may increase losses of the coplanar filters.

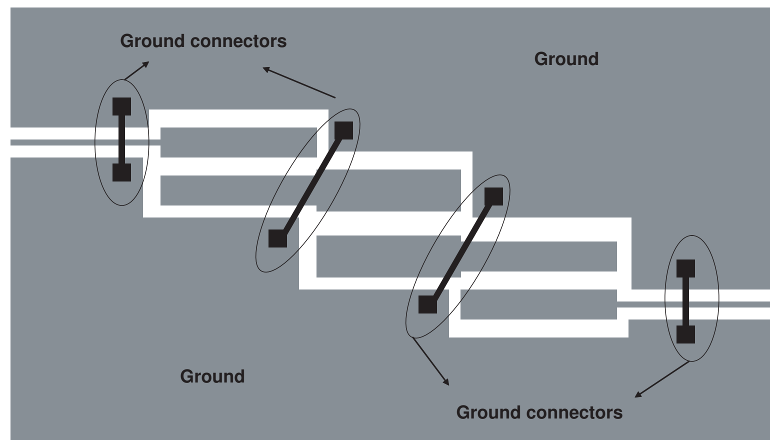


Figure 5.1: Illustration of parallel-coupled resonator filters using CPW lines.

This chapter systematically studied a microstrip-like transmission line in CMOS, the thin film microstrip (TFMS) transmission lines. These transmission lines may offer a high Q-factor and ease-of-design for coupled-line filters. The structure comprises a conductor with a ground plane in the lowest metallization layer to shield the signal lines from the lossy silicon substrate. Since standard CMOS processes

offer multiple metallization layers, different configurations for the TFMS lines can be realized, among which an optimum configuration must be identified. In this chapter, the performance of three TFMS lines realized in a 0.18-μm CMOS technology are investigated. The unloaded Q-factor (Q_u) around 60 GHz is determined for the quarter-wavelength lines. The results provide important guidelines in 60 GHz edge-coupled bandpass filter designs which will be demonstrated in the next chapter.

5.2 TFMS Structure

A standard 0.18-μm CMOS technology is used in this work. Although this technology is not the most likely choice for most millimeter wave circuits, it is sufficient for studies of passive components, considering cost, availability and throughput time.

Fig. 5.2 shows the layer configuration of the 0.18-μm CMOS process, with six metallizations. The top metallization M6 has a thickness of 2.05 μm. The other metallizations M1-M5 have a thickness of 0.54 μm. The distance between adjacent metallizations is 0.9 μm. The total thickness of the SiO_2 layers is 9.1 μm. A ground plane is made in M1.

Similar to conventional microtrip lines, the TFMS lines made in standard CMOS have loss contributions from the conductor losses of the signal lines and the ground plane, dielectric losses, and radiation losses. Within the limits of the material properties and layer dimensions, the main trade-off that can be made to reduce loss is between the thickness of the signal lines and the thickness of the dielectric substrate. Given a certain line width, a thicker signal line leads to less conductor losses. This can be done by stacking adjacent metallizaiton layers, for instance, M6 and M5. However, it should be noted that, the resulted reduced dielectric layer thickness underneath the signal line in turn increases the conduc-

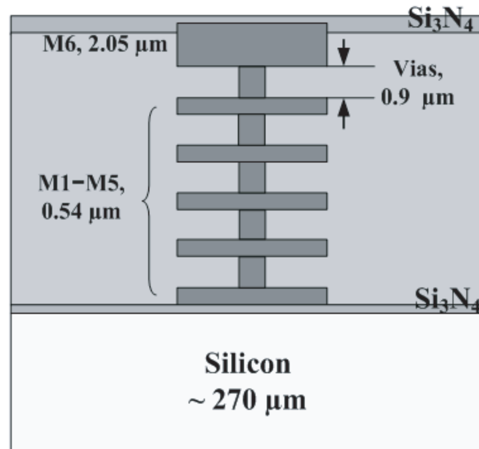
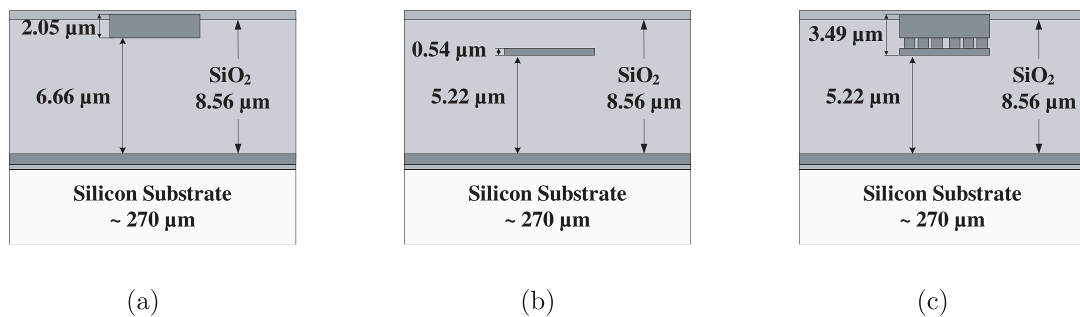


Figure 5.2: Layer configuration in a 0.18-μm CMOS process.

tor loss. Thus, trade-offs between options need to be revealed. In this work, we consider three options to implement the signal lines: using M6 only (TFMS-M6), using M5 only (TFMS-M5), and stacking M6 and M5 through vias (TFMS-M56). The cross-sectional view of the three configurations are shown in Fig. 5.3.



(a) (b) (c)

Figure 5.3: Configurations of TFMS lines: (a) TFMS-M6. (b) TFMS-M5. (c) TFMS-M56.

M6 is the highest metallization layer above ground. The thickest dielectric layer of TFMS-M6 allows the widest signal line for a certain line characteristic impedance. M5 is the most viable choice for broadside coupling [69]. A thickened signal line of 3.49 μm is made in TFMS-M56 attempting to reduce the conductor losses. However, it should be noted that in TFMS-M56, the conductivity of M5 is lower than that of M6, and the use of vias also introduces uncertainty in the total

conductivity. Thus the ability to reduce the conductor loss in the signal lines may be compromised.

To identify the best choice of quarter-wavelength line resonators in terms of low loss, the unloaded Q-factor at the resonance frequency of 60 GHz must be experimentally determined and compared for the above three options.

Before presenting the measured data, the definition and method to determinate the unloaded Q-factor will be discussed.

5.3 Unloaded Q-factor

For an arbitrary resonant circuit, the unloaded Q-factor is defined as the ratio of the stored energy to the average power loss in a cycle [70]:

$$Q_u = 2\pi f_0 \frac{\text{Stored Energy}}{\text{Average Power loss}}\bigg|_{f=f_0}, \tag{5.1}$$

where f_0 is the resonance frequency.

If the equivalent circuit at and around the resonance frequency is a series or parallel resonance circuit, the unloaded Q-factor of the resonant circuit can be defined as the change in reactance X or susceptance Y per deviation:

$$Q_u = \frac{f_0}{2R}\frac{dX}{df}\bigg|_{f=f_0}, \tag{5.2a}$$

$$Q_u = \frac{f_0}{2G}\frac{dY}{df}\bigg|_{f=f_0}, \tag{5.2b}$$

where $Z = R + jX$, and $Y = G + jY$ represent the impedance or the admittance of the series or parallel resonance circuit respectively.

The above definitions will be used to derive the Q_u of the quarter-wavelength line resonators. The quarter-wavelength lines exhibit series or shunt resonances with a fundamental resonance frequency of $f_0 = c/\left(\sqrt{\varepsilon_r}\lambda_0\right)$ when open or short circuited as shown in Fig. 5.4.

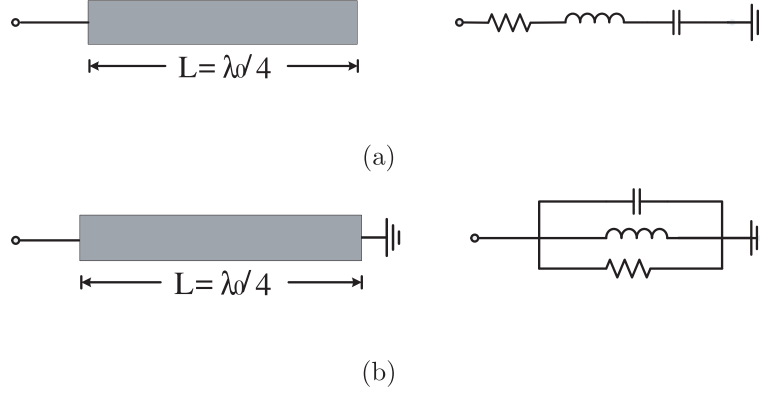


Figure 5.4: $\lambda_0/4$ line resonators and equivalent circuits. (a) Open-circuited and (b) short-circuited.

Since the unloaded Q-factor is a measure of the intrinsic line resonator, either a perfect open or a perfect shorted $\lambda_0/4$ line will lead to the same Q_u. Here an short-circuited quarter-wavelength line will be examined. Under the condition of small losses, $\alpha l < 0.1$ Np, where α is the attenuation constant, and l is the line length, we have $\tanh(\alpha l) \approx \alpha l$. The input impedance $Z_{in} = Z_0 \tanh(\alpha + j\beta)l$ can be then approximated by:

$$Z_{in} = Z_0 \frac{1 - j \tanh \alpha l \cdot \cot \beta l}{\tanh \alpha l - j \cot \beta l} \approx Z_0 \frac{1 - j\alpha l \cdot \cot \beta l}{\alpha l - j \cot \beta l}, \tag{5.3}$$

where Z_0 is the characteristic impedance, and β is the phase constant of the line.

Around the series resonance frequencies where $\beta l = (2n-1)\,\pi/2$, $\cot(\beta l) \approx -\beta l$, and the input impedance is reduced to

$$Z_{in} = \frac{Z_0}{\alpha l + j\beta l} \tag{5.4}$$

Substituting (5.4) into the definition of Q_u in (5.2a), with the assumptions that Z_0 and β are independent of frequency, Q_u can be evaluated as

$$Q_u = \left.\frac{\beta}{2\alpha}\right|_{f=f_0}, \tag{5.5}$$

Eq. (5.5) suggests that Q_u of the line resonator is determined by two characteristics of the transmission line: the attenuation factor α and the phase constant

β. Since an ideal open or short termination is not realistic in microwave measurements, these characteristics are be obtained by measuring the two-port quarter-wavelength lines around the resonance frequency in this work. The values of α and β are found from $\gamma = \alpha + j\beta$, where the propagation constant γ is obtained from the ABCD-parameters converted from the two-port S-parameters as

$$\gamma = \cosh^{-1}(A)/l \tag{5.6}$$

5.4 Experiment of TFMS Lines

5.4.1 Fabrication and Measurement

TFMS lines in the three configurations with widths ranging from 1.5 μm to 85 μm are fabricated for two-port on-wafer measurements using GSG probes. All the ground pads are made by stacked layers of M6 to M1 through vias. The line lengths are 820 μm. "Thru" lines of 150 μm in TFMS-M6 configuration and 170 μm in TFMS-M5 and TFMS-M56 configurations are fabricated for de-embedding. After de-embedding, the intrinsic length of the TFMS-M6 lines is 670 μm, whereas the intrinsic length of TFMS-M5 and TFMS-M56 lines is 650 μm, which lead to approximately the required quarter wavelength at 60 GHz. A die photo is shown in Fig. 5.5 with the group of TFMS-M6 and TFMS-M56 lines and a "thru_M6" line for de-embedding. TFMS-M5 lines are not visible since the metal layer M5 is too thin. Therefore the die photo is not shown here.

Measurements were performed using Anritsu's ME7808B VNA, which was calibrated using the LRRM technique with an ISS from 50 GHz to 80 GHz. A "thru" de-embedding is performed for each line as described in chapter 2.

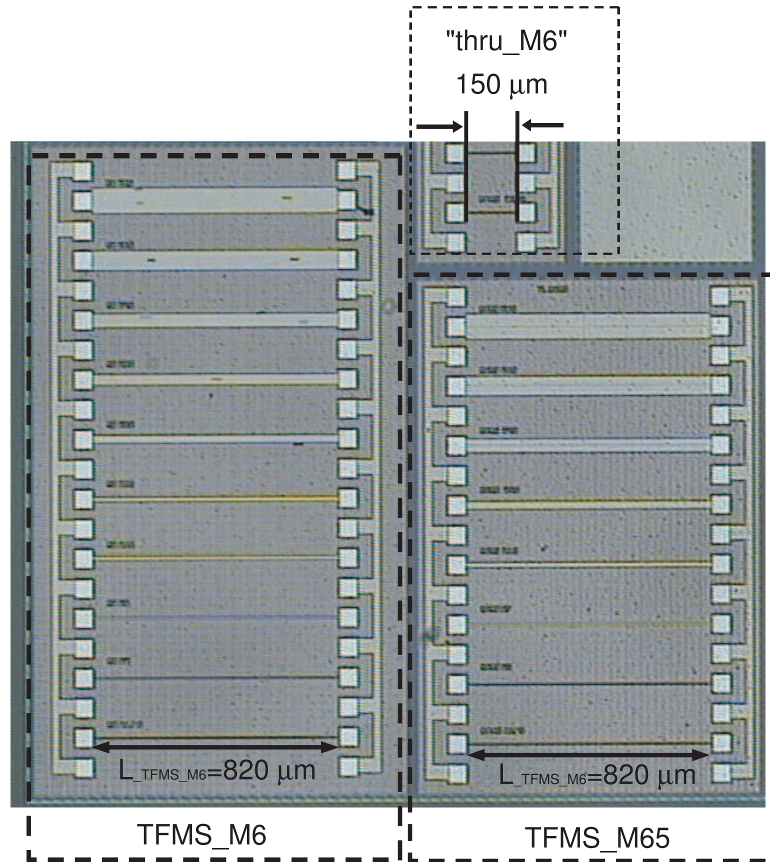


Figure 5.5: Fabricated TFMS lines.

5.4.2 Results

Evaluation of Q_u

The extraction of Q_u follows the procedure described in Section 5.3. As an example, the extracted α and β for a TFMS-M6 line with W=12 μm, L=670 μm is shown in Fig. 5.6.

An examination of the conditions for deriving Eq. (5.5) is necessary. The non-dispersion condition is confirmed through β in Fig. 5.6(b). Fig. 5.7(a) shows that the condition for a considerably small loss of $\alpha l < 0.1$ Np is satisfied in this case. Similar observations are made in all of the lines under study. The quarter-wavelength frequency f_0 is determined where $\beta L/\pi = 0.5$ as illustrated in

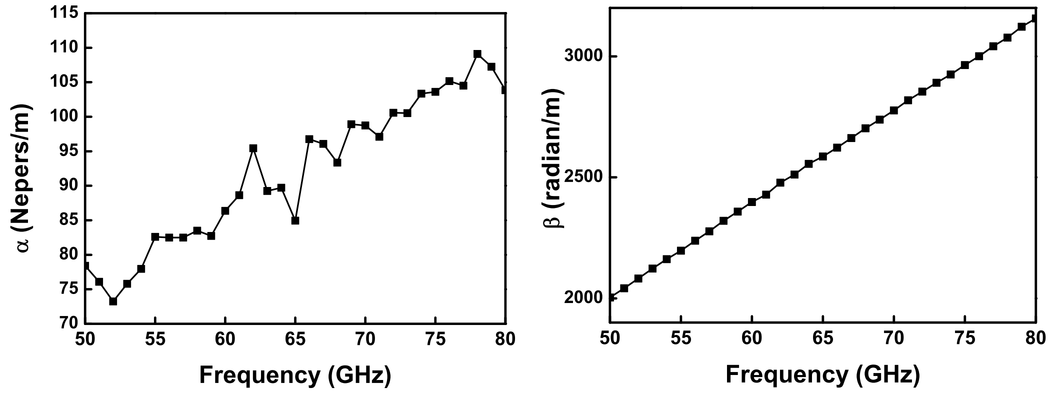


Figure 5.6: Extracted α and β for a TFMS-M6 line with W=12 μm, L=670 μm.

Fig. 5.7(b).

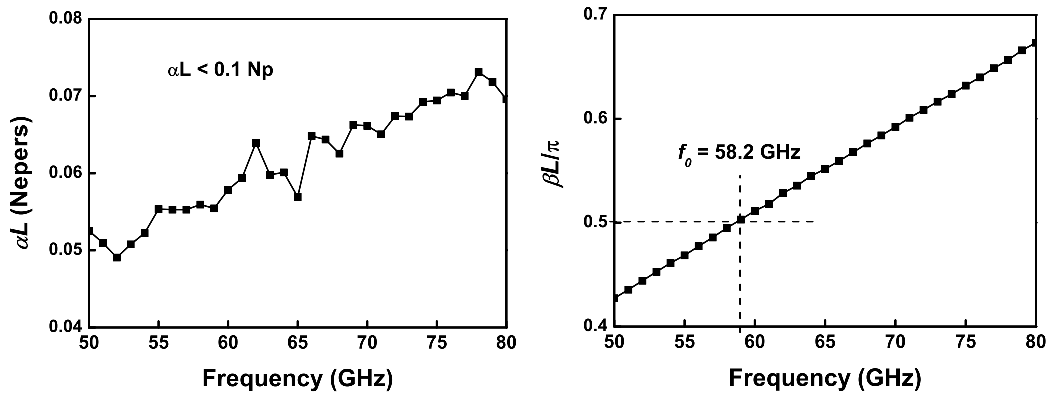
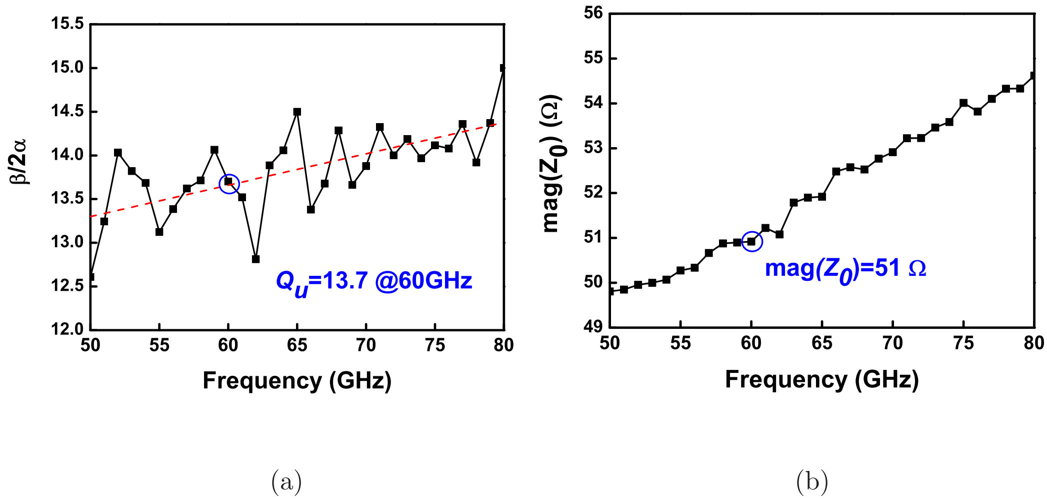


Figure 5.7: (a) Examination the condition of small loss. (b) Determination of the resonance frequency f_0 for the $\lambda/4$ line where $\beta L/\pi = 0.5$ for a TFMS-M6 line with $W = 12$ μm, $L = 670$ μm.

With both conditions satisfied, Q_u is extracted using Eq. (5.5) and obtained at f_0 shown in Fig. 5.8(a). The extracted characteristic impedance $Z_0 = \sqrt{B/C}$, where B and C are the elements in the ABCD-parameters, is further provided in Fig. 5.8(b).



(a) (b)

Figure 5.8: (a) Extracted Q_u and (b) Magnitude of the characteristic impedance $|Z_0|$ for a TFMS-M6 line with W=12 μm, L=670 μm.

EM simulators including Sonnet EM, Momentum, and HFSS are also evaluated. The measured data for TFMS-M6 lines is compared with simulation results using various simulators shown in Fig. 5.9. Simulated Q_u values show a similar trend as a function of line widths but differ among simulators. The difference between the simulators might be due to the way the thick metal is modeled.

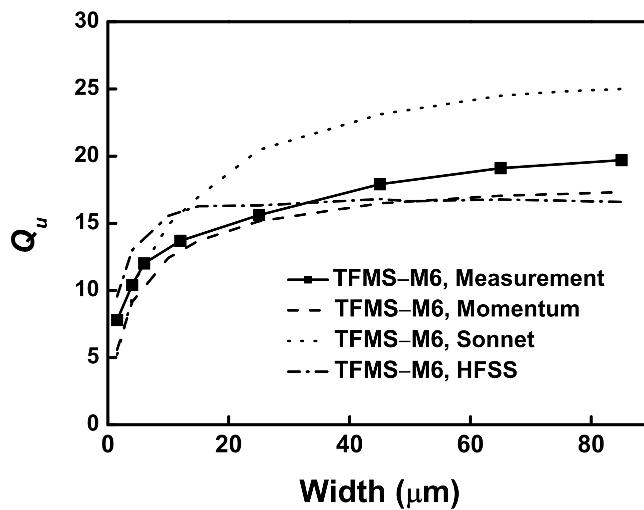


Figure 5.9: Comparison of simulated and measured Q_u of TFMS-M6 lines.

Comparison of Q_u

A comparison of the extracted Q_u from measurements for the three TFMS lines is provided in Fig. 5.10. It is clear that TFMS-M6 has the highest Q_u, whereas

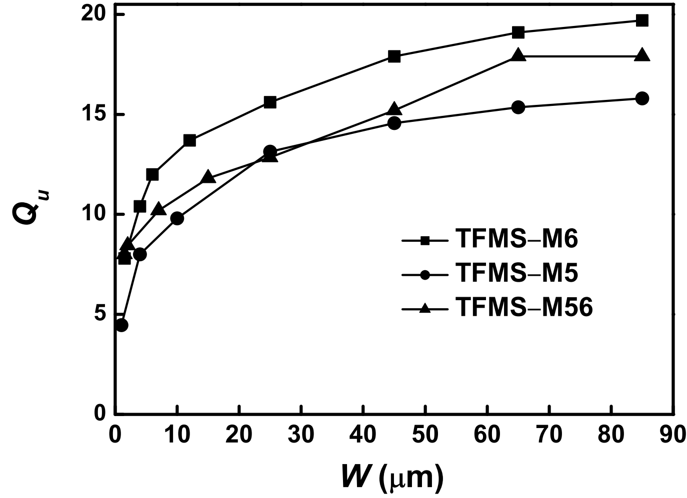


Figure 5.10: Comparison of measured Q_u of TFMS lines resonators at the resonance frequency.

TFMS-M5 has the lowest Q_u. Further, for line widths smaller than 20 μm, where the conductor loss dominates, Q_u increases rapidly with increasing line width. For transmission lines wider than 20 μm, where the conductor loss does not decrease with increasing line width while dielectric loss becomes more significant, Q_u almost becomes constant. This indicates that choosing a reference characteristic impedance lower than 50 Ω in filter design may result in significant improvement due to the saturated Q_u values.

In Fig. 5.11, the relationship between the measured unloaded Q-factor, the characteristic line impedance, and the line width is shown. The TFMS-M6 lines have a higher $\mathrm{Q_u}$ value than the other two configurations at the same characteristic impedance or line width. We therefore conclude that TFMS-M6 lines have the highest $\mathrm{Q_u}$ and are the optimum choice.

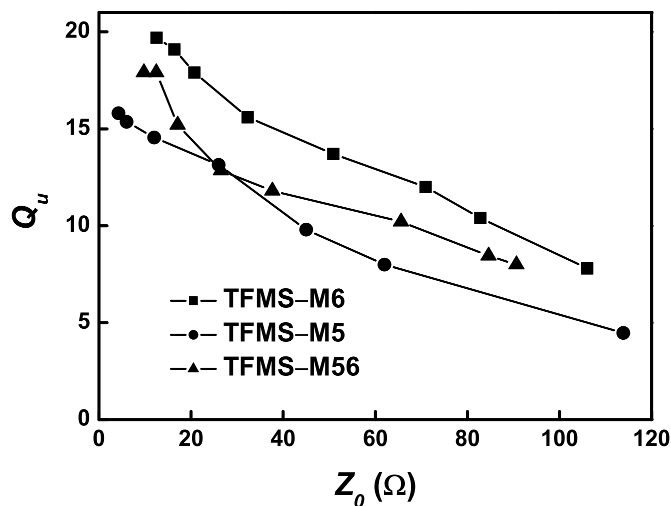


Figure 5.11: Measured Q_u of TFMS-M6 and TFMS-M5 line resonators against the line width at 60 GHz.

5.5 Conclusions and Recommendations

Based on a commercial 0.18-μm CMOS process, this work establishes an optimum configuration for TFMS lines for millimeter wave applications. Unloaded Q-factors at 60 GHz are compared for three viable configurations over a broad range of line widths and characteristic impedances. It is found that signal lines in the top metallization M6 only and a ground plane in the lowest metallization M1 provides the highest unloaded Q-factors, especially for wider lines or lower characteristic impedances compared to lines with M5 and M6 stacked. To further illustrate the effects of the unloaded Q-factors of TFMS lines, filters using $\lambda/4$ these TFMS configurations will be discussed in the next chapter.

CHAPTER 6

Millimeter Wave Filters in 0.18-μm CMOS

6.1 Introduction

In the transceiver front-end blocks, bandpass filters are mainly used for interference rejection. As an example, consider a radar system in the 76-77 GHz band as illustrated in Fig. 6.1 [71]. Blocks 1 to 4 show the possible usage of the bandpass filters in the front-end. Filter 1 and 2 in the receive path provide rejection of the undesired frequencies. Filter 3 and 4 and the power amplifier (PA) in the transmit path are used to filter the spurious components from the oscillator and the power amplifier. For instance, a carrier at 76 GHz generated from a 19 GHz oscillator using multipliers may contain undesired components which need to be filtered out.

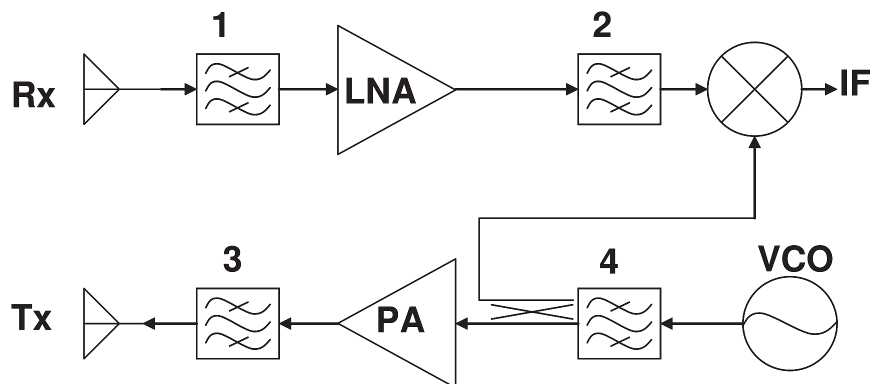


Figure 6.1: Block diagram of the millimeter-wave front-end of an automotive radar system.

At millimeter wave frequencies, distributed filters using transmission line res-

onators are preferable over lumped LC filters. The lumped inductors and capacitors usually have lower available Q-factors and the design strongly depends on the availability of accurate models at these frequencies. Transmission lines on the other hand, have the advantages that they have more scalable and accurate models, allow straightforward designs, and are easy to layout. Meanwhile, size becomes less an issue due to the small wavelengths at millimeter wave frequencies.

In the previous chapter, the thin film microstrip (TFMS) line resonators at 60 GHz with three viable configurations in a 0.18-μm CMOS have been investigated. It has been proven that using the top metal M6 for signal lines with a ground plane in the lowest metal layer M1 promises the highest unloaded Q-factor, which is around 15 for a 50 Ω line impedance.

6.2 Narrow Bandpass Filters

This section addresses the needs for narrow bandpass filters at millimeter wave frequencies, which have been rarely reported before this work. Filters with a narrow bandwidth of 5% at 50 GHz and 95 GHz were reported by using a Si-BCB (BenzoCycloButene) technology with reported insertion losses of 4.6 dB and 7 dB respectively [72]. As one of the earliest reported filters in standard CMOS process, in [69], a filter achieves a 2.7 dB insertion loss at 60 GHz, but is not very selective with a bandwidth exceeding 50%.

In this work, the narrow bandpass filters with a measured 3-dB bandwidth of 10% at 60 GHz and 77 GHz in a standard 0.18-μm CMOS technology are demonstrated. The loss mechanism in the narrow bandpass filters are examined with the assistance of EM simulators.

Design of Filters

The same technology with a layer configuration as shown in Fig. 5.2 is used for the filters. The design follows the Chebyshev filter theory. The first step is to determine the prototype element values g_i for lowpass filters. For example, a second-order Chebyshev filter with a 0.5-dB ripple and a cut-off frequency of 1 are given by: g_0=0, g_1=1.4029, g_2=0.7071, g_3=1.9841.

Secondly, using design equations (6.1a) to (6.1e) [73], the even-mode and odd-mode characteristic impedances (Z_{0ei} and Z_{0oi}) of the coupled transmission lines resonators for the jth section are determined for a target 0.5-dB fractional bandwidth (FBW) of 5% (j=1,2,3). It can be shown that for second-order Chebyshev filters, the 3-dB bandwidth is 1.39 times the 0.5-dB FBW, i.e., 6.9% .

$$\frac{J_{01}}{Y_0} = \sqrt{\frac{\pi}{2}\frac{FBW}{g_0 g_1}} \tag{6.1a}$$

$$\frac{J_{j,j+1}}{Y_0} = \frac{\pi FBW}{2}\sqrt{\frac{1}{g_j g_{j+1}}},\ (j = 1 \text{ to } n-1) \tag{6.1b}$$

$$\frac{J_{n,n+1}}{Y_0} = \sqrt{\frac{\pi}{2}\frac{FBW}{g_n g_{n+1}}} \tag{6.1c}$$

$$(Z_{0e})_{j,j+1} = \frac{1}{Y_0}\left[1 + \frac{J_{j,j+1}}{Y_0} + \left(\frac{J_{j,j+1}}{Y_0}\right)^2\right],\ (j = 0 \text{ to n}) \tag{6.1d}$$

$$(Z_{0o})_{j,j+1} = \frac{1}{Y_0}\left[1 - \frac{J_{j,j+1}}{Y_0} + \left(\frac{J_{j,j+1}}{Y_0}\right)^2\right],\ (j = 0 \text{ to n}) \tag{6.1e}$$

After that, Sonnet EM is used to construct a transformation map between Z_{0e}, Z_{0o} and the width W and spacing S of the coupled TFMS lines. Fig. 6.2 shows the structures of even- and odd-mode coupled-line resonators with push-pull ports.

The even and odd-mode characteristic impedances are obtained by $Z_{0e} = 2Z_c$ and $Z_{0o} = Z_c/2$. A transformation map from Z_{0e} and Z_{0o} to the W and S for a coupled-line resonator is shown in Fig. 6.3.

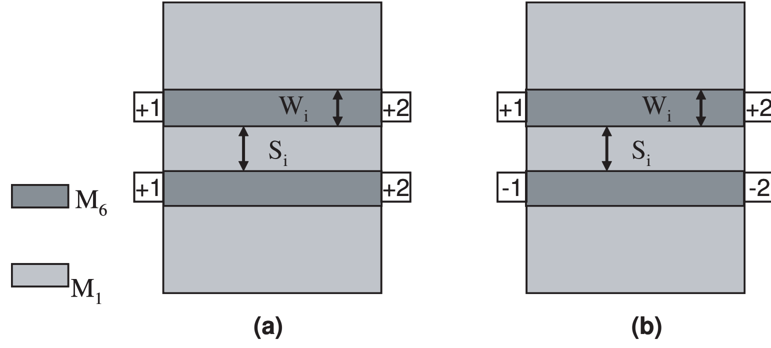


Figure 6.2: Structures of even- and odd-mode coupled lines simulated in Sonnet EM.

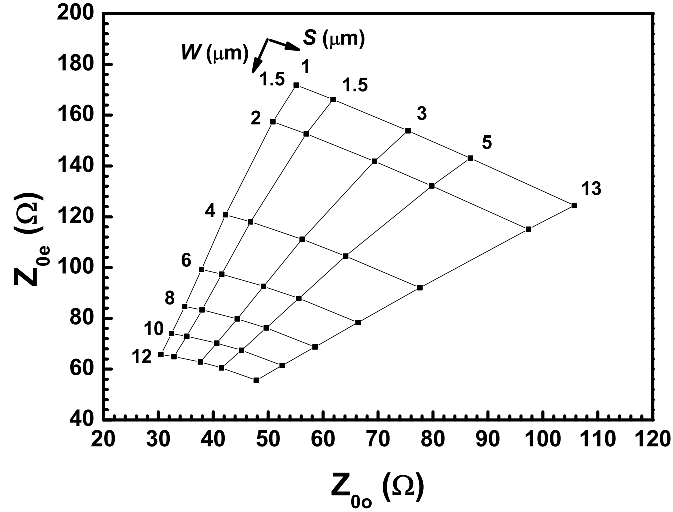
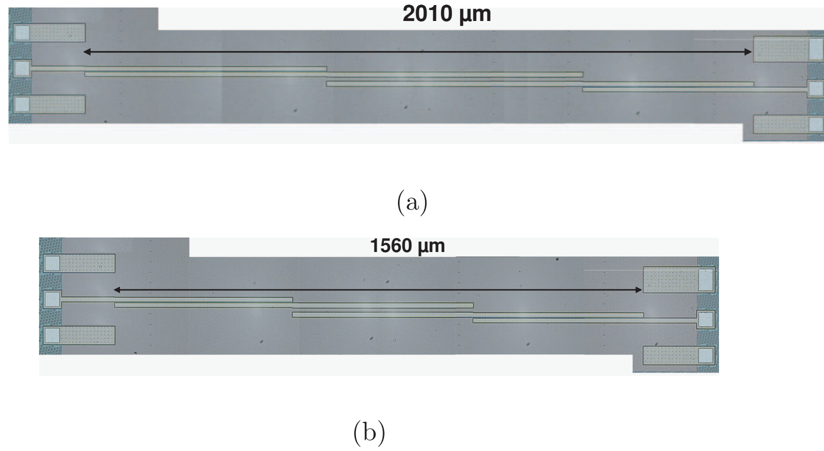


Figure 6.3: Transformation map between even-mode and odd-mode characteristic impedances (Z_{0e} and Z_{0o}) and layout parameters (width W and spacing S).

Next, using this map and Sonnet EM, the precise widths W and spacings S are determined such that the resultant Z_{0e} and Z_{0o} match the desired values. EM also predicts the ϵ_{eff} value to be around 3.5 for the coupled lines of interest. Finally, lengthsL_j are chosen to be $\lambda/4$ for each section of the filters at both frequencies. Table 6.1 lists the design and layout parameters for the coupled-line resonators.

6.2.1 Designed Structures

Two 2nd-order Chebyshev bandpass filters with a center frequency of 60 GHz and 77 GHz and targeted bandwidth of 5% were designed and manufactured as shown in Fig. 6.4.



(a)

(b)

Figure 6.4: Micrographs of the designed filters with a target fractional bandwidth of 5% at center frequencies of (a) 60 GHz and (b) 77 GHz.

6.2.2 Results

The measured responses of the filters are shown in Fig. 6.5 and Fig. 6.6 respectively. The 60 GHz filter exhibits a return loss of 11 dB and an insertion loss of

Table 6.1: Design Parameters for Inductors

j	$(Z0_e)_j$	$(Z0_i)_j$	W_j	S_j	L_j at 60 GHz	L_j at 77 GHz
	(Ω)	(Ω)	(μm)	(μm)	(μm)	(μm)
1	64.63	40.97	11.2	4	670	520
2	54.25	46.37	12.7	13	670	520
3	64.63	40.97	11.2	4	670	520

9.3 dB at the center frequency of 59.8 GHz with a 3-dB bandwidth of 6.2 GHz. The 77 GHz filter shows a return loss of 10 dB and an insertion loss of 9.3 dB at the center frequency of 76.8 GHz with a 3-dB bandwidth of 7.7 GHz.

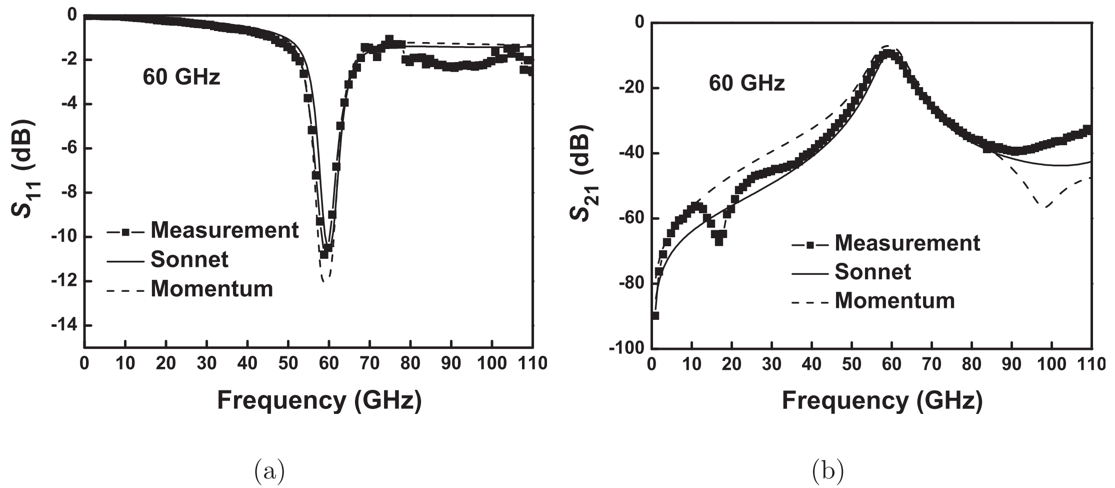


Figure 6.5: Measured and de-embedded data compared with simulation results using Sonnet EM and Agilent's Momentum for the 60-GHz bandpass filter. (a) Return loss. (b) Insertion loss.

The S-parameters are compared to the simulation results from Sonnet EM and Agilent's Momentum (version ADS2006A). Good agreement is observed between the experimental data and Sonnet EM and Momentum simulations for both filters.

6.2.3 Loss Analysis

For a coupled-line resonator filter, the insertion loss is due to dissipation loss and mismatch loss at the center frequency [74]. Mismatch loss can be neglected in a filter designed for a uniform reference impedance (50 Ω in our case). Therefore, the insertion loss is due to dissipation and it will be discussed in the following analysis. The loss tangent of SiO_2, the finite conductivity of M1 and M6 and the finite conductivity of the silicon all introduce dissipation losses, and thus affect the unloaded Q of the coupled-line resonators [74].

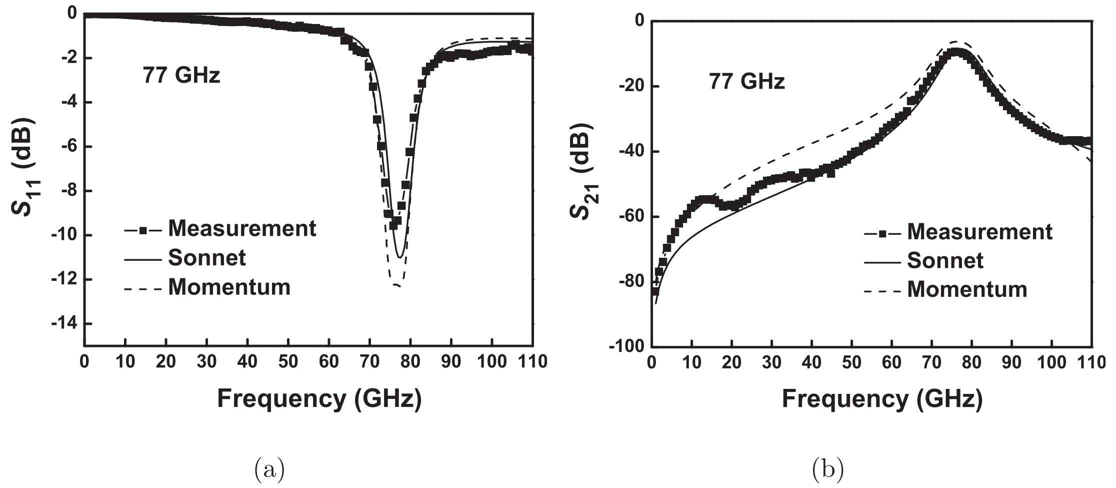


Figure 6.6: Measured and de-embedded data compared with simulation results using Sonnet EM and Agilent's Momentum for the 77-GHz bandpass filter. (a) Return loss. (b) Insertion loss.

To differentiate the dissipation losses, five filters are simulated in Sonnet EM. The cross-sectional view is shown in Fig. 6.7 and the respective insertion losses are shown in Fig. 6.8. The first structure (a) assumes the filter to be lossless and thus has an insertion loss of 0 dB. The second structure (b) includes the SiO_2 loss tangent, and introduces 0.7 dB loss. Including the lossy conductor M6 in the third structure (c) raises the insertion loss to 6.4 dB. In (d) the conductivity of M1 is included which increased the loss to 9.5 dB. Finally, in (e) the conductivity of the bulk silicon is included. The performance improves slightly since the substrate now contributes to the reduced losses in the return path. However, the improvement is minor.

The above result reveals the various loss contributions of the proposed filter structure. The lossy conductors in M6 and the non-ideal ground in M1 are the main reasons for power dissipation. Moreover, the dissipation losses increase the 3-dB bandwidths from 6.6% in (a) to 10% in (d) for both filters. This is also observed in Fig. 3 where the 3-dB bandwidth increases when losses increase. Also,

the ripples are obliterated due to the dissipative losses. The ideal 60 GHz filter has two frequency poles at 59.7 GHz and 61.7 GHz, whereas the 77 GHz filter has poles at 76.9 GHz and 79.4 GHz. The real filters for both show mono-pole responses.

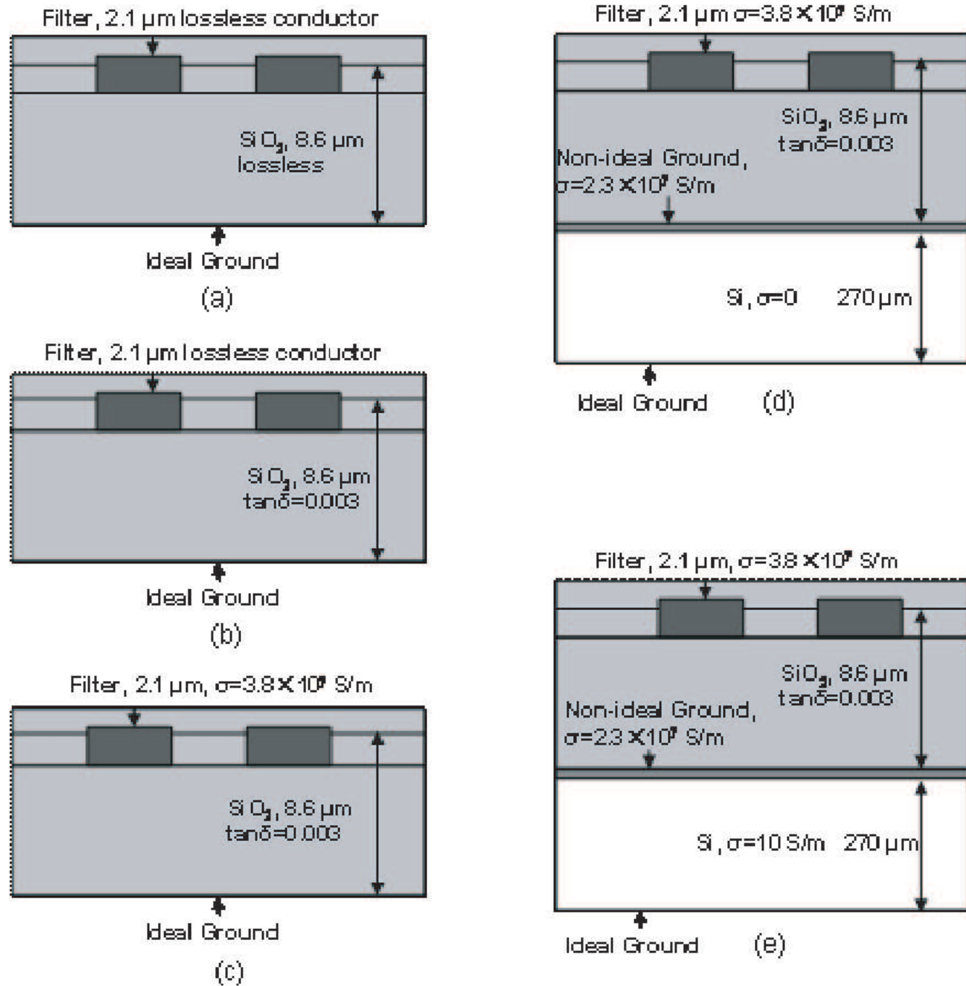


Figure 6.7: Loss analysis. (a) Non-dissipative filter. (b) Filter with lossy SiO_2 dielectric layer included. (c) Filter with lossy conductors in M6 included. (d) Filter with lossy ground plane in M1 and ideal silicon substrate. (e) Actual filter.

For comparison, Fig. 6.9 shows a plot of the insertion loss versus bandwidth for the reported millimeter-wave filters with bandwidths less than 20% in different technologies of MEMS, LTCC, Si-BCB, SiGe [72, 75–82]. Table 6.2 summarizes the performances of the presented filters, with comparison to previously published

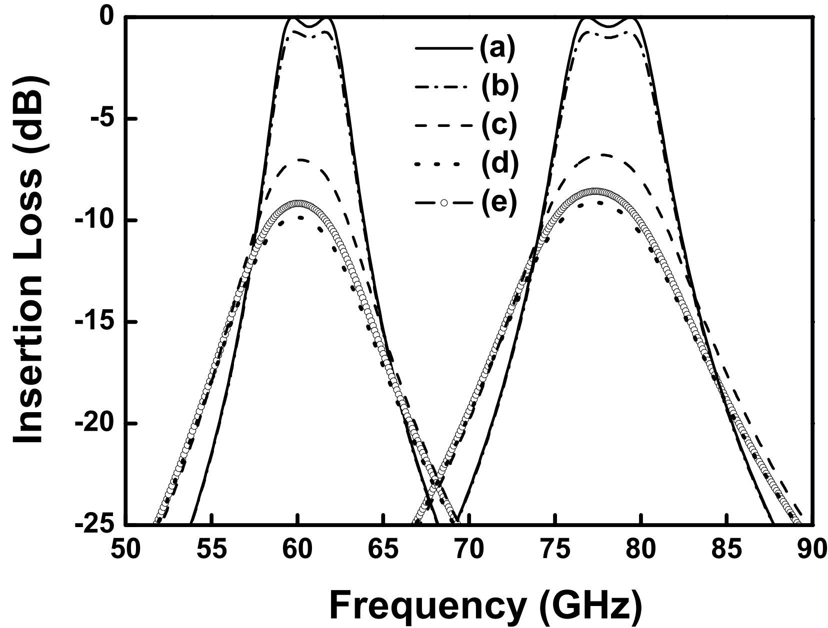


Figure 6.8: Simulated insertion losses of the five configurations in Fig. 6.7.

narrow bandpass filters.

The insertion loss of the CMOS filters is high due to the relatively low Q of the resonators ($Q_u \approx 15$). However, there is scope for improvement by making changes in the process technology. To assess the impact of using copper metallization instead of aluminum, the filters were simulated again with a typical copper alloy conductivity value of 4.4×10^7 S/m for M1 and M6. This leads to an improved insertion loss of 7.7 dB with a bandwidth of 9% at 60 GHz. This suggests the capability of standard CMOS (back-end with copper on all layers) to approach similar performance as GaAs with MEMS as reported in [80]. Other options include: increasing the SiO_2 thickness which leads to wider strips, increasing the thickness of M6 and M1, or compensating the losses by an additional amplifier.

Table 6.2: Performance Comparison of Previously Published Narrow Bandpass Filters and This Work

Ref.	Technology	f_c (GHz)	3-dB BW (%)	IL (dB)	Core Area (mm^2)
[75]	Si MEMS	60	8.0	1.5	22.8
[75]	Si MEMS	60	2.7	2.8	22.0
[75]	Si MEMS	60	4.3	3.4	26.0
[72]	Si-BCB	50	5.0	4.6	12.2
[72]	Si-BCB	94	5.0	7.0	3.90
[76]	LTCC	60	3.5	4.0	6.30
[77]	LTCC	60	16.7	1.5	4.58
[78]	LTCC	60	3.5	2.4	2.60
[79]	LTCC	60	2	3	4.24
[80]	LTCC	60	6.9	5.0	1.10
[80]	GaAs MEMS	60	10.0	6.8	-
[82]	SiGe:C	77	15.5	6.4	0.01
This work	0.18-μm CMOS	60	10	9.3	0.14
This work	0.18-μm CMOS	77	10	9.3	0.11

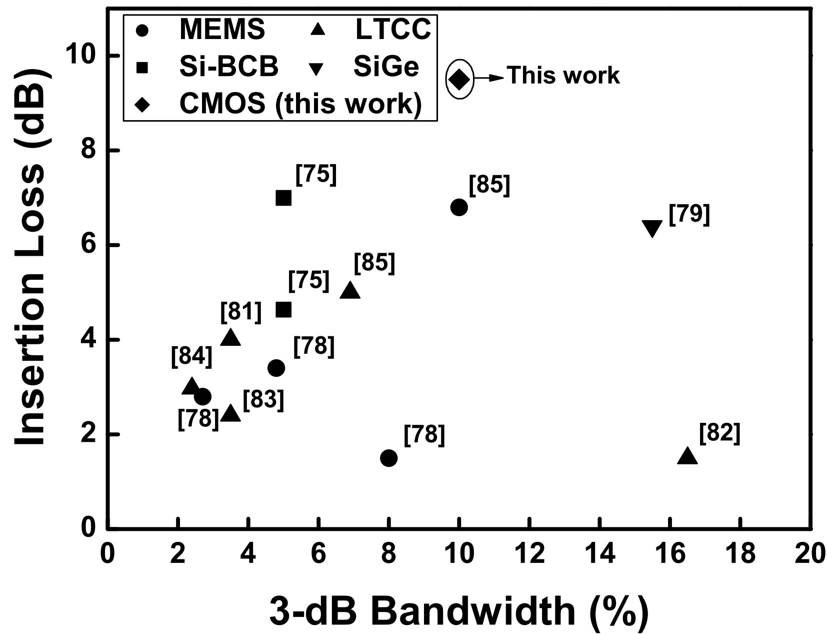


Figure 6.9: Insertion loss versus 3-dB bandwidth for reported millimeter-wave narrow bandpass filters in different technologies [75, 78-85].

6.3 Bandpass Filters with Small to Moderate Bandwidths

This section further shows the feasibility of millimeter wave bandpass filters with small to moderate bandwidths in standard CMOS. Since it is desirable to estimate the minimum achievable insertion loss of the bandpass filters for a given bandwidth in transceiver system designs, the relationship between the filter insertion loss and bandwidth must be determined. For this purpose, a systematic design and measurement of two group of 60 and 77 GHz coupled-line bandpass filters with measured bandwidths from 10% to 50% is demonstrated. The relationship between IL and BW is experimentally determined.

Table 6.3 lists the design parameters and the determined layout parameters for the filters. Wider bandpass filters require more coupling and thus smaller spacing. Note that, there are constraints on the implementation of wideband filters due to

Table 6.3: Design and layout parameters for the filters with various 0.5-dB FBWs

0.5-dB FBW (%)	3-dB BW (%)	$(Z_{0e})_{1,3}$ (Ω)	$(Z_{0o})_{1,3}$ (Ω)	$W_{1,3}$ (μm)	$S_{1,3}$ (μm)	$(Z_{0e})_2$ (Ω)	$(Z_{0o})_2$ (Ω)	W_2 (μm)	S_2 (μm)
5	7	64.63	40.97	11.2	4	54.25	46.37	12.7	13
10	14	72.33	38.87	9.8	2.3	59.13	43.36	12	6.4
20	28	84.86	37.54	7.8	1.4	70.75	39.20	10	2.5
30	42	95.77	37.82	6.3	1.1	84.85	37.54	7.9	1.4
40	56	105.86	38.93	5.3	1	101.44	38.36	5.8	1

the process rules, which allow a minimum line spacing of 1.5 μm for M6 layer. Hence, the fabricated filters for target FBWs larger than 20% are adjusted to the minimum possible spacing. EM also predicts the ϵ_r to be around 3.5 for the coupled lines of interest. Finally, lengths L_j of the coupled-line resonators are chosen to be $\lambda/4$=670 μm at 60 GHz, and 520 μm at 77 GHz.

The response of the narrow bandpass filter with a target FBW of 5% has been shown in Fig. 6.5. The responses of the remaining four filters with target FBWs ranging from 10% to 40% are shown in Fig. 6.10(a) to Fig. 6.10(d). Also shown in the figures are the simulated S-parameters using Sonnet's EM. A good agreement is observed between the simulation and measured results. Similar results are obtained for the 77 GHz filters.

Cohn approximated the center frequency insertion loss (IL) as follows [74]:

$$IL = \frac{4.343}{FBW} \sum_{i=1}^{n} \frac{g_i}{Q_{ui}} \ \text{(dB)} \ , \tag{6.2}$$

where Q_{ui} are the unloaded Q-factors of the ith resonator, and n is the order of the filter. This formula assumes small to moderate losses only, a condition which may be violated in CMOS processes. Therefore the relationship between IL and FBW must be validated experimentally. This paper presents this relationship through

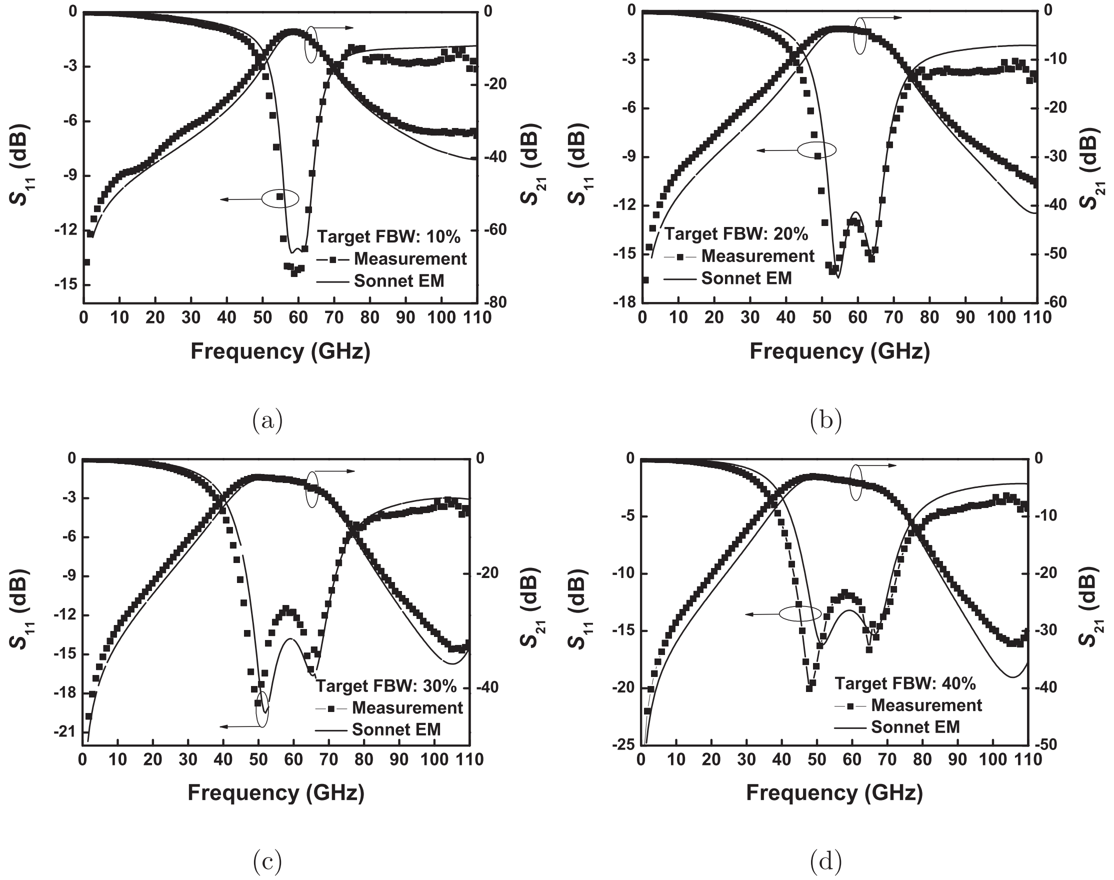


Figure 6.10: Measured and simulated responses of filters with target FBWs of 10% to 40% at 60 GHz.

measurements and compares it with Cohn's approximate formula.

Measured insertion losses for all the sample filters are plotted against the measured 3-dB bandwidths shown in Fig. 6.11. The measured 3-dB bandwidths increase slightly from the theoretical values for all fabricated filters, presumably due to the dissipative losses of the filters. The predicted center frequency insertion loss is shown as the dashed line using Cohn's formula in ([74]) using the unloaded Q-factors. The measured performance coincides well with Eq. (6.2). It can be seen that an insertion loss better than 3 dB is achievable for filters with a 3-dB bandwidth larger than 50%, but increases to 9 dB for a 3-dB bandwidth of 10%. The insertion loss, however, does not increase inverse proportionally with the decreasing bandwidth, due to the higher resonator Qui associated with narrower

bandwidth filters. The performance of filters reported in [69, 83, 84] implemented with similar technologies are also shown for comparison. It is noted that the filters in [83] are higher order filters and subsequently have higher losses.

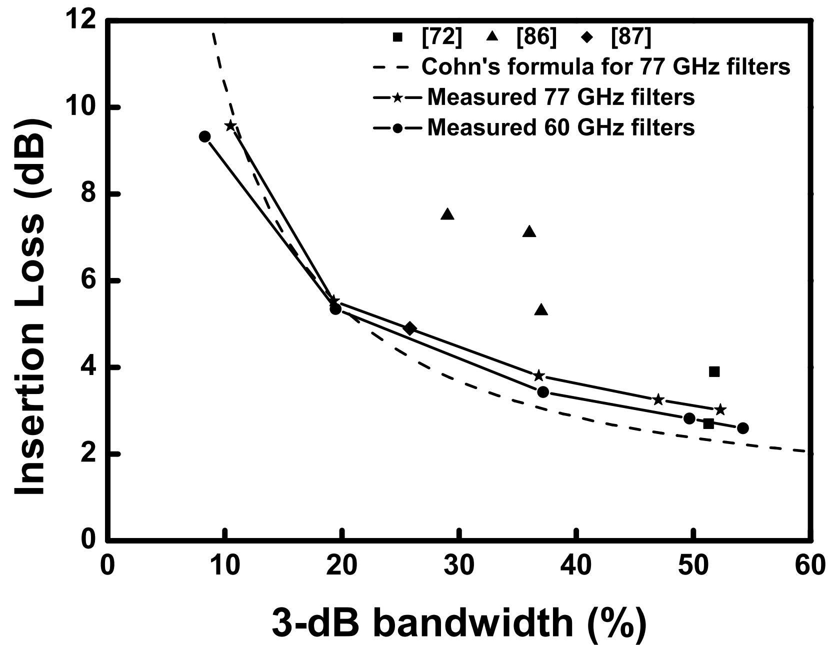


Figure 6.11: Insertion loss against 3-dB bandwidth for filters at 60 GHz. The theoretical relationship by Cohn's formula is shown. Measured data is compared with the performance of filters reported in [72, 86, 87].

6.4 Conclusions and Recommendations

This work demonstrates the potential of implementing millimeter-wave bandpass filters with narrow bandwidths and minimized insertion losses in a standard CMOS process without any post-processing steps. For a narrow bandpass filter with a bandwidth of 10% in the TFMS configuration in a standard 0.18-μm CMOS technology, the insertion loss is around 9.3 dB. The loss is mainly due to the lossy conductors in M6 and the non-ideal ground plane in M1. Back simulations indicate that, by using copper instead of aluminum, the TFMS filters in a standard

CMOS can achieve a similar insertion loss as in GaAs with MEMS. Further, a systematic design and implementation of filters with various bandwidths is shown. Some layout parameters of the wideband filters are constrained due to process limitations. The relationship between the insertion loss and the fractional bandwidth is established experimentally and largely coincides with Cohn's formula. Trade-offs thus can be made in the design of the 60 GHz and 77 GHz filters in CMOS.

CHAPTER 7

Conclusions and Recommendations

With the aggressive downscaling of the technology nodes, CMOS technology has become a promising candidate for integrating radio front-end circuits operating at microwave and millimeter wave frequencies. This has stimulated tremendous interest in developing high performance CMOS microwave and millimeter wave integrated circuits. For successful CMOS IC design, accurate models of the on-chip active and passive components are essential. Modeling efforts are needed to accommodate the trends in practical applications: smaller technology nodes, ever increasing data rate and higher operating frequencies.

In this thesis, the microwave noise performance of MOSFETs in a 65nm CMOS process has been characterized, the modeling of inductor to account for the influence of metal dummy fills inserted in advanced CMOS process is presented, and the design of resonators and filters at 60 GHz and 77 GHz in a standard CMOS process is demonstrated. The major contributions are:

- Development of a framework for microwave noise behavior characterization of MOSFETs, which allows a detailed quantification of the respective contributions of the noise sources in the MOSFETs. The way to de-embed a complex substrate network is also presented. The determination of the intrinsic noise sources facilitates the understanding and verification of the noise properties in short channel devices. The important parameters influencing the scaling of the noise figure with gate length are identified.

- Investigation of the influence of uniformly inserted floating metal dummy fills on the microwave performance of spiral inductors. A method is proposed for updating an existing inductor model fast and accurately by modifying the oxide capacitance analytically.

- Design of millimeter wave bandpass filters with narrow and wide bandwidths in a standard CMOS process without post-processing steps. Extension of the conventional microstrip line filter theory in standard CMOS by inserting a ground plane. Experimental establishment of the relationship between the center frequency insertion loss and bandwidth.

In this chapter, the main results and findings of the work are summarized and recommendations for further research work are discussed.

7.1 Measurements and De-embedding

Chapter 2 provides the basis for the experimental research carried out in this work. After the on-wafer calibration and measurements, de-embedding is a crucial step for obtaining accurate S-parameters and noise parameters of the DUTs. Various de-embedding methods are reviewed and compared with several sets of experiments which are categorized as three cases: S-parameter de-embedding for transmission lines, S-parameter de-embedding for source grounded transistors, and noise parameter de-embedding for source grounded transistors.

By using only one extra "thru" standard, the passive devices with identical interconnects and contact pads on the two ports can be accurately de-embedded up to tens of GHz. A modified model of the "thru" standard is proposed to account for the shunt parasitics of the interconnects. Measurement results of Case 1 show that the accuracy is improved significantly above 60 GHz. For reasons of accuracy, simplicity, and wafer-area efficiency, this method has been adopted for

experimental characterization of the two-port passive components and circuits in this thesis.

For transistors with the source connected to ground, the effects of the source ground legs must be considered, especially at higher frequencies. A "thru-short" method proposed as an alternative to the widely used "open-short" method is utilized to de-embed the transistors with source connected to ground. It enables the extraction of the effective resistance and inductance of the source ground legs. Due to the skin effect and inductive effect, the impedance of the source ground legs, which provide a negative feedback to the transistors, becomes more significant as frequency increases. Cases 2 and 3 demonstrate the effects of the source ground legs on the S-parameters and noise parameters respectively.

Since the components generally shrink in size and operate at higher frequencies with lower power, more difficulties will be faced in the accurate on-wafer measurements. Below suggestions for future research in de-embedding techniques are listed.

- From the aspect of saving wafer area for the extra standards and reducing the procedure complexity, the "thru" method is a promising method and may be extended to more applications. As shown in this work, by further incorporating the distributed effect of the interconnect in the "thru" model, the accuracy is improved above 60 GHz. This method could be further investigated for better understanding of the scaling factor k.

- Due to the distributed effects of the parasitics at higher frequencies, lumped-element based de-embedding method may have limitations as frequency further increases. Further efforts can be made to developing methods based on general network parameters.

7.2 Microwave Noise Modeling of MOSFETs

Chapter 3 presents the characterization of the microwave noise performance of the MOSFETs with scaled gate lengths based on experimental results. The noise analysis methodology for the extraction of intrinsic and extrinsic noise sources is demonstrated. It can be quantified that the noise from the intrinsic part of the MOSFET including the channel and gate oxide layer dominates the overall noise at lower frequencies while the contribution from the extrinsic noise, especially the gate resistance rapidly increases at higher frequencies. Thus the gate resistance, which is inversely proportional to the gate length, is the main concern in the extrinsic contribution in the downscaling.

Further analysis is performed for the intrinsic noise sources, i.e., the drain current noise and the gate current noise. Although the drain current noise is mostly determined by the drain current, smaller channels result in a larger drain current noise with the same drain current due to the various short channel effects, characterized by a larger excess drain thermal noise factor γ. Similarly, although the induced gate noise is generated by the coupling through a gate capacitance C_{gs} which is proportional to the gate length, the induced gate noise in smaller gate length MOSFETs does not scale down proportionally, characterized by an increased excess induced gate noise factor β. The reason for the raise in β is presumably due to the increased gate resistance which also impacts on the induced gate noise. Both the increase in γ and in β hinder the improvement of the intrinsic minimum noise figure, while the impact from the latter has an growing influence at higher frequencies based on a sensitivity study. The results highlight the importance of the gate resistance and induced gate noise in determining the overall minimum noise figure of the MOSFETs.

Future work is needed from the point of view of both process evolution and circuit applications. Below topics merit further research are listed.

- Currently, in the small-signal equivalent circuit parameter extraction, optimization is needed for part of the parameters. Methods to enhance the accurate determination of the parameters, especially the most critical ones, such as the gate resistance, are yet to be developed. More experimental data may be required. Measured data at higher frequencies and measurements for more bias conditions including the cold condition (zero drain bias) could be used for further verification.

- Experiments are needed to further verify the intrinsic noise components. For example, the low-frequency noise measurements specifically for the flicker noise and gate tunneling noise are preferred.

- Presently, the substrate noise modeling is not discussed in detail, since the contribution from the substrate is minor compared to noise from the intrinsic part and the gate resistance. However, it is shown that the importance of the substrate noise is also increasing as the frequency increases. Thus, further research efforts may be extended to the accurate modeling of substrate noise.

- These results should be applied to a low noise design for verification and illustration of their applicability.

7.3 Effects of Metal Dummy Fills

On-wafer inductors are one of the most crucial passive components in integrated circuits. The quality-factor of the inductors exerts direct impact on the behavior of circuits such as low-noise amplifiers, mixers, and oscillators. The problem investigated in chapter 4 of this thesis was triggered by the emerged requirement of inserting metal dummy fills in open areas all over the wafer. The influence of the metal dummy fills on the on-wafer inductors is characterized experimentally

through measuring fourteen pairs of inductor counterparts with and without metal dummy fills.

A lower quality-factor and a lower self-resonant frequency of the inductors are observed with metal dummy fills. A slight reduction of the series inductance of the inductor is found which may be attributed to the eddy current induced in the metal dummy fills inserted inside the inner turn of the inductors. However, the dominant factor has been found to be the increased oxide capacitance, which is caused by the effectively reduced physical thickness of the oxide layer between the spiral and the substrate due to the inserted metal dummy fills. The change in the oxide capacitance can be characterized by analytical formulas in terms of the density of the inserted metal dummy fills. It has been demonstrated that by updating the oxide capacitance values in the inductor models, the performance of inductors with metal dummy fills can be accurately predicted. This finding allows designers to quickly update the existing inductor models to account for the influences of the metal dummy fills. Further research could be extended in the directions proposed below:

- Research is still ongoing to more comprehensively understand the impact of the metal dummy fills and to suppress their impact. As recently reported in [85], the use of larger metal dummy fills and placing them more concentrated in the center open area of the spiral inductors instead of a uniform insertion underneath the inductors can reduce the degradation of the inductor quality factor.

  Other possibilities of coping with the metal dummy fills could be to connect them to the substrate, or to use interlaced metal dummy fills in different layers.

- The investigation of the effects of metal dummy fills usually must be con-

ducted experimentally. However, a large number of sample and measurement points may be needed to achieve a more generalized conclusion. To enhance the efficiency of this approach, a more sophisticated design of experiment (DOE) needs to be developed.

7.4 Millimeter Wave Filters

Integrating millimeter wave systems in CMOS technology has been very challenging. Remarkable improvement of MOSFET RF performance has been achieved. However, the millimeter wave performance of the passives is still limited, due to the high losses in the finite conductivity conductors and the low resistivity silicon substrate. The research in this thesis exploits a TFMS technique by using a ground plane in the lowest metallization layer to reduce the substrate losses and demonstrates successful design of millimeter wave coupled line filters in a standard CMOS process.

Since multiple metalization layers in CMOS processes allow different options to construct the transmission lines, trade-offs can be made to reduce either the conductor losses or the dielectric losses by thickening the signal lines or maintaining the highest oxide thickness. The best option must be determined in terms of the lowest Q_u of $\lambda/4$ line resonators for the filter design. It is concluded that for millimeter wave applications, using only top metallization layer as the signal line is the best option for the 0.18-μm CMOS technology.

Further, bandpass filters at 60 GHz and 77 GHz are designed and implemented in a 0.18-μm CMOS technology using the studied TFMS lines. Measured 3-dB bandwidths ranging from 10% to 60% are achieved. Narrow bandpass filters suffer from a high insertion loss, which is mainly due to the conductor losses in M6. Simulation result of filters with copper as the metallization material in stead of aluminum, which is provided in the 0.18-μm CMOS process, shows to approach

similar performance as reported in GaAs technology. The relationship between the center frequency insertion loss and the 3-dB bandwidth for the on-chip filters is experimentally estabished and verified by theorectical prediction.

The results from this research have two implications. First, based on the given technology, trade-offs can be made in choosing the bandwidth of the bandpass filters in the transceiver systems. Secondly, better process options, such as higher conductivity metallizations and a thicker dioxide layer, are highly needed to enhance the capability of CMOS technology in the millimeter wave range.

Recommendations for further research efforts in CMOS millimeter wave bandpass filters are given below.

- The key to improve the performance of coupled-resonator filters is to have higher Q-factor resonators. This is particularly important for narrowband filters, where there is room for improvement of the insertion loss. Process development to fundamentally promote the quality-factor of CMOS technology at millimeter wave frequencies is highly needed.

- Design efforts can be made to identify better resonator topologies. For line resonators, one way could be to design the filters at a lower reference impedance than 50 Ω, which requires wider line widths associated with higher Q-factors. Other forms such as short-ended line resonators, open-loop or closed-loop ring resonators, need to be systematically investigated.

- Designing of wideband filters may be limited by the process limitations in the minimum line width and line spacing. Broadside coupled lines can be explored by using adjacent metallization layers for the coupled lines. However, there are disadvantages in this configuration too, because only the top metallization layer is made the thickest with the highest conductivity in conventional CMOS processes, while the other metallization layers have a much

lower conductivity. In addition, designing of filters with asymmetric coupled lines is more complex.

- In this work, conventional coupled-resonator filter synthesization techniques are based on a lossless filter prototype. In reality, due to the finite Q-factor of the resonators, a larger bandwidth is usually resulted. Moreover, the center-frequency insertion loss may obliterate the ripples of the prototype filters. In order to have more precise designs, synthesization techniques incorporating the effects of the Q-factor at the design stage need to be developed.

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