STUDY OF SAW RESONATOR BASED
BAND PASS DELTA-SIGMA MODULATORS

SUN WAI HOONG
(B. App. Sc.(Hon.), University of Toronto)

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Summary

This thesis explores the possibility of employing surface acoustic wave (SAW) resonators in delta-sigma modulators. Delta-sigma modulators employing SAW resonators promise digitization of signals with high selectivity at high frequencies. A fourth order band pass continuous time delta-sigma modulator employing SAW resonators with a centre frequency of 224.7 MHz was designed and implemented. The modulator was fabricated in 0.8um BYR technology. During testing, the fabricated modulator displayed clear noise shaping with two RLC resonators at a centre frequency of 1 MHz. It was later tested with a crystal resonator and a RLC resonator, also at a centre frequency of 1 MHz, as part of the devised testing strategy. Clear noise shaping was not observed in two separate testing sessions. It was then decided that the testing of the modulator would stop at this stage. The modulator was found to be highly sensitive to small changes in the capacitance of the compensation capacitor. Simulations performed support this observation. Future work could look into making the anti-resonance cancellation circuit more robust.
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List of Abbreviations

Abbreviations

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<th>Description</th>
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<td>ADC</td>
<td>Analog to digital converter</td>
</tr>
<tr>
<td>BP</td>
<td>Band pass</td>
</tr>
<tr>
<td>CT</td>
<td>Continuous time</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital to analog converter</td>
</tr>
<tr>
<td>DR</td>
<td>Dynamic range</td>
</tr>
<tr>
<td>DT</td>
<td>Discrete time</td>
</tr>
<tr>
<td>HRZ</td>
<td>Half-return to zero</td>
</tr>
<tr>
<td>IF</td>
<td>Intermediate frequency</td>
</tr>
<tr>
<td>LP</td>
<td>Low pass</td>
</tr>
<tr>
<td>MEMS</td>
<td>Microelectromechanical structures</td>
</tr>
<tr>
<td>NRZ</td>
<td>Non-return to zero</td>
</tr>
<tr>
<td>OSR</td>
<td>Over sampling rate</td>
</tr>
<tr>
<td>RF</td>
<td>Radio frequency</td>
</tr>
<tr>
<td>RMS</td>
<td>Root mean square</td>
</tr>
<tr>
<td>RZ</td>
<td>Return to zero</td>
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<tr>
<td>SAW</td>
<td>Surface acoustic wave</td>
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<tr>
<td>SNR</td>
<td>Signal to noise ratio</td>
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Symbols

\[ \Delta \Sigma \] Delta-sigma
Chapter 1 - Introduction

Radio frequency (RF) receivers are widely used in televisions, radios and cellular telephones. With the phenomenal popularity of cellular telephones in recent years, much money has been poured into research in universities and companies to reduce the size and power consumption of cellular telephones. The conventional receiver architecture, the superheterodyne receiver, introduced by Armstrong way back in 1918, is used in 98% of RF receivers (Abidi, 1995). Since then, other receiver architectures have been invented and proposed. The direct conversion (Abidi, 1995) and image-reject receiver (Abidi, 1995), (Razavi, 1997) are among the more common of these other receiver architectures. Universities and companies are continuously researching architectures that would offer a reduction in size and power consumption, to replace the superheterodyne receiver.

1.1 Motivation

The RF receiver consists basically of three parts, RF at the front end, intermediate frequency (IF) in the middle and the baseband portion at the back. This architecture is commonly referred to as the superheterodyne receiver. It is illustrated in Fig. 1.1.

![Superheterodyne receiver architecture](Galton, 2002)
It is widely used in communication systems worldwide because it has good dynamic range, high linearity and is very selective in terms of frequency. However, there are drawbacks to this architecture. It requires numerous analog filters and resonators, which take up a lot of circuit area. In addition, the many analog filtering and amplification stages consume a lot of power. This is because parasitics and the analog IF filters, which have low characteristic impedance need to be driven with large currents (Abidi, 1995).

To reduce power dissipation and total circuit area of the RF receiver, new receiver architectures are now being researched. A novel receiver architecture, the direct conversion receiver shown in Fig. 1.2, proposes that the IF portion be removed and the RF signal be directly converted to baseband signal.

Fig. 1.2 Direct conversion receiver architecture (Galton, 2002)

The removal of the IF portion eliminates the need for IF filters and amplifiers. This clearly reduces the power dissipation and circuit area of the RF receiver. However, this architecture faces several problems. It is highly sensitive to even order non-linearity, which can corrupt the baseband signal (Galton, 2002). Moreover, since the local...
oscillator frequency is in the same range as the RF signals, the local oscillator signal can potentially radiate out to other receivers and be down converted to baseband together with the desired RF signal (Galton, 2002). This would add noise to the baseband signal in the form of dc offset. Compounding this is the dc offset that results from circuit mismatches (Galton, 2002).

Another architecture proposes that the digitization of the signal be done at the IF stage. This architecture depicted in Fig. 1.3 is referred as a superheterodyne receiver with a band pass analog to digital converter (ADC). The digitization of the signal at the IF stage means that analog baseband filters and amplifiers would not be needed. Also, the demodulation of the signal from IF to baseband would be done digitally. This results in reduction in power dissipation and savings in circuit area for the RF receiver. This architecture is a compromise between the superheterodyne and the direct conversion receiver architecture. Although the reduction in power dissipation and circuit area is less than the direct conversion receiver architecture, this architecture is easier to implement.

![Fig. 1.3 Superheterodyne receiver architecture with a band pass ADC (Galton, 2002)]
To digitize the signal at the IF stage, the ADC would need to be operating at a higher frequency. It would also need to be a band pass ADC.

Most of the band pass delta-sigma ADCs reported up to date, are implemented in discrete time and use switched capacitors (Singor, 1995) (Bazarjani, 1998). However, they can operate only at low frequencies. Their maximum operating frequencies are limited by the bandwidth of the operational amplifier and the long time constants for the circuit waveforms to settle (page 11, Cherry, 1999). Large glitches, due to switching transients at the virtual ground nodes of the operational amplifiers and aliasing add to the problems of operating discrete time ADCs at high frequencies (Gregorian, 1986).

On the contrary, continuous time delta-sigma ADCs do not have all the problems above faced by discrete time delta-sigma ADCs. Their performance is however limited by low frequency selectivity (low Q) of LC resonators at high frequencies (Shoaei, 1995) (Gao, 1998).

This problem may be solved, by substituting LC resonators with mechanical resonators. Microelectromechanical structures (MEMS) resonators (Nguyen, 1999), surface acoustic wave (SAW) resonators (Ruppel, 1993) and crystal resonators (Vig, 2003) are some examples of mechanical resonators. They can have high frequency selectivity (high Q) and MEMS resonators, in particular, can be integrated with integrated circuits, hence reducing further the circuit area of the RF receiver.

This thesis examines the possibility of realizing a continuous time delta-sigma ADC employing SAW resonators. Its primary application is its use in the superheterodyne receiver with band pass ADC architecture. It can also be used in
applications that need digitization of signals at high operating speeds with high frequency selectivity.

1.2 Thesis Outline

This thesis is divided into 6 chapters. Chapter 1 explains the motivation of the research topic. It also outlines the thesis. Chapter 2 introduces the fundamentals of ADC, ADC modulators and delta-sigma ADC modulators. Reviews of previous work on delta-sigma ADC modulators are also contained in the chapter. Chapter 3 delves into the theory behind the design of the band pass continuous time delta-sigma ADC employing SAW resonators. The anti-resonance cancellation, a novel method used in the design, is discussed in this chapter. This chapter also looks at the system-level simulation of the design. Chapter 4 deals with circuit-level implementation of the design. Chapter 5 presents testing methods and results. Chapter 6, lastly, summarizes the research topic and suggests methods and improvements for future work.
Chapter 2 – Fundamentals and Development of ADC

This chapter introduces the basics of ADC. The operation of the ADC is examined and investigated. Parameters used in quantifying the performance of the ADC are also touched on. It tracks the evolution of the ADC and the improvements in performance in subsequent ADCs. The delta-sigma (ΔΣ) ADC is examined and the advantages of continuous time (CT) ADCs over discrete time (DT) ADCs are listed down. Lastly, previous papers on ΔΣ ADCs are discussed.

2.1 Ideal ADC

An ADC converts a continuous analog signal to discrete bits at a sampling frequency, $F_s$. This is illustrated in Fig. 2.1. The ideal relationship between the incoming signal $V_{in}$ and the discrete bits $b_{N-1}....b_1b_0$ is shown in equation (2.1). $\Delta$ is the amount represented by 1 unit of $b_0$, the least significant bit of the discrete output bits. The relationship between $\Delta$ and $V_{\text{ref}}$, the full value of $V_{in}$ is listed in equation (2.2).

$$V_{in} = (2^0 b_0 + 2^1 b_1 + \ldots + 2^{N-1} b_{N-1}) \Delta \pm V_e$$

(2.1)

where $-1/2 \Delta < V_e < 1/2 \Delta$

$$\Delta = \frac{V_{\text{ref}}}{2^N}, \text{ where } N \text{ = number of bits used in ADC}$$

(2.2)

E.g.

If a 1-bit ADC is implemented and $V_{\text{ref}} = 2$, then

$$\Delta = \frac{2}{2^1} = 1 \quad \text{and} \quad -0.5 < V_e < 0.5$$
Note that there is a maximum quantization error, $V_e$ of $1/2 \Delta$. Quantization error is inevitable and inherent in ADCs. The ADC samples the incoming signal at the sampling frequency, $F_s$ and assigns it to the nearest quantized level. This assignment of quantized level results in $V_e$. $F_s$ is determined by the maximum frequency of the incoming signal, $V_{in}$. It has to be at least twice the highest frequency component of $V_{in}$.

### 2.2 Quantization Error

Quantization error limits the performance of the ADC. It is important that quantization error is investigated and calculated since it has a large effect on the performance of the ADC. Therefore a model for quantization error is needed. Fig. 2.2 shows the circuit that derives a model for the quantization error.


\[ V_e = V_q - V_{in} \]

\[ \therefore V_q = V_{in} + V_e \] (2.3)

Equation (2.3) shows the relationship between \( V_{in} \) and its value after it is assigned a quantized level, \( V_q \). The difference between \( V_q \) and \( V_{in} \) is \( V_e \), which is referred to as quantization error or quantization noise. Equation (2.3) is obvious but extremely useful in the calculations of quantization errors in ADCs.

### 2.3 Root Mean Square value of \( V_e \)

One of the performance measures of ADC is signal to noise ratio (SNR). Finding the SNR of a particular ADC would require the root mean square (RMS) value of \( V_e \).

To find \( V_e \), a stochastic approach is employed. \( V_e \) is assumed to be evenly distributed between \( \pm \Delta/2 \) as depicted in Fig. 2.3. The calculations done to obtain \( V_{e_{\text{rms}}} \) is shown in equation (2.4).

![Fig. 2.3 Assumed probability density function for \( V_e \)](image)

\[
V_{e_{\text{rms}}} = \left[ \int_{-\infty}^{\infty} x^2 f_e(x) \, dx \right]^{1/2} = \frac{1}{\Delta} \left[ \int_{-\Delta/2}^{\Delta/2} x^2 \, dx \right]^{1/2} = \frac{\Delta}{\sqrt{12}} \] (2.4)
2.4 Nyquist-Rate ADCs

There are two main types of ADCs. They are Nyquist-rate and delta-sigma (ΔΣ) ADCs. Nyquist-rate ADCs sample the incoming signal at twice the frequency of the highest frequency component of the incoming signal. The advantage of Nyquist-rate ADCs is its low sampling rate. However, as will be shown later, this would result in lower SNR compared to ΔΣ ADCs.

2.4.1 SNR of Nyquist-Rate ADCs

SNR is defined in equation (2.5) below,

\[
\text{SNR} = 20 \log \left( \frac{V_{\text{in(rms)}}}{V_{\text{noise(rms)}}} \right)
\]  

(2.5)

A sinusoidal signal with a peak-to-peak value of \(V_{\text{ref}}\) is considered. The sinusoidal would have a negative peak of \(-V_{\text{ref}}/2\) and a positive peak of \(V_{\text{ref}}/2\). It would then have a rms value of \(V_{\text{ref}}/(2\sqrt{2})\).

\[
\text{SNR}_{\text{max}} = 20 \log \left( \frac{V_{\text{ref}}}{\sqrt{2} \cdot \frac{V_{\text{LSB}}}{\sqrt{12}}} \right) = 20 \log \left( \frac{V_{\text{ref}}}{2\sqrt{2} \cdot \frac{V_{\text{ref}}}{2^n \sqrt{12}}} \right) = 20 \log \left( \frac{2^n \sqrt{12}}{2\sqrt{2}} \right) = 20 \log \left( 2^n \frac{3}{\sqrt{2}} \right) = 20 \log 2^n + 20 \log \frac{3}{\sqrt{2}} = 6.02N + 1.76
\]  

(2.6)
Equation (2.6) indicates an improvement of 6dB for every bit added to the ADC. This agrees with our intuition where quantization error would decrease by one half for every bit added to the ADC. A decrease of one half in quantization error corresponds to a 6dB increase in SNR.

The SNR$_{\text{max}}$ derived above is the top limit for Nyquist-rate ADCs. To get better SNR$_{\text{max}}$ for a fix number of bits, something more needs to be done. Section 2.5 introduces the low pass (LP) $\Delta\Sigma$ ADC where SNR$_{\text{max}}$ is better than the SNR$_{\text{max}}$ derived above for Nyquist-rate ADCs for the same number of bits.

2.4.2 Dynamic Range

The performance of an ADC is also measured by its dynamic range (DR). To find the DR of an ADC, the SNR of the ADC is plotted against its input amplitude. The DR of the ADC is the range of input amplitudes that result in an SNR that is above zero.

2.5 LP $\Delta\Sigma$ ADCs

LP $\Delta\Sigma$ ADCs can improve the SNR$_{\text{max}}$ beyond the theoretical maximum limit derived above for Nyquist-Rate ADCs. It does so by spreading the quantization noise over a larger frequency range. They can be thought of exchanging bandwidth for better SNR. LP $\Delta\Sigma$ ADCs can be implemented with and without noise shaping. LP $\Delta\Sigma$ ADCs with noise shaping shapes the noise away from the spectrum of the signal, thus resulting in better SNR$_{\text{max}}$ than without noise shaping.
2.5.1 LP $\Delta \Sigma$ ADCs without Noise Shaping

LP $\Delta \Sigma$ ADCs without noise shaping is an improvement over Nyquist–rate ADCs. It improves on the $\text{SNR}_{\text{max}}$ by spreading the quantization noise over a larger frequency spectrum. Hence the higher the sampling frequency, the more the noise is spread over the frequency spectrum. This is the reason for the improvement in $\text{SNR}_{\text{max}}$ for LP $\Delta \Sigma$ ADCs without noise shaping over Nyquist-rate ADCs.

2.5.1.1 Noise Analysis of LP $\Delta \Sigma$ ADCs without Noise Shaping

The quantization error of the LP $\Delta \Sigma$ ADC is assumed to be white noise. This means that the quantization noise is spread evenly across $-F_s/2$ and $F_s/2$, where $F_s$ is the sampling frequency. This is illustrated in Fig. 2.4. In the previous section, it was found that $V_{e(mso)} = \Delta/\sqrt{12}$. Hence the noise power would be $\Delta^2/12$ and is the area under the spectral density graph as shown in equation (2.7). The height of the spectral density graph, $S_e(f)$ can be found using equation (2.8).

$$P_e = \int_{-F_s/2}^{F_s/2} S_e^2(f) \, df = h^2 F_s = \frac{\Delta^2}{12}$$  \hspace{1cm} (2.7)
\[ h = \frac{\Delta}{\sqrt[6]{12F_s}} \]  

(2.8)

2.5.1.2 SNR\textsubscript{max} of LP ΔΣ ADCs without Noise Shaping

Although the LP ΔΣ ADC is operating at \( F_s \), the signal of interest resides within the spectrum of \( F_o \). Hence the output of the LP ΔΣ ADC can be passed through a low pass filter, which band limits it to \( F_o \), and the signal of interest would not be affected. The noise above \( F_o \) would however be eliminated. This is depicted in Fig. 2.5.

![Fig. 2.5 ΔΣ ADC without noise shaping](image)

This reduces the power of the noise at the output of the LP ΔΣ ADC and increases the SNR. Hence the higher the sampling frequency, the better the SNR would be. It is of interest to know the improvement to the SNR, due to the higher sampling frequency. Below shows the calculations.

\[
P_{\text{e}(\text{after low pass filter})} = \int_{-F_o}^{F_o} S_e^2(f)df = h^2.2F_o = \frac{\Delta^2}{12F_s}.2F_o = \frac{\Delta^2 2F_o}{12 F_s} = \frac{\Delta^2}{12 \text{OSR}}
\]

Over Sampling Rate (OSR) = \( F_s/2F_o \)

For a sine wave with a peak to peak value of \( V_{\text{ref}} \).
\[ P_s = \left( \frac{V_{\text{ref}}}{2\sqrt{2}} \right)^2 = \frac{V_{\text{ref}}^2}{8} = \frac{\Delta^2 2^{2N}}{8} \]

Hence

\[ \text{SNR}_{\text{max}} = 10 \log \left( \frac{P_s}{P_s(\text{after low pass filter})} \right) = 10 \log \left( \frac{\Delta^2 2^{2N}}{8} \frac{8}{\Delta^2} \right) = 10 \log \left( \frac{3}{2} 2^{2N} \right) + 10 \log \text{OSR} \]

\[ = 6.02N + 1.76 + 10 \log(\text{OSR}) \quad (2.9) \]

From equation (2.9), doubling the OSR would result in a 3dB increase in \( \text{SNR}_{\text{max}} \), one half of the increase in \( \text{SNR}_{\text{max}} \) if an extra bit is added. The result above shows that \( \text{SNR}_{\text{max}} \) does not improve significantly with higher sampling rates. A better way has to be found.

### 2.5.2 LP \( \Delta \Sigma \) ADCs with Noise Shaping

In LP \( \Delta \Sigma \) ADCs without noise shaping, the quantization noise is assumed to be white, constant from \(-F_s/2 \) to \( F_s/2 \). Now, the performance of the LP \( \Delta \Sigma \) ADCs can be improved if the quantization noise is shaped away from the signal of interest and a filter is applied after that. The filter is to allow the signal of interest to pass through and reject all the other frequencies. This would significantly reduce the noise since the signal of interest would not have much noise, having had most of it shaped away into other frequencies that are not of interest.

The \( \text{SNR}_{\text{max}} \) of the LP \( \Delta \Sigma \) ADC with noise shaping depends very much on the order of the modulator. The higher the order of the modulator, the better the \( \text{SNR}_{\text{max}} \). The
SNR\textsubscript{max} for both the first and second order LP ΔΣ ADC with noise shaping would be derived below.

### 2.5.2.1 First Order LP ΔΣ ADC with Noise Shaping

A block diagram of a LP ΔΣ modulator is shown in Fig 2.6. The order of the LP ΔΣ modulator is determined by the order of the loop filter, H(z).

![Fig. 2.6 Block diagram of LP ΔΣ modulator](image)

A first order LP ΔΣ modulator would have a first order loop filter, while a second order LP ΔΣ modulator would have a second order loop filter and so on.

A common first order loop filter used is H(z) = 1/(z-1). The signal transfer function, S(z) and the noise transfer function, N(z) are given in equations (2.10) and (2.11) respectively.
SNR_{max} is listed in (2.12).

\[
SNR_{max} = 6.02N + 1.76 - 5.17 + 30 \log(OSR)
\]  \hfill (2.12)

Equation (2.12) shows that the SNR\(_{max}\) increases by 9dB with every doubling of the sampling frequency (Inose, 1963). This is an improvement over the 3dB increase witnessed in the LP ΔΣ ADC without noise shaping. The SNR\(_{max}\) can be further improved by increasing the order of the loop filter as shown in the next section.

2.5.2.2 Second Order LP ΔΣ ADC with Noise Shaping

A popular second order transfer function used in the loop filter of the ΔΣ modulator is shown in (2.13)

\[
H(z) = \frac{2z - 1}{(z - 1)^2}
\]  \hfill (2.13)

The signal transfer function, S(z) and the noise transfer function, N(z) are given below.
The SNR for a second order LP $\Delta \Sigma$ ADC with noise shaping improves 15dB with every doubling of the sampling frequency (2.5bits/octave) as shown in equation (2.14) (Inose, 1963). This is a significant improvement over the 9dB experienced by the first order LP $\Delta \Sigma$ ADC. It is expected that the SNR would improve further with increasing order of the LP $\Delta \Sigma$ modulator.

$$S(z) = \frac{H(z)}{1 + H(z)} = \frac{2z - 1}{(z - 1)^2} = \frac{2z - 1}{2z - 2 + 1 + 2z - 1} = \frac{2z - 1}{z^2}$$

$$N(z) = \frac{1}{1 + H(z)} = \frac{1}{1 + \frac{2z - 1}{(z - 1)^2}} = \frac{1}{z^2 - 2z + 1 + 2z - 1} = \frac{(z - 1)^2}{z^2} = (1 - z^{-1})^2$$

$$SNR_{max} = 6.02N + 1.76 \cdot 12.9 + 50\log(\text{OSR})$$  \hspace{1cm} (2.14)$$

The SNR for a second order LP $\Delta \Sigma$ ADC with noise shaping improves 15dB with every doubling of the sampling frequency (2.5bits/octave) as shown in equation (2.14) (Inose, 1963). This is a significant improvement over the 9dB experienced by the first order LP $\Delta \Sigma$ ADC. It is expected that the SNR would improve further with increasing order of the LP $\Delta \Sigma$ modulator.

### 2.5.3 Band Pass $\Delta \Sigma$ ADCs

Band pass (BP) $\Delta \Sigma$ ADCs are an extension of LP $\Delta \Sigma$ ADCs. LP $\Delta \Sigma$ ADCs employ low pass filters; hence they are effective for signals that are of low frequencies or near DC. BP $\Delta \Sigma$ ADCs on the other hand can pass a band of frequencies in the frequency spectrum and hence lend themselves to applications that involve modulation of signals, like radio and television transmission.
The transfer function of the loop filter of BP ΔΣ modulator can be derived from the loop filter of LP ΔΣ modulator. This is done by performing the substitution $z^{-1} \rightarrow -z^{-2}$. When applied to the previously introduced second order LP ΔΣ loop filter modulator transfer function, a fourth order BP ΔΣ modulator loop filter transfer function is obtained. This is shown in equation (2.15).

$$H(z) = \frac{2z-1}{(z-1)^2} = \frac{2z^{-1} - z^{-2}}{(1-z^{-1})^2} \xrightarrow{z^{-1} \rightarrow -z^{-2}} \frac{-2z^{-2} - z^{-4}}{(1+z^{-2})^2} = \frac{-(2z^{-2} + z^{-4})}{(z^{-2} + 1)^2} \quad (2.15)$$

The resulting fourth order BP ΔΣ ADC would have similar SNR$_{\text{max}}$ with its LP ΔΣ ADC counterpart. The BP ΔΣ ADC operating frequency (resonant frequency) would be a quarter of its sampling frequency.

### 2.6 Continuous Time ΔΣ ADCs

The previous sections on ΔΣ ADCs had the loop filters of the modulators in discrete time (DT). However, ΔΣ modulators can have their loop filters built in continuous time (CT). There are several possible advantages of having ΔΣ modulators implemented in CT. They are the following.

1) DT ΔΣ modulators typically employ switched capacitor circuits. The operating frequency of these circuits is limited by the bandwidth of the operational amplifier
and the settling time of circuit waveforms. Typically, several time constants are
needed for the circuit waveforms to settle. On the contrary, waveforms of CT ΔΣ
modulators vary continuously. The requirement on operational amplifiers’ bandwidth
is also lowered if any operational amplifier is used.

2) Switching transients result in the appearance of large glitches on the virtual ground
nodes of the operational amplifier in DT ΔΣ modulators. CT ΔΣ modulators do not
experience this problem. Large glitches can be kept away from the virtual ground
nodes of the operational amplifier.

3) Aliasing is a problem that is faced when working in the DT domain. Signals that are
a multiple of the sampling frequency cannot be differentiated (Gregorian, 1986).
Hence, DT ΔΣ modulators need an additional filter at the inputs to reject signals that
are above the sampling frequency. CT ΔΣ modulators, however, do not face the
phenomenon of aliasing. It can be shown that anti-aliasing is inherent in CT ΔΣ
modulators (page 11, Cherry, 1999).

2.7 Background on Previous Work

Inose, Yasuda and Murakami wrote the first paper on ΔΣ ADCs in 1962 (Inose,
1962). Inose and Yasuda went on to write a second paper on it in the following year,
which contains analysis of the first and second order CT ΔΣ ADC (Inose, 1963). In it, the
9dB and 15dB improvement for the respective modulators are derived.
Candy generated interest in ΔΣ ADCs with a paper on double integration DT ΔΣ ADC in 1985, more than twenty years after it first appeared (Candy, 1985). His paper is the first in deriving the relationship between DT and CT loop filters.

Koch and Heise followed up on Candy’s work by implementing a double integration CT ΔΣ ADC that operated at 15 MHz (Koch, 1986). It had a peak SNR of 77dB for an over sampling rate of 62.5.

Pearce and Baker were the first to write on BP ΔΣ ADCs in 1987 (Pearce, 1987). Schreier and Snelgrove further introduced it to a wider audience in a more popular journal (Schreier, 1989).

Thurston, Pearce and Hawksford paved the way for a systematic design methodology for CT ΔΣ modulators (Thurston, 1991). They introduced in 1991, the impulse-invariant transformation to derive the CT loop filter from the DT loop filter. However their method was not able to realize the equivalence between CT and DT ΔΣ modulators completely because of lack of controllability.

Shoaei and Snelgrove corrected that in 1994 (Shoaei, 1994). Their paper described the right method for impulse-invariant transformation and had full controllability to achieve the equivalence between DT and CT ΔΣ modulators.

Shoaei then attempted to build a 250 MHz fourth-order BP CT ΔΣ modulator, but high fabrication tolerances and the lack of common-mode feedback circuitry compromised the final performance of the design (Shoaei, 1996), (Shoaei, 1997).

Schreier and Snelgrove also described the method of impulse-invariant transformation for achieving equivalence between DT and CT ΔΣ modulators (Schreier, 1996). However, the problem was approached in a different manner from (Shoaei, 1996).
The modulator was represented in state-space in modulators (Schreier, 1996) while (Shoaei, 1996) represented it in pole-zero form.

A 3.6 MHz fourth order BP CT ΔΣ modulator was reported by Jayaraman, Asbeck, Nary, Beccue and Wang (Jayaraman, 1997). The modulator had a peak SNR of 41 dB and a dynamic range of 42dB at an OSR of 64.

Gao and Snelgrove designed and tested a 3.8 GHz second order BP CT ΔΣ modulator (Gao, 1997). The peak SNR and dynamic range was found to be 49 dB and 60dB respectively but at an incredibly high OSR of 10,000.

Gao, Cherry and Snelgrove reported a fourth order CT BP ΔΣ modulator that operated at an even higher frequency. A modulator that ran at 4 GHz was published (Gao, 1998). It had a peak SNR of 53 dB and a dynamic range of 62 dB at an OSR of 500.

Cherry and Snelgrove also came up with a fourth order BP ΔΣ modulator that operated at 4 GHz. (Cherry, 2000). It had a peak SNR of 37 dB and a dynamic range of 40 dB at an OSR of 100.

The above CT ΔΣ modulators are limited by low frequency selectivity (low Q) of LC resonators at high frequencies (Shoaei, 1995) (Gao, 1998). This would result in lower dynamic range and lower peak SNR for modulators operating at high frequencies.

SAW resonators have the potential to overcome this weakness of LC resonators. They have high selectivity (high Q) at high frequencies. CT ΔΣ modulators employing SAW resonators in their loop filters would in turn have higher dynamic range and higher $\text{SNR}_{\text{max}}$ at high frequencies.
Chapter 3 – Design of CT ΔΣ Modulator Employing SAW Resonators

The previous chapter has highlighted the advantages of a BP CT ΔΣ modulator employing SAW resonators. This chapter would examine the methods that were used to realize the modulator. They are the impulse invariant transformation, multi-feedback architecture and the anti-resonance cancellation. The electrical model of the SAW resonator is also introduced. System-level simulations of the modulator are included in this chapter. They were performed in Matlab and Cadence to verify the functionality and performance of the modulator.

3.1 Impulse Invariant Transformation

Design of the BP CT ΔΣ modulator employing SAW resonators begins with the selection of a DT ΔΣ modulator loop filter transfer function. A DT ΔΣ modulator loop filter transfer function is selected based on its order, which has a huge bearing on its SNR$_{\text{max}}$. Having selected a DT loop filter transfer function, the equivalent CT loop filter transfer function can then be derived. This is done through impulse-invariant transformation (Gardner, 1986).

Fig. 3.1 and Fig. 3.2 show a CT ΔΣ modulator and a DT ΔΣ modulator. They would be equivalent if they produce the same sequence of output bits. This situation is ensured when the inputs to the quantizers are made to be exactly the same at the sampling instances of both modulators.
If the initial conditions are the same, then the inputs to the quantizer, \( x(n) \) can be guaranteed to be the same if equation (3.1) is observed (Thurston, 1991).

\[
Z^{-1}\{\hat{H}(z)\} = L^{-1}\left\{\hat{R_D}(s)\hat{H}(s)\right\} \bigg|_{t=0T}\tag{3.1}
\]

where \( R_D(s) \) is the transfer function of the digital to analog converter (DAC)
or equation (3.2), in the time domain (Shoaei, 1996)

\[
h(n) = \left[ r_d(t) \ast \hat{h}(t) \right]_{t=nT_s} = \int_{-\infty}^{\infty} r_d(\tau) \hat{h}(t-\tau) d\tau \bigg|_{t=nT_s} \tag{3.2}
\]

Equations (3.1) and (3.2) are powerful and systematic tools to transform a DT ΔΣ modulator that has a certain noise shaping behaviour to a CT modulator that would have the same noise shaping behaviour. The DT ΔΣ modulator and the derived CT ΔΣ modulator are equivalent modulators. Notice that the derived CT ΔΣ modulator loop filter transfer function is dependent on the transfer function of the DAC. Hence the choice of DAC affects the derived CT ΔΣ modulator loop filter transfer function. The pulse shapes of non-return to zero (NRZ), return to zero (RZ) and half-return to zero DAC are given in Fig. 3.5. Tables for impulse invariant transformation on band pass loop filters are given in Appendix A.1 and A.2.

Fig. 3.5 Pulse shapes of NRZ, RZ and HRZ
3.2 Transfer Function of SAW Resonator

To use a SAW resonator in the loop filter of a BP CT ΔΣ modulator, an electrical model of the SAW resonator would need to be found. There are numerous electrical models of the SAW resonator. More complicated electrical models are good models for a wider range of frequencies. The electrical model shown in Fig. 3.6 is typically used for two port SAW resonators (Cavin, 1992). It models the SAW resonator well, in general and near the resonant frequency of the SAW resonator, particular.

![Fig. 3.6 Electrical model of SAW resonator](image)

The electrical model of the SAW resonator in Fig. 3.6 gives a second order numerator and a second order denominator in the transfer function. The transfer function is shown in equation (3.3)

\[
\frac{V_{out}}{V_{in}} = \frac{C_p}{C_2 + C_p} s^2 + \frac{C_p R_m}{L_m (C_2 + C_p)} s + \frac{(C_m + C_p)}{(C_2 + C_p) L_m C_m} \frac{1}{s^2 + \frac{R_m}{L_m} s + \frac{(C_m + C_2 + C_p)}{C_m} \frac{1}{L_m (C_2 + C_p)}}
\]  

(3.3)
The transfer function in (3.3) results in a resonance frequency given by (3.4)

\[ \omega \cdot = \frac{(C_m + C_2 + C_p)}{C_m L_m (C_2 + C_p)} \]  

(3.4)

It also indicates the presence of an anti-resonance peak. The anti-resonance frequency can be calculated from the expression in (3.5).

\[ \omega \cdot = \frac{C_m + C_p}{C_p L_m C_m} \]  

(3.5)

Fig. 3.7 shows the simulated frequency response of RFM’s R02108 SAW resonator with a centre frequency of 224.7 MHz. The resonance and anti-resonance peaks can be clearly seen and are very close to each other. The anti-resonance peak would prove to be an obstacle to the using of SAW resonators in BP CT ΔΣ modulators. This will be shown in section 3.3.
Fig. 3.7 Frequency response of 224.7 MHz RFM’s R02108 SAW resonator

### 3.3 Multi-Feedback Architecture and Anti-Resonance Cancellation

When electronic resonators are used to implement loop filters in CT ΔΣ modulators, the loop filter could be made to have the exact transfer function that would be needed. However, when SAW resonators are used to implement them, the transfer function of the loop filters takes on a rigid structure. SAW resonators have fixed transfer functions. This would be an obstacle to having SAW resonators in loop filters of CT ΔΣ modulators. Novel and state of the art techniques would need to be employed.
3.3.1 Design Methodology of CT ΔΣ Modulator

A BP DT ΔΣ modulator can be transformed to a BP CT ΔΣ modulator using impulse invariant transformation. Having done so, it needs to be realized. However, this proved to be a challenge. This sub-section would go through the design methodology of a BP CT ΔΣ modulator and hence in the process illustrate the obstacles that would have to be overcome and the methods used to overcome it.

The fourth order BP DT ΔΣ modulator with a loop filter transfer function shown in (3.6) is considered.

\[ H_{BP}(z) = \frac{2z^{-2} + z^{-4}}{(1 + z^{-2})^2} \]  

To realize the above DT ΔΣ modulator in CT, the architecture shown in Fig. 3.8 is proposed.

![Fig. 3.8 Fourth order BP CT ΔΣ modulator with one feedback path](image)
The CT $\Delta\Sigma$ architecture shown in Fig. 3.8 uses two BP loop filters. It has a non-return to zero (NRZ) DAC on its one feedback path, which is added to two different points on the forward path. They have different gains, $k_2$ and $k_4$. The transfer function “seen” from output bit to quantizer input for path 1 is

$$H_{path1}(z) = k_2 \frac{z-1}{z^2 + 1}, \tag{3.7}$$

while for path 2, the transfer function seen is

$$H_{path2}(z) = k_4 \frac{0.7854z^3 - 0.7854z^2 + 0.7854z - 0.7854}{(z^2 + 1)^2}. \tag{3.8}$$

The total transfer function seen due to both path 1 and path 2 would be

$$H_{path1}(z) + H_{path2}(z) = k_2 \frac{(z-1)(z^2 + 1)}{(z^2 + 1)^2} + k_4 \frac{0.7854z^3 - 0.7854z^2 + 0.7854z - 0.7854}{(z^2 + 1)^2} \tag{3.9}$$

To make the above open loop CT $\Delta\Sigma$ equivalent to $H_{BP}(z)$, equation (3.10) has to be satisfied.

$$H_{BP}(z) = H_{path1}(z) + H_{path2}(z) \tag{3.10}$$

However, with the above architecture, the equation above cannot be satisfied. This is because there are four numerator coefficients but only two tunable coefficients. The architecture in Fig. 3.8 suffers from a lack of controllability. A way has to be found
to add two more tunable coefficients, so that there would be four tunable coefficients to fully control the four numerator coefficients.

### 3.3.2 Multi-Feedback Architecture

Omar Shoie solved the lack of controllability problem by adding a second feedback path. It was first proposed in (Shoie, 1994) and (Shoie, 1995). The architecture in Fig. 3.9 solves the controllability problem and is called multi-feedback architecture.

![Fourth order BP CT ΔΣ modulator with second feedback path](image)

Fig. 3.9 Fourth order BP CT ΔΣ modulator with second feedback path

\[ H_{BP}(z) \] is again considered. Paths 1 and 3 have a NRZ DAC on their feedback paths. The transfer function seen from the output bit to the input of the quantizer for path 1 is
Path 3 on the other hand has a transfer function of

$$H_{path3} = k_{4NZ} \frac{0.7854z - 0.7854}{(z^2 + 1)^2}$$  \hspace{1cm} (3.12)$$

Path 2 and path 4 have a return to zero (RZ) DAC on their feedback path. For path 2, the transfer function seen from the output bit to the input for the quantizer is

$$H_{path2}(z) = k_{2RZ} \frac{0.2929z - 0.7071}{z^2 + 1}$$  \hspace{1cm} (3.13)$$

while path 4 has a transfer function of

$$H_{path4}(z) = k_{4RZ} \frac{0.5077z - 0.8330z^2 + 0.0476z + 0.2777}{(z^2 + 1)^2}$$  \hspace{1cm} (3.14)$$

To have the CT $\Delta\Sigma$ modulator equivalent to the DT $\Delta\Sigma$ modulator employing $H_{BP}(z)$ in its loop filter, the transfer functions of the four paths are added together and equated to $H_{BP}(z)$.

$$H_{BP}(z) = H_{path1}(z) + H_{path2}(z) + H_{path3}(z) + H_{path4}(z)$$
Equation (3.15) has four numerator coefficients and four tunable coefficients. Hence the open loop CT $\Delta\Sigma$ transfer function can be fully controlled. The CT $\Delta\Sigma$ modulator can be made equivalent to a DT $\Delta\Sigma$ modulator employing $H_{BP}(z)$ in its loop filter using multi-feedback architecture.

3.3.3 Anti-Resonance Cancellation

The transfer function of the SAW resonator has been found earlier to be of the form

\[
\frac{2z^2 + 1}{(z^2 + 1)^2} = k_{2NZ} \frac{(z - 1)(z^2 + 1)}{(z^2 + 1)^2} + k_{2RZ} \frac{(0.2929z - 0.7071)(z^2 + 1)}{(z^2 + 1)^2} + k_{4NZ} \frac{0.7854z^3 - 0.7854z^2 + 0.7854z + 0.7854}{(z^2 + 1)^2} + k_{4RZ} \frac{0.5077z^3 - 0.8330z^2 + 0.0476z + 0.2777}{(z^2 + 1)^2} \tag{3.15}
\]

Equation (3.15) has four numerator coefficients and four tunable coefficients. This form would introduce an additional numerator coefficient compared to the form of the band pass circuit, $A/(s^2 + \omega^2)$. With an additional numerator coefficient, the multi feedback architecture would suffer from a lack of controllability, since it would have one less tunable coefficient to fully control the open loop CT $\Delta\Sigma$ transfer function.
To be able to control the numerator coefficients fully, the number of coefficients in the numerator has to be reduced. This could be done if the order of the numerator is reduced from second order to lower orders. A method to achieve that was hence invented. It is named anti-resonance cancellation. The circuit is shown in Fig. 3.10.

With the anti-resonance cancellation network, the transfer function of the SAW resonator would be simplified to

\[
\frac{V_{out}}{V_{in}} = \frac{1}{s^2 + \frac{R_m}{L_m} s + \frac{1}{L_m \left( \frac{C_m + C_2 + C_p}{C_m} \right)}}
\] (3.17)

if \( VC_1/C_g = C_p/(C_2 + C_{in}) \)

The second order numerator in equation (3.17) has been reduced to a constant. This reduction in the numerator would allow the tunable coefficients to fully control the
numerator coefficients and hence also the open loop transfer function of the CT ΔΣ modulator. Fig. 3.11 shows the frequency response of RFM’s R02108 SAW resonator with a centre frequency of 224.7 MHz with the anti-resonance cancellation network. It clearly shows the elimination of the anti-resonance peak visible in Fig. 3.7.

![Graph showing frequency response](image)

**Fig. 3.11** Frequency response of 224.7 MHz RFM’s R02108 SAW resonator with anti-resonance cancellation network

### 3.4 Design of Fourth Order BP CT ΔΣ Modulator Employing SAW Resonators

The design of the fourth order BP CT ΔΣ modulator employing SAW resonators started with the selection of a second order LP DT ΔΣ loop filter transfer function. The transfer function of the double integration modulator was selected. It is shown in (3.18).
A BP DT ΔΣ modulator loop filter transfer function could be created from a LP DT ΔΣ modulator by performing the substitution \( z^{-1} \rightarrow -z^{-2} \). The resultant loop filter transfer function would be of twice the order of the loop filter transfer function of LP DT ΔΣ modulator. The BP DT ΔΣ modulator loop filter transfer function derived from the LP double integration modulator loop filter transfer function is shown in (3.19). Both modulators would have similar SNR_{\text{max}}

\[
H_{\text{LP}}(z) = \frac{-2z^{-1} + z^{-2}}{(1 - z^{-1})^2}
\] (3.18)

\[
H_{\text{fourth order}}(z) = \frac{2z^{-2} + z^{-4}}{(1 + z^{-2})^2}
\] (3.19)

The SAW resonator that would be used was RFM’s R02108 SAW resonator. It has a centre frequency of 224.7 MHz. Its transfer function is of the form

\[
H_{\text{SAW}}(s) = \frac{As^2 + Bs + C}{s^2 + Ds + E}
\] (3.20)

If the SAW resonator with the above transfer function is used in the loop filter, the numerator of the CT ΔΣ modulator could not be fully controlled since there would be more numerator coefficients than tunable coefficients. Hence, the order of the numerator of the SAW resonator needed to be reduced. The anti resonance cancellation circuit from
Fig 3.9 was used to achieve this goal. The resulting transfer function from the above mentioned method has a form of

\[ H_{\text{SAW\_res\_with\_anti\_res\_cancellation}} = G \frac{\omega_0^2}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \]

where \( G = \frac{1}{\omega_0^2 L_m (C_2 + C_p)} \)

With the reduced order of the numerator, the numerator of the BP CT \( \Delta \Sigma \) modulator could now be fully controlled. To have \( H_{\text{SAW\_res\_with\_anti\_res\_cancellation}} \) in the form as \( H(s) \) in appendix table A.1 and A.2, a gain of \( 1/G \) was added to cancel off the gain of \( G \) in the SAW resonator. \( 1/G \) is found to be around 1,400 in (3.21). The component values are taken from the data sheet of RFM’s R02108 in appendix D.1.

\[
\frac{1}{G} = \omega_0^2 L_m (C_2 + C_p) = (2\pi \times 224.7 \times 10^6)^2 259.222 \times 10^{-6} (0.5 + 2.3) \times 10^{-12}
\]

\[ = 1,446.76 \approx 1,400 \quad (3.21) \]

The multi-feedback architecture in Fig. 3.12 was proposed and would be used to realize the fourth order BP CT \( \Delta \Sigma \) modulator employing SAW resonators. It has a period delay in its feedback path and the two DACs that are used are HRZ DAC and RZ DAC. They were arbitrarily chosen from the three DACs in Fig. 3.5.

If the analysis in section 3.3.2 were to be performed on Fig.3.12, it would yield (3.22).
Matlab was used to solve the equation above. The Matlab code is listed in Appendix B.1. The tunable coefficients were found to be

\[
\frac{2z^2 + 1}{(z^2 + 1)^2} = k_{2HZ} \frac{(0.2929z + 0.7071)(z^2 + 1)}{(z^2 + 1)^2} + k_{2RZ} \frac{(0.7071z + 0.2929)(z^2 + 1)}{(z^2 + 1)^2} \\
+ k_{4HZ} \frac{0.2929z^3 + 0.7071z^2 + 0.2929z + 0.7071}{(z^2 + 1)^2} \\
+ k_{4RZ} \frac{0.1994z^3 + 1.1260z^2 + 0.6595z + 0.0152}{(z^2 + 1)^2}
\]

Matlab was used to solve the equation above. The Matlab code is listed in Appendix B.1. The tunable coefficients were found to be

\[k_{2HZ} = -1.0042\]
\[k_{2RZ} = 3.1408\]
\[k_{4HZ} = -1.0868\]
\[k_{4RZ} = 0.4502\]

As an exercise, HRZ DAC is replaced with NRZ DAC in Fig. 3.12 to illustrate the effect that the DACs have on (3.22). This would affect the calculated values of the tunable coefficients. With NRZ DAC in place of HRZ DAC, (3.22) would become

\[
\frac{2z^2 + 1}{(z^2 + 1)^2} = k_{2NZ} \frac{(z + 1)(z^2 + 1)}{(z^2 + 1)^2} + k_{2RZ} \frac{(0.7071z + 0.2929)(z^2 + 1)}{(z^2 + 1)^2} \\
+ k_{4NZ} \frac{0.2146z^3 + 1.7850z^2 + 1.7850z + 0.2146}{(z^2 + 1)^2} \\
+ k_{4RZ} \frac{0.1994z^3 + 1.1260z^2 + 0.6595z + 0.0152}{(z^2 + 1)^2}
\]
To calculate the new tunable coefficients, the Matlab code in Appendix B.1 was slightly modified. The modified Matlab code is given in Appendix B.2. The new tunable coefficients were found to be the following.

\[ k_{2NZ} = -1.0042 \]
\[ k_{2RZ} = 4.1450 \]
\[ k_{4NZ} = -1.0868 \]
\[ k_{4RZ} = 1.5369 \]

The exercise above has shown that the selection of DACs affects the calculated values of the tunable coefficients.

*Fig. 3.12 Fourth order BP CT ΔΣ modulator employing SAW resonators*
3.5 System-Level Simulation of Fourth Order BP CT ΔΣ Modulator Employing SAW Resonators

The fourth order BP CT ΔΣ modulator employing SAW resonators was simulated using Simulink, a graphical based simulator in Matlab. The structure of the modulator was created in Simulink, mostly with components that were readily available in the simulator. However, the simulator did not have a HRZ DAC and RZ DAC. Hence, two Matlab programs were written to simulate the respective DACs. HRZ DAC and RZ DAC Matlab programs are listed in Appendix B.3 and B.4 respectively. The loop filter transfer function is the result of gain, G being cancelled off by $1/G$ and Q of the SAW resonator being set to infinity. The equivalent BP DT ΔΣ modulator was also simulated and compared with the BP CT ΔΣ modulator.

A ΔΣ modulator shapes the noise from the frequency band of interest. Hence, to evaluate the performance of ΔΣ modulators, a frequency domain representation of the output bits of the modulator is needed. This was achieved in Matlab by using its “psd” command. The output bits of the modulator were represented and stored as +1 for logic high and −1 for a logic low. The number of output bits used was 16,384.

Fig. 3.13 shows the structure of the fourth order BP CT ΔΣ modulator employing SAW resonators created in Simulink. The equivalent fourth order BP DT ΔΣ modulator was also simulated so that its spectrum could be compared to the spectrum of the fourth order BP CT ΔΣ modulator employing SAW resonators. Fig 3.15 shows the structure for the BP DT ΔΣ modulator created in Simulink. The SNR was calculated for both CT and DT modulators. The Matlab code used for the calculation of the SNR is given in Appendix B.5.
3.5.1 Results

Fig 3.14 shows the output spectrum of the fourth order BP CT ΔΣ modulator employing SAW resonators with the sampling frequency, Fs normalized to 1. It displays clear evidence of noise shaping. The output spectrum of its equivalent DT modulator is shown in Fig. 3.16. The noise shaping behaviour near the signal’s frequency in the BP CT ΔΣ modulator and its DT equivalent modulator is quite similar.

Fig. 3.17 and Fig. 3.18 show the SNR vs. input signal amplitude plots for the fourth order BP CT ΔΣ employing SAW resonators and its DT equivalent. Peak SNR of the CT ΔΣ modulator was measured to be 69.4392 dB. Its dynamic range was estimated to be 87 dB. These values are close to the peak SNR and dynamic range for its DT equivalent. The fourth order BP DT ΔΣ modulator has a peak SNR of 70.4652 dB and a dynamic range of 82 dB.
Fig. 3.13 Fourth order BP CT ΔΣ modulator employing SAW resonators in Simulink
Fig. 3.14 Output spectrum of fourth order BP CT ΔΣ modulator employing SAW resonators
Fig. 3.15 Fourth order equivalent BP DT ΔΣ modulator in Simulink
Fig. 3.16 Output spectrum of equivalent fourth order BP DT $\Delta \Sigma$ modulator
Fig. 3.17 SNR vs. input signal amplitude for the fourth order BP CT ΔΣ modulator employing SAW resonators

Fig. 3.18 SNR vs. input signal amplitude for equivalent fourth order BP DT ΔΣ modulator
3.6 Circuit Simulation of Ideal Fourth Order BP CT ΔΣ Modulator Employing SAW Resonators

The fourth order BP CT ΔΣ modulator employing SAW resonators was simulated in Cadence. This was done to ensure that the modulator worked with an ideal electrical model of a SAW resonator with anti-resonance cancellation. In the Matlab simulation done previously, the SAW resonator with anti-resonance cancellation was represented in transfer function form. Hence, this simulation is a further extension of the Matlab simulation done earlier and a step closer to reality. Ideal operational amplifiers, D flip flops, AND gates and comparators were employed in this simulation. The Verilog-HDL codes of the ideal components are given in the Appendix C.1, C.2 and C.3. The schematic is shown in Fig. 3.19.

The SAW resonator that was used in the simulation had a centre frequency of 433.92 MHz. Although the centre frequency used in this simulation would be different from the centre frequency of the actual fourth order BP CT ΔΣ modulator employing SAW resonators, this would not affect the validity and the usefulness of the simulation as its objective was to observe whether noise shaping was still present. In addition, the values of the tunable coefficients would stay the same. The centre frequency of 433.92 MHz is also higher than the actual centre frequency of 224.7 MHz and the electrical components used had ideal frequency responses.

The spectrum was obtained by using the “calculator” function in cadence and applying “psd” on 4096 output bits from the modulator.
Fig. 3.19 Block diagram of ideal fourth order BP CT ΔΣ modulator employing SAW resonators in Cadence
3.6.1 Results

The spectrum is shown in Fig. 3.20. Noise shaping can be clearly seen near the frequency of interest. This shows that the modulator works with an electrical model of a SAW resonator with anti-resonance cancellation.

Fig. 3.20 Output spectrum of ideal fourth order BP CT ΔΣ modulator employing SAW resonators
3.7 Summary

The techniques that were employed to realize the modulator were introduced and analyzed. The electrical model of the SAW resonator was also investigated and simulated. With these, the ideal fourth order BP CT ΔΣ modulator employing SAW resonators was simulated in Matlab and Cadence. The simulation results displayed clear noise shaping and showed the concept to be viable. In the next chapter, the implementation of the fourth order BP CT ΔΣ employing SAW resonators would be looked at and analyzed.
Chapter 4 – Circuit Implementation

The previous chapter had confirmed the plausibility of employing SAW resonators in CT ΔΣ modulators. This chapter deals with the implementation of the fourth order BP CT ΔΣ modulator employing SAW resonators. An overview of the modulator is presented in the first section of the chapter. Then, the construction of each sub-system and circuits in the sub-system is shown, explored and examined. Circuit-level simulation of the complete modulator, both schematics and post-layout simulation are covered at the end of the chapter. The layout of the modulator is also included.

4.1 Fourth Order BP CT ΔΣ Modulator Employing SAW Resonators

Fig. 4.1 shows the block diagram of the fourth order BP CT ΔΣ modulator employing SAW resonators. This is depicted in more detail in Fig. 4.2 where the circuit blocks and connections are clearly illustrated. The modulator was designed for RFM’s R02108 SAW resonator, which has a centre frequency of 224.7MHz. The sampling frequency of the modulator is 898.8MHz.

The input signal goes to the adder and is added with the outputs of the DAC feedbacks. The output from the adder is then piped to the SAW resonator and the anti-resonance cancellation network represented as ARCN in Fig. 4.2. Subtraction of anti-resonance cancellation output from the output of the SAW resonator is done in the BiMOS differential amplifier. The BiMOS differential amplifier has a gain of 1.4. The next 3 differential amplifiers would provide a gain of 1,000 to the circuit with each differential amplifier having a gain of 10. Together with the BiMOS differential
amplifier, these amplifications would result in a total gain of 1,400. The operations above are repeated since this modulator is a fourth order CT ΔΣ.

After the second amplification of 1000, the signal goes to the differential amplifier and is amplified by 6. This is to normalize the signal, which was at the full scale amplitude of 50mV, (full scale amplitude of DAC feedback) to the full scale amplitude of 300mV (full scale amplitude of comparator). This is followed by the comparator, where the signal is sampled and quantized. After that, the signal goes to the output buffer. It also goes to the NRZ latch in the feedback path. The output buffer shields the load away from the rest of the modulator. The output of the modulator is taken at Vout.

While in the feedback path, the NRZ latch inflicts a delay of half a period on the signal. The signal then splits into two paths. The RZ latch on the bottom path creates a delay of another half a period for a total delay of one period. This path generates RZ pulses. The top path, with a NRZ latch and a RZ latch, forces a period delay on the signal for a total delay of one and a half periods. This path produces the HRZ pulses. The RZ and HRZ pulses are then fed to the four DAC feedbacks.

The DAC feedbacks would amplify the signal according to the calculated feedback coefficients. The outputs of the DAC feedbacks are then added to the points on the forward path indicated in Fig. 4.1 and Fig. 4.2.
Fig. 4.1 Block diagram of fourth order BP CT ΔΣ modulator employing SAW resonators
Fig. 4.2 Circuit blocks and connections of fourth order BP CT ΔΣ modulator employing SAW resonators
4.2 Comparator

The comparator samples and quantizes Vin. There are various ways to implement a comparator. Multi-stage comparators (Poujois, 1978), (Vittoz, 1985) or latched comparators (Yukawa, 1985) may be used to realize a fully-differential comparator with high resolution. A latched comparator, which consists of a preamplifier and two NRZ latches that are connected back to back, is used. This architecture allows the comparator to operate at a higher speed than a multi-stage architecture and with good resolution (page 318, Johns, 1997). In the next 2 sections, the structure and operation of the preamplifier and NRZ latch would be examined. This would be followed by an investigation on the operation of the comparator.

4.2.1 Preamplifier

The preamplifier circuit is shown in Fig. 4.3. It consists of a differential pair and two pairs of emitter followers. The emitter followers are placed at the front and at the back of the differential pair. The front pair of emitter followers serves as a buffer between the differential pair and the circuit before. Placing emitter followers after the differential pair has been found to improve the regeneration time of the comparator (page 146, Cherry, 1999). It would also eliminate clock feed through noise (Lee, 1992).

Fig. 4.4 shows the frequency response of the preamplifier. The preamplifier’s bandwidth was measured to be 2.44 Gigahertz, higher than the sampling frequency of 898.8 MHz. Its -3dB phase shift was found to be –70 degrees.
Ven, R3, R4 and R5 determine the gain of the preamplifier. The relationship of gain versus Ven for the preamplifier is shown in Fig. 4.5. The preamplifier was designed to have a gain of seven. This was achieved by biasing Ven at 1.35V.

Fig. 4.3 Schematic of preamplifier
Fig. 4.4 Frequency response of post-layout preamplifier

Fig. 4.5 Gain of preamplifier versus Ven from post layout simulation
4.2.2 NRZ Latch

The NRZ latch in Fig. 4.6 consists of a track and a latch section. Both sections consist of a differential pair that is switched by Vclk and Velkb. Ven controls the current flowing through the differential pair through transistor Q7. Emitter followers placed at the back of the latch serve as buffers between the latch and the next circuit.

When Vclk is high and Velkb is low, Q1 and Q2 would conduct the current generated in Q7. It would be in the tracking phase. The signal would be amplified and its output would be tracking its input. When Vclk goes low and Velkb goes high, Q3 and Q4 would turn on and Q1 and Q2 would stop conducting. It would enter the latching phase. During this phase, the outputs just before Vclk goes low are latched. The outputs are connected to the bases of Q3 and Q4 in a positive feedback manner. This would allow the outputs to be pushed to the full scale amplitude of the NRZ latch. The maximum full scale amplitude of the NRZ latch is determined using equation (4.1).

\[
I_{CQ7} = \frac{Ven - Vbe}{R_3} = \frac{1.35 - 0.85}{0.5k} = 1mA
\]

\[
V_{full\_scale} = R2 \times I_{CQ7} = 1mA \times 0.3k = 300mV
\]

(4.1)
4.2.3 Operation of Comparator

Fig. 4.7 shows the block diagram and clock configuration of the comparator.

Fig. 4.6 Schematic of NRZ latch

Fig. 4.7 Block diagram of comparator
The preamplifier amplifies the signal before the signal is sampled and latched. The insertion of a preamplifier into the comparator improves the regeneration time of the comparator. In addition, emitter followers after the preamplifiers eliminate clock feedthrough.

The amplified signal from the preamplifier then goes to the NRZ latch. When clk is low, the first differential pair is functioning. The comparator is in the track phase. When clk goes high and the comparator enters its latch phase, the second differential pair of the first NRZ latch and the first differential pair of the second NRZ latch starts conducting. The second differential pair of the first NRZ latch drives the signal to the full scale amplitude of the comparator. When clk goes low again, the second differential pair of the second NRZ latch takes over in latching the signal to the output from the second differential pair of the first NRZ latch. During this phase, the first differential pair of the first NRZ latch is conducting and tracks the input signal. The comparator is back in the track phase.

Fig. 4.8 depicts the simulated waveforms obtained from the comparator. It shows the comparator latching the signal to its output on the rising edge of the clock. The input just before the clock rises is sampled and latched.
Fig. 4.8 Waveforms from comparator
4.3 DAC RZ and DAC HRZ

DAC RZ and DAC HRZ are used to produce RZ and HRZ pulses respectively. Both are constructed from the NRZ latch and the RZ latch. The track and latch architecture used in the latches allow them to operate at high frequencies (page 318, Johns, 1997). In addition, the construction of DAC RZ and DAC HRZ are highly similar with minor differences. This reduces the effort that is needed in their layout. The NRZ latch has been discussed previously. In the next section, the RZ latch will be examined. The construction and operation of the DAC RZ and DAC HRZ will be studied in the subsequent sections.

4.3.1 RZ Latch

The RZ latch in Fig. 4.9, like the NRZ latch, also consists of a track and a latch section. The construction of the track section is similar to the NRZ latch. In the latch section, the transistors are diode connected. This is different from the NRZ latch where the transistors are connected in a positive feedback manner. The design of the latch section in the RZ latch forces the outputs to be the same during the latch phase. To test the operation of the RZ latch, an NRZ latch is placed before it as in Fig. 4.10. The circuit was simulated and its waveforms are laid out in Fig. 4.11. The input is sampled and latched on the rising edge of the clock. On the falling edge, the latch phase starts and the outputs are forced to the same value.
Fig. 4.9 Schematic of RZ latch

Vin → NRZ → RZ → Vout

clk_bar

inv → clk

Fig. 4.10 Test circuit for RZ latch
Fig. 4.11 Waveforms from RZ latch simulation
4.3.2 Operation of DAC RZ

A NRZ latch and a RZ latch make up the DAC RZ shown in Fig 4.12. Each latch would inflict a delay of half a period on Vin for a total delay of one period. The outputs would be latched on the falling edge of clk.

![Fig. 4.12 Block diagram of DAC RZ](image)

4.3.3 Operation of DAC HRZ

The DAC HRZ component illustrated in Fig. 4.13 consists of two NRZ latches and a RZ latch. Three latches would produce a total delay of one and a half periods. The outputs would be latched on the rising edge of clk. They would be forced to the same values when clk is low.

![Fig. 4.13 Block diagram of DAC HRZ](image)
4.4 Anti-Resonance Cancellation Circuit

The anti-resonance cancellation circuit consists of RFM’s R02108 SAW resonator, anti-resonance cancellation network and the BiMOS differential amplifier. This is the heart of the modulator and is essential to the proper functioning of it. The construction of the anti-resonance cancellation circuit has the anti-resonance cancellation network implemented off-chip. Having it off-chip would give more flexibility in the tuning of the anti-resonance cancellation circuit. Meanwhile, the subtraction is performed on-chip. It was felt that this would reduce its parasitic capacitance and improve its frequency response compared to it being performed off-chip. The next section looks at the BiMOS differential amplifier. The implementation and the operation of the anti-resonance cancellation circuit are investigated in the following section.

4.4.1 BiMOS Differential Amplifier

Fig. 4.14 shows the BiMOS differential amplifier. The BiMOS differential amplifier consists of a pair of identical BiMOS, M1 and M2 and a current source. The BiMOS differential amplifier is used because it has very large input impedance. Having very large input impedance is crucial in the functioning of the CT ΔΣ modulator employing SAW resonators. This is explained in the following section.

The frequency response of the BiMOS differential amplifier is given in Fig. 4.15. From it, the bandwidth of the BiMOS differential amplifier was found to be 6.81 Gigahertz and its corresponding phase shift was measured to be -69 degrees. Its bandwidth is much higher than the sampling frequency of 898.8 MHz.
Vbias, R1, R2, R3 and W/L ratio of MOS control the gain of the amplifier. Fig. 4.16 shows the graph of gain versus Vbias for the BiMOS differential amplifier. To achieve a gain of 1.4, a voltage of 1.35 had to be applied at Vbias.

Fig. 4.14 Schematic of BiMOS differential amplifier
Fig. 4.15 Frequency response of post-layout BiMOS differential amplifier

Fig. 4.16 DC gain of BiMOS differential amplifier versus Vbias from post-layout simulation
4.4.2 Operation of Anti-Resonance Cancellation Circuit

The anti-resonance cancellation circuit consists of RFM’s R02108 SAW resonator, capacitor Cg, variable capacitor VC1 and the BiMOS differential amplifier. The anti-resonance cancellation circuit is shown in Fig. 4.17.

Vin goes into the SAW resonator and the anti-resonance cancellation network. The anti-resonance cancellation network can be adjusted with VC1. This would change the cancellation conditions. The output of the anti-resonance cancellation network is subtracted from the output of the SAW resonator with the BiMOS differential amplifier, the subtractor. It is important that the subtractor has high input impedance. Low input impedance at the subtractor would affect the anti-resonance cancellation circuit adversely. This is because the derivation of the transfer function of the SAW resonator with anti-resonance cancellation is based on the assumption that the subtractor has infinite input impedance. This matter is addressed by using the BiMOS differential amplifier.
amplifier as the subtractor. The BiMOS differential amplifier has very large input impedance.
4.5 DAC Feedback

The DAC feedback in Fig. 4.18 controls the feedback coefficients, which is essential for the modulator to operate properly. Two emitter followers and two differential pairs make up the DAC Feedback. The emitter followers serve as a buffer for the circuit before, the RZ latch given in Fig. 4.9. Two differential pairs are needed to allow in phase amplification and out of phase (180 degrees phase shift) amplification. If in phase amplification is needed, then a voltage will be applied at Vkp while Vkn is grounded. However, if out of phase amplification is needed, then Vkp is grounded and a voltage is applied at Vkn. With this architecture, the feedback coefficients can be adjusted by tuning Vkp or Vkn. Magnitude of Vkp and Vkn determines the amplification level.

It was decided that the full scale amplitude of the DAC feedback would be 50mV. Previously in Chapter 3, the feedback coefficients were found to be the following for the fourth order BP CT ΔΣ modulator employing SAW resonators.

\[
\begin{align*}
  k_{2HZ} &= -1.0042, \quad k_{2RZ} = 3.1408 \\
  k_{4HZ} &= -1.0868, \quad k_{4RZ} = 0.4502
\end{align*}
\]

100Ω resistors were placed at the collectors of the differential pair to obtain the graph of peak to peak voltage of Vout (Vout-p-p) versus Vkp for DAC feedback illustrated in Fig. 4.18. The placing of 100Ω resistors at the collectors of the differential pair would become clear in section 4.6.2. From Fig. 4.19, the voltages that need to be applied to Vkp and Vkn to obtain the required feedback coefficients are found. They are the following.

\[
\begin{align*}
  V_{kn} - k_{2HZ} &= 1.33V, \quad V_{kp} - k_{2RZ} = 2.40V \\
  V_{kn} - k_{4HZ} &= 1.35V, \quad V_{kp} - k_{4RZ} = 1.00V
\end{align*}
\]
Fig. 4.18 Schematic of DAC feedback

Fig. 4.19 Vout-p versus Vkp from post-layout simulation of DAC feedback
4.6 Adder

The adder adds the outputs from the DAC feedbacks to the forward path. It is implemented with a current adder. The summed current is then translated to voltage with the pair of resistors from the differential amplifier. The differential amplifier also converts the input voltage to current. It was felt that a current adder was easier to implement than a voltage adder. It could be constructed from the differential amplifier that was used throughout the modulator circuit. The differential amplifier is investigated in the next section. The following section would examine the operation of the adder.

4.6.1 Differential Amplifier

Fig. 4.20 below shows the differential amplifier. It is used to amplify signals throughout the modulator. It is also used in the adder. The differential amplifier is simple but effective. It has a pair of transistors, Q1, Q2 and a current source. Vbias and R3 control the current generated in the current source.

The post layout frequency response of the differential amplifier is plotted in Fig. 4.21. The bandwidth and -3dB phase shift of the differential amplifier was found to be 4.66 Gigahertz and –64 degrees respectively. This bandwidth would be sufficient for the modulator, which has a sampling frequency of 898.8 MHz.

The differential amplifier is needed to produce gains of 1, 6 and 10. The Vbias voltages that are needed to produce these gains can be obtained from Fig. 4.22. Fig. 4.22 illustrates the relationship between the gain and Vbias of the differential amplifier. The values of Vbias for the above said gains are listed below.

Gain of 1 – Vbias = 0.875V
Gain of 6 - $V_{bias} = 1.30V$

Gain of 10 – $V_{bias} = 1.75V$

Fig. 4.20 Schematic of differential amplifier
Fig. 4.21 Frequency response of post-layout differential amplifier

Fig. 4.22 DC gain of differential amplifier versus Vbias from post-layout simulation
4.6.2 Operation of Adder

The adder is implemented with a differential amplifier. Fig. 4.23 shows the connections between the adder and the DAC feedbacks. The adder adds the signal on the forward path with the outputs from the DAC feedbacks in the feedback path. The gain for the signal on the forward path is set at one. DAC feedback converts the signal at its input to current. The current at full scale amplitude is 0.5mA. The adding of the signals takes place in the 100Ω resistors at the collectors of the differential amplifier. Voltage is generated when the current generated from the signal in the forward path combines with the current generated by the DAC feedbacks. The full scale amplitude of the DAC feedback is 50mV. Similarly, the full scale amplitude of the modulator is 50mV.

Fig. 4.23 Connections between DAC feedback and adder
4.7 Output Buffer

The output buffer circuit is shown in Fig. 4.24. It consists of a differential pair and a current source. The circuit is simple but it satisfies the requirements of an output buffer. It is used to shield the circuit from load capacitance. Without output buffer, the load capacitance could degrade the performance of the modulator. It should also have low output impedance. The output buffer has 4 resistors in parallel at the collector of the transistors. In the unlikely but possible scenario that the outputs are shorted to ground or another voltage, the power dissipation across each of the resistors would be reduced. Thus the possibility of the resistors being overheated would be lessened. Output buffers should have two important characteristics, large input impedance and small output impedance. The input impedance of the output buffer is calculated in (4.2) and output impedance shown in (4.3)

\[
R_{\text{in}} = 2r_x = \frac{2V_T (\beta + 1)}{I_E} = \frac{2(25mV)(100 + 1)}{0.75mA} = 6.73k \quad (4.2)
\]

while

\[
R_{\text{out}} = R_c = 50\Omega \quad (4.3)
\]

Fig. 4.25 shows the frequency response of the output buffer. Its bandwidth was estimated to be 3.49 Gigahertz. This is above the sampling frequency of the modulator. Its –3B phase shift was found to be –54 degrees.

The output buffer is needed to have a gain of one. From Fig. 4.26, a Vbias of 1.6V would result in a gain of one for the output buffer.
Fig. 4.24 Schematic of output buffer

Fig. 4.25 Frequency response of post-layout output buffer
Fig. 4.26 DC gain of output buffer versus Vbias from post-layout simulation
4.8 Emitter Follower

The emitter follower shown in Fig. 4.27 is used as a buffer in the circuit. Emitter followers have high input impedances and low output impedances and hence are good devices to put after components that are sensitive to low input impedance or before components that demand low output impedance. The current passing through the emitter is shown in (4.4)

\[
I_E = \frac{V_{cm} - V_{be}}{R_E} = \frac{4 - 0.85}{1k} = 3.15mA
\]  

The input impedance of the emitter follower is calculated in (4.5)

\[
R_{in} = r_\pi + (\beta + 1)R_E = \frac{(\beta + 1)V_T}{I_E} + (\beta + 1)R_E = \frac{(100 + 1)25mV}{3.15mA} + (100 + 1)1k = 101.8k
\]  

\(\beta\) is assumed to be 100

while the output impedance of the emitter follower is found in (4.6)

\[
R_{out} = R_E || \frac{r_\pi}{\beta + 1} \approx \frac{r_\pi}{\beta + 1} = \frac{V_T}{I_B(\beta + 1)} = \frac{V_T}{I_E} = \frac{25mV}{3.15mA} = 7.9\Omega
\]  

The frequency response of the emitter follower is given in Fig. 4.28. Fig. 4.28 shows the bandwidth of the emitter follower to be 70.29 Gigahertz and its 3dB phase shift to be –24 degrees.
Fig. 4.27 Schematic of emitter follower

Fig. 4.28 Frequency response of post-layout emitter follower
4.9 Clock Circuit

Fig. 4.29 shows the on-chip clock circuit that is used to generate the signals clk and clk_bar. It consists of an emitter-coupled logic (ECL) inverter circuit depicted in Fig. 4.30 and emitter followers at the outputs of the clock circuit. The ECL architecture allows the clock circuit to operate at high frequencies. The emitter followers serve two purposes. They act as a buffer between the clock circuit and the circuits that the clock circuit drives. They also bring the signals clk and clk_bar down to the correct voltage level.

$V_{bias\_ECL}$ is biased at 1.35V. The peak to peak voltage of the clock signals ($V_{p-p\_clk}$) is derived below in (4.7).

$$I_{e_{Q1}} = \frac{V_{bias\_ECL} - V_{be}}{R4} = \frac{1.35 - 0.85}{0.5k} = 1mA$$

$$V_{p-p\_clk} = I_{e_{Q1}} \times R2 = 1mA \times 0.3k = 300mV$$  \hspace{1cm} (4.7)
Fig. 4.29 Block diagram of clock circuit

Fig. 4.30 Schematic of ECL inverter
4.10 Schematic Simulation

The complete circuit was simulated in Cadence. Spectre was used as the simulation engine. The simulation was run for 5us of simulation time and would, depending on workstation speed and load, need about 7 to 10 hours of real time. This would allow 4096 points to be used for the generation of the output spectrum of the fourth order BP CT ΔΣmodulator employing SAW resonators. The output spectrum was generated using the “calculator” function in Cadence. The command used is shown below.

\[
\text{psd(VT(“/Voutp”) - VT(“/Voutn”))}
\]

The points were taken from 443ns to 5us at an interval of 1.11259ns for a total of 4096 points.

Fig. 4.31 shows the output spectrum from the schematic simulation of the modulator. The frequency of the signal is at 224.7MHz. Noise shaping can be clearly seen at around the signal’s frequency.
Fig. 4.31 Output spectrum of fourth order BP CT ΔΣ modulator employing SAW resonators from schematic simulation
4.11 Layout

Layout was done using “layoutplus” tool from Cadence. The technology used for the chip was AMS 0.8um SiGe BYR.

4.11.1 Layout Considerations

1) Crosstalk

The signal in one track could interfere with the signal of another track that is close by, affecting the integrity of the signal. In a pair of long and parallel tracks, the effect of crosstalk is increased. This could be critical if the signal amplitudes in the tracks are small. This undesirable phenomenon could be reduced by putting ground or power tracks between long and parallel lines or between tracks with small amplitudes in their signals. Ground and power tracks are quiet and serve as a shield between the tracks. This technique could reduce crosstalk between tracks.

2) Noisy power supplies of digital circuits

Power supplies of digital circuits are relatively noisy. Digital circuits turn on and off frequently when they are operating and this introduces spikes in its supplies. If these noisy power supplies of digital circuits are also connected to analog circuits, they could introduce noise in the analog circuits and may lessen the accuracy of the analog circuits. This situation could be avoided by using different supplies for analog and digital circuits. In this way, noise in power supplies of digital circuits could be kept away from analog circuits.
3) Parasitic capacitance

Every track laid introduces parasitic capacitance to the circuit. Longer tracks would have more parasitic capacitance than shorter tracks. Parasitic capacitance in the circuit could be reduced by laying the layout in a compact manner. A compact layout could allow the modulator to operate at higher frequencies because of its lower parasitic capacitance.

4.11.2 Cells used in layout

The layout contains NPN bipolar junction and NMOS transistors. For both transistors, the cell layout from the software library was used. The cell layout for NPN bipolar junction was obtained from the NPN111 layout library while the layout for the NMOS device was picked from the NMOS layout library.

4.11.3 Characteristics and fabrication of chip

The layout of the modulator does not include the anti-resonance cancellation network. Having it off-chip would give more flexibility in the tuning of the anti-resonance cancellation circuit. The resonators are also off-chip resonators.

The chip was fabricated at CMP in Grenoble, France. The size of the die was 2400 um x 2460 um and has a total of 55 pads. A 68-pin ceramic quad flat pack (CQFJ68) was selected as the package for the die. The layout of the fourth order BP CT ΔΣ modulator employing SAW resonators is given in Fig. 4.32. Fig. 4.33 shows a microphotograph taken of the fourth order BP CT ΔΣ modulator employing SAW resonators.
Fig. 4.32 Layout of fourth order BP CT ΔΣ modulator employing SAW resonators
Fig. 4.33 Microphotograph of fourth order BP CT ΔΣ modulator employing SAW resonators
4.12 Post Layout Simulation

After the layout of the circuit was completed, the parasitic resistance and capacitance of the circuit was extracted and added onto the circuit for post layout simulation. The spectrum from the post layout simulation was obtained and is shown in Fig. 4.34. The signal’s spectrum can be seen clearly at 224.7MHz. Noise shaping is still obtained at around the signal’s frequency despite the added parasitics.
Fig. 4.34 Output spectrum of fourth order BP CT $\Delta\Sigma$ modulator employing SAW resonator from post-layout simulation
4.13 Summary

This chapter had explored, analyzed and simulated the various of the sub-systems and circuits that made up the fourth order BP CT ΔΣ employing SAW resonators. Schematic and post-layout simulation of the complete modulator was performed. The simulations displayed clear noise shaping and confirmed the earlier conceptual simulations performed in Chapter 3. To ensure the functionality of the modulator, the modulator would be tested with RLC resonators at a low frequency. Once the functionality of the modulator is confirmed, one RLC resonator would be replaced with a crystal resonator and an anti-resonance cancellation network. The network would then be tuned to obtain noise shaping before the second RLC resonator is replaced like the first one. The second network would also be tuned to obtain noise shaping. If successful, the crystal resonators would be replaced with high frequency R02108 SAW resonators. The anti-resonance cancellation network would then be tuned to obtain noise shaping.
Chapter 5 - Testing

The testing of the fourth order BP CT ΔΣ modulator employing SAW resonators chip began with the testing of the components in the test circuit block of the chip. Of immediate concern was the functionality of the various components that made up the modulator and the modulator itself. The functionality of the various components was verified and the biasing voltages needed for the specified gains were obtained. This paved the way for the testing of the modulator at a low centre frequency.

5.1 Testing setup

Fig. 5.1 shows the setup used to test the fourth order BP CT ΔΣ modulator employing SAW resonators. There were two pairs of power supply lines. One pair of power supply was for analog supply while the other pair was for digital supply. Separation of analog and digital supplies would ensure that the noisy digital supplies would not affect the sensitive analog circuits. Reference voltages were used for a number of inputs. They were mainly for biasing pins that were used to control the gain of the component. Reference voltages were also used to control the feedback coefficients of the DAC Feedbacks, Vk**. A signal generator was used to generate the signals for Vinp and Vinn, the inputs to the fourth order BP CT ΔΣ modulator employing SAW resonators.
5.2 Testing strategy

A testing strategy was conceived. The modulator would be initially tested with RLC resonators at a low frequency. Testing would then progress to crystal resonators. Crystal resonators were used because they have characteristics that are similar to SAW resonators but are available at low centre frequencies. Finally, the modulator would be tested with SAW resonators. The steps in the testing strategy are elaborated further below.

1) Functional testing – To test the functionality of the ΔΣ modulator, 1 MHz RLC resonators were used in place of the anti-resonance cancellation circuits. This was to ensure that the modulator was functional.

2) Testing of Modulator with a 1 MHz Crystal Resonator with Anti-Resonance Cancellation Network and a 1 MHz RLC Resonator - When the functionality of the modulator is confirmed, one 1 MHz RLC resonator would be removed and replaced with a 1 MHz crystal resonator with anti-resonance cancellation network. This would have to be done because it would not be possible to vary two variable capacitors at the same time.

3) Testing of Modulator with two 1 MHz Crystal Resonator with Anti-Resonance Cancellation Network - When clear noise shaping is obtained after the tuning of the variable capacitor in one anti-resonance cancellation circuit, the other 1 MHz RLC resonator would be replaced with another 1 MHz crystal resonator with anti-
resonance cancellation network. The other variable capacitor would then be similarly tuned to obtain clear noise shaping.

4) Testing of Modulator with SAW resonators with anti-resonance cancellation network at high frequencies – After the modulator has been tested to work at low frequencies, the testing would then proceed to SAW resonators at high frequencies. This testing would follow the procedures outlined in the testing of the modulator with crystal resonators in steps 2) and 3).

![Diagram](image_url)  
**Fig. 5.1 Setup to test fourth order BP CT ΔΣ modulator employing SAW resonators**
5.3 Functional Testing

The modulator was tested with 1 MHz RLC resonator to test the functionality of the chip. The values were the following, \( R_m = 10\Omega \), \( L_m = 320\mu H \), \( C_m = 100\text{p} \) and \( C_2 = 100\text{n} \). The modulator was operated at a clock frequency of 4 MHz. Fig. 5.2 shows the spectrum output of the modulator with 1 MHz RLC resonators. The signal’s spectrum is at 1 MHz. Noise shaping near the signal’s frequency can be clearly seen in Fig. 5.2.

Fig. 5.2 Output spectrum of fourth order BP CT \( \Delta \Sigma \) modulator employing SAW resonators with 1 MHz RLC resonators
5.4 Testing of Modulator with a 1 MHz Crystal Resonator with Anti-Resonance Cancellation Network and a 1 MHz RLC Resonator

The modulator was tested with a 1 MHz crystal resonator with anti-resonance cancellation circuit and a 1 MHz RLC resonator. The modulator was operated at a clock frequency of 4 MHz. Fig. 5.3 shows the best possible spectrum output of the modulator with the above configuration. The signal’s spectrum could be seen at 1 MHz. However, no clear noise shaping could be seen.

Fig. 5.3 Output spectrum of fourth order BP CT ΔΣ modulator employing SAW resonators with 1 MHz crystal resonator and 1 MHz RLC resonator
The above configuration was attempted a second time to obtain clear noise shaping.

Fig. 5.4 Output spectrum of fourth order BP CT ΔΣ modulator employing SAW resonators with 1 MHz crystal resonator and 1 MHz RLC resonator: second attempt

Fig. 5.4 shows the best spectrum output that was obtainable from the modulator for the second attempt. Again, no clear noise shaping can be seen. It was then decided that the testing would stop at this stage since no clear noise shaping could be seen in two attempts.
5.5 Discussion

The fourth order BP CT ΔΣ modulator employing SAW resonators had a functioning circuit. With 1 MHz RLC resonators, clear noise shaping could be seen. One 1 MHz RLC resonator was then replaced with a 1 MHz crystal resonator with anti-resonance cancellation network. In two separate attempts, clear noise shaping could not be seen. The possible reasons for the above observations are:

1) high sensitivity of anti-resonance cancellation circuit

The anti-resonance cancellation circuit seems to be very sensitive to small variations in capacitance and minor external disturbances. The circuit was also found to be sensitive to minor external disturbances. It has been observed that the touching of the variable capacitor with a metal object would affect the output spectrum of the modulator.

Simulations were performed on the anti-resonance cancellation circuit to support the above observations. These simulations were done with RFM’s R02108 resonator that has a centre frequency of 224.7 MHz.

Fig. 5.5 shows the output spectrum of the fourth order BP CT ΔΣ modulator employing SAW resonators with VC1 = 2.3pF. Noise shaping can be clearly seen.
Fig. 5.5 Output spectrum of fourth order BP CT ΔΣ modulator employing SAW resonators from post-layout simulation with VC1 = 2.3 pF

Output spectrum of the fourth order BP CT ΔΣ modulator employing SAW resonators with VC1 = 2.35 pF is given in Fig. 5.6. Noise shaping disappears when VC1 is increased slightly from 2.3 pF to 2.35 pF. It also disappears when VC1 is decreased from 2.3 pF to 2.1 pF. The output spectrum of the fourth order BP CT ΔΣ modulator employing SAW resonators with VC1 = 2.1 pF is depicted in Fig. 5.7. The high sensitivity of the anti-resonance cancellation circuit observed in the testing of the modulator is also seen in the simulations. From the simulations, noise shaping disappears with small deviations of VC1 from 2.3 pF. This may be the reason behind the low repeatability of results experienced in the testing of the modulator. The small window for noise shaping could make optimal manual tuning of VC1 difficult.
Fig. 5.6 Output spectrum of fourth order BP CT ΔΣ modulator employing SAW resonators from post-layout simulation with VC1 = 2.35pF

Fig. 5.7 Output spectrum of fourth order BP CT ΔΣ modulator employing SAW resonators from post-layout simulation with VC1 = 2.1pF
2) precision of a manually adjusted variable capacitor

The attainment of optimal cancellation conditions is limited by the precision of the manually adjusted variable capacitor. The precision of a manually adjusted variable capacitor would undoubtedly be worse than the inherent precision of a variable capacitor since it would be extremely difficult to make small and minute adjustments of a variable capacitor employing manual means. The apparent high sensitivity of the anti-resonance cancellation circuit could have resulted in a very narrow range of capacitance for the variable capacitor to achieve optimal cancellation. This could be beyond the precision of a manually adjusted variable capacitor.

5.6 Summary

The fabricated fourth order BP CT ΔΣ modulator employing SAW resonators was tested. A testing strategy was defined. The functionality of the modulator was initially confirmed by testing the modulator with RLC resonators at a centre frequency of 1 MHz. Clear noise shaping could be seen at the output spectrum of the modulator. Having confirmed the functionality of the modulator, a 1 MHz RLC resonator was replaced with a 1 MHz crystal resonator with anti-resonance cancellation network. It was then tested on two separate occasions. On both occasions, clear noise shaping could not be seen. During the testing of the modulator, the anti-resonance cancellation circuit has been observed to be highly sensitive. Simulations performed on the anti-resonance cancellation circuit seem to support this observation. This may be the reason behind the difficulty in obtaining optimal tuning with the variable capacitor and the low repeatability of results experienced in the testing of the modulator.
Chapter 6 - Conclusion

In this chapter, a summary of the thesis and the conclusions that were arrived at are presented. It also looks at ways to improve the fourth order BP CT ΔΣ modulator employing SAW resonators in the future.

6.1 Conclusions

A fourth order BP CT ΔΣ modulator employing SAW resonators has been designed, implemented and tested. The CT loop filter transfer function was derived from the loop filter of the double integration DT ΔΣ modulator using impulse invariant transformation. Hence, the CT modulator would exhibit the same noise shaping characteristics as its DT counterpart. The anti-resonance cancellation circuit and Shoaei’s multi-feedback architecture were needed to realize the modulator. The structure modulator was simulated in Simulink of Matlab. It showed clear noise shaping. The modulator was implemented in 0.8um BYR technology. Clear noise shaping was seen in its post layout simulation. The functionality of the modulator chip was confirmed when its spectrum showed clear noise shaping with 1 MHz RLC resonators. A 1 MHz RLC resonator was later replaced with a 1 MHz crystal resonator and with anti-resonance cancellation network. It was then tested in two separate testing sessions to allow for another attempt for optimal tuning of the compensation capacitor, VC1. This was in response to the high sensitivity of the anti-resonance cancellation circuit observed in testing. On both occasions, clear noise shaping could not be seen. It was then decided that the testing of the modulator would stop at this stage. The possible reasons behind this observation were investigated in Chapter 5.
6.2 Future Work

Testing of the fourth order BP CT ΔΣ modulator employing SAW resonators has revealed possible weaknesses in the anti-resonance cancellation circuit. The anti-resonance cancellation circuit was found to be highly sensitive to small variations in capacitance and external disturbances. It makes optimal tuning of the variable capacitor difficult and results in low repeatability of results. Future work could look into making the anti-resonance cancellation circuit more robust.
References


Appendix
Appendix A

A.1 Impulse Invariant Transformation Table for Second Order Transfer Function

<table>
<thead>
<tr>
<th></th>
<th>( \frac{H(s)}{s^2 + \left( \frac{\pi}{2} \right)^2} )</th>
<th>( \frac{s \pi}{s^2 + \left( \frac{\pi}{2} \right)^2} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>NRZ</td>
<td>( \frac{z + 1}{z^2 + 1} )</td>
<td>( \frac{z - 1}{z^2 + 1} )</td>
</tr>
<tr>
<td>RZ</td>
<td>( \frac{0.7071z + 0.2929}{z^2 + 1} )</td>
<td>( \frac{0.2929z - 0.7071}{z^2 + 1} )</td>
</tr>
<tr>
<td>HRZ</td>
<td>( \frac{0.2929z + 0.7071}{z^2 + 1} )</td>
<td>( \frac{0.7071z - 0.2929}{z^2 + 1} )</td>
</tr>
</tbody>
</table>
### A.2 Impulse Invariant Transformation Table for Fourth Order Transfer Function

<table>
<thead>
<tr>
<th></th>
<th>( \left( \frac{\pi}{2} \right)^2 )</th>
<th>( \left( \frac{\pi}{2} \right)^2 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( H(s) )</td>
<td>( \left( \frac{\pi}{2} \right)^2 \left( s^2 + \left( \frac{\pi}{2} \right)^2 \right)^2 )</td>
<td>( \left( \frac{\pi}{2} \right)^2 \left( s^2 + \left( \frac{\pi}{2} \right)^2 \right)^2 )</td>
</tr>
<tr>
<td><strong>NRZ</strong></td>
<td>( 0.2146z^3 + 1.7850z^2 + 1.7850z + 0.2146 ) ( \frac{1}{(z^2 + 1)^2} )</td>
<td>( 0.7854z^3 - 0.7854z^2 + 0.7854z + 0.7854 ) ( \frac{1}{(z^2 + 1)^2} )</td>
</tr>
<tr>
<td><strong>RZ</strong></td>
<td>( 0.1994z^3 + 1.1260z^2 + 0.6595z + 0.0152 ) ( \frac{1}{(z^2 + 1)^2} )</td>
<td>( 0.5077z^3 - 0.8330z^2 + 0.0476z + 0.2777 ) ( \frac{1}{(z^2 + 1)^2} )</td>
</tr>
<tr>
<td><strong>HRZ</strong></td>
<td>( 0.2929z^3 + 0.7071z^2 + 0.2929z + 0.7071 ) ( \frac{1}{(z^2 + 1)^2} )</td>
<td>( 0.2777z^3 + 0.0476z^2 - 0.8330z + 0.5077 ) ( \frac{1}{(z^2 + 1)^2} )</td>
</tr>
</tbody>
</table>
Appendix B

B.1 Matlab Code for Calculation of Feedback Coefficients – HRZ and RZ DAC

Source: pages 40 and 41 from (Cherry, 1999)
Comments: Modified by Sun Wai Hoong for calculation of feedback coefficients for SAW-employing fourth order BP CT ΔΣ modulator.

```matlab
%Matlab for multifeedback modulators
w0=pi/2;

%Do 2\textsuperscript{nd}-order NRZ system
[a2,b2,c2,d2]=tf2ss([0 0 w0^2],[1 0 w0*w0]);
syc2=ss(a2,b2,c2,d2);
syd2n=c2d(syc2,1);

%Find RZ system
sysd2r=sysd2n;
syd2r.b=inv(syc2.a)*(expm(syc2.a)-expm(syc2.a*0.5))*syc2.b;

%Find HRZ system
sysd2h=sysd2n;
syd2h.b=inv(syc2.a)*(expm(syc2.a*0.5)-eye(size(syc2.a)))*syc2.b;

%Below: (z^2+1)/(z^2+1) for multiplying 2\textsuperscript{nd} order coeffs by
tf2=tf([1 0 1],[1 0 1],1);
tfd2n=tf(sysd2n)*tf2;
tfd2r=tf(sysd2r)*tf2;
tfd2h=tf(sysd2h)*tf2;

%Do 4\textsuperscript{th}-order NRZ system
[a4,b4,c4,d4]=tf2ss([0 0 0 0 w0^4],[1 0 2*w0*w0 0 w0^4]);
syc4=ss(a4,b4,c4,d4);
syd4n=c2d(syc4,1);

%Find RZ system
sysd4r=sysd4n;
syd4r.b=inv(syc4.a)*expm(syc4.a)-expm(syc4.a*0.5))*syc4.b;

%Find HRZ system
sysd4h=sysd4n;
syd4h.b=inv(syc4.a)*(expm(syc4.a*0.5)-eye(size(syc2.a)))*syc4.b;

%Find 4\textsuperscript{th} order transfer functions
tfd4n=tf(syd4n);
```
tf4r=tf(sysd4r);

%Create LHS matrix to solve—assume RZ and HRZ DACs
amat=zeros(4,4);
num=tf4r.num(:); amat(:,1)=num(2:5)';
num=tf2r.num(:); amat(:,1)=num(2:5)';
num=tf4h.num(:); amat(:,1)=num(2:5)';
num=tf2h.num(:); amat(:,1)=num(2:5)';

%Solve for feedback k’s to satisfy 2*z^2+1
kd=amat \ [2;0;1;0];
k4r=kd(1)
k2r=kd(2)
k4h=kd(3)
k2h=kd(4)
B.2 Matlab Code for Calculation of Feedback Coefficients – HRZ and NZ DAC

Source: pages 40 and 41 from (Cherry, 1999)
Comments: Modified by Sun Wai Hoong for calculation of feedback coefficients for SAW-employing fourth order BP CT ΔΣ modulator.

```matlab
w0=pi/2;

% Do 2nd-order NRZ system
[a2,b2,c2,d2]=tf2ss([0 0 w0^2],[1 0 w0*w0]);
syc2=ss(a2,b2,c2,d2);
syd2n=c2d(syc2,1);

% Find RZ system
sysd2r=sysd2n;
syd2r.b=inv(syc2.a)*(expm(syc2.a)-expm(syc2.a*0.5))*syc2.b;

% Find HRZ system
sysd2h=sysd2n;
syd2h.b=inv(syc2.a)*(expm(syc2.a*0.5)-eye(size(syc2.a)))*syc2.b;

% Below: (z^2+1)/(z^2+1) for multiplying 2nd order coeffs by
tf2=tf([1 0 1],[1 0 1],1);
tfd2n=tf(sysd2n)*tf2;
tfd2r=tf(sysd2r)*tf2;
tfd2h=tf(sysd2h)*tf2;

% Do 4th-order NRZ system
[a4,b4,c4,d4]=tf2ss([0 0 0 0 w0^4],[1 0 2*w0*w0 0 w0^4]);
syc4=ss(a4,b4,c4,d4);
syd4n=c2d(syc4,1);

% Find RZ system
sysd4r=sysd4n;
syd4r.b=inv(syc4.a)*expm(syc4.a)-expm(syc4.a*0.5))*syc4.b;

% Find HRZ system
sysd4h=sysd4n;
syd4h.b=inv(syc4.a)*(expm(syc4.a*0.5)-eye(size(syc2.a)))*syc4.b;

% Below: (z^2+1)/(z^2+1) for multiplying 4th order coeffs by
tf4n=tf(sysd4n);
tfd4r=tf(sysd4r);
```
tfd4h=\text{tf}(\text{sysd4h});

\text{%Create LHS matrix to solve—assume RZ and HRZ DACs}
amat=\text{zeros}(4,4);
num=\text{tfd4r.num}(:,1)=\text{num}(2:5)';
num=\text{tfd2r.num}(:,1)=\text{num}(2:5)';
num=\text{tfd4n.num}(:,1)=\text{num}(2:5)';
num=\text{tfd2n.num}(:,1)=\text{num}(2:5)';

\text{%Solve for feedback k’s to satisfy } 2*z^2+1
kd=amat \backslash [2;0;1;0];
k4r=kd(1)
k2r=kd(2)
k4n=kd(3)
k2n=kd(4)
B.3 Simulink Model for Half Return to Zero DAC

Source: Matlab
Comments: Modified by Sun Wai Hoong to simulate Half Return to Zero DAC in Simulink

function [sys,x0,str,ts] = mixedm(t,x,u,flag)
% MIXEDM An example integrator followed by unit delay M-file S-function
% Example M-file S-function implementing a hybrid system consisting
% of a continuous integrator (1/s) in series with a unit delay (1/z).
%
% See sfuntmpl.m for a general S-function template.
%
% See also SFUNTMPL.
%
% Copyright (c) 1990-1998 by The MathWorks, Inc. All Rights Reserved.
% $Revision: 1.24$

% Sampling period and offset for unit delay.
dperiod = 1;
doffset = 0;

switch flag

% Initialization

% Derivatives

% Update

% Output
% case 3
    sys = mdlOutputs(t,x,u,doffset,dperiod);

% Terminate
% case {1, 2, 4, 9}
    sys = [];
    % do nothing

otherwise
    error(['unhandled flag = ',num2str(flag)]);
end

% end mixedm

%===========================================================================
% mdlInitializeSizes
% Return the sizes, initial conditions, and sample times for the S-function.
%===========================================================================
% function [sys,x0,str,ts]=mdlInitializeSizes(dperiod,doffset)

sizes = simsizes;
sizes.NumContStates = 0;
sizes.NumDiscStates = 0;
sizes.NumOutputs  = 1;
sizes.NumInputs   = 1;
sizes.DirFeedthrough = 1;
sizes.NumSampleTimes = 1;

sys = simsizes(sizes);
x0  = [];
str = [];
ts  = [dperiod/2 0];
    % sample time

% end mdlInitializeSizes

%===========================================================================
% mdlDerivatives
% Compute derivatives for continuous states.
%===========================================================================
%
function sys=mdlDerivatives(t,x,u)

sys = u;

end mdlDerivatives

function sys=mdlUpdate(t,x,u,dperiod,doffset)

next discrete state is output of the integrator
if abs(round((t - doffset)/dperiod) - (t - doffset)/dperiod) < 1e-8
    sys = x(1);
else
    sys = [];
end

end mdlUpdate

function sys=mdlOutputs(t,x,u,doffset,dperiod)

Return output of the unit delay if we have a
sample hit within a tolerance of 1e-8. If we
don't have a sample hit then return [] indicating
that the output shouldn't change.
if (t - doffset)/dperiod - floor((t - doffset)/dperiod) < dperiod/2
    sys = 0;
else
    sys = u;
end

end mdlOutputs
B.4 Simulink Model for Return to Zero DAC

Source: Matlab
Comments: Modified by Sun Wai Hoong to simulate Return to Zero DAC in Simulink

function [sys,x0,str,ts] = mixedm(t,x,u,flag)
% MIXEDM An example integrator followed by unit delay M-file S-function
% Example M-file S-function implementing a hybrid system consisting
% of a continuous integrator (1/s) in series with a unit delay (1/z).
% See sfuntmpl.m for a general S-function template.
% See also SFUNTMPL.
% Copyright (c) 1990-1998 by The MathWorks, Inc. All Rights Reserved.
% $Revision: 1.24 $

%d Sampling period and offset for unit delay.
dperiod = 1;
doffset = 0;

switch flag
  % Initialization
  case 0
    [sys,x0,str,ts] = mdlInitializeSizes(dperiod,doffset);
  % Derivatives
  case 1
    sys = mdlDerivatives(t,x,u);
  % Update
  case 2,
    sys = mdlUpdate(t,x,u,dperiod,doffset);
  % Output
  case 3
sys=mdlOutputs(t,x,u,doffset,dperiod);

%%%%%%
% Terminate %
%%%%%%

case {1, 2, 4, 9}
sys = [];
% do nothing

otherwise
error(['unhandled flag = ',num2str(flag)]);
end

% end mixedm

%===========================================================================
% mdlInitializeSizes
% Return the sizes, initial conditions, and sample times for the S-function.
%===========================================================================

function [sys,x0,str,ts]=mdlInitializeSizes(dperiod,doffset)

sizes = simsizes;
sizes.NumContStates  = 0;
sizes.NumDiscStates  = 0;
sizes.NumOutputs     = 1;
sizes.NumInputs      = 1;
sizes.DirFeedthrough = 1;
sizes.NumSampleTimes = 1;

sys = simsizes(sizes);
x0  = [];
str = [];
ts  = [dperiod/2 0];
% sample time

% end mdlInitializeSizes

%===========================================================================
% mdlDerivatives
% Compute derivatives for continuous states.
%===========================================================================

%function sys=mdlDerivatives(t,x,u)
%sys = u;

% end mdlDerivatives

%
%===========================================================================
% mdlUpdate
% Handle discrete state updates, sample time hits, and major time step
% requirements.
%===========================================================================
%
%function sys=mdlUpdate(t,x,u,dperiod,doffset)

% next discrete state is output of the integrator
%if abs(round((t - doffset)/dperiod) - (t - doffset)/dperiod) < 1e-8
%  sys = x(1);
%else
%  sys = [];
%end

% end mdlUpdate

%
%===========================================================================
% mdlOutputs
% Return the output vector for the S-function
%===========================================================================
%
function sys=mdlOutputs(t,x,u,doffset,dperiod)

% Return output of the unit delay if we have a
% sample hit within a tolerance of 1e-8. If we
% don't have a sample hit then return [] indicating
% that the output shouldn't change.
if (t - doffset)/dperiod - floor((t - doffset)/dperiod) < dperiod/2
  sys = u;
else
  sys = 0;
end

% end mdlOutputs
B.5 Matlab Code for Calculation of SNR

Author: Wang Xiaofeng  

% --- Macro definition ---
% Receive the data from the work space  
% outsig is the output signal sequence of the modulator
outp=yout';
N = length(outp);
N=16384;
% N is the number of the samples; it should be power of 2.
OSR = 64;
% OSR is the oversampling ratio
BW = N/2/OSR;
% BW is the interest bandwidth
Fs = 1;
% Fs is the sampling frequency. It should be 1 after normalization.

BWbb = round(0.25*N-BW/2);
% BW beginning bin
BWeb = round(0.25*N+BW/2);
% BW ending bin
% --- Macro definition end ---

% --- Power spectrum calculation ---
w = hanning(N);
% Hanning windowing
[Pxx,f] = psd(outp,N,Fs,w,N/2);
% [magnitude,frequency] =
% (signal,sample number,sampling frequency,window,overlap number)
Pyy = Pxx*norm(w)^2/sum(w)^2*2;
% De-normalization of the hanning windowing
% --- Power spectrum calculation end ---

% --- SNR calculation ---
total_power = sum(Pyy(BWbb:BWeb));
% Total power of the interest bandwidth
[sigpw,fsigbintmp] = max(Pyy(BWbb:BWeb));
fsigbin = fsigbintmp + BWbb -1;
% Find the signal bin fsigbin

% Find the signal beginning bin
sbb = fsigbin;
while (Pyy(sbb-1) < Pyy(sbb)) & (sbb>BWbb);
    sbb = sbb-1;
end

% Find the signal ending bin
seb = fsigbin;
while (Pyy(seb+1) < Pyy(seb)) & (seb<BWeb);
    seb = seb+1;
end

% Calculate the total signal power
%signal_power = sigpw;
signal_power=sum(Pyy(sbb:seb));
% Calculate the total noise power
noise_power = total_power - sum(Pyy(sbb:seb)) + [Pyy(sbb-1)+Pyy(seb+1)]/2*(seb-sbb);
% Calculate the SNR
SNR = 10*log10(signal_power/noise_power)
% --- SNR calculation end ---

% (The end)
% -----------------------------
Appendix C

C.1 Verilog HDL Code for “And” Gate

// Verilog HDL for “VerilogLib”, “and2” “behavioral”

module and2 (Y, A, B);
    output Y;
    input A;
    input B;

    and (Y, A, B);
endmodule

C.2 Verilog HDL Code for D Flip Flop

// Verilog HDL for “VerilogLib”, “dff” “behavioral”

module dff (d, q, reset, sysclk);
    output q;
    input d;
    input reset;
    input sysclk;
    reg q;

    always @(posedge sysclk or posedge reset)
        begin
            if (reset)
                q=0;
            else
                q=d;
        end
endmodule
C.3 Verilog HDL Code for Inverter

// Verilog HDL for “VerilogLib”, “inv1” “behavioral”

module inv1 (Y,A);
    output Y;
    input A;

    not (Y,A);

endmodule
Appendix D

D.1 Data Sheet of RFM’s R02108 SAW Resonator

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Sym</th>
<th>Notes</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tolerance from 224.700 MHz</td>
<td>I0</td>
<td>2, 3, 4, 5</td>
<td>224.625</td>
<td>224.775</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>Insertion Loss</td>
<td>I0</td>
<td>1, 2, 6</td>
<td>1.6</td>
<td>2.0</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Quality Factor</td>
<td>Q0</td>
<td>5, 6, 7</td>
<td>18,190</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temperature Stability</td>
<td>T0</td>
<td>10</td>
<td>25</td>
<td>40</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Frequency Temperature Coefficient</td>
<td>TFC</td>
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<td></td>
<td></td>
<td>ppm/°C</td>
<td></td>
</tr>
<tr>
<td>Absolute Value during the First Year</td>
<td>F0</td>
<td>1</td>
<td>≤160</td>
<td></td>
<td>ppm/µs</td>
<td></td>
</tr>
<tr>
<td>RF Equivalent RLC Model</td>
<td>R0</td>
<td>5, 7, 9</td>
<td>20</td>
<td>25</td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>Motional Resistance</td>
<td>L0</td>
<td>256,222</td>
<td></td>
<td></td>
<td>µH</td>
<td></td>
</tr>
<tr>
<td>Motional Inductance</td>
<td>L0</td>
<td>1,93520</td>
<td></td>
<td></td>
<td>µH</td>
<td></td>
</tr>
<tr>
<td>Motional Capacitance</td>
<td>C0</td>
<td>5, 6, 9</td>
<td>2.2</td>
<td>2.5</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>Transducer Static Capacitance</td>
<td>C0</td>
<td>5, 6, 9</td>
<td>2.3</td>
<td></td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>Test Failure Short Inductance</td>
<td>LTEST</td>
<td>2.7</td>
<td>200</td>
<td></td>
<td>µH</td>
<td></td>
</tr>
</tbody>
</table>

CAUTION: Electrostatic Sensitive Device. Observe precautions for handling.

Notes:
1. Frequency aging is the change in I0 with time and is specified at 45°C or less. Aging may exceed the specification for prolonged temperatures above 45°C. Typically, aging is greatest the first year after manufacture, decreasing significantly in subsequent years.
2. The center frequency, I0, is measured at the minimum insertion loss point, I0min, with the resonator in the 50 Ω test system (200 MHz ± 2.1). The short inducance, L0min, is known for parallel resonance with C0 at I0. Typically, specification of L0min is less than the resonator I0.
3. One or more of the following United States patents apply: 4,454,888 and 4,816,195 and others pending.
4. Typically, equipment designs utilizing this device require emissions testing and government approval, which is the responsibility of the equipment manufacturer.
5. Unless noted otherwise, case temperature T0 = 25°C.
6. The design, manufacturing process, and specifications of this device are subject to change without notice.
7. Defined mathematically from one or more of the following directly measured parameters: I0, 3-dB bandwidth, I0 versus T0, and C0. Turnover temperature, T0, is the temperature of maximum (or zero) frequency deviation of the resonator. Typically, a 3-dB frequency deviation at 25°C (average), T0 = 120°C.
8. Turnover temperature, T0, is the temperature of minimum (or zero) frequency deviation of the resonator. Typically, a 3-dB frequency deviation at 25°C (average).
224.7 MHz SAW Resonator

Electrical Connections
This one-port, two-terminal SAW resonator is bidirectional. The terminals are interchangeable with the exception of circuit board layout.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Connection</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Terminal 1</td>
</tr>
<tr>
<td>2</td>
<td>Terminal 2</td>
</tr>
<tr>
<td>3</td>
<td>Case Ground</td>
</tr>
</tbody>
</table>

Typical Test Circuit
The test circuit inductors, L<sub>T</sub>, is tuned to resonate with the static capacitance, C<sub>0</sub> at F<sub>C</sub>.

Electrical Test:

Power Test:

Typical Application Circuits

Typical Low-Power Transmitter Application:

Typical Local Oscillator Application:

Temperature Characteristics
The curve shown on the right accounts for resonator contribution only and does not include oscillator temperature characteristics.

Equivalent LC Model
The following equivalent LC model is valid near resonance:

Case Design

Dimensions

<table>
<thead>
<tr>
<th>Dimensions</th>
<th>Min</th>
<th>Max</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.30</td>
<td>0.366</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B</td>
<td>0.18</td>
<td>0.425</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C</td>
<td>2.50</td>
<td>3.50</td>
<td>0.008</td>
<td>0.138</td>
</tr>
<tr>
<td>D</td>
<td>0.16</td>
<td>0.018</td>
<td></td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>0.08</td>
<td>0.000</td>
<td>0.200</td>
<td>0.000</td>
</tr>
<tr>
<td>F</td>
<td>2.54</td>
<td>0.100</td>
<td>0.100</td>
<td>0.100</td>
</tr>
<tr>
<td>G</td>
<td>2.54</td>
<td>0.100</td>
<td>0.100</td>
<td>0.100</td>
</tr>
<tr>
<td>H</td>
<td>1.02</td>
<td>0.040</td>
<td></td>
<td></td>
</tr>
<tr>
<td>J</td>
<td>1.40</td>
<td>0.065</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>