# Characterization of *n-n* Ge/SiC heterojunction diodes

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In this paper we investigate the physical and electrical properties of germanium deposited on 4*H* silicon carbide substrates by molecular beam epitaxy. Layers of highly doped and intrinsic germanium were deposited at 300 and 500 °C and compared. Current-voltage measurements reveal low turn-on voltages. The intrinsic samples display ideality factors of 1.1 and a reverse leakage current of $9\times10^{-9}$ A/cm$^2$, suggesting a high quality electrical interface. X-ray diffraction analysis reveals the polycrystalline nature of the high-temperature depositions, whereas the low-temperature depositions are amorphous. Atomic force microscopy shows that the low-temperature layers have a rms roughness of 3 nm. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2987421]

Silicon carbide (SiC) is the best placed semiconductor material for future generations of power electronic devices. SiC power diodes are now commonplace,[1] taking advantage of the material's superior reverse breakdown voltage, lower on-resistance, and faster switching speed when compared to silicon (Si). However, while steps toward a SiC metal-oxide-semiconductor field-effect transistor (MOSFET) continue to be made, the development of a commercial device is still being hindered by the material's high concentration of traps at the $SiC/SiO_2$ interface,[2] which reduces the material's low channel mobility. To overcome this, a heterojunction solution has been proposed,[3] whereby silicon forms an epitaxial layer upon a SiC substrate. This combines the advantages of the two materials; the high carrier mobility and the potential for a carbon-free oxide on the silicon, while retaining the reverse blocking capabilities of the SiC. Here we report on the use of germanium (Ge) as the narrow bandgap layer to form a Ge/SiC heterojunction. Ge has carrier mobilities that exceed silicon, with electron mobility reaching 3900 cm/V s at 300 K.[4] Despite this advantage Ge has long been overlooked as a semiconductor material due to its processing difficulties and the lack of a natural oxide material. Now however, "high-*K*" dielectrics are being developed for use on Ge with permittivities surpassing that of $SiO_2$.[5]

Here, Ge/SiC heterojunction structures are being investigated for two distinct purposes. Thin, highly doped layers of Ge are deposited using molecular beam epitaxy (MBE), potentially for use as low-resistance Ohmic contacts in rectifying SiC devices. Thicker, intrinsic Ge layers are investigated for use as a drift layer on SiC in advanced power devices. High- and low-temperature depositions of each layer type are investigated to compare the advantages of amorphous and polycrystalline Ge on SiC. However, with a significant lattice mismatch between the two materials, the primary aim of this work is to investigate whether a quality electrical interface is attainable for either application. All the layers are analyzed physically to extract crystallinity and surface morphology data. In addition, electrical characterization was performed to evaluate the electrical quality of the junction.

A *n*-type (0001) Si face, 4° off axis, 4*H*-SiC wafer was purchased from Cree Inc. with a 10 $\mu$m, lightly *n*-type doped ($1.4\times10^{15}$ cm$^{-3}$) epitaxial layer. This was diced into $10\times10$ mm$^2$ samples before germanium films were deposited using MBE (V100S). Prior to deposition, the wafer was cleaned using a standard Radio Corporation of America-2 (RCA2) clean[6] ($H_2O:HCl:H_2O_2$) followed by a hydrofluoric acid dip to remove the oxide formed during the RCA2 process. This cleaning process has been demonstrated[3] to be of high quality as indicated by the low reverse leakage current. This was followed by a high-temperature bake within the MBE system to desorb the native oxide and any other contaminants. *N*-type highly doped germanium (HD-Ge) layers ($N_{D,Ge}=5\times10^{19}$ cm$^{-3}$), 100 nm in thickness, were deposited at a rate of 0.1 Å s$^{-1}$ with antimony as the dopant at temperatures of 300 and 500 °C. Also deposited were intermediate layers of intrinsic germanium (*i*Ge), 1 $\mu$m in thickness, at a rate of 1 Å s$^{-1}$ at temperatures of 300 and 500 °C. No dopant was intentionally added to these layers; however, these were capped with a highly doped *n*-type Ge layer to improve contact Ohmicity. Consequently diffusion from these layers is believed to have made the intermediate layers lightly *n*-type. With HD-Ge caps on all the diodes, it is expected that nickel (Ni) will form a good Ohmic contact with Ge. In a similar situation, Ni has been shown[7] to form a low-resistance Ohmic contact with Ge on a gallium arsenide substrate. 400 nm of Ni was sputtered onto the Ge surfaces and patterned using a lift-off process creating dots 200 and 400 $\mu$m in diameter. These were formed into mesa diode structures by etching the remaining Ge. Ni was also sputtered onto the back SiC surface to form a back contact. The HD-Ge samples were further annealed at 450 °C in nitrogen ambient for 5 min to analyze the improved top and bottom contact Ohmicity and the effect of the anneal on the electrical properties of the rectifiers.

The crystallinity, and hence the conducting properties, of the Ge layers was investigated using x-ray diffraction (XRD) analysis. The importance of this is underlined by a reported[8] 500 times rise in Ge resistivity from its crystalline

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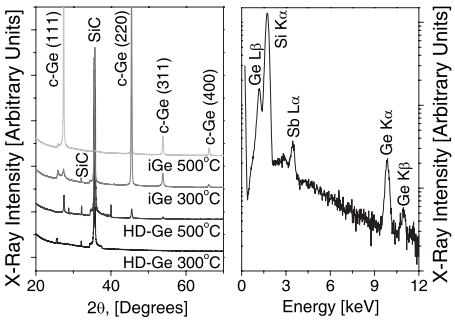


FIG. 1. XRD $\theta-2\theta$ scans of the MBE Ge layers deposited on 4*H*-SiC and EDX of the 300 °C HD-Ge layer deposited on 4*H*-SiC.

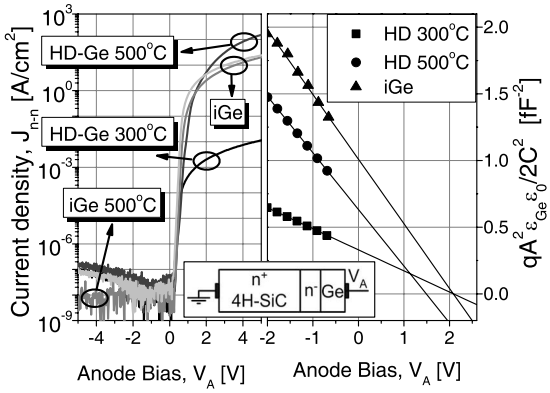


FIG. 3. Typical semilog *I-V* and *C-V* carried out before annealing on 200 nm diameter test diodes on the MBE layers deposited on 4*H*-SiC.

to amorphous state, thus suggesting a similar drop in mobility. Cubic-Ge spikes are apparent from the $\theta-2\theta$ scans in Fig. 1. Also evident is the *n*-type 4*H*-SiC substrate for all the deposition conditions. Four main Ge peaks are evident for the HD-Ge and *i*Ge samples deposited at 500 °C, suggesting that the Ge formed by the MBE process is polycrystalline. It was reported[9] that the orientation of Ge films on silicon improved with thicker layers, and this appears to be true here as well, with the peaks of the 1 $\mu$m *i*Ge samples larger and more defined than those of the 100 nm HD-Ge samples. The 300 °C HD-Ge layer displays an absence of Ge spikes suggesting that there is no crystalline Ge on this layer. To test for amorphous Ge on the 300 °C HD-Ge sample, energy dispersive x-ray (EDX) analysis was carried out. This technique is not reliant upon the material under scrutiny being crystalline for identification, unlike the XRD analysis. Figure 1 shows that distinct Ge peaks were found along with peaks of the dopant element, antimony. Silicon is also highly visible, however, carbon is outside the range of this particular scan.

To process advanced power devices such as a MOSFET using a Ge/SiC heterojunction structure, the Ge layer will need to be smooth to minimize channel scattering after oxide growth. Hence, atomic force microscopy (AFM) analysis was used to study the quality of the surface. AFM scans taken prior to Ge deposition show smooth surfaces, although there is some evidence of step bunching having occurred during the SiC epitaxy growth. The rms roughness of the wafer is 1.5 nm. Figure 2 displays the contrasting surface

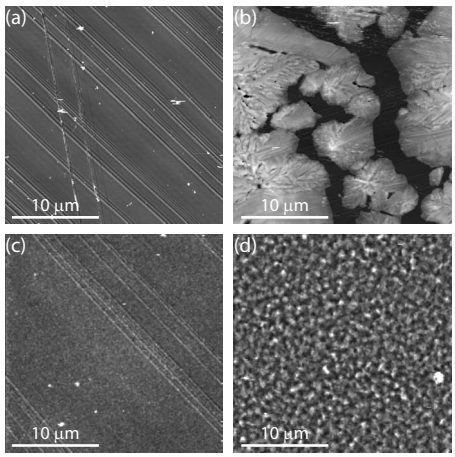


FIG. 2. 25 $\mu$m² AFM micrographs of the MBE Ge layers deposited on 4*H*-SiC (a) HD-Ge, 300°; (b) HD-Ge, 500 °C; (c) *i*Ge, 300 °C; and (d) *i*Ge, 500 °C. The height scales are [(a) and (c)] 25, (b) 1.25, and (d) 250 nm.

roughnesses that appear over a 25 $\mu$m square area of each Ge layer. The low-temperature depositions of Figs. 2(a) and 2(c) reveal a rms roughness of 4 and 3 nm, respectively, with the HD-Ge surface showing no evidence of crystalline Ge, confirming again its amorphous nature. Meanwhile, both 500 °C samples appear polycrystalline in nature. These crystals are distinct in the 100 nm layer of HD-Ge, with a rms roughness of 55 nm. It can be seen from the micrograph of this sample that the Ge has formed into distinct crystalline clusters, with the SiC surface evident between them. The 500 °C *i*Ge sample has a rms roughness of 45 nm, and the crystal grains are much smaller. Clusters such as these occur when atoms deposited on a surface seek an atomic site that minimizes the total energy of the system.[10] Dangling (unattached) bonds add energy, and so atoms will begin to cluster together on a flat surface to minimize the number of unattached bonds. If this continues to occur two-dimensionally, then these are known as islands. The greater the deposition temperature, the more energy each atom will have to find a nucleation site, and hence, fewer larger islands are formed, as in Fig. 2(b). High temperatures also allow atoms already deposited to migrate to a higher layer, and hence the islands start to form vertically from the substrate, known as a cluster. A possible remedy is to use a surface active agent (surfactant) to aid a smooth heterolayer growth by introducing Group-V atoms onto the surface. Sb has been shown[11] to change the growth mechanism within Ge/Si layers from Stranski–Krastanov (islanding) to layer by layer.

Typical current-voltage (*I-V*) curves for the Ge/SiC *n-n* heterojunction devices are shown in Fig. 3 from which ideality factors and resistivity values were extracted for each MBE Ge layer. All the diodes display a very low turn-on voltage, with the devices starting to turn on around 0.3 V. The 500 °C *i*Ge diode produced a response with the lowest reverse leakage current of $9.1\times10^{-9}$ A/cm² at −10 V and an ideality factor of 1.08. The 300 °C *i*Ge diode produced a similar ideality factor of 1.12 and a reverse leakage current of $4.5\times10^{-7}$ A/cm². Such low ideality factors indicate that the current transport is dominated by thermionic emission and not recombination, thus proving the electrical quality of the Ge/SiC junctions. This is further indicated by the low reverse leakage current. Both *i*Ge diodes are fairly resistive, however, since the 300 and 500 °C, 1 $\mu$m Ge layers are estimated to make up 70% and 62% of the total device resistance, respectively. The 300 °C HD-Ge layer is extremely resistive, which can be attributed to the amorphous layer

having a significantly reduced electron mobility. However, with an ideality factor of 1.12 it is another high quality interface. The 500 °C HD-Ge diode, meanwhile, displays a relatively low resistance but an ideality factor of 2.23. The polycrystalline HD-Ge layer in this device is estimated to be responsible for 10% of the total device resistivity. The poor interface quality of this device could be explained by the discontinuous surface morphology displayed in Fig. 2(b). This patch contact suggests that Ni is directly in contact with the SiC, thus reducing the resistance at high voltages. It also explains the poor turn-on characteristic as current is able to travel through paths of varying resistance. It can be concluded from these results that all the diodes display a very low turn-on voltage, but the *i*Ge layers form better quality junctions with the SiC than the HD-Ge layers. However, when deciding the appropriate deposition temperature, a trade-off clearly exists between the surface smoothness and Ge crystallinity, which impacts on reverse leakage current and series resistance. Despite this, the reverse leakage of the 300 °C *i*Ge diode is good and with a reasonably flat surface; this diode could be considered the most appropriate for use as a drift layer on SiC for advanced power devices. The HD-Ge layers have the potential to make very low-resistance contacts to SiC, but further work needs to be carried out on improving the layer quality using thicker layers or improving the growth technique.

Annealing was carried out on the highly doped diodes. The 300 °C HD-Ge sample annealed at 450 °C exhibited a much improved forward current, three orders of magnitude higher than in Fig. 3. However, the annealing had a detrimental effect on the 500 °C sample, reducing the forward current one order of magnitude, though it did reduce the ideality factor to 1.22. These results suggest that the anneal transformed the layers into a single nickel germanide layer upon the SiC surface. In both cases, the anneal raised the reverse leakage one order of magnitude, most likely due to a reduction in the Ge/SiC effective barrier height.

Capacitance-voltage (*C-V*) measurements were performed at frequencies ranging from 1 to 500 kHz, and typical $(1/C^2)-V$ plots are shown in Fig. 3. The $(1/C^2)-V$ curves of an abrupt heterojunction can be analyzed using the expressions found in Ref. 3. The built-in potential values of 2.0 and 1.5 V were extracted from the 300 and 500 °C HD-Ge diodes, respectively. The built-in potential of the *i*Ge diodes were both 2.2 V. Barrier height values extracted from the *I-V* plots using a method involving the saturation current[12] produced values ranging from 1.13 eV for the 500 °C HD-Ge diode to 1.17 eV for the 500 °C *i*Ge diode. These are less than the *C-V* built-in potentials and could be explained by low barrier height zones appearing within the region of higher barriers as referred to by the Tung model.[13] Low barrier height regions could appear due to surface defects and will dictate the current flow in a direct regime, such as the *I-V* measurements. However, during *C-V* measurements, they are screened by the higher barriers. This Tung[13] effect may be accentuated by the low doping level of the SiC epitaxial layer.

In summary, it has been proven that high quality electrical junctions can be formed with a low turn-on voltage from Ge/SiC *n-n* heterojunction structures despite the large lattice mismatch between the two materials. The thicker layers of intrinsic Ge formed the best of these junctions with ideality factors of 1.1, indicating that the current transport is dominated by thermionic emission. The temperature of deposition remains a trade-off between surface quality and reverse leakage current, with the 500 °C *i*Ge diode providing the lowest reverse leakage current but a very rough surface. This would be most suitable as a Schottky diode device. Despite having a slightly greater leakage current, the 300 °C *i*Ge diode has a smooth surface of 3 nm and can be considered the most appropriate of the samples for use as a drift layer on SiC for advanced power devices.

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