Low-voltage Organic Thin Film Transistors (OTFTs) with Solution-processed High-*k* Dielectric cum Interface Engineering

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Abstract

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Although impressive progress has been made in improving the performance of organic thin film transistors (OTFTs), the high operation voltage resulting from the low gate areal capacitance of traditional SiO_2 remains a severe limitation that hinders OTFTs' development in practical applications. In this regard, developing new materials with high-*k* characteristics at low cost is of great scientific and technological importance in the area of both academia and industry.

In this thesis, we first describe a simple solution-based method to fabricate a high-*k* bilayer Al_2O_y/TiO_x (ATO) dielectric system at low temperature. Then the dielectric properties of the ATO are characterized and discussed in detail. Furthermore, by employing the high-*k* ATO as gate dielectric, low-voltage copper phthalocyanine (CuPc) based OTFTs are successfully developed. Interestingly, the obtained low-voltage CuPc TFT exhibits outstanding electrical performance, which is even higher than the device

fabricated on traditional low-*k* SiO_2. The above results seem to be contradictory to the reported results due to the fact that high-*k* usually shows adverse effect on the device performance. This abnormal phenomenon is then studied in detail. Characterization on the initial growth shows that the CuPc molecules assemble in a "rod-like" nano crystal with interconnected network on ATO, which probably promotes the charge carrier transport, whereas, they form isolated small islands with amorphous structure on SiO_2. In addition, a better metal/organic contact is observed on ATO, which benefits the charge carrier injection. Our studies suggest that the low-temperature, solution-processed high-*k* ATO is a promising candidate for fabrication of high-performance, low-voltage OTFTs.

Furthermore, it is well known that the properties of the dielectric/semiconductor and electrode/semiconductor interfaces are crucial in controlling the electrical properties of OTFTs. Hence, investigation the effects of interfaces engineering on improving the electrical characteristics of OTFTs is of great technological importance. For the dielectric/semiconductor interface, an octadecylphosphonic acid (ODPA) self-assembled monolayer (SAM) is used to modify the surface of ATO (ODPA/ATO). For the electrode/semiconductor interface, a simple *in-situ* modified Cu (*M*-Cu) is employed as source-drain (S/D) electrodes in stead of commonly used Au. The electrical characteristics of pentacene TFT are drastically enhanced upon interfaces modification. Moreover, by encapsulating the *M*-Cu with a thin layer of Au (Au/*M*-Cu), the device performance is further improved. The detailed mechanism is systematically explored.

Finally, organic electronic devices on flexible plastic substrates have attracted much attention due to their low-cost, rollability, large-area processability, and so on. One of the

most critical issues in realization flexible OTFTs is the integration of gate dielectrics with flexible substrates. We have successfully incorporated the ODPA/ATO with Au coated flexible polyimide (PI) substrate. By using Au/*M*-Cu as S/D electrode, the flexible pentacene TFTs show outstanding electrical performance. In addition, the mechanical flexibility and reliability of the devices are studied in detail. Our approach demonstrates an effective way to realize low-cost, high-performance flexible OTFTs.

論文摘要

儘管在提高有機薄膜晶體管（OTFTs）的性能方面已經取得了顯著地進步，但是由傳統二氧化矽介電層的低面電容密度引起的高驅動電壓一直是阻礙其在實際應用中發展的絆腳石。因此，開發具有低成本、高介電常數等特點的新型材料對於學術界和工業界都具有非常重要的意義。

本文首先介紹了一種簡單的溶液法在低溫下制備高介電常数的 Al_2O_y/TiO_x（ATO）材料體系， 并詳細表徵和討論了它的介電性能。通過運用 ATO 作為介電層，我們成功地製備了低電壓銅酞菁（CuPc）基 OTFT。有趣的是，該低電壓器件顯示出優異的性能，並且遠遠超過在二氧化矽上製備的器件性能。這個結果似乎和報道的結果相矛盾，因為高介電常數往往對器件性能造成不利影響。本文就此异常現象進行了詳細研究。基於初期生長的研究表明，在 ATO 表面上，CuPc 分子組裝成有利於載流子輸運的棒狀晶體，并形成網狀結構。相反，在 SiO_2 表面上 CuPc 分子卻形成由無定形結構組成的孤立小島。此外，在 ATO 上還觀察到了更好的金屬/有機分子接觸，有利於載流子的注入。以上研究表明溶液法製備的 ATO 在实现高性能、低電壓的 OTFT 方面有著非常實用的前景。

此外，界面的性質對決定 OTFT 的電學性能非常關鍵。因此研究界面功能化對提高器件性能的作用也非常重要。在應用十八烷基磷酸（ODPA）和原位改性的 Cu

（*M*-Cu）分別對介電層/半導體、電極/半導體界面進行修飾后，并五苯（pentacene）基 OTFT 的電學性能得到大幅提高。此外，通過採用一薄層金覆蓋的 *M*-Cu 做電極（Au/*M*-Cu），器件性能得到進一步提升。本文就其詳細的機理進行了討論。

最后，由於具有低成本，可捲曲，可大面積加工等特點，柔性有機電子器件引起了廣汎關注。實現柔性 OTFT 的關鍵問題之一就是介電層同柔性襯底之間的結合。在此，我們成功地將 ODPA 和 ATO 集成到金覆蓋的柔性聚酰亞胺襯底上。通過使用 Au/*M*-Cu 做電極，柔性 pentacene TFT 顯現出優異的電學性能。另外，本文就器件的機械柔性及可靠性也做了詳細地探討，從而展示了一個實現低成本高性能柔性 OTFT 的有效途徑。

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Chapter 1 Introduction

Since the discovery of the photoconducting properties of anthracene in 1906, organic semiconductors have come into sight of scientists all over the world [1]. For a long time before 1970's, the main research activities were devoted to developing the application of organic semiconductors in the area of photocopies, i.e. photosensitive drums. In fact, it is the discovery of near-metallic conductivity of doped polyacetylene in 1977 that really stimulated intensive interest in organic semiconductors [2], and exciting progress had been made in both design of novel organic semiconductors and device fabrication techniques in the flowing decades. Notably, the Nobel Prize in Chemistry of 2000 was awarded to Heeger *et al.* for this great discovery, which had led to a booming field called "organic electronics". Due to unique electronic performance of organic semiconductors, combining with other outstanding properties, such as low cost, light weight, flexibility and low temperature processing, a huge market of about one billion dollar in organic electronics has opened up a variety of applications, such as organic light-emitting diode (OLED) [3, 4], organic field-effect transistors (OFETs) [5, 6], physical and chemical sensors [7, 8], radio-frequency tags (RFIDs) [9] and organic solar cells [10, 11].

Organic semiconductors are in essential a class of π-conjugated organic materials with alternate C-C and C=C bonds. Conventionally, they can be categorized into two groups, i.e., oligomers (also called as small molecules) and polymers. Fig. 1.1 shows some frequently used organic semiconducting materials. Small molecules are usually processed by thermal evaporation in vacuum, and they tend to crystallize and exhibit high ordering. On the other hand, polymers have the advantage of being processed via solution-based techniques, such as spin-coating, drop-casting and ink-jet printing, but are likely to be amorphous and possess low structural regularity.

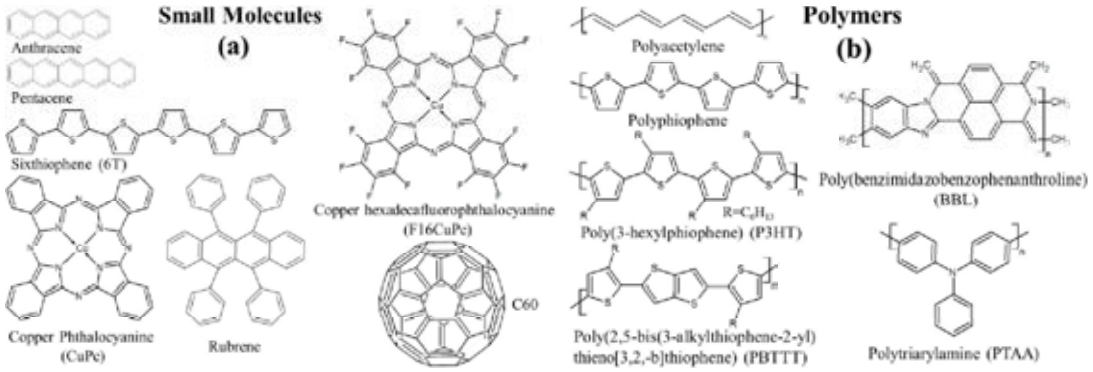

Fig. 1.1 Some common organic semiconductors: (a) small molecules and (b) polymers.

The concept of field-effect transistor (FET) was first proposed by Lilienfeld in his patent in 1930 [12]. He depicted that a FET behaved as a parallel plate capacitor which accumulating charge carriers controlled by a gate electrode bias, and forming conducting channel between source and drain electrodes. Until 1960, this fascinating

concept was eventually realized by Kahng *et al.* using a silicon-based metal-oxide-semiconductor (MOS) structure. And more than twenty years later, the first organic field-effect transistor (OFET) was reported by Ebisawa *et al.* using polyacetylene as the active channel material [13]. From the point of view of reducing material costs and environmental concerns, many OFETs are now designed based on the thin-film transistor (TFT) model, which allows the devices to use less conductive materials in the conducting channel region. A prototype of OTFT is shown in Fig. 1.2. Early studies on organic thin film transistors (OTFTs) were performed on the basis of thermally oxidized SiO_2/highly-doped Si configuration which acting as dielectric and gate electrode pack, respectively, because the above system had been well-developed in amorphous Si TFTs industry [6]. Despite many excellent properties, such as large band gap (~ 9 eV), high purity and low density of defects, SiO_2 suffers from a relatively low dielectric constant (k = 3.9) [14]. A direct consequence of a low k is the low area capacitance density of gate dielectric (~ 11 nF/cm^2 for 300 nm SiO_2), which resulting in a high driving voltage to operate an OTFT, in the order of several tens volts. On the other hand, with the development in device performance of OTFTs, the realistic applications are getting close to the consumers, and low operation voltage is a prerequisite. Moreover, SiO_2 as a gate dielectric is unfortunately incompatible with

high-throughput production, such as roll-to-roll fabrication. So in these regards, finding new dielectric materials that have high-*k* which allowing low-operation voltage and are also potentially compatible with large-area production (e.g. solution-processed) is of great importance in both academia and industry.

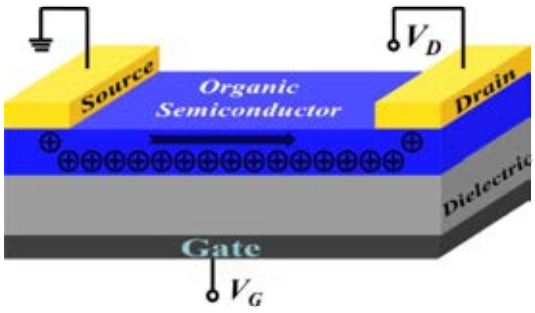

Fig. 1.2 A prototype of organic thin film transistor (OTFT).

The main focus of this thesis is on the realization of low-voltage OTFTs basing on solution-processed high-*k* dielectric. At first, a novel and simple solution-processed metal-oxide dielectric system is introduced, and an exciting high-performance OTFT is achieved. Then, an in-depth study is pursued to discover the mechanism behind. Followed by this, interface engineering is employed to further improve the device performance. Finally, an attempt to integrate the solution-processed dielectric with flexible substrate is made to demonstrate its compatibility with future large scale application. To make it clear and logical, the thesis is organized as follows:

In Chapter 2, an overview of organic semiconductors and some theoretical background relevant to this work are provided. In particular, the working principle of OTFTs is introduced and explained, and the charge carrier transport in organic semiconductors is discussed. Methods involved in electrical parameters extraction are also addressed, followed by a brief review on the dielectric materials.

In Chapter 3, we give a brief introduction on the materials, processing methods and characterization techniques used in the thesis.

In Chapter 4, a detailed study on the solution-processed high-*k* dielectric is present, and a low-voltage OTFT is demonstrated.

Chapter 5 addresses the issue of why our high-*k* dielectric can achieve high-performance of device, which seemed to be contradictory to the results reported by other groups, since high-*k* is regarded as detrimental to the device performance because of the energy disorder induced in the dielectric/organic interface [15].

Chapter 6 exhibits the effectiveness of interface engineering in the improving the overall device performance, which involves both of dielectric/organic interface and electrode/organic interface. Upon careful interface engineering, the device performance can be obviously enhanced.

In Chapter 7, an attempt of incorporation of the solution-processed dielectric with polyimide (PI) substrates is made to fabricate flexible OTFTs, and excellent device performance is achieved. Additionally, the mechanical performance including flexibility and reliability is examined and discussed in detail. The results in Chapter 4, 5 and 6 are published in scientific journals (see publication list on page 171), and those in Chapter 7 is submitted.

Finally, in Chapter 8, a general summary is deduced basing on this work and some suggestions on future research are proposed.

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Chapter 2 Background

This chapter provides an overview of the theoretical background for small molecule semiconductors and organic thin film transistors (OTFTs). It begins by describing the intrinsic electronic structure of small molecules, and then the working principles of OTFTs are addressed. Subsequently, several charge transport models in organic semiconductors are discussed, and followed by the introduction of electrical parameter extraction in OTFTs. Finally, a brief review on the gate dielectrics will be delivered.

2.1 Intrinsic electronic structure of small molecule semiconductors

It is known to all that, for free carbon atoms, the electron configuration is $1s^2 2s^2 2p^2$, and they usually adopt sp^3 hybridization due to the unique chemical performance, which is referred to as single bond. On the other hand, from the point of view of molecular physics, a double bond can also form between two carbon atoms resulting from a sp^2 hybridization. In this configuration, the $2s$, $2p_x$ and $2p_y$-orbitals of each

carbon atom are combined to form the sp^2-hybrid orbital. The above three degenerated orbitals are coplanar and oriented at an angle of 120° between each other, as depicted in Fig. 2.1a. Chemical bonds formed by these orbitals are called σ bonds, which are localized between two adjacent carbon atoms. On the other hand, the remaining fourth orbital, p_z, is orthogonal to the plain of sp^2 orbitals, as shown in Fig. 2.1b. Since the distance between neighboring carbon atoms is small enough, the overlap between p_z orbitals is possible. The side-by-side overlap of the p_z orbitals then produces the so-called molecular bonding π- and antibonding π∗-orbitals with delocalized density of electrons above and below the sp^2 orbital plain (i.e., molecule plane). Furthermore, according to the Pauli Exclusion Principle and the Hund's rule, the π and π∗ orbitals are referred to as the highest occupied molecular orbitals (HOMO) and lowest unoccupied molecular orbitals (LUMO), as illustrated in Fig. 2.1c.

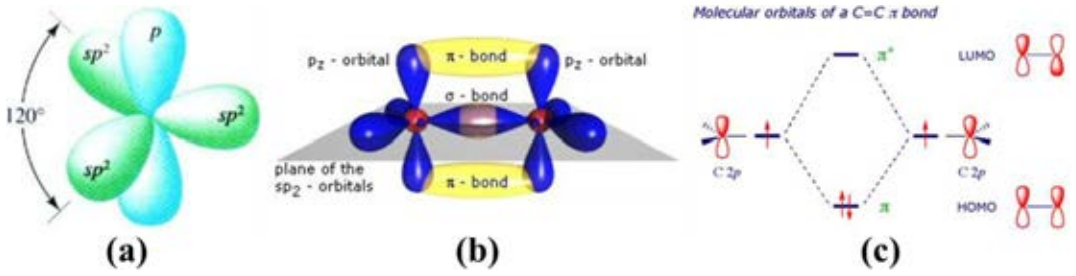

Fig. 2.1 (a) Illustration of orbitals of carbon sp^2-hybridization; (b) Formation of π-bond in ethylene: the p_z orbitals overlap above and below the plane of sp^2-orbitals; (c) Formation of molecular orbitals [1].

In a π-conjugated system whose carbon atoms are connected by alternating single and double bonds, all carbon atoms contribute a p_z orbital to construct an extended π-orbital with π-electrons delocalized over the entire molecule. If a large number of molecules are put together with high ordering and the inter-molecular orbital overlap is sufficient, the formation of extended electronic states in organic semiconductor appears. The transport of positive charge (hole) occurs through the HOMO and negative charge (electron) occurs through the LUMO [2]. And the energy difference between the HOMO and LUMO is the band gap of the organic semiconductor.

When two molecules are put together in a coplane configuration, their interaction will lead to a splitting of HOMO and LUMO levels. In organic crystals, the molecules are closely packed, the interaction among the HOMOs and LUMOs of large number of molecules then give rise to the formation of valence and conduction band. Brédas *et al.* studied theoretically the effect of the intermolecular distance of cofacial dimers on the electronic splitting of their HOMO and LUMO levels [3], and the results are shown in Fig. 2.2. As can be seen, the HOMO exhibits a larger splitting than that of LUMO, and the amplitudes decay exponentially with increasing the intermolecular distance, which can be simply regarded as the decrease of intermolecular π-orbital overlap. Qualitatively, the larger the splitting of the HOMO in the organic crystal, the higher the

mobility of holes, and similarly, it is also true for LUMO and electrons. The calculations confirm the crucial impact of orbital overlap on the electronic splitting and therefore on the intrinsic mobility. In organic crystals, the degree of orbital overlap varies largely with different crystallographic directions due to their highly structural anisotropy.

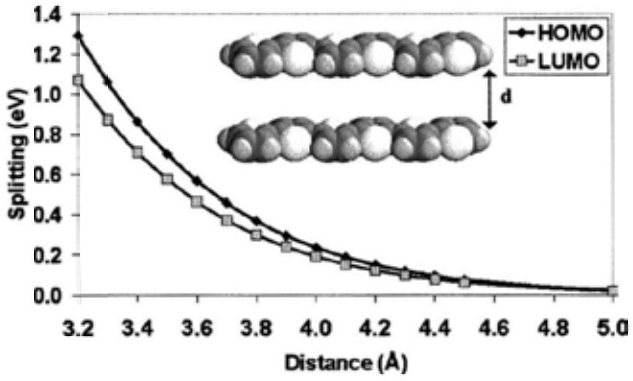

Fig. 2.2 Evolution of the calculated electronic splitting of the HOMO and LUMO levels in a cofacial sexithienyl dimer system as a function of the intermolecular separation.

Bao *et al.* calculated the variation of electronic splitting through displacing neighboring molecules along their long/short molecular axis involved in the cofacial configuration [4]. Fig. 2.3 depicts the impact of translation of the top tatracene molecule on the HOMO and LUMO electronic splitting (the intermolecular distance is kept unchanged). As seen, the molecular overlap is reduced with displacement, and as a result, the splitting is expected to be decreased. It is interesting to note the fact that there

are some oscillations in the values of the splitting with different period. The different oscillation period gives an important consequence that small translation can result in larger electronic splitting in LUMO than in HOMO, and therefore, the mobility of electrons can be possibly higher than that of holes in this configuration. On the other hand, the splittings also exhibit maxima and minima, which occurs when the benzene rings of first molecule overlap entirely or half of the ring of the second molecules, as shown in Fig. 2.3. Again, this phenomenon can be explained by considering the shape of the HOMO and LUMO orbitals.

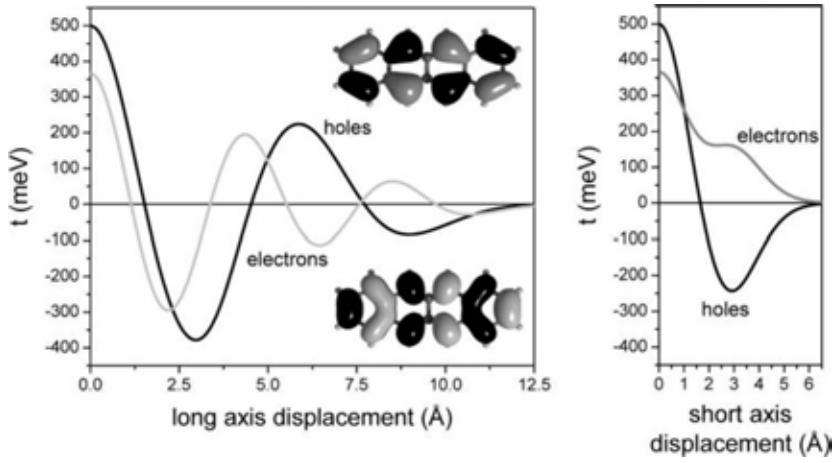

Fig. 2.3 Influence of molecular displacement along its long axis (lower left) and short axis (lower right) on the electronic splittings of the HOMO and LUMO levels in a tetracene dimer system separated by 3.4 Å [4].

2.2 Organic field-effect transistors

Field-effect transistor (FET) is a three-end electronic device that uses gate electric field to modulate source/drain current through "conductive channel" formed in semiconducting material. A FET is constructed by three parts: an insulator (dielectric), a layer of semiconductor and three electrodes. The term organic field-effect transistor (OFET) is referred to a class of field-effect transistor whose channel is built up with an organic semiconductor, such as pentacene and rubrene. For the sake of environmental protection and saving materials, the thickness of the channel layer is reduced to several tens of nanometers, which then gives rise to the so-called organic thin film transistor (OTFT).

2.2.1 Architecture of OTFTs

OTFTs have been fabricated with various device architectures, as illustrated in Fig. 2.4a-d. Due to the fragility of organic semiconductors, deposition of organic semiconductor on the top of insulator is much easier than the opposite. As a result, most of current OTFTs are fabricated adopting the bottom-gate (BG) geometry, with either top-contact (TC) or bottom-contact (BC). On the other hand, this configuration borrows

the concept of silicon TFT, using thermally grown SiO_2 as gate dielectric. Because of commercially availability of high-quality Si/SiO_2 substrate, the bottom-gate geometry has dominated the field. Each of these structures has its own advantages and drawbacks. Top contact OTFTs in general exhibit lower contact resistance than bottom contact ones. This is possibly due to the increased metal-semiconductor contact area in the former configuration. However, because the electrodes are deposited through a shadow mask, the dimension of the channel region is restricted by the size of mask, usually has a length of tens of microns. On the other hand, with bottom contact, the electrodes can be patterned by means of traditional micro-photolithography, which ensuring a high resolution. Unfortunately, devices with this configuration usually show high contact resistance, which are likely due to the structural disorder in the contacting area between the deposited organic semiconductor and the electrodes.

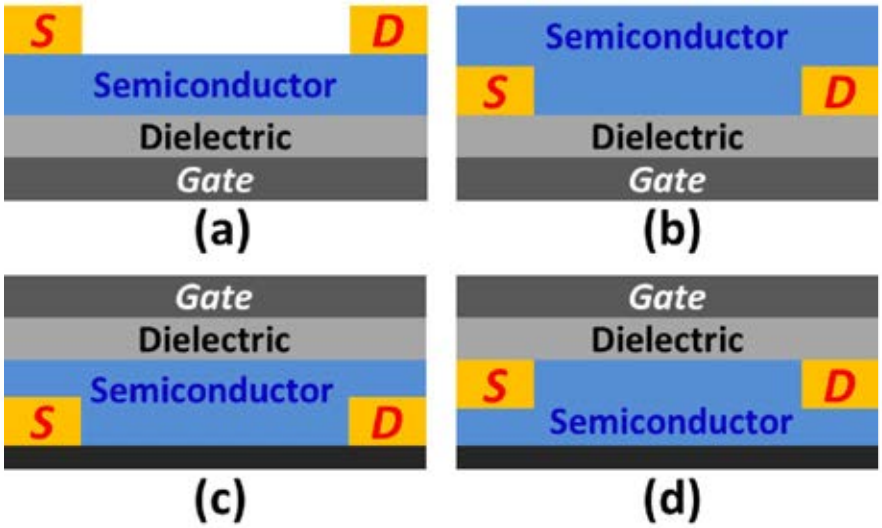

Fig. 2.4 Schematic of common architectures of organic thin film transistors (OFETs): (a) top-contact/bottom-gate (TCBG), (b) bottom-contact/bottom-gate (BCBG), (c) top-gate/bottom-contact (TGBC) and (d) top-gate/top-contact (TGTC).

2.2.2 Operation principles of OTFTs

The operation of OTFTs is basing the metal-insulator-semiconductor (MIS) structure which is designed to modulate the charge density in the device. Unlike the several operation modes in inorganic transistors, the OTFT is primarily operated in an accumulation mode [5, 6]. Since most reported high performance OTFTs are those fabricated with p-type organic semiconductors, the following section will focus on the operation of p-type devices in the accumulation mode.

For a p-channel OTFT, the gate and the drain are both negatively biased and the

source is grounded, as shown in Fig. 2.5a. By applying a negative bias on the drain electrode (V_{DS}), holes are injected from the source electrode into the active layer, and then accumulated in the interface of dielectric/semiconductor by the gate electric field across the insulator upon applying a negative gate bias (V_{GS}). The accumulated holes at the semiconductor/insulator interface form a conducting channel between the source and the drain, and then move under the drive force of the source-drain electric field and finally enter the drain end. The accumulated charge density is proportional to the magnitude of V_{GS} and the areal capacitance of dielectric (C_i), and can be simply calculated by $V_{GS} \cdot C_i$ if we assume that the voltage drop across the dielectric and the accumulation layer is negligibly small. It is important to note that not all of the charges in accumulation layer are mobile, but only a part of them will contribute to the current in the transistor. Due to the presence of defects and impurities in the vicinity of the dielectric/organic interface region, some of these charges will be trapped. The deep traps must be filled at first before the current flowing through the transistor occurs. As a result, a more negative V_{GS} than a certain onset voltage, i.e. the so-called threshold voltage (V_T), must be applied to the gate electrode in order to induce a conducting channel in the dielectric/semiconductor interface, and the effective gate voltage reduces to V_{GS} - V_T accordingly.

Under constant V_{GS} ($|V_{GS}| > |V_T|$), the source-drain current (I_{DS}) is controlled by the V_{DS}. For $|V_{DS}| << |V_{GS}\text{-}V_T|$, a linear density gradient of accumulated charge is formed between source and drain, as shown in Fig. 2.5b. The current-voltage relations in a TFT can be derived basing on the gradual channel approximation [7], which assuming that the vertical electric field across the gate insulator is much stronger than the transverse electric field between source and drain. According to this assumption, the I_{DS} can be calculated from two separate one-dimensional equations. Firstly, the free charge density at position x within the channel can be connected with the gate voltage through following equation:

$$n(x) = C_i|V_{GS} - V(x) - V_T| \qquad (2.1)$$

where $n(x)$ is the free charge areal density, C_i is the capacitance areal density of the gate dielectric, V_{GS} is the gate voltage, $V(x)$ is the potential of semiconductor at position x and V_T is the threshold voltage. Secondly, the current is then calculated by applying a one-dimensional current equation between source and drain, which can be written as:

$$I_{DS} = -Wn(x)\mu\frac{dV}{dx} = -W\mu C_i|V_{GS} - V(x) - V_T|\frac{dV}{dx} \qquad (2.2)$$

where W is the channel width, μ is the field-effect mobility and dV/dx is the lateral electric field. If we define $x = 0$ at the source contact, then we will have $x = L$ at the

drain contact (L is the channel length). Therefore, $V(0) = V_S = 0$ and $V(L) = V_{DS} = V_D$ can be rationalized, where V_S and V_D are the source and drain voltages, respectively. Assuming that the μ *is* constant in the semiconductor, through integrating Equation 2.2 from $x = 0$ to $x = L$, one can obtain the resulting current-voltage equation:

$$I_{DS} = \frac{W}{L}\mu C_i \left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right] \qquad (2.3)$$

Since $|V_{DS}| << |V_{GS}\text{-}V_T|$, the quadratic term in V_{DS} can be neglected. Therefore the current-voltage equation can be simplified as:

$$I_{DS} = \frac{W}{L}\mu C_i (G_{GS} - V_T)V_{DS} \qquad (2.4)$$

As seen, the I_{DS} is linearly proportional to the V_{DS}, hence, the operation of OTFTs in this situation is called linear region.

When the V_{DS} increases negatively, the voltage drop over the insulator and semiconductor becomes a function of the position in the channel. At the source contact, the voltage drop and the accumulated charge density remains unchanged. At the drain contact, however, the voltage drop decreases, resulting in a lower charge density as compared to that of the source contact, and the accumulated charge density exhibits a continuous decrease from source to train. At the point when $|V_{DS}| = |V_{GS}\text{-}V_T|$, the

charge density in the drain contact decreases to zero, the so called "pinch-off" is reached, as shown in Fig. 2.5c. Beyond this point, a further increase in V_{DS} will not result in an increase in drain current, and the device is said to operate in the saturation region, i.e. $|V_{DS}| > |V_{GS}\text{-}V_T|$, as illustrated by Fig. 2.5d. The current is then expressed by:

$$I_{DS} = \frac{W}{2L}\mu C_i(V_{GS} - V_T)^2 \qquad (2.5)$$

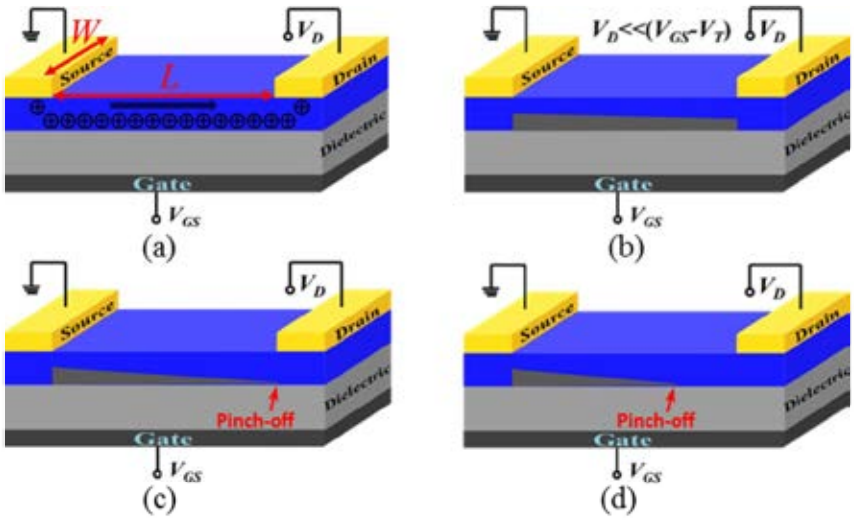

Fig. 2.5 Operation principles of organic thin film transistors.

2.3 Charge transport mechanisms

As having been discussed in previous section, organic semiconductors are those compounds made of sp^2 hybridized carbons, which also referred to as conjugated organic materials. For big conjugated molecules, the p_z orbitals are delocalized and form an extended π system all over the molecule. Only the loosely bound π-electrons can be transferred from molecule to molecule, and they are the source of charge transport in organic semiconductors. Though much attention has been paid in the exploration of the nature of charge transport in organic semiconductors, there are still controversy in this field. Below, we will summarize some models proposed to explain the charge transport in organic semiconductors.

2.3.1 Band transport

Band transport originates from the mechanism involved in inorganic crystals. The energy levels of individual atoms widen into bonding and anti-bonding orbitals, which then forms the valence band and conduction band. At T = 0, the valence band is completely filled while the conduction band is empty. Injection of electrons into the valence band can occur either by thermal excitation with intrinsic semiconductor or

through doping with extrinsic semiconductor. The movement of the delocalized electrons in the conduction band are scattered by phonons. The macroscopic mobility can be approximately expressed by following equation [8]:

$$\mu_0 \approx \frac{e\tau_0}{kT}\frac{W^2a^2}{\hbar^2} \qquad (2.6)$$

where W is a measure of the bandwidth, a is related to the lattice constant and τ_0 is the mean lifetime of the Bloch states. Form the above equation it is clear that in the band transport mechanism, the mobility decreases with increasing temperature.

In a conjugated molecule crystal, both the van-der-Waals force between molecules and the intermolecular electronic coupling through π-π-interactions are very weak, and the weak electronic coupling is easily broken by phonons and lattice disorder, resulting in localized states. Band-like transport has been reported in high purity organic single crystals at low temperatures, such as anthracene [9] and pentacene [10]. However, for most organic semiconductors, due to the existence of grain boundaries and impurities, a high degree of disorder is often observed, which will lead to the ruling out of band-like transport.

2.3.2 Polaron transport

The main reason for the band transport model fails to explain the charge transport in organic semiconductors is that it cannot account for the critical polarization phenomenon in these materials. The detailed mechanism of polarization in organic solids has been discussed in depth by Silinsh *et al.* [11]. Briefly, due to the weak coupling between neighboring molecules in organic semiconductors, a strong localization of excess charge carrier is often observed, which can result in the polarization of their surroundings. Consequently, the whole entity is not a naked charge any more, but a "dressed charge" formed by polarization cloud containing a charge in its center. The quasi-particle is called "polaron". Basing on the origin of polarization, polaron can be divided into three categories, as illustrated in Fig. 2.6. In the first type, the polarization originates from the interaction between a charge carrier and electrons of surrounding molecules in organic semiconductors. The process is called electronic polarization and the resulting quasi-particle is called "electronic polaron", as shown in Fig. 2.6a. The second type is called "molecular polaron". The molecular polaron is arisen from interaction between excess charge carrier and molecular phonons, see Fig. 2.6b. Such interaction can also take place between excess charge carriers and lattice of organic semiconductors, resulting in displacement of atomic nuclei. This is referred to

the third type, the so-called “lattice polaron”, as can be seen from Fig. 2.6c.

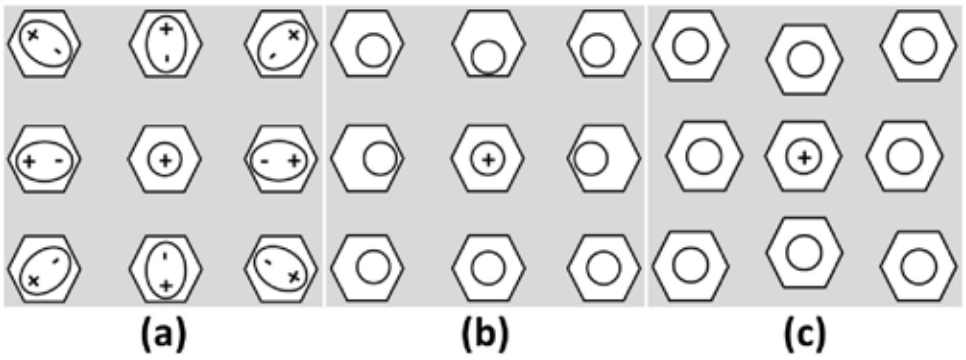

Fig. 2.6 Schematics of different polarization: (a) electronic polarization, (b) molecular polarization and (c) lattice polarization.

One can estimate the stability of the polaron by defining two typical times: the residence time (τ_{res}) and polarization time (τ_p). The former defines the average time that a charge will reside on a molecule, and the later corresponds to the time involved in the formation of electronic cloud around the charge. The magnitude of both typical times can be estimated through Heisenberg’s uncertainty principle expressed by following equation:

$$\tau \leq \frac{\mathrm{h}}{\Delta E} \qquad (2.7)$$

where ΔE is a characteristic energy. The typical value for τ_{res} is on the order of 10^{-14} s for organic semiconductors. In case of electronic polaron, the τ_p ranges between 10^{-16} s

to 10^{-15} s, which is much smaller than τ_{res}. And the ΔE is in the range of 1.5 to 2 eV. As for molecular polaron, the τ_p increases to about 10^{-14} s, and the characteristic energy involved is on the order of 10 mV to 100 meV. On the other hand, for the lattice polaron, the τ_p and ΔE are estimated to be 10^{-12}-10^{-11} s and ~10 meV, respectively.

2.3.3 Hopping transport

In organic semiconductors, due to the localization of the charge carriers on defect sites, the charge transport mechanism is mainly based on phonon-assisted hopping from one localized site to another [2, 12, 13]. Such a hopping transport occurs near the Fermi energy and generally leads to low charge carrier mobility. Under zero electric field, the charge carrier transfer rates between sites *i* and *j* will reach a thermal equilibrium. The process can be expressed by following equation:

$$f(\varepsilon_i)\left(1-f(\varepsilon_j)\right)v_{ij} = f(\varepsilon_j)(1-f(\varepsilon_i))v_{ji} \qquad (2.8)$$

where ε is the energy level of the site, v_{ij} is the transfer rate from site *i* to site *j*, while v_{ji} refers to the reverse transfer, and *f* is the Fermi-Dirac distribution. And we have:

$$f(\varepsilon_i,\eta) = 1/\left[1+exp\left(\frac{\varepsilon_i-\eta}{kT}\right)\right] \qquad (2.9)$$

The equilibrium condition can then be expressed as:

$$\frac{v_{ij}}{v_{ji}} = exp\left(-\frac{\varepsilon_j - \varepsilon_i}{kT}\right) \qquad (2.10)$$

To date, dozens of different hopping transport models have been proposed basing on varied physical principles and approximations. One of the most commonly used hopping models is that developed by Bassler [14]. It relies on the following assumptions: (1) the electronic polarization energy of a charge carrier on a molecule is subject to fluctuations; (2) transport occurs through hopping among localized states whose density of states (DOS) is described by a Gaussian distribution of variance σ; (3) charge transport is random walk described by a generalized master question of the Miller-Abrahams form [15]:

$$v_{ij} = v_0 exp(-\gamma|R_{ij}|)\begin{cases} exp\left(-\frac{\varepsilon_j - \varepsilon_i}{kT}\right) & \varepsilon_j > \varepsilon_i \\ 1 & \varepsilon_j \leq \varepsilon_i \end{cases} \qquad (2.11)$$

where v_0 is the hopping attempt frequency, γ is the inverse localization length and R_{ij} is the intersite distance; and (4) position disorder with a Gaussian distribution of variance Σ is existed in addition to the energetic disorder. From a Monte Carlo simulation, Bassler finally derives a universal law that relating the mobility to the Σ through:

$$\mu = \mu_0 exp\left[-\left(\frac{2}{3}\frac{\sigma}{kT}\right)^2\right] exp\left|C\left(\frac{\sigma}{kT}\right)^2 - \Sigma^2\right|\sqrt{F} \qquad (2.12)$$

where C is an empirical constant and F is the electric field. The main feature of hopping mechanism is the temperature dependence of the mobility, which increases with increasing the temperature.

2.3.4 Multiple trapping and thermal release (MTR) model

The multiple trapping and thermal release (MTR) model was developed by Comber *et al.* to account for the mobility in hydrogenated amorphous silicon [16]. The model is built up based on the assumption that charge carrier transport occurs in extended states, but the majority of the injected carriers in the semiconductor are trapped in states localized in the forbidden gap. These traps can be deep or shallow, depending on the position of their energy level, as described in Fig. 2.7.

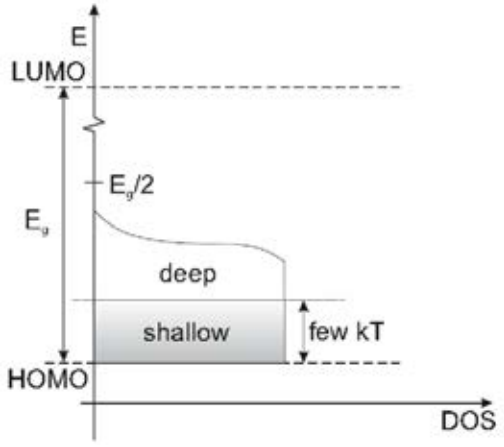

Fig. 2.7 Distribution of trap states in the band gap. Taking p-type semiconductor as an example, shallow traps energy is just few kT above the valence band.

Later, it was further developed by Horowitz *et al.* to understand the charge transport in well-ordered OFETs [17]. It differentiates the energy levels into localized levels and transport band which are separated by a mobility edge that represents the boundary between them. The model also assumes that the majority of the carriers injected into the semiconductor are immediately trapped by trap levels with a probability close to one. These trapped charge carriers then undergo thermally detrapping and are released to transport band where they can move freely and contribute to the conduction, until they are trapped again by other trap levels [4]. Fig. 2.8 gives a brief illustration on the mechanism. The drift mobility in organic semiconductor can be described as:

$$\mu_D = \mu_0 \alpha exp\left(\frac{\varepsilon_T}{\kappa T}\right) \qquad (2.13)$$

where α is the ratio between the effective density of states at the transport band edge and the density of traps, ε_T is the energy of the trap state and μ_0 is the mobility at the band edge.

Fig. 2.8 Illustration of charge transport mechanism of multiple trapping and thermal release [4].

On the other hand, the conductivity of the organic semiconductor can be calculated by following equation:

$$\sigma = \mathrm{e} \cdot n_f \cdot \mu_0 \qquad (2.14)$$

where n_f is the concentration of free carriers, μ_0 is the microscopic mobility and e represents the electronic charge. Here we introduce a new parameter, θ, which represents the fraction of free charges:

$$\theta = \frac{n_f}{n_{tot}} \; ; \; n_{tot} = n_f + n_t \qquad (2.15)$$

where n_{tot} is the concentration of total charges and n_t is the concentration of trapped charges. Equation 2.15 can be rewritten as:

$$\sigma = e \cdot n_{tot} \cdot \theta \cdot \mu_0 \qquad (2.16)$$

Equation 2.16 reveals that a thermally-activated conductivity can be interpreted

either by a thermally activated mobility μ that equals $\theta \cdot \mu_0$ and a constant charge density n_{tot}, or by a thermally activated charge density n_f that equals $\theta \cdot n_{tot}$ and a constant mobility μ_0. In this case, the field-effect mobility at low-gate bias equals the effective mobility μ, and is therefore thermally activated, whereas it approaches the slow variation of the mobility μ_0 at high V_G.

The success of the MTR model relies on its ability to account for temperature and gate voltage dependent mobility. However it often gives abnormally high density of trap states. This is due to the fact that the MTR model is valid only for a trap distribution consisting of a shallow distinct energy level close to the main transport band.

2.4 Parameters extraction

The electrical performance of an OTFT is characterized by parameters including field-effect mobility (μ), threshold voltage (V_T), on/off current ratio and subthreshold swing (SS). The contact resistance (R_C) is another important parameter in OTFTs. In this section, we will give a brief discussion on the extraction of these parameters.

2.4.1 Current-voltage (*I-V*) characteristics

Because the drain current (I_{DS}) is modulated by two independent voltages, i.e., the drain voltage (V_{DS}) and the gate voltage (V_{GS}), current-voltage (*I-V*) characteristics can be represented by two ways. In the first way, the V_{DS} is set as constant, we can get the relationship of I_{DS} versus V_{GS}, and the resulting curve is called transfer curve. In the second way, we can obtain a set of curves of I_{DS} against V_{DS} at several discrete V_{GS} values, and the obtained curves are called output curves. Fig. 2.9 exhibits representative transfer curve and output curves of a pentacene TFT. From the output curves, the linear region and saturation region can be clearly observed.

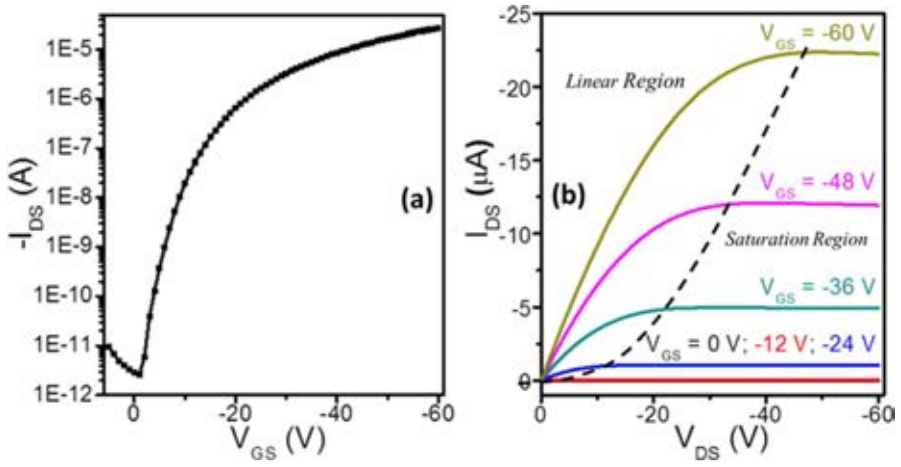

Fig. 2.9 Representative transfer curve (a) and output curves (b) of a pentacene TFT.

2.4.2 Field-effect mobility (μ) and threshold voltage (V_T)

As having been discussed in Section 2.2.1, there are two different working regions in an OTFT, i.e., linear region (small V_{DS}) and saturation region (high V_{DS}). In linear region, the current-voltage (*I-V*) relationship can be expressed by the following equation:

$$I_{DS} = \frac{W}{L}\mu C_i(V_{GS} - V_T)V_{DS} \qquad (2.17)$$

By analyzing the above equation, it is clear that the field-effect mobility in the linear region can be extracted from the transconductance (g_m) (defined by the change of I_{DS} with V_{GS}) at constant V_{DS}. Through conducting such manipulation, we can obtain:

$$g_m = -\frac{\partial I_{DS}}{\partial V_{GS}}\Big|_{V_{DS}=constant} = -\frac{W\mu WC_i}{L}V_{DS} \qquad (2.18)$$

Therefore, the linear mobility μ deduced from Equation 2.18 is given by:

$$\mu = -g_m \frac{L}{W}\frac{1}{C_i}\frac{1}{V_{DS}}\Big|_{V_{DS}=constant} \qquad (2.19)$$

The V_T in linear region can be obtained by fitting the transfer curve to a linear curve, and the intercept in the horizontal axis gives the value of V_T, as depicted in Fig. 2.10a.

In saturation region, on the other hand, the *I-V* relationship is described by:

$$I_{DS} = \frac{W}{2L}\mu C_i(V_{GS} - V_T)^2 \qquad (2.20)$$

The above equation reveals that the square root of $|I_{DS}|$ is linearly dependent on the V_{GS}. Therefore, if we plot $(|I_{DS}|)^{1/2}$ as a function of V_{GS}, μ can be extracted from the slope of the curve (K) as shown in Fig. 2.10b. As a result, μ can be calculated through following equation:

$$\mu = \frac{2L}{W}\frac{1}{C_i}K^2 \qquad (2.21)$$

In saturation region, V_T can be obtained by extrapolating the linear fit of $(|I_{DS}|)^{1/2}$ versus V_{GS} curve to the horizontal axis, as described in Fig. 2.10b. Considering the realistic application of OTFTs, it is desirable to keep the V_T close to 0 V. V_T can originate from several effects, such as built-in dipoles, impurities, interface states and in particular, charge traps in semiconductors and dielectric layers also contribute to the V_T [18]. V_T can be reduced by increasing the gate capacitance and, as a result, induces more charges at lower applied gate voltages.

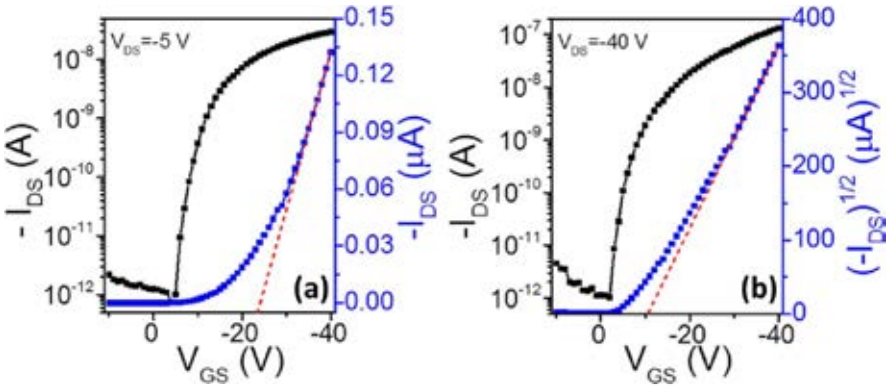

Fig. 2.10 Representative transfer curves of OTFT in (a) linear region and (b) saturation region.

2.4.3 On/off current ratio and subthershold swing (*SS*)

On/off current ratio, also referred to on/off ratio for short, is an important parameter that characterizes the ability of a transistor to switch a signal from "off" to "on". It can be extracted from the transfer curve of an OTFT, and equals to the ratio between the on-state current (I_{on}) and the off-state current (I_{off}), as shown in Fig. 2.11. The on/off ratio is thus defined by:

$$on/off\ ratio = \frac{I_{on}}{I_{off}} \qquad (2.22)$$

Generally, on/off ratio should be as large as possible in order to get a nice switching behavior. Typical values of on/off ratio for OTFTs range from 10^3 to 10^8.

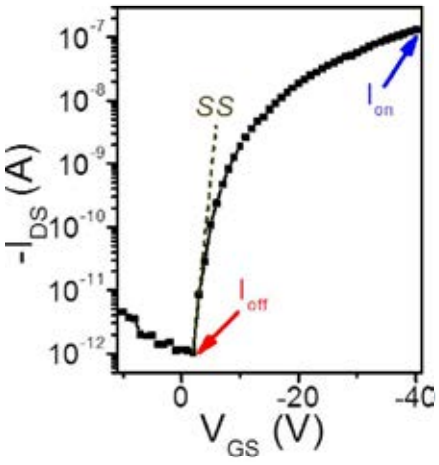

Fig. 2.11 Schematic of determining on/off state current and the subthreshold swing (*SS*) from transfer curve.

Subthreshold swing (*SS*) characterizes the speed of a transistor switches from the off-state to the on-state. *SS* can be extracted from the transfer curve by fitting a straight line to the steepest part in the subthreshold region and calculating its reciprocal, as illustrated in Fig. 2.11, and is therefore defined as:

$$SS = \frac{\partial V_{GS}}{\partial(log|I_{DS}|)} \qquad (2.23)$$

The lower limit of *SS* is about 60 mV/dec [19]. The smaller the value of *SS* is, the better the switching property an OTFT has.

2.4.4 Contact resistance (R_C)

Unlike the above parameters that can be extracted directly from the transfer curve, the contact resistance (R_C) of an OTFT is an implicit parameter which cannot be obtained from simple *I-V* curve. The *I-V* characteristics discussed in previous sections are based on the assumption that the contacts at source and drain are ohmic, meaning negligible resistance as compared to the channel. However, this is not fulfilled in a realistic transistor. In general, the typical contact resistances in OTFTs are in the range of 10 kΩcm -10 MΩcm [20, 21], which are significantly larger than those found in inorganic counterpart. High contact resistance generally leads to a considerable voltage drop at the source-drain contacts, resulting in a decrease of the apparent field-effect mobility and an increase of the threshold voltage. Such effects are often observed in short channel devices.

2.1.1.1 Origin of contact resistance

When travelling from the source to drain, the movement of charge carriers will be blocked by several resources. Taking a bottom-gate top-contact pentacene TFT as an example (as shown in Fig. 2.5a), the blocking resources include: (1) the injection barrier in the source electrode/pentacene interface, (2) resistance arises from the

thickness of pentacene film, referred to access resistance, (3) resistance corresponds to the length of the channel, (4) resistance again comes from the access resistance and (5) extraction barrier in the drain electrode/pentacene interface. These resources can be simply regarded as three transistors in series. The resistances caused by the carrier injection and the access to channel in the source contact can be grouped into source contact resistance (R_S), and the resistance associated with crossing the channel is called channel resistance ($R_{channel}$), and the third resistance resulted from the opposite process as the source contact is termed drain contact resistance (R_D). In convention, the term contact resistance (R_C) is always used, and it represents the sum of R_S and R_D. To realize ohmic contact in OTFTs, it is crucial to make sure that the R_C is much smaller when compared to $R_{channel}$.

From modern semiconductor physics, it is known that creating an ohmic contact requires a perfect band alignment between the metal work function (W_F) and the energy levels of the semiconductor, which follows the Mott-Schottky rule [19]. Thus, the electronic structure at the metal/organic semiconductor interface plays an important role in determining the charge injection and extraction characteristics of the contact. However, even though good alignment in energy level, many metal-organic semiconductor interfaces do not follow the Mott-Schottky rule, which is mainly due to

the interface dipole induced in the interface during the fabrication of devices, and such dipole is commonly observed in Au/pentacene interface [22, 23]. The interface dipole (Δ) will shift the vacuum level of the semiconductor with respect to the metal, thus resulting in an increase in the injection energy barrier. To solve this problem, interface engineering, such as self-assembled monolayer (SAM) modification [24], inserting a buffer layer between contact and semiconductor [25, 26] or using metal-oxide with preferred energy bands [27], have been used to optimize the metal/organic semiconductor interface properties, and many promising results have been achieved.

The access resistance can be simply minimized by optimizing the device structure. The deposition of metal on organic semiconductor usually gives rise to a much lower contact resistance than expectation, which can be ascribed to the penetration of metal atoms into the organic semiconductor, and sometimes even extends to the channel region [28]. This can be regard as a reduction in access resistance. On the other hand, deposition of organic semiconductor on metal surface often exhibits high disorder in film structure in the vicinity of the contacts, which then leads to an increase in access resistance [29]. The channel dimension also plays an important part in influencing the contact resistance. As discussed previously, in ohmic contact, the contact resistance is much smaller as compared to the channel resistance. To ensure this condition, one must

be careful when scaling the device, because the contact resistance in short-channel devices can quickly become the dominating resistance. In addition, to avoid the fringing field effect at the edges of the channel, the W/L of a transistor should always be ≥ 10.

2.1.1.2 Extraction of contact resistance

In general, there are three methods that most commonly used to extract the contact resistance. We will give a brief introduction of these methods in this section.

2.1.1.2.1 Transfer line method (TLM)

A key feature of the contact resistance is the superlinear output characteristics at low drain voltages. At this region, the total resistance R_{total} for a given channel length L can be expressed as:

$$R_{total} = \frac{\partial V_{DS}}{\partial I_{DS}}\Big|_{V_{DS}\to 0} = R_{channel} + R_C \qquad (2.24)$$

In the above equation, $R_{channel}$ is positively proportional to the channel length. As a result, one can quantitatively measure the contact resistance of OTFT by extrapolation, and further differentiate these two resistances. The first step is to fabricate a series of

devices with different channel length (the channel width is unchanged) on the same semiconductor film, then measure the total resistance in linear region (small V_{DS}) and plot the resistance against channel length. By linear extrapolating the obtained plot to L = 0 which eliminates the channel resistance, one can estimate the contact resistance directly from the intercept of vertical axis. This method is known as the transmission line method (TLM) [30, 31]. Because the contact resistance is closely connected with the channel width, it is more practical to use channel width normalized resistance (defined by $R{\cdot}W$) instead [32, 33]. Fig. 2.12 shows an example of a normalized resistance ($R{\cdot}W$) versus channel length (L) plot, and the $R_C{\cdot}W$ can be determined by extrapolating the fitted line to L = 0. In addition, the linear region mobility can be calculated from the slop of the fitting line [32].

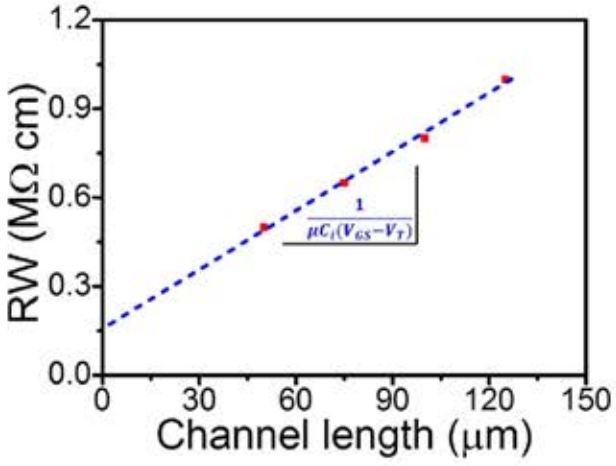

Fig. 2.12 Illustration of transfer line method (TLM).

This method has been widely used to extract the contact resistances in OTFTs because of its simplicity. However, it has its own disadvantages. On one hand, a lot work needs to be done in order to fabricate and test a series of transistors with different channel length. On the other hand, it cannot be taken for granted that all the transistors have similar channel and contact characteristics, such as, morphology, defects density and crystal orientation, even if they are fabricated in the same run. Finally, it cannot separate the contact resistances at the source and the drain electrodes individually.

2.1.1.2.2 Gated four-probe technique

As mentioned in the previous section, the TLM method cannot give the respective value of source and drain contact resistance. An alternative method to TLM is the gated four-probe technique, which consists of introducing two additional narrow, voltage sensing electrodes that slightly protruding into the channel, as depicted in Fig. 2.13 [28]. Electrical characterization is then carried out by sweeping the drain voltage V_{DS} at a constant gate voltage V_{GS} or sweeping V_{GS} at a constant V_{DS} while monitoring the drain current I_{DS} and probe potentials V_1 and V_2. In the linear region of OTFT operation ($|V_{DS}| << |V_{GS} - V_T|$), the charge carrier density in the channel is assumed to be

uniform and exhibits a linear drop with electrostatic potential along L from source to drain. Therefore, with the values of V_1 and V_2, a linear extrapolation of the potential profile to each contact is performed, and the potential drops at each contact, ΔV_S and ΔV_D, can be calculated by following equations:

$$\Delta V_S = 2V_1 - V_2 \qquad (2.25)$$

$$\Delta V_D = V_D - (2V_2 - V_1) \qquad (2.26)$$

With the known I_{DS}, hence, the contact resistance at each contact can be directly calculated through equations:

$$R_S = \frac{\Delta V_S}{I_{DS}} \qquad (2.27)$$

$$R_D = \frac{\Delta V_D}{I_{DS}} \qquad (2.28)$$

where R_S and R_D are the contact resistance at the source and drain electrode, respectively.

As seen, the gated four-probe technique can isolate the contribution of source and drain contact from the total contact resistance, and it is relatively simpler than the TLM method since it can determine the R_C using only one device. However, it is important to keep in mind that a crucial limitation for the gated four-probe technique is that the

validity of the extrapolated channel potential profile will be restricted in the linear region of OTFT operation, where the channel potential drop can be expected to be linear along the channel.

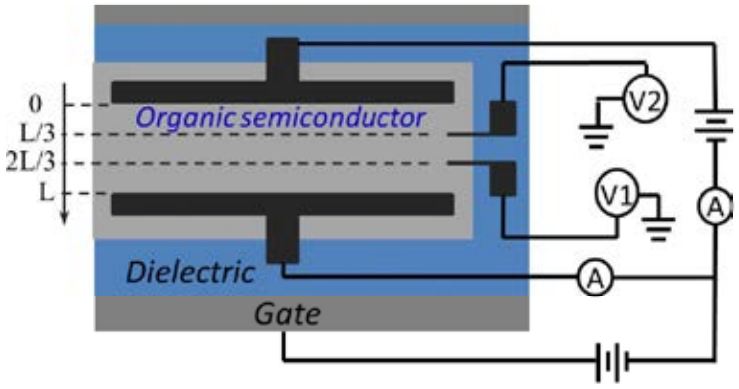

Fig. 2.13 Illustration of gated four-probe technique.

2.1.1.2.3 Kelvin probe force microscopy (KPFM)

In the previously described techniques, extrapolation of measured data is required in order to obtain the contact resistance. An even more powerful method that uses an atomic force microscope (AFM) tip to probe the potential along the channel of the transistor is develop, which is called Kelvin probe force microscopy (KPFM) [34, 35]. Fig. 2.14 shows the experimental setup of KPFM. During experiment, a conductive AFM tip scans over the working OTFT channel twice. On the first run, the surface morphology of the device is recorded; on the second run, the tip is pulled a small

distance (~10 nm) away from the device and then retraces the channel while recording the electrostatic potential simultaneously. The electrostatic potential data are then converted into the surface potential profile of device, as shown in Fig. 2.14. Through the potential drops ΔV_S and ΔV_D at source and drain interfaces, one can calculate the respective contact resistance by the following equations:

$$R_S = \frac{\Delta V_S}{I_{DS}} \qquad (2.29)$$

$$R_D = \frac{\Delta V_D}{I_{DS}} \qquad (2.30)$$

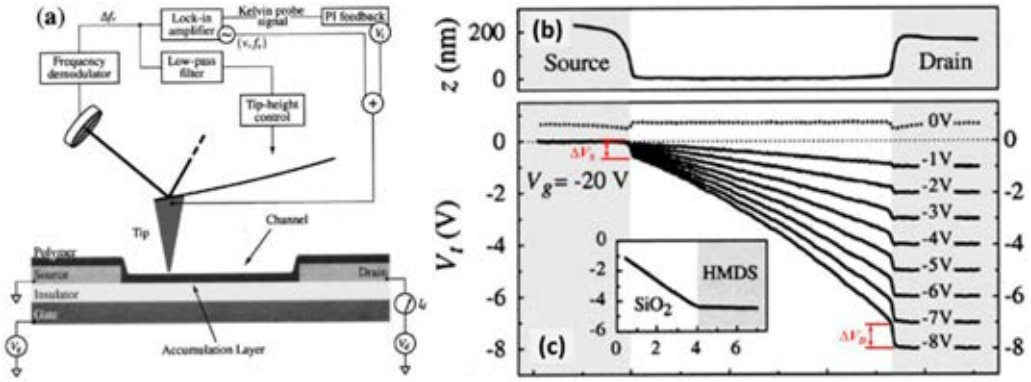

Fig. 2.14 (a) Schematic diagram of the experimental setup and the TFT structure, (b) topographic profile of the device along the channel direction and (c) plots of potential profiles as a function of drain voltage [34].

It is clear that the KPFM has an obvious advantage over the gated four-probe technique because it can record the entire channel potential profile in time instead of extrapolating a linear profile through only two points (see Fig. 2.13 and Fig. 2.14 as a comparison). In addition, more detailed information about the potential variations at grain boundaries in the channel can also be obtained by this technique.

2.5 Gate dielectrics

The operation of OTFTs is based on the well-known "metal-oxide-semiconductor" (MOS) structure which has been extensively studied in Si based electronics [19]. In this structure, the oxide serves as an insulating layer, i.e., dielectric layer, which controls the formation of conducting channel in the organic semiconductor. As a result, the properties of the dielectric layer are of great importance in influencing the device performance.

Due to the inherently low mobility of organic semiconductors, the S/D current in OTFTs is usually in the order of $< 10^{-4}$ A. As a result, to make the device working properly, the dielectric layer must show a low leakage, which is required to be at least one order of magnitude lower than that of S/D current. Defects, pinholes and cracks in

the dielectric layer can lead to a severe leakage and dielectric breakdown. In addition, the surface roughness of dielectrics also plays an important role in influencing the device electrical characteristics [36-38]. Initial studies of OTFTs are based on thermally oxidized SiO_2/highly doped Si as dielectric/gate electrode pair, mainly due to the fact that they are well established in amorphous Si TFTs, and they are commercially available with high quality, including low leakage, high breakdown voltage and low roughness. However, with the impressive development of the OTFTs achieved in recent years, drawbacks of this system have been increasingly revealed. On one hand, the fabrication of thermally oxidized SiO_2 requires high temperature, which is energy consuming and incompatible with flexible plastic substrate. On the other hand, due to the low dielectric constant of SiO_2, the capacitance density is usually very small. Consequently, a high voltage, typically larger than 30 V is needed to drive the device, which is unacceptable for low-end applications, such as RF-ID cards, potable sensors, e-papers, and so on.

Achieving high capacitance density in OTFTs is of great importance, considering the low intrinsic mobilities of the organic semiconductors and the requirements in the low-end applications in which low driving voltage is a prerequisite. At the same time, keeping the leakage currents as low as possible can reduce the power consumption in

devices [39], and easy processing of dielectric materials is of technical importance when planning the commercialization in real world. In these regards, convenient, low-cost solution-based methods to produce novel gate dielectrics are highly desired, especially in high throughput fabrication, such as ink-jet printing and role-to-role production.

The areal capacitance of gate dielectric can be simply expressed by:

$$C_i = \frac{\varepsilon_0 k}{d} \qquad (2.31)$$

where ε_0 is the permittivity of vacuum, k is the relative permittivity of the gate dielectric and d is the thickness of gate dielectric. As seen, by either decreasing d or increasing k, one can get an increased C_i. For the former approach, researchers have used very thin organic dielectrics, including self-assembled monolayers (SAMs) and polymers to realize high areal capacitance [40-43]. The advantages of using organic dielectrics are that they can be processed through solution based technology at low temperature. However, they also show some inherent drawbacks. For SAMs, because they are sensible to the processing environment, especially water vapor, peculiar carefulness must be paid in producing this kind of dielectrics. On the other hand, due to the extremely thin thickness of SAMs (typically 2~3 nm), it is hard to control the quality,

because a single defect can leak to a direct leakage. In addition, they have difficulties in integration with large area flexible substrates. For polymers, because the low dielectric constants they have (usually < 3), the thickness of this layer must be controlled in precision in order to decrease the leakage current. At the same time, to obtain high quality thin film, extra polymerization is usually needed [44].

On the other hand, the application of high-*k* dielectrics, such as TiO_2 [45], Al_2O_3 [46], HfO_2 [47] and ZrO_2 [48], is a promising alternative to achieve high gate capacitance, since they can easily maintain low leakage with a moderate thickness. More importantly, they can be solution-processible [49, 50], which is highly desired for high throughput fabrication. In addition, the unfavorable hydroxyl groups (OH^-) present in the surface of native oxides can be easily passivated by introducing SAMs or thin layers of polymers [51, 52].

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Chapter 3 Materials and Experimental Techniques

This chapter will introduce the materials, device fabrication details and characterization methods used in this thesis.

3.1 Materials

All the materials used in this thesis are bought from Sigma-Aldrich.

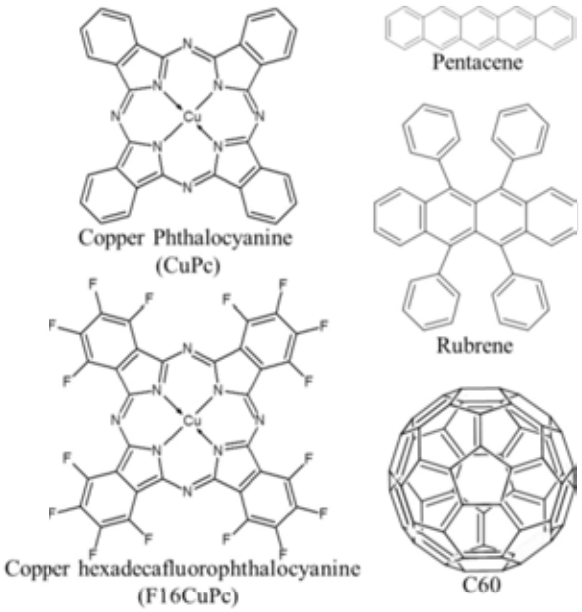

Fig. 3.1 Chemical structures, full names and abbreviations of organic semiconductors used in this thesis.

The chemical structures, full names and abbreviations of the organic semiconducting materials used in this thesis are shown in Fig. 3.1. Copper phthalocyanine (CuPc) (80%) and copper hexadecafluorophthalocyanine (F_{16}CuPc) (80%) are purified twice by gradient temperature sublimation under a high vacuum (<10^{-4} Pa) before use. Pentacene (≥99.9%), rubrene (≥98%), C60 (≥99%) are used as received without further purification.

The TiO_x precursor is titanium(IV) isopropoxide (TIP), $Ti(OC_3H_7)_4$, with a molecular weight of 284.22 and a purity of 99.999%. The Al_2O_y precursor is aluminum nitrate nonahydrate, $Al(NO_3)_3{\cdot}9H_2O$, with a molecular weight of 375.13 and a purity of 99.997%.

Solvents, including 2-methoxyethanol, acetic acid, acetone, ethanol, isopropanol, and methanol, are used as received. The detailed information of these solvents is summarized in Table 3.1.

Table 3.1 List of physical properties of solvents used in this thesis.

Name	Molecular formula	Molecular weight	Assay (%)	Boiling point (℃)
2-methoxyethanol	CH3OCH2CH2OH	76.09	99.8	124
Acetone	CH3COCH3	58.08	99.9	56
Acetic acid	CH3COOH	60.02	99.7	117
Ethanol	CH3CH2OH	46.07	99.9	78
Isopropanol	(CH3)2CHOH	60.1	99.5	82
Methanol	CH3OH	32.04	99.8	65

Heavily n-doped Si wafers with 300 nm thermally oxidized SiO_2 (n^{++}-Si/SiO_2) on surface are used as the substrates for ordinary devices. 125 μm thick polyimide (PI) membranes are used as substrates for flexible devices.

The electrodes materials, including gate electrodes and source-drain (S/D) electrodes, are Al, Ag, Au, Cr and Cu. Assays of these metals are 99.99%.

Octadecylphosphonic acid (ODPA) serves as a self-assembled monolayer (SAM) chemistry with an assay of 98%. Its molecule structure is given in Fig. 3.2.

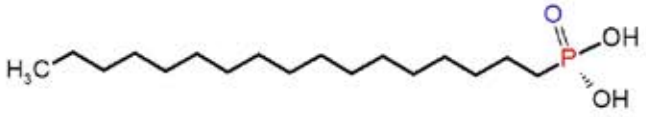

Fig. 3.2 Molecule structure of octadecylphosphonic acid (ODPA).

3.2 Device fabrication procedures

TiO_x sol is prepared by solving TIP in a mixture of methanol and acetic acid with a typical volume ratio of 1:30:1 for TIP:methanol:acetic acid. The solution is sealed and then vigorously stirred by magnetic stirrer for 12hrs before use.

Al_2O_y sol is prepared by solving aluminum nitrate nonahydrate in 2-methoxyethanol with a typical concentration of about 0.5 Mol/L. The sol is then sealed and stirred for 12hrs before use.

n^{++}-Si/SiO_2 wafers are firstly cut into small pieces with size of 1.25 cm × 1.25 cm, and then cleaned by acetone, isopropanol and ethanol successively in ultrasonic bath for 10 min in each round, followed by blowing dry with N_2 before use.

Metal-oxide dielectric is fabricated by a two-step procedure. At first, the TiO_x sol is spin coated onto n^{++}-Si/SiO_2 substrates at 5000 r/min for 40 s, and then baked at 200 ± 5 ^oC for ~ 3 min on a hotplate. Secondly, the Al_2O_y sol is then spin coated onto the above substrates and then baked at the same condition as that of TiO_x. The obtained dielectric layer is constructed by a double layer system, i.e., Al_2O_y/TiO_x, and it is referred to ATO for short thereafter. For SAM modification, the ATO substrates is immersed into an ODPA-isopropanol solution (~ 5 mMol/L) for 17 hrs under sealed condition, and then washed by isopropanol ultrasonically for 6 min. After washing, the substrates are then blown dry with N_2. The SAM modified ATO substrates are referred to ODPA/ATO for short thereafter.

PI substrates are cut into pieces with dimension of 2 cm × 2 cm and then cleaned by

isopropanol and ethanol ultrasonically for 10 min in each round before use. 5nm Cr and 30 nm Au are deposited onto the substrates via thermal evaporation under vacuum (5×10^{-4} Pa) with a rate of 0.3 Å/s. After that, the ODPA/ATO is fabricated by the same method introduced previously, the only difference is that Al_2O_y sol is spin-coated at 4000r/min for 20s.

Thin film devices are fabricated by thermally evaporation of organic semiconductors (CuPc, F_{16}CuPc, pentacene and C60) and the S/D electrodes onto the substrates and detailed experimental parameters will be discussed in the corresponding chapters. Rubrene single crystal are grown on the substrates by a physical vapor transportation (PVT) method [1]. The S/D electrodes are defined by placing two Au film onto the rubrene single crystal [2].

3.3 Characterization

3.3.1 Electrical performance testing

Both the leakage and capacitance of the devices are tested based on the n^{++}-Si/dielectric/Au (MIM) structure. The leakage is examined by Keithley 4200 SCS, and the capacitance is obtained by HP 4284A in a frequency range from 20 Hz to 1M

Hz.

The electrical characteristics of the transistors are tested by the Keithley 4200 SCS on a probe station. The gate electrode of the device fabricated on n^{++}-Si substrate is defined by scribing the substrate with a diamond pen. The transfer curves are obtained by sweeping V_{GS} at a constant V_{DS}, and the output curves are obtained by sweeping V_{DS} at a set of different V_{GS} values.

3.3.2 Atomic force microscope (AFM)

The morphology of the dielectrics and the organic semiconductors are characterized by atomic force microscope (AFM, Nanoscope IIIa).

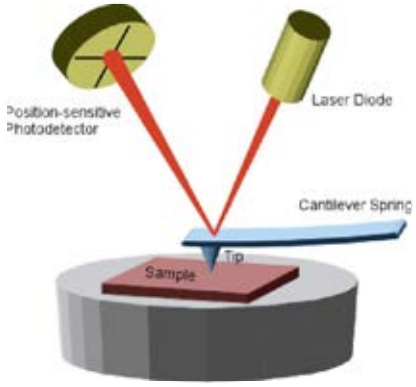

Fig. 3.3 Working principle of atomic force microscopy (AFM) [3].

The working principle of AFM is measuring a deformation of a cantilever while

scanning over a sample surface. A sharp tip, with radius of usually less than 10 nm, is mounted at the end of the cantilever, whose length ranges between 100 μm and 200 μm. An incident laser beam is reflected to a position-sensitive photodetector (4-field diode) by the cantilever, and consequently, the deformation can be measured by the detector, as illustrated in Fig. 3.3 [3, 4]. In order to increase the laser reflection yield, the cantilever backside is usually coated with Au or Pt. Static deformation of the cantilever due to the interaction between the tip and the sample surface can therefore be used for the surface investigation [5]. The photodetector allows us to measure the sample surface normal force by analyzing the current difference in the vertical segments and parallel force through the horizontal segments. A piezoelectric dynamic feed-back system allows not only the height measurements but also constant-height scanning with pm accuracy.

The most commonly used AFM operation modes are tapping mode and contact mode. In tapping mode, the cantilever oscillates at its resonance frequency and bounces up and down on the sample surface. And the photodetector records the signal of cantilever deformation caused by the attractive interaction between tip and sample surface. This mode is relatively slow in getting the surface information, but it can protect the sample against destroying by the tip. While in contact mode, the tip is placed

near to the sample surface with distance of sub-nanometer, and the photodetector records the deformation of the cantilever caused by the repulsive force between tip and sample surface. A severe drawback of contact mode is that the sample surface is easily damaged.

3.3.3 Kelvin probe force microscopy (KPFM)

Kelvin probe force microscopy (KPFM) is a well-established technique to measure the contact potential differences (CPDs) between a reference electrode and a sample [6-8]. The KPFM technique is developed on the basis of AFM. In KPFM, two conductors (the cantilever tip and sample) placing in a small distance can be simply viewed as a parallel plate capacitor. The contact potential difference between the two materials is expressed by the following equation [9]:

$$V_{CPD} = -(\emptyset_1 - \emptyset_2)/e \qquad (3.1)$$

where $\emptyset_1$ and $\emptyset_2$ are the work functions of the tips and samples, respectively, e is the electron charge. The mechanical oscillation of cantilever, at frequency ω, will induce changes in the distance between the two materials, and hence the capacitance is

changed accordingly. Consequently, the periodic vibration of the distance between the tip and sample at ω will induce an alternating current $i(t)$ given by:

$$i(t) = V_{CPD}\omega\Delta C \cos \omega t \qquad (3.2)$$

where ΔC is the variation in capacitance. We can apply an external bias (V_{bias}) to neutralize this current, as can be seen form the following equation:

$$i(t) = (V_{bias} + V_{CPD})\omega\Delta C \cos \omega t = 0 \qquad (3.3)$$

The KPFM technique depends on measuring zero $i(t)$ with the application of external V_{bias} between the two plates to eliminate the electric field. Thus, CPD can be determined by $V_{CPD} = -V_{bias}$.

KPFM has been widely used in studying the electrical properties of organic electronic devices, e.g., contact resistance and defects in grain boundary. Despite the superior spatial resolution with relatively high energy sensitivity as compared with other techniques, KPFM still has some disadvantages. First, before measuring the absolute surface potential of a sample by KPFM, the work function of the probe must be known ahead. Second, it can only give the variations of molecularly averaged surface potential when absorbents present in a semiconductor sample surface. Third, an

abrupt morphological height change can disturb the precision of KPFM. Fourth, a relatively long time, usually one or two hours, is needed to acquire a surface potential image of the sample [8].

3.3.4 X-ray diffraction (XRD)

Many materials are assembled in crystallized structure, which means their atoms are arranged in periodical 3-dimensional (3D) arrays. These crystals are constructed by unit cells through which the smallest number of atoms repeats to form the whole 3D array. Depending on their symmetry, the unit cells can be cubic, triclinic, monoclinic, hexagonal, or some other types. The sizes of these unit cells are called the lattice constants. Taking cubic cell as an example, the structure can be clearly defined just by one parameter, i.e., the distance between two nearest atoms, we refer it as a_0. There exists a series of parallel plains containing atoms with different areal density in the 3D cubic system. Each set of parallel plains can be labeled by a unique Miller index, (h k l). The distance (d_{hkl}) between a certain (h k l) plain can be calculated by the following equation [10]:

$$d_{hkl} = \frac{a_0}{\sqrt{h^2+k^2+l^2}} \qquad (3.4)$$

Early in 1913, Bragg *et al.* developed a theory to explain why the cleavage faces of crystals appear to reflect X-ray beams at certain angles of incidence (θ) [11], as given in:

$$n\lambda = 2dsin\theta \qquad (3.5)$$

where d is the distance between the parallel atomic layers in a crystal, λ is the wavelength of the incident X-ray beam, and n is an integer. This observation is an example of X-ray wave interference, which is known as "Bragg's law". By combining the above two equations, one can see that the X-ray diffraction technique can be used to determine the lattice parameters of a crystal.

Two theories are involved in using Bragg's law to determine the lattice parameters. The first theory is the interference of waves. When two waves, whose wavelength and frequency are the same, propagate in parallel, the resulting wave is the superposition of the two waves. If the two waves are in phase, the amplitude of the resultant wave will be the sum of the two amplitudes. On the contrary, if they are 180° out of phase, the resultant amplitude is the difference between the two amplitudes, i.e., they would cancel each other out. The other theory is the simple trigonometry, as depicted in Fig. 3.4. When two waves are reflected by two parallel lattice planes, one wave will travel a

longer distance ($2l$) than the other. The distance $2l$ can be related to the space between the two planes (d), and the angle between the incident wave and lattice plane (θ). As can be seen from Fig. 3.4, the relationship between l, d and θ can be expressed by:

$$l = d \sin\theta \qquad (3.6)$$

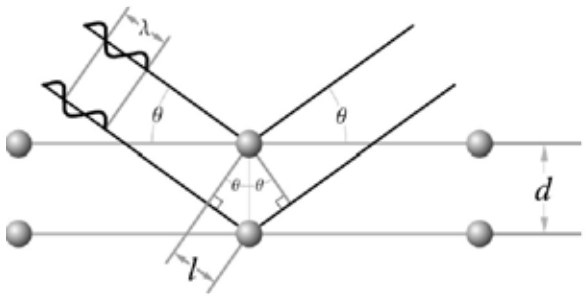

Fig. 3.4 Illustration of determining lattice plane space through Bragg's law.

In case of $2l$ is exactly equal to one wavelength (λ) or any integral multiples of λ (i.e. $n\lambda$), the two waves will propagate parallelly in phase again, and accordingly a constructive interference occurs. As a result, the above equation can be changed to:

$$d = \frac{n\lambda}{2\sin\theta} \qquad (3.7)$$

The most common mode used in X-ray diffraction techniques in the θ-2θ geometry. From the peaks of the X-ray diffraction pattern, one can easily identify the compound species, the crystal phases and the lattice constants. At the same time, it allows one to estimate the average volume crystallite size (D) through Scherrer equation [12]:

$$D = \frac{K\lambda}{\beta \sin\theta} \qquad (3.8)$$

where K is a particle shape-related constant and equals to 0.9 by convention, and β is the full width at half maximum (FWHM) of the diffraction peak.

3.3.5 Grazing incidence X-ray diffraction (GIXD)

Traditional X-ray diffraction has been used for decades to characterize the structure of bulk crystalline materials due to the weak interaction between X-ray and matter, negligible multiple scattering and long penetration depth (typically on the order of 0.1 - 10 mm) [13]. However, this technique is not sensitive to the surface structure of the materials. Recently, take the advantage of very intense X-ray sources such as synchrotron radiations, the structural analysis on the surface and/or interface of crystallite materials has become possible. One experimental strategy is to use the

so-called grazing incidence geometry, in which total reflection of X-rays by a surface can be achieved when the incident angle is less than a critical angle of the surface. The typical grazing angle is in the range of 0.05–1.5°, dependent on the electron density of the substrate and the energy of the X-rays. At this situation, the sample interacts weakly with the X-rays, and only an evanescent wave can penetrate into and then scatter in it. Therefore, the X-ray intensity is highest at the surface. In addition, it is possible to further increase the surface selectivity by decreasing the incident angle in order to induce faster attenuation of the evanescent wave. Basing on this total reflection phenomenon, Murra *et al.* have develop a new technique for studying the structures of crystal surfaces as well as overplayed interfaces [14], and it is known as grazing incidence X-ray diffraction (GIXD), which is also referred to as grazing incidence x-ray scattering (GIXS). GIXD has been commonly used to characterize "in-plane" crystal structures in the surface region, ranging from a few nanometers to several hundred nanometers below the sample surface.

Fig. 3.5 shows the most commonly used geometry setup in GIXD characterization, where a two-dimensional detector is used to record the diffraction of X-ray. The advantage of this geometry is that it allows measuring the "in-plane" and "out-of-plane" crystal structures of the sample at the same time. The analysis of GIXD is based on the

kinetic theory, which is based on two simplified assumptions: (1) the scattering electron density of atoms is spherically symmetrical and (2) the contribution from multiple scattering events is negligible. For two dimensional crystals, condition for diffraction appears in the xy plane is that the horizontal component of the scattering vector, labeled as q_{xy} ($q_{xy} = q_{\parallel} \approx \frac{4\pi}{\lambda} \sin\theta_{hor}$, where $2\theta_{hor}$ is the in-plane angle between the incident beam and the diffracted beam), must be consistent with a reciprocal lattice, as expressed by [15]:

$$q_{xy} = q_{hk} = 2\pi(ha^* + kb^*) \qquad (3.9)$$

where a^* and b^* are the reciprocal in-plane lattice vectors, h and k are the indexes of the reciprocal lattice point. On the other hand, no such restriction exists for the vertical component (labeled as q_z in Fig. 3.10) along the surface normal of the scattering vector, which is defined by:

$$q_z = q_{\perp} = \frac{2\pi}{\lambda} \sin\alpha \qquad (3.10)$$

where α refers to the angle between the diffracted beam and the substrate surface. Consequently, the GIXD patterns obtained from two-dimensional crystals are composed of two-dimensional array of rods, called Bragg rods (BRs), which extend parallel to q_z.

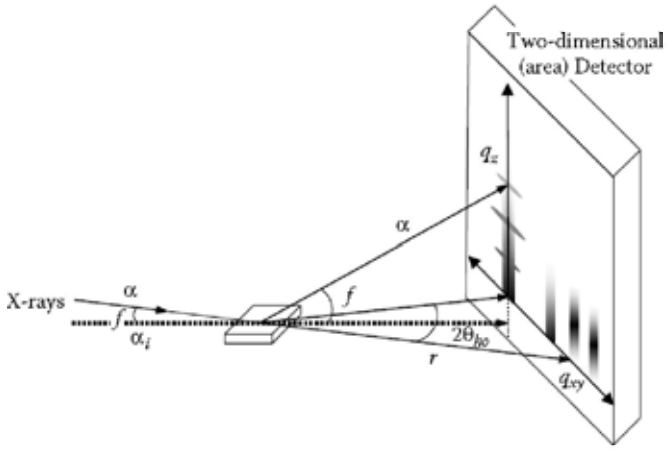

Fig. 3.5 Geometrical illustration of 2-D GIXD [15].

3.3.6 X-ray photoelectron spectroscopy (XPS)

Photoelectron spectroscopy is a widely used technique that usually employed to explore the electronic state and chemical composition of samples. The technique is based on the well-known photoelectric effect first discovered by Hertz in 1887, and then theoretically studied by Einstein in 1905 who for the first time introduced the concept of photon to explain the ejection of electrons from a material surface when exposed to light with certain wavelength. Fig. 3.6 shows the structure of a typical photoelectron spectroscopy experimental setup.

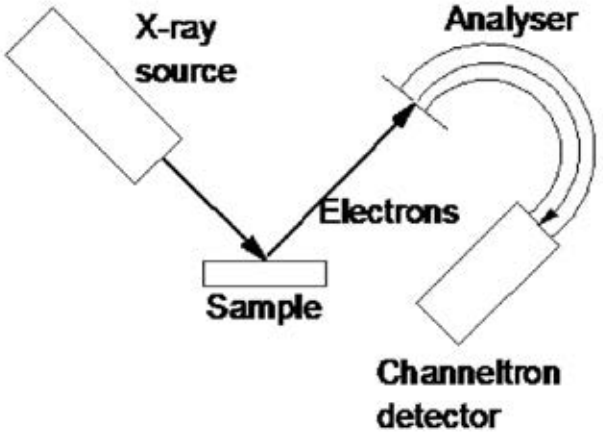

Fig. 3.6 Simplified schematic of photoelectron spectroscopy experimental setup [16].

Photons with energy *hv* irradiate on a sample surface will cause emission of electrons. These electrons with different kinetic energies are collected by an electron lens system and then analyzed by a detector. Conventionally, this technique can be subdivided into ultraviolet photoelectron spectroscopy (UPS) and X-ray photoelectron spectroscopy (XPS) depending on the excitation irradiation source and the excited electron energy. For UPS, UV-light is used as the excitation source, and the resulting emitted valence electron has a kinetic energy of < 40 eV. On the other hand, in XPS, core level electrons with energy > 40 eV are excited by soft X-ray radiation. Generally, a dual anode X-ray gun (Al Ka and Mg Ka) is used as the source of XPS in common laboratory equipment. Although the X-ray has a strong penetration effect into the sample (typically several microns), due to the strong interaction between electrons and matter, only those

electrons with high kinetic energy in the very near surface region (less than 10 nm) can escape from the sample [17]. Such characteristics make XPS a suitable method to explore the surface electronic states of a sample.

Fig. 3.7 shows a schematic illustration on the principle of photoelectron emission. At first, an incident X-ray with energy *hv* collides with a core electron, and then results in the electron to be released from the electronic shell. The kinetic energy (*KE*) of the released electron is directly related to the binding energy (*BE*) of the electron to the nucleus. On the other hand, due to the ejection of electron, there is an unfilled hole in the position of the missing electron. The hole is unstable, as a result, electron from the outer valence shell will fill this unstable hole, leading to emission of a Auger electron in order to conserve the whole energy [18]. Similarly, the kinetic energy of Auger electron is again directly related to the binding energy of the electron to the nucleus. Basing on the fact that each element has a unique set of electron binding energies, the above two processes can therefore be used to identify the elements. By collecting the kinetic energies of electrons, one can calculate the binding energies of electrons through the following equation [19]:

$$BE = h\nu - KE - \varphi_{spec} \qquad (3.11)$$

where φ_{spec} is a correction factor that is dependent on the spectrometer itself. Theoretically, the above equation can be used to calculate the binding energy of emitted electrons. However, this equation varies slightly depending on the conductivity of the samples. For a conducting sample, the calculation of binding energy is exactly the one presented above because the Fermi levels of the sample surface and spectrometer are equivalent. On the other hand, for insulating samples, the above case is no longer true, because a difference in Fermi levels exists between sample surface and spectrometer. As a result, charge accumulation occurs above the sample surface, which results in an upward shift in spectrometer's Fermi level. To correct this phenomenon, the obtained XPS data need to be calibrated to other peaks. The most commonly used calibration peak is Carbon 1s (C1s) at a binding energy of 285.1 V.

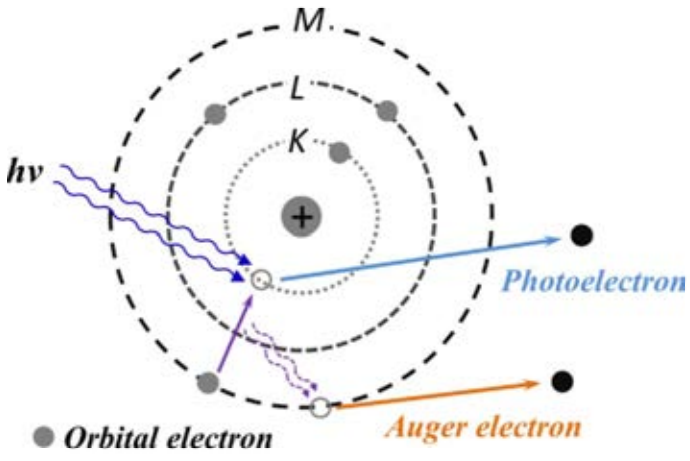

Fig. 3.7 Illustration of principle of photoelectron process [20].

An important issue of analyzing the XPS data is how to determine the composition of the sample. Noting that the integral area of binding energy curve is proportional to the number of atoms emit electrons at that binding energy, therefore, one can determine the composition of the sample surface by calculating the ratio of each integral area. However, for each element, a unique sensitive factor must be introduced in calculating this ratio. Because every XPS system has its own sensitive factor, it is difficult to obtain a precise composition unless the exact factors are given.

In addition to analytical information about the surface, it is also highly demanded to obtain information about the distribution of chemical composition with depths which is considerably larger than the escape length of electrons. Nondestructive methods, including variation of emission angle and variation of exciting photon energy are proposed, but in practice the chemical composition obtained are limited within depth of only approximately 5 nm. To obtain information about the deeper inner part of sample, destructive methods are required, and ion bombardment is one of the most universally used techniques. To avoid chemical effects, depth profiling in XPS is usually performed with a noble gas. Chemical information as a function of depth is acquired by using alternate cycles of sputtering and analysis.

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Chapter 4 Solution-processed High-*k* Gate Dielectric

In this chapter, a low-temperature solution-processed high-*k* dielectric system is introduced. The physical and chemical properties of the dielectric system are characterized and analyzed in detail. A model is proposed to account for the relationship between capacitance and frequency. Finally, low-voltage CuPc based OTFTs are demonstrated by using the high-*k* dielectric system.

4.1 Introduction

A great deal of research interest has been devoted to organic thin film transistors (OTFTs) during the past decades, as they have many advantages such as light weight, flexibility, and low temperature and solution processibility [1]. Much progress has been made in improving the performance of OTFTs, however, high operation voltage resulting from intrinsically low charge carrier mobility of organic semiconductors remains a severe limitation that hinders their development in practical applications [2]. For low-power applications, such as RFID tags, flat panel displayers, and portable electronics, it is a prerequisite to achieve high device performance at acceptably low voltage. Typically, this issue can be addressed through increasing the capacitance density of the gate dielectrics (C_i) by means of either increasing the dielectric constant (k) or decreasing the thickness (d) ($C_i=\varepsilon_0 k/d$). The latter approach has been demonstrated by utilizing self-assembled

monolayers (SAMs) and multilayers (SAMTs) [3-5], as well as polymers [6, 7]. However, due to the low dielectric constants (typically < 3) of organic materials, an extremely thin dielectric thickness is required. This demands a particularly careful preparation of the dielectric layer (as a very small amount of defects can already cause high leakage current) and makes the scale-up of OTFT fabrication difficult.

Application of high-*k* inorganic metal-oxides, such as TiO_2, HfO_2, ZrO_2 and Al_2O_3, instead of organic dielectrics, offers a promising alternative. Among these binary metal-oxides, TiO_2 is known to have the highest *k* value, but has the disadvantage of a negligible band offset against Si [8] and the easy formation of an interface layer even at low temperature [9]. Moreover, a higher permittivity value is usually accompanied by a smaller band gap, resulting in larger leakage currents through the gate dielectric. On the other hand, HfO_2 and ZrO_2 tend to form polycrystalline phases at relatively low temperature, resulting in the formation of grain boundaries that will degrade the dielectric performances [10]. In comparison, the merits of Al_2O_3 are its large band gap and band offset with Si [8] and excellent thermal stability [11]. Although the *k* value of Al_2O_3 is moderate, it can be used in combination with TiO_2 considering the fact that they have characteristics complementary to each other. On the other hand, typical processing routes for metal-oxide dielectrics, including chemical vapor deposition (CVD) [12], atomic layer deposition (ALD) [13] and radio-frequency (rf) magnetron sputtering [14] are often associated with high temperature, require expensive, high vacuum equipment, and are time consuming to produce. To achieve roll-to-roll metal-oxide fabrication and to make it compatible with large area flexible substrates, it is crucial to develop low-temperature, solution-processed routings for the fabrication of metal-oxides as gate dielectrics.

Here, we describe a novel solution-processed method to fabricate a 45 nm thick, bilayer Al_2O_y/TiO_x (ATO) dielectric system at low temperature (200 ± 5 °C). The obtained dielectric system exhibits a very smooth surface (RMS=0.22 nm), a low leakage current density (10^{-5} A/cm^2), and a high capacitance density of 250 nF/cm^2. By applying such a system as the gate dielectric, we achieve high performance of copper phthalocyanine (CuPc) based OTFTs at a driving voltage as low as -1.5 V, and the hole mobility (μ), threshold voltage (V_T), on/off ratio, and subthreshold swing (SS) are determined to be 0.06 cm^2/Vs, -0.5 V, 2×10^3, and 160 mV/dec, respectively. Our approach demonstrates a low-temperature, scalable process for fabrication of high-capacitance gate dielectric, which is a key step towards the realization of low-voltage OTFT circuits.

4.2 Experimental details

Titanium oxide (TiO_x) sol was prepared by dissolving titanium (IV) isopropoxide (TIP) ($Ti(OC_3H_7)_4$, 99.99%, Aldrich) into a mixture of methanol and acetic acid in a concentration of about 0.1 Mol/L, and then vigorously stirred for 24 h in ambient conditions. Aluminum oxide (Al_2O_y) sol was prepared by dissolving aluminum nitrate nonahydrate ($Al(NO_3)_3\cdot9H_2O$, 99.99%, Aldrich) into 2-methoxylethanol in a concentration of about 0.5 Mol/L and then stirred for 12 h in ambient conditions.

Prior to dielectric layer deposition, heavily n-doped Si wafers (n^{++}-Si) (acting as gate electrodes) were ultrasonically cleaned by acetone, isopropanol and ethanol, in

succession, and then used immediately for spin-coating after blown dry with N_2 gas. The TiO_X layer was deposited by spin-coating the TiO_X sol onto the cleaned n^{++}-Si substrates at 5000 r/min for 40 s, followed by baking at 200 ± 5 °C for 5 min to ensure the hydrolyzation and decomposition of the precursor. Subsequently, the Al_2O_y layer was deposited by spin-coating the Al_2O_y sol onto the cooled TiO_X-coated substrates and then baked at the same condition as that of TiO_X.

After deposition of the dielectric layers, bottom gate, top contact (BGTC) OTFTs were fabricated by vacuum deposition of CuPc (30 nm, 3×10^{-4} Pa, 0.01 nm/s growth rate) onto the substrates at the substrate temperature of 180 °C, followed by vacuum deposition of gold as source (S)-drain (D) electrodes (30 nm, 3×10^{-4} Pa, 0.03 nm/s growth rate) through a shadow mask with dimensions of L (channel length) = 70 μm and W (channel width) = 2500 μm. As for leakage and capacitance characterization, a metal-insulator-metal (MIM) structure was fabricated by direct deposition of 30 nm-thick gold dots with diameter of 1000 μm onto the single layer TiO_X and bilayer ATO dielectric system through a shadow mask.

The surface morphology of the solution-processed dielectric and CuPc film was characterized by atomic force microscopy (AFM, Nanoscope IIIa Vecco) in tapping mode. The elemental analysis of the spin-coated metal-oxides were characterized by XPS spectrometer (VG Scientific ESCALAB 250, equipped with two ultra–high vacuum (UHV) chambers) measurements and all binding energies were referenced to the C 1s peak at 284.6 eV of the surface adventitious carbon, the depth profiling was performed by Ar^+ etching with an EX05 argon gun at ion beam voltage of 3 keV and emission current

of 2 μA. The frequency-dependent capacitance of the MIM structure was measured by HP 4284A in a frequency range of 20 Hz-1M Hz. The electrical performances of the OTFTs were measured in ambient conditions using Keithley 4200 SCS.

4.3 Results and discussion

4.3.1 Structure of dielectric film

The X-ray diffraction (XRD) characterization is conducted on the solution-processed single layer TiO_x and ATO system, and the results is shown in Fig. 4.1. The absence of diffraction peaks in the XRD patterns reveals the amorphous nature of the oxides obtained at low processing temperature. Fig. 4.2a shows the tapping mode AFM image of the ATO system. As seen, the ATO exhibits a homogenous and smooth surface with a root mean square (RMS) roughness value of ~ 0.22 nm in an area of 5 μm × 5 μm. In addition, as shown in Figure 1b, no surface defects and pinholes are observed in the higher resolution AFM image. The cross-sectional analysis along a scan line (Fig. 4.2c) further confirms the high quality of the solution-processed film with a surface height fluctuation within 0.6 nm. The single TiO_x layer (AFM image not shown here) also shows similar structure, and has a considerably lower roughness than the reported TiO_2 dielectric layer which is obtained from a sol-gel and has a roughness value of 4 nm [15]. The dielectric surface roughness is an important factor that can influence the performance of OTFTs. A rough dielectric surface has been proven to be harmful to charge carrier transport in organic semiconductors. It can induce physical traps and barriers [16], or

disturb the growth of the semiconductor layer [17]. Therefore the smooth surface of our ATO system is an ideal property for high performance OTFTs.

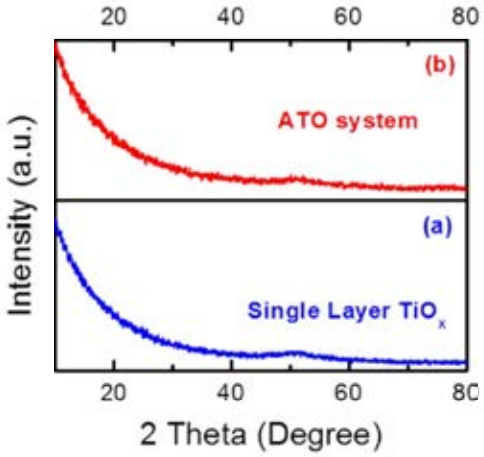

Fig. 4.1 X-ray diffraction (XRD) patterns of (a) single layer TiO_x and (b) ATO system.

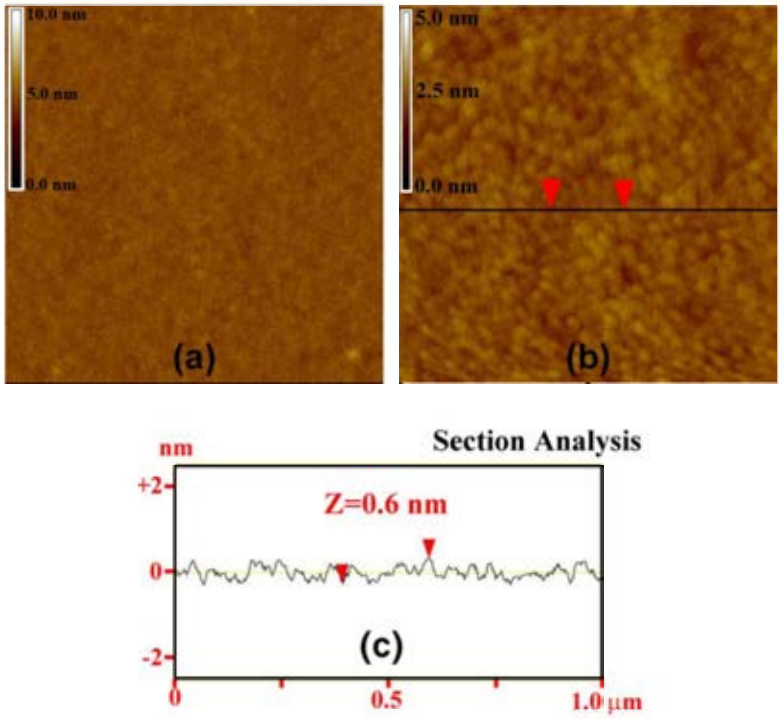

Fig. 4.2 AFM images of ATO system in an area of (a) 5 µm × 5 µm, (b) 1 µm × 1 µm and (c) Cross-sectional height profile obtained from the black solid line in (b).

4.3.2 XPS characterization

In order to investigate the chemical structure of the spin-coated dielectric films, XPS measurements are conducted. Fig. 4.3 shows the atomic composition profiles of O, Al, C, Ti, and Si as a function of etching time obtained from the ATO system. We note that no N atom is detected in the film, indicating completely decomposition of Al precursor ($Al(NO_3)_3 \cdot 9H_2O$). As can be seen in region I, the stoichiometry of the top Al_2O_y layer remains unchanged throughout the thickness of the layer, and no Si and Ti are detected in this region. The atomic ratio of Al to O in region I is about 2:2.7, giving an y value of 2.7. With increasing etching time, the intermixing layer containing Al_2O_y and TiO_x, which can be observed in region II, manifests a continuous change of the relative atomic ratios of Al, Ti, and O. Beneath region II is a more complex intermediate layer containing Al, Ti, Si, and O, marked as region III. The Si in region III should originate from the native SiO_2 layer on the surface of n^{++}-Si substrates. The total thickness of the ATO system is estimated to be 45 nm (measured by AFM). The inset of Fig. 4.3 shows the depth profiles of atomic composition obtained from a 15 nm thick, single layer TiO_x. There exists a transition layer consisting of TiO_x and native SiO_2 in the spin-coated TiO_x film, as noted by the changes in the composition of the film. Interestingly, as observed in both ATO system and single layer TiO_x, the C atom percentage at the surface is high and then decreases drastically as the etching depth increases. The high C concentration at the surface is usually attributed to contamination during sample handling; on the other hand, the absence of C atoms in the inner part of the oxide layer reveals that the Ti precursor ($Ti(OC_3H_7)_4$) is also completely decomposed. In the case of single layer TiO_x, the atomic ratio of Ti and Si to O is smaller than 2, suggesting that some oxygen vacancies exist in

the transition layer. The impact of these oxygen vacancies on the electronic properties of the oxide layer will be discussed later. The atomic concentration obtained here is meaningful in the relative values, because of the low accuracy of XPS itself. To get a more precise atomic concentration, one can use other techniques, such as inductively coupled plasma-atomic emission spectrometry (ICP-AES) and secondary ion mass spectrometry (SIMS).

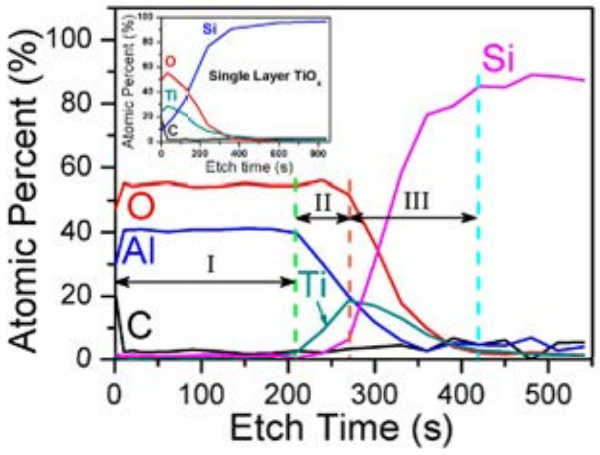

Fig. 4.3 Atomic composition profile of ATO system as a function of etch time; inset: Atomic composition profile of single layer TiO_x.

4.3.3 Leakage current and capacitance

To characterize the electrical properties of the solution-processed dielectric, we fabricate an Au/Metal-oxides/n^{++}-Si (MIM) sandwiched structure and test its current-voltage characteristics. Fig. 4.4a shows the typical leakage current density versus bias voltage plots of a single layer TiO_x and ATO system. As can be seen from Fig. 4.4, the single layer TiO_x exhibits an asymmetrical curve shape, with current density of ~

10^{-5} A/cm^2 at - 2 V and nearly 0.1 A/cm^2 at + 2 V (electric field strength: ~ 1.7 MV/cm). This is likely due to the zero conduction band offset at the Si/TiO_x interface [8] and the different work function of Si and Au, making electron injection from one electrode easier than the other, as shown in left side of Fig. 4.4b. We also note that the dip of the leakage current is shifted away from the zero bias; this might be caused by the charge trapping at the defects (e.g. oxygen vacancies) within the amorphous TiO_x/SiO_2 transition layer. After deposition of the Al_2O_y layer, the leakage current is reduced by 4 orders of magnitude under positive bias of + 2 V (electric field strength: ~ 0.5 MV/cm). The reduction of leakage is due to the blocking of electron conduction path by the Al_2O_y layer, as can be seen from the right side of Fig. 4.4b. For both the single layer and bilayer devices we observe an abrupt slope change of the leakage current at high positive bias as indicated by the transition from region A to B as shown in Fig. 4.4a. Similar phenomenon has also been observed by Mahapatra *et al.* and studied in detail [18]. According to their analysis, the conduction in region A is governed by a charge hopping process and the conduction in region B is dominated by both Proole-Frenkel emission and trap assisted tunneling processes [18]. Detailed characterization and modeling of the voltage and temperature dependences of the leakage current is needed to verify if the above explanation fits our system, and will be carried out in our future work.

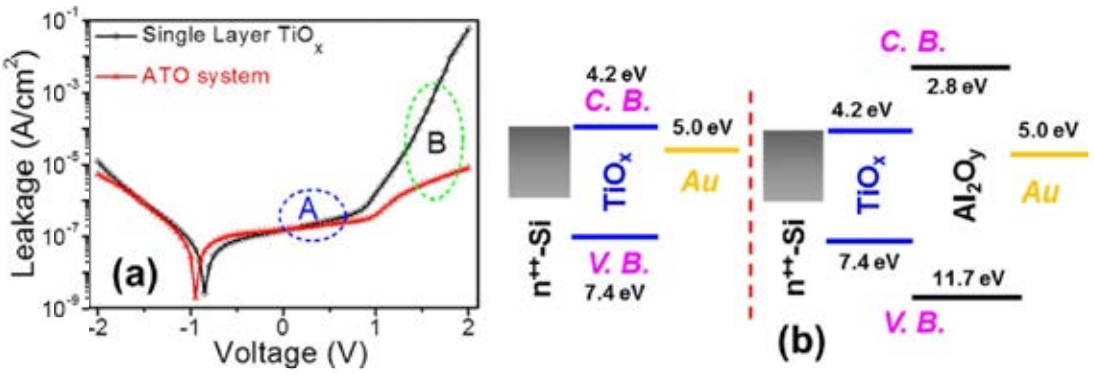

Fig. 4.4 (a) Band structures of single layer TiO_x and bilyer ATO with n^{++}-Si and Au as electrodes and (b) leakage current density versus bias voltage characteristics of MIM structures.

Fig. 4.5a exhibits the frequency dependence of capacitance density for the Au/ATO/n^{++}-Si (MIM) structure measured under different bias voltages. The inset corresponds to that of the single layer TiO_x under 0 V bias. During the measurements, bias voltage is applied to the top Au electrode, while the bottom Si substrate is grounded. For single layer TiO_x, under a bias voltage of 0 V, the total capacitance density is ~850 nF/cm^2 at 20 Hz. As shown in Fig. 4.3, as the TiO_x/SiO_2 transition layer is present in the spin-coated film in the case of single layer TiO_x, it is appropriate to calculate the equivalent permittivity of this transition layer instead of that of TiO_x. Using the thickness value of 15 nm, an equivalent k value of about 15 can be extracted. As for the ATO system, capacitance density is reduced owing to the introduction of another capacitor (i.e. Al_2O_y) in series. As can be seen in Fig. 4.5a, application of a forward bias (biasing positively on the Au electrode) results in higher capacitance of the MIM structure, compared to zero or reverse bias. Similar bias dependent capacitance has been observed by Yarmarkin *et al.* in the Au/TiO_2/Pt resistive switching device [19]. They attribute this phenomenon to the variation of space charge distribution, i.e., the redistribution of

oxygen vacancies in the film driven by the applied voltages. This may also explain our ATO system, because our XPS results suggest the existence of oxygen vacancies in the vicinity of the TiO_x/SiO_2 transition layer. The oxygen vacancies in TiO_2 are known to be positively charged and mobile [20]. The formation mechanism of positively charged oxygen vacancies is as follows [21]:

$$O_O^x \rightarrow V_O^{\cdot} + e' + 1/2O_2(g) \qquad (4.1)$$

$$O_O^x \rightarrow V_O^{\cdot\cdot} + 2e' + 1/2O_2(g) \qquad (4.2)$$

where $V_O^{\cdot}$ is the single positively charged oxygen vacancy and $V_O^{\cdot\cdot}$ is the double positively charged vacancy. The formation energy of oxygen vacancy with various charge stages has been fully studied by some theoretical works. For TiO_2, the transition energy levels of 2+/1+ and 1+/0 oxygen vacancies are located in the band gap around 0.7 eV and 0.5 eV, respectively below the conduction band minimum, as depicted in the Fig. 4.6a. The relatively low formation energy of positively charged vacancy is the reason of commonly observed n-type semiconducting behavior in TiO_2 [22]. On the other hand, oxygen vacancies can also exist in Al_2O_3 by the same mechanism. However, for Al_2O_3, the transition energy levels are located at 3.1 eV and 2.7 eV for 2+/1+ and 1+/0 oxygen vacancies, respectively, which are much larger than that of TiO_2 [23]. At the same time, the ionization energy of oxygen vacancy is almost proportional to the band gap of oxide semiconductors, larger band gap results in higher formation energy of positively charge oxygen vacancies, as deduces from literature [23]. The corresponding band structure of Al_2O_3 associated with oxygen vacancies is given in Fig. 4.6b. The high formation energy of positively charged oxygen vacancies accounts for the excellent insulating performance

of Al_2O_3. As a result, in bilayer ATO, we attribute the positively charged oxygen vacancies to the TiO_x layer other than the Al_2O_y layer.

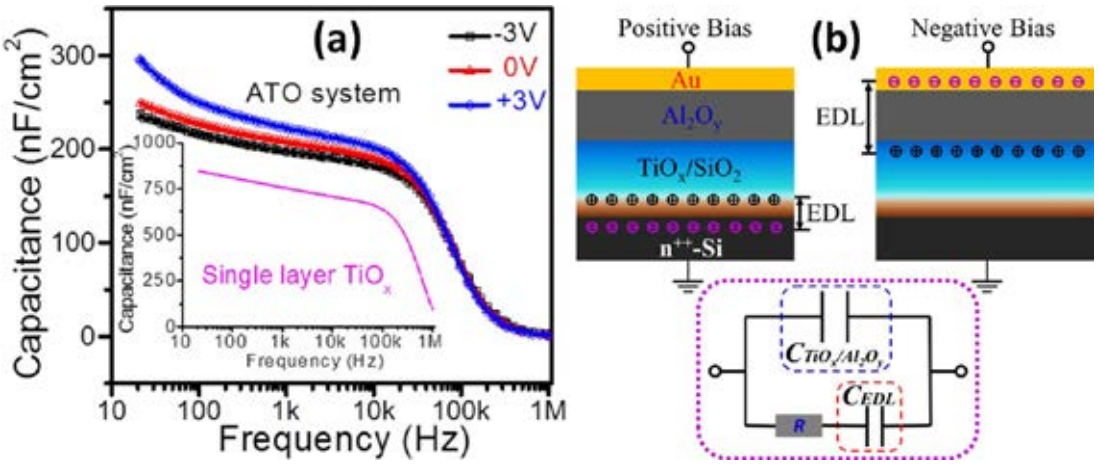

Fig. 4.5 Capacitance density versus frequency plots of MIM structures; (b) Schematic view of the ATO capacitor and the equivalent circuit (lower part).

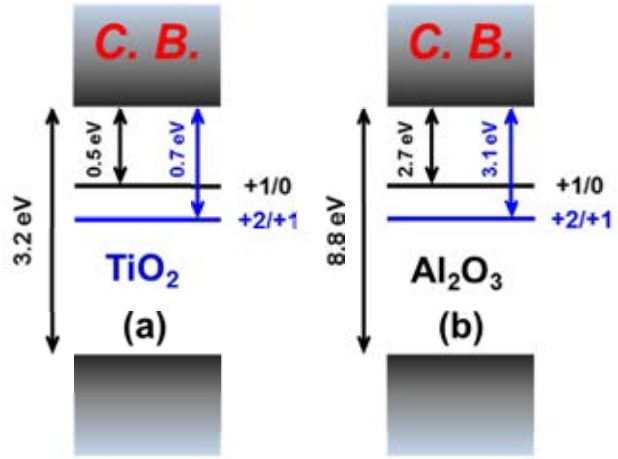

Fig. 4.6 Illustration of energy transition levels of oxygen vacancies in (a) TiO_2 and (b) Al_2O_3.

Having this in mind, one can infer that under forward bias, the oxygen vacancies will be repelled away from the mixing layer and accumulate close to the bottom Si substrate. This positively charged oxygen vacancy accumulation layer induces additional electrons

at the bottom electrode, forming an "electric double-layer" (EDL) capacitor. The capacitance of such an EDL could be enlarged due to its thickness (a few nanometers) [24]. On the other hand, in the situation of reverse bias, the oxygen vacancies will be attracted towards the Au electrode, and then blocked at Al_2O_y/TiO_x interface (as shown in Fig. 4.5b), resulting in a larger thickness of the EDL capacitance. This explains the bias voltage dependence of the capacitance of ATO system observed in Fig. 4.5a. Similar results have also been reported by other groups [25, 26].

Besides the bias dependence, we also observe a slight increase of capacitance density at low frequencies. The increase of capacitance at low frequency is often related to the Maxwell-Wagner space charge polarization which is inherently a nonuniform charge accumulation [27, 28]. This process is also referred to as electrode polarization according to Gonon *et al.*, in which the mobile charges form an EDL against the electrodes resulting in a bias modulated EDL capacitance [29]. As discussed previously, in the intermixing layer of ATO system, oxygen vacancies are positively charged and mobile. Under an AC bias with sufficiently low frequencies, the oxygen vacancies will have enough time to respond to the bias change and go back and forth in the vicinity of the space charge layer, which can be viewed as a macroscopic dipole oscillating with the field. The lower the frequency is, the larger the distance of oscillation, and ultimately the larger the capacitance density. To illustrate the mechanism for the voltage and frequency dependent capacitance, a simple model with an equivalent circuit is proposed in Fig. 4.5b. To calculate the equivalent dielectric constant of the ATO system, the low frequency (20 Hz) capacitance value of 250 nF/cm^2 under zero bias is considered. Using the thickness of 45 nm, an equivalent dielectric constant of about 13.3 is expected.

4.3.4 Low-voltage CuPc TFTs

To demonstrate the effectiveness of our ATO system, bottom-gate, top-contact (BGTC) CuPc TFTs with gold source-drain electrodes are fabricated using the bilayer system as the gate dielectric. More than 5 ATO substrates are used, and 4 devices on each substrate are fabricated and tested. The device yield is about 90%. Fig. 4.7a shows the output curves of a representative CuPc TFT. Due to the high capacitance of our ATO system, the device can work effectively at operation voltages as low as -1.5 V. The output curves exhibit clear linear and saturation regions. Though moderate leakage current still exists at zero drain voltage, its magnitude is much smaller than the corresponding saturated channel current at respective gate voltages. Fig. 4.6b shows the corresponding transfer curve in the saturation region and $(-I_{DS})^{1/2}$ versus V_{GS} plot. By using a linear fit of the plot in Fig. 4.7b, V_T in the saturation region can be determined from the following equation:

$$I_{DS} = \frac{W}{2L} C_i \mu (V_{GS} - V_T)^2 \qquad (4.1)$$

where W is the channel width, L is the channel length, V_T is the threshold voltage, μ is the hole mobility, and C_i is the capacitance density of the gate dielectric. To extract the hole mobility of CuPc TFTs, the C_i value of the ATO system under zero bias of 250 nF/cm^2 at 20 Hz is considered. From Fig. 4.6b, the hole mobility (μ), threshold voltage (V_T), on/off ratio, and subthreshold swing (SS) are determined to be 0.06 cm^2/Vs, -0.5 V, 2×10^3, and 160 mV/dec, respectively. Interestingly, the properties of the low-voltage CuPc TFTs using ATO system as the gate dielectric are better than those prepared on various high-k

metal-oxide thin films, such as ZrO_2 [30], Al_2O_3, Ta_2O_5 [31], and HfO_2 [32], and even higher than the value reported by Wang *et al.* (~0.04 cm^2/Vs) [33], which is the highest mobility for CuPc thin film transistors so far to the best of our knowledge. Noting that the capacitance density of the ATO system in steady–state condition is a little bit larger than that measured at 20 Hz (as inferred from Fig. 4.5a), we may have overestimated our mobility by a factor of 1.5. As discussed previously, the low atomic scale roughness of our ATO system may benefit charge carrier transport in the channel, resulting in improved performance. In addition, it is worth noting that a *SS* value of only 160 mV/dec is remarkably small. *SS* determines the voltage swing required for a transistor to turn from "off" to "on", and should be as low as possible, with a theoretical limit of about 60 mV/dec at room temperature [34]. Fabrication of OTFTs with *SS* smaller than 180 mV/dec is thought to be a significant leap forward [35, 36].

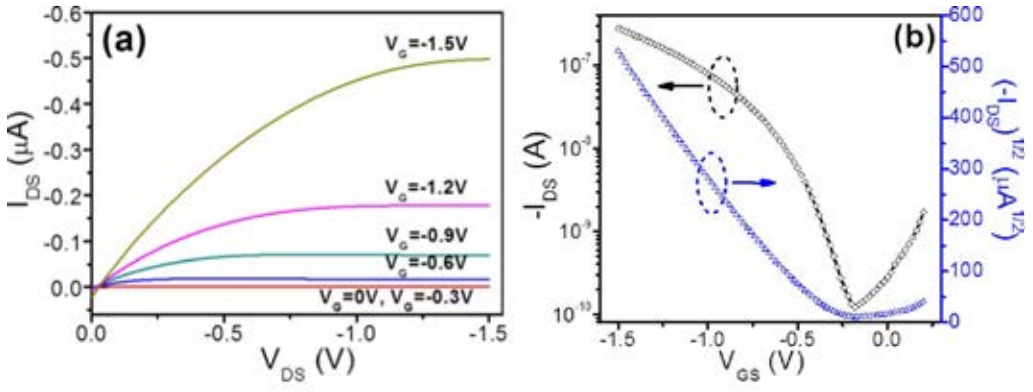

Fig. 4.7 (a) Output curves and (b) Transfer curve of CuPc TFT using ATO system as dielectric.

4.4 Conclusion

In summary, we have successfully achieved low-voltage OTFTs by introducing a solution-processed, low-temperature cured high-*k* ATO system as the gate dielectric. The bilayer dielectric system exhibits a very smooth surface with RMS of about 0.22 nm, an equivalent *k* value of 13.3, a high capacitance of 250 nF/cm^2 and a low leakage current density of 10^{-5} A/cm^2. Upon using the high-*k* ATO as the gate dielectric, CuPc based OTFTs exhibit hole mobility as high as 0.06 cm^2/Vs and *SS* value of only 160 mV/dec under an operation voltage as low as -1.5 V. Our low-temperature, solution-processed method for fabrication of high-*k* gate dielectric provides a feasible approach to realize low-voltage circuits.

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Chapter 5 Study of CuPc OTFT with High-*k* Gate Dielectric

In this chapter, we will present at first that the solution-processed high-*k* ATO based low-voltage CuPc TFTs can result in a much higher device performance as compared to traditional SiO_2 based devices. However, our findings seem contradictory to the reported results of other groups, because the high-*k* is usually detrimental to the field-effect mobility due to the carrier localization caused by high dipolar disorder in the interface of dielectric and organic semicondcutor. The mechanism behind is studied in detail in this chapter.

5.1 Introduction

Organic thin film transistors (OTFTs) have spurred tremendous interest in recent years because of their low manufacturing costs and potential applications in various state-of-art electronics, such as flexible displays [1, 2], electronic papers [3], and sensors [4, 5]. Although impressive progress in the electrical performance has been steadily achieved over the past decades, one of the major obstacles that hamper the development and realistic applications of OTFTs is the rather high voltage that is frequently in the order of tens of volts for device operation. One promising method to solve this critical issue is to increase the gate capacitance, which can induce a high charge carrier density at the conducting channel under a low gate voltage [6].

Successes have been realized for low-voltage OTFTs by utilizing very thin organic layers and high-*k* materials as gate dielectrics [7-10]. A lot of research work has regarded insulating metal-oxides as favorable high-*k* materials that can be used for these applications in organic field-effect transistors (OFETs). In practical, typical fabrication routes for high-*k* metal-oxide dielectrics, such as atomic layer deposition [11], radio-frequency magnetron sputtering [12] and chemical vapor deposition [13], require expensive, high-vacuum equipments, and are time consuming to produce functioning layers. Besides, solution-assisted techniques, such as spin-coating and ink-jet printing, are basically applied for polymeric dielectrics that, on the other hand, possess low values of capacitance. Consequently, it is of significant importance to develop a solution-based technique for the fabrication of high-*k* metal-oxides as gate dielectrics, in order to turn OTFTs into more reliable applications for low-cost, large-area devices.

In general, the electrical parameters of OTFTs, such as field-effect mobility (μ), threshold voltage (V_T) and subthreshold swing (SS), are mainly dependent on the molecular structure of the semiconducting film [14-17]. It has been proven that the mobility of OTFTs is mainly dependent on the layer-by-layer growth and structural ordering of the active layer [14]. Therefore, control over the initial growth of an organic semiconductor layer is of considerable importance since the charge transport in the channel of OTFTs is mainly restricted to the first several monolayers in the vicinity of semiconductor-dielectric interface [18, 19]. In a vacuum deposition condition, the structure of the organic semiconductor thin film is influenced by the growth conditions, e.g. substrates temperature, deposition rate, surface properties of the dielectrics and so on. Among various factors, the surface energy of dielectrics shows significant impact on the initial growth of the organic layers. High surface

energy will result in stronger interaction between molecular and the substrate, and then decrease the π-π stacking of organic molecules paralleling to the dielectric surface.

In this section, the solution-processed high-*k* ATO is used as gate dielectric for low-voltage OTFTs, and the result show that the resultant CuPc based devices exhibit superior performance. The low-voltage TFTs present highly improved electrical characteristics as compared to those of high-voltage (-40 V) devices based on traditional SiO_2. Studies on the microstructure of CuPc thin films reveal that the enhancement of performance is attributed to the interconnected "rod-like" crystallized structure in the initial growth stage, which results from the relatively low surface energy of the solution-processed high-*k* dielectrics. Furthermore, Kelvin probe force microscopy (KPFM) characterization reveals a preferred energy band alignment at the CuPc/ATO interface. The presented results imply that the solution-processed high-*k* dielectrics can be used effectively in high-performance, low-voltage OTFTs.

5.2 Experimental details

n^{++}-Si wafers with thermally grown 300 nm SiO_2 layer were firstly cleaned with acetone, isopropanol and ethanol successively by ultrasonic, and further cleaned by O_2 plasma for 3 min before use; solution-processed high-*k* ATO is fabricated by the same procedure introduced in Chapter 4.

CuPc TFTs were fabricated by vacuum deposition of CuPc molecules onto the above two types of substrates under a pressure of about 3×10^{-4} Pa and a deposition rate of about 0.1 Å/s with substrates temperatures of 180 ^{o}C. Then 30 nm gold

source-drain (S/D) electrodes were deposited onto the organic layer through a shadow mask under a pressure of about 3×10^{-4} Pa and a deposition rate of about 0.3 Å/s. The channel length (L) and width (W) are 56 μm and 1500 μm, respectively. Pentacene, copper hexadecafluorophthalocyanine (F_{16}CuPc) and C60 TFTs were prepared by the same procedure but with the substrates temperature of 60 °C, 180 °C and 110 °C, respectively, and the S/D electrodes are Au for pentacene and F_{16}CuPc, and Ag for C60. Single crystals of rubrene were grown onto the substrates by physical vapor transportation (PVT) method at sublimation temperature of 245 °C in Ar atmosphere with a flow rate of 100 sccm. Then devices were fabricated by placing Au-films onto the rubrene single crystals as the source and drain electrodes [20].

The electrical characteristics of the devices were measured in ambient condition using Keithley 4200 SCS. The morphologies of the CuPc thin films were characterized by atomic force microscopy (AFM, Nanoscope IIIa Vecco) in tapping mode. The X-ray diffraction (XRD) patterns of CuPc layer were obtained on an X-ray diffractometer (Simens, D5000) using Cu $K\alpha$ radiation (λ=0.154 nm) at a scan rate of 0.02° 2θ/s, and the average crystallite sizes of CuPc were determined by the Scherrer equation using the FWHM (full width at the half maximum) data of the diffraction peak [21]. The two-dimensional grazing incidence X-ray diffraction (GIXD) patterns were obtained at beamline BL14B1 (λ=1.24 Å) of the Shanghai Synchrotron Radiation Facility with an incident angle of 0.06°. The surface potential of the CuPc film was measured in air using Kelvin probe force microscopy (KPFM) method. A goniometer from Solon Tech. (Shanghai) Co. Ltd. with a SimpleCAST software was used to measure contact angles. Deionized water (γ_L = 72.8 mN/m, γ_L^d = 21.8 mN/m, γ_L^p = 51.0mN/m) and ethylene glycol (γ_L= 48.3 mN/m, γ_L^d = 29.3 mN/m, γ_L^p = 19.0mN/m) were chosen as the probing liquids. The contact angles were measured for

three times and the average values were used to evaluate the surface energy of the dielectrics according to the following equations [22, 23]:

$$\gamma_L(1+\cos\theta) = 2\sqrt{\gamma_S^d \gamma_L^d} + 2\sqrt{\gamma_S^p \gamma_L^p} \qquad (5.1)$$

$$\gamma_S = \gamma_S^d + \gamma_S^p \qquad (5.2)$$

where θ was the contact angle between dielectrics and the probing liquids; γ_S and γ_L were the surface energy of the dielectric and the probing liquid, respectively, and the superscripts d and p referred to the dispersive and polar components of the surface energy, respectively.

5.3 Results and discussion

5.3.1 Devices electrical characteristics

CuPc TFTs with bottom-gate top-contact geometry are fabricated on SiO_2 and ATO using Au as the S/D electrodes. 6 devices on each substrate are fabricated and then tested in ambient condition. Fig. 5.1a shows a representative output characteristics of the CuPc TFTs on SiO_2. With increasing V_{DS}, the output curves exhibit clear linear and saturation behavior. Fig. 5.1b gives the corresponding transfer curves in the saturation region. The device possesses a moderate on/off ratio on the order of 10^3 and a subthreshold swing (SS) of 5.9 V/dec. SS is defined by $\partial V_{GS}/\partial log\left|I_{DS}\right|$ in the subthreshold region, and should be as low as possible since a small ∂V_{GS} can turn the transistor from fully "off" to fully "on" state, which is crucial for low-power application. In general, OFETs possess relatively large SS due to the localized hole-trapping states near the highest occupied molecular orbital (HOMO) or

electron-trapping states near the lowest occupied molecular orbital (LUMO) levels of organic semiconductors [24]. The high *SS* value is a shortcoming of OFETs, and results from a combination of factors, such as low gate dielectric capacitance density, low breakdown voltage, and high parasitic capacitances at insulator-semiconductor interface. On the other hand, the *SS* can also be used to estimate the maximum density of interface traps (N_{trap}) at the semiconductor/dielectric interface through the following equation [25, 26]:

$$N_{Trap}^{Max} = \left(\frac{qSSlog(e)}{kT} - 1\right)\frac{C_i}{q} \qquad (5.3)$$

where q is the electronic charge, *SS* is the subthreshold swing, e is the Euler's number, k is Boltzmann's constant, T is the absolute temperature and C_i is the gate dielectric capacitance density. For SiO_2, the estimated maximum trap density is 6.7×10^{12} cm^{-2}. Other figures-of-merit of OTFTs can be obtained from the plot of $(-I_{DS})^{1/2}$ versus V_{GS} by fitting the data to the following equation:

$$I_{DS} = \frac{W}{2L}C_i\mu(V_{GS} - V_T)^2 \qquad (5.4)$$

where W is the channel width, L is the channel length, C_i is the capacitance density of the gate dielectrics, V_T is the threshold voltage, and μ is the mobility. For traditional 300 nm SiO_2 (k = 3.9), the capacitance density is about 11 nF/cm^2. Data in the region of V_{GS} form -25 to -40 V are taken for this fitting, and the obtained μ and V_T are 2.8×10^{-3} cm^2/V s and -6.0 V, respectively.

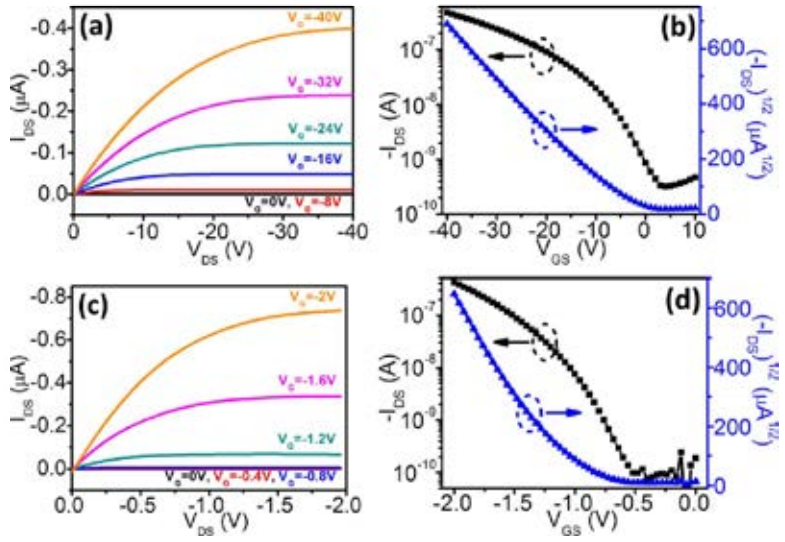

Fig. 5.1 (a) Output curves and (b) Transfer curve of CuPc TFT on SiO_2; (c) Output curves and (d) Transfer curve of CuPc TFT on ATO.

Table 5.1 Summary of the electrical characteristics of devices on different dielectrics as well as the corresponding dielectric surface properties.

Dielectrics	Electric performance					Surface properties			
		μ (cm^2/Vs)	V_T (V)	on/off ration	SS (mV/dec)	RMS (nm)	Contact angle (Degree)		Surface energy (mJ/m^2)
							DI water	Ethylene glycol	
ATO	CuPc	0.15	-1.1	5×10^3	232	0.22	35.5	28.3	71.3
	Pentacene	1.1	-0.99	3×10^3	256				
	Rubrene	7.0	-0.08	10^4	101				
SiO_2	CuPc	2.8×10^{-3}	-6.0	10^3	5.9×10^3	0.21	<5	<1	>87
	Pentacene	0.12	-2.3	10^4	5.1×10^3				
	Rubrene	2.5	4.9	10^5	1.1×10^3				

Fig. 5.1c shows the output curves of a representative CuPc TFTs on ATO. Due to the high capacitance density of the gate dielectric (250 nF/cm^2) [27], the device works effectively at an operation voltage as small as -2 V. Clear linear and saturation regions can be observed from the output curves. Fig. 5.1d exhibits the corresponding transfer curves in the saturation region. The μ, V_T, on/off ratio, and *SS* are determined to be 0.15 cm^2/Vs, -1.1 V, 5×10^3, and 232 mV/dec, respectively. Notably, the *SS* is effectively decreased due to high capacitance density of ATO which improving the coupling

between the gate and the conducting channel [24]. The estimated interface trap density is about 4.5×10^{12} cm^{-2} for ATO, which is obviously lower than that of SiO_2. It is interesting to note that the mobility of the low-voltage CuPc device gated with solution-processed high-*k* ATO is superior to those prepared on other high-*k* dielectrics, such as $SrTiO_3$ [28], Al_2O_3, Ta_2O_5 [29], and ZrO_2 [30], and can even be comparable to that of CuPc single crystal nano-wires based transistors with mobility of 0.2~0.4 cm^2/Vs, which is believed to possess higher mobility than the counterpart thin film devices because of the stronger overlap and intermolecular coupling between π-orbits of adjacent molecules in single crystal structure [16]. The origin of the outstanding performance of our devices will be further discussed in detail in following part. The gate electric field of ATO is about 0.44 MV/cm under a gate voltage of -2 V. This value is similar to that of 300 nm SiO_2 when V_{GS} = -13 V, and the corresponding μ estimated from Fig. 5.1b is approximately 1.7×10^{-3} cm^2/Vs. The electrical characteristics for both SiO_2 and ATO based OTFTs are summarized in Table 5.1. The results clearly show that the electrical properties of the device on ATO were much higher than that on SiO_2. However, as reported by many groups, the use of high-*k* gate dielectrics can lead to a declining of mobility due to the carrier localization caused by high dipolar disorder at the interface between high-*k* dielectrics and organic semiconductor [31, 32]. Interestingly, our present results exhibit a converse trend, i.e., higher mobility is obtained on high-*k* dielectrics. This phenomenon must be studied in detail.

5.3.2 Morphologies of dielectrics and CuPc fims

The electrical property of OTFTs can be influenced by several aspects, such as dielectric surface property, organic layer structures, and semiconductor-dielectric interface characteristics. Therefore, we firstly carried out the atomic force microscopy (AFM) investigations to explore the morphological properties, and the results are exhibited in Fig. 5.2. It is shown that both surfaces of SiO_2 and ATO are very smooth with similar root-mean-square (RMS) roughness of 0.21-0.22 nm. Hence, the influence of dielectric surface roughness on the electrical performance of CuPc TFTs can be excluded.

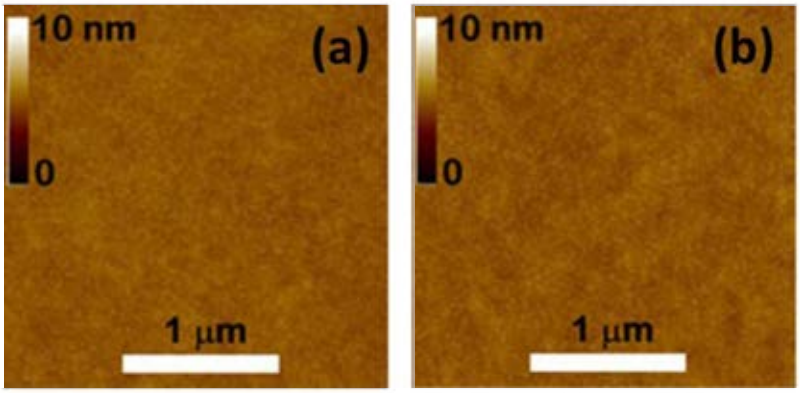

Fig. 5.2 AFM images of (a) traditional thermally oxidized SiO_2 and (b) solution-processed ATO.

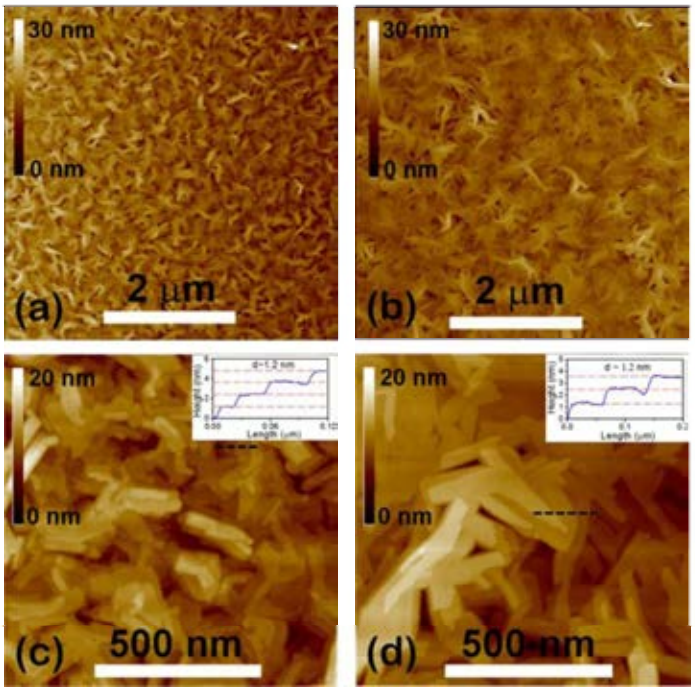

Fig. 5.3 AFM images of 25 nm CuPc film deposited on (a) SiO_2 and (b) ATO in an area of 5 μm × 5 μm; (c) and (d) are the respective high-resolution images (1 μm × 1 μm), insets are the corresponding cross-sectional analysis along the dash lines.

Then the morphology of CuPc films deposited on the above two substrates are also characterized to investigate its influence on the devices performance. Fig. 5.3a and b show the AFM images of 25 nm CuPc thin films deposited onto SiO_2 and ATO, respectively. The CuPc film deposited on SiO_2 is composed of high-density small dendritic clusters packing in a homogenous structure. Similar morphology is also observed for CuPc deposited on ATO, but with a higher structural ordering and a slightly larger feature size. Besides, the CuPc films on the two dielectrics exhibit nearly identical surface roughness with an RMS value of approximately 1.8 nm. Moreover, layer-by-layer structures are observed from the high-resolution AFM images for the CuPc layers on both dielectrics (Fig. 5.3c and d). A terrace height of 1.2 nm is estimated from the cross-sectional profile along the dash line (insets of Fig.

5.3c and 2), which is in good agreement with a molecular layer height of CuPc deposited on oxide substrates [19, 33, 34].

5.3.3 Crystal structure of CuPc films

On the other hand, the crystallographic structure of the CuPc films also plays an important role in determining the device performance. Depending on the processing condition, CuPc films may exhibit single phase or mixed phases. For vacuum deposited CuPc thin films, the metastable α-phase and thermally stable β-phase are two most commonly observed crystalline phases [35]. Both α and β phases possess monoclinic structure, which differ only in the tilt angle of the molecule plane with respect to the intermolecular stacking direction [16]. However, the α-phase has a smaller tilter angle than that of β-phase, suggesting better π-electron overlap in α-CuPc versus β-CuPc. Fig. 5.4 shows the X-ray diffraction (XRD) patterns of 25 nm CuPc thin films deposited on SiO_2 and ATO at substrates temperature of 180 ^{o}C. A single sharp reflection peak at 2θ of 6.9^{o} assigned to the (200) plane of α-phase CuPc can be observed from both patterns [28]. This peak corresponds to an interplanar distance of about 1.3nm, which is good agreement with the previous AFM results. The full-width at half-maximum (FWHM) of the (200) diffraction peak of CuPc films deposited on SiO_2 and the solution-processed high-k dielectrics are estimated to be 0.34^{o} and 0.30^{o}, respectively. The average crystallite sizes of CuPc are calculated using the Scherrer equation, and the results are listed in Table 5.1. As seen, the average crystallite size of CuPc on the solution-processed high-k dielectrics (26.7 nm) is a little bit larger than that on SiO_2 (23.5 nm). Noting that the conventional XRD

characterization can only give us the information of structural ordering in the direction perpendicular to the substrates, the lower intensity of the diffraction peak with CuPc on ATO may result from the loosened packing of CuPc crystals within the thin film as compared to SiO_2, other than the lower crystallization, which will be discussed in detail later

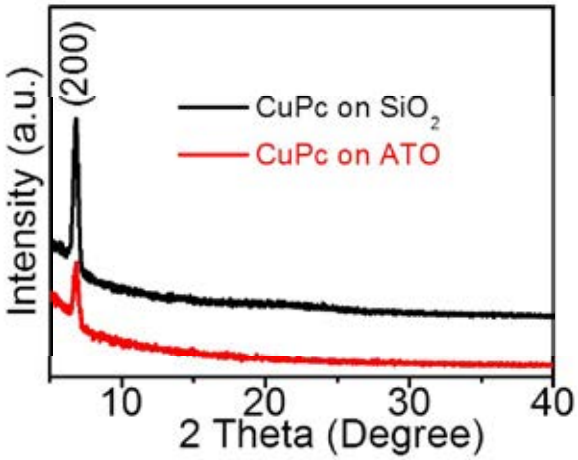

Fig. 5.4 XRD patterns of 25 nm CuPc film on the two types of dielectrics.

5.3.4 Initial growth study

The above results indicate similar properties of the two dielectric surface and the corresponding organic layers. As having been discussed previously, the charge carrier transport is primarily confined to the interface between the gate dielectrics and the organic semiconductors [19, 22], it is then of great importance to study the initial growth of the CuPc films on both dielectrics. As shown in Fig. 5.5a, the CuPc molecules aggregate together and form isolated small islands with an average size of approximately 50 nm when deposited on SiO_2 with a thickness of 1.2 nm. When the thickness further increases to 2.4 nm, the nucleation of the subsequent isolated multilayer islands occur on the top of the bottom layer, although a continuous bottom

layer is not complete yet (Fig 5.5b). More CuPc molecules depositing onto the surface result in lateral growth of the islands. Then, the islands merge together to form a flat layer with some small voids, and new islands start to grow at the same time (Fig. 5.5c). This kind of initial growth can be assigned to the Stranski-Krastanov mode [36], which occurs when the interaction between the molecules and the substrates are stronger than that between the molecules [37]. Further deposition of CuPc molecules forms incomplete subsequent layers that limiting the transport of charge carriers and causing decreased mobility, which is in accordance with the device performance obtained from our devices.

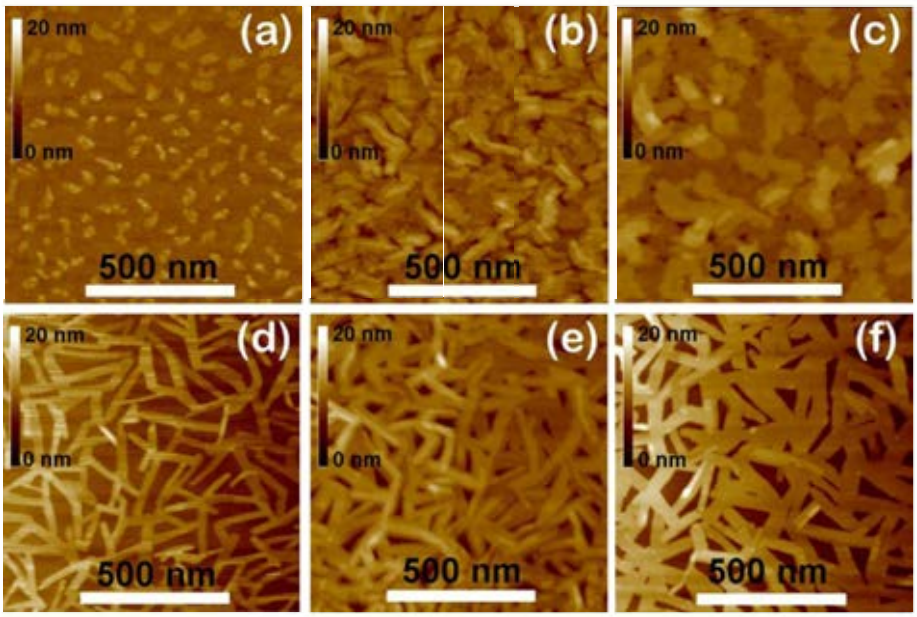

Fig. 5.5 AFM images of CuPc deposited on SiO_2 with nominal thicknesses of (a) 1.2 nm, (b) 2.4 nm and (c) 3.6 nm; AFM images of the CuPc deposited on ATO with nominal thicknesses of (d) 1.2 nm, (e) 2.4 nm and (f) 3.6 nm.

In contrast, CuPc exhibits a completely different growth mode when deposited on ATO. At the beginning, the CuPc molecules assemble in randomly oriented rod-like crystals with an average size of approximately 30 × 150 nm (Fig. 5.5d). These rod-like crystals are highly interconnected, constructing a "net" on the surface of

ATO. When the thickness is increased to 2.4 nm and 3.6 nm, the CuPc films grow vertically, and form more densified "nets" with much larger feature sizes on top of the underneath "net" (Fig. 5.5e and f). This initial growth can be described by the Volmer-Veber growth mode [36], in which the deposited molecules are more strongly bonded to each other than to the substrate [37]. These highly interconnected "nets" can provide sufficient paths for the flow of charges, benefit the charge transport at the interface, and thus enhance the mobility.

5.3.5 Surface energy characterization

Generally, the initial nucleation process of organic molecules under the same deposition condition is mainly affected by the surface energy of the substrates [17, 38]. In other words, the initial growth of organic molecules is dependent on two competing interactions, i.e., molecule-substrate interaction and molecule-molecule interaction. For instance, lower surface energy with weak interaction between the molecule and the substrate will result in a favorable columnar stacking for molecules (rod-like crystals of CuPc), while higher surface energy will induce horizontal alignment of the molecules that tend to cover the substrate surface to reduce the total free energy [39]. In order to clarify the correlation between the dielectric surface properties and the initial growth of CuPc on different dielectrics, the contact angles of DI water and ethylene glycol on the dielectric surfaces are measured to estimate the surface energy [23], and the results are summarized in Table 5.1. SiO_2 substrates are tested immediately after O_2 plasma treatment, and the ATO substrates are examined instantly after fabrication. As can be seen from Table 5.1, ATO has a lower surface energy than SiO_2. Since the surface roughness of the two dielectrics is similar and the

deposition condition of CuPc is the same, we infer that the difference in the dielectric surface energy determines the different initial growth characteristics of CuPc. That is, lower surface energy of the solution-processed high-*k* dielectrics leads to weaker interaction between the organic molecules and the dielectrics, so the deposited CuPc molecules have a longer migration distance on the dielectric surface to form oriented rod-like CuPc crystals, resulting in a lowered nucleation density,

5.3.6 In-plane structure of CuPc films

The CuPc molecules can present a closer packing structure with higher structural ordering in the direction parallel to the substrate at the semiconductor-dielectric interface on those substrates with lower surface energy than that on higher surface energy substrate [17]. To further verify our arguments, the in-plane structures of very thin CuPc films (2.4 nm) on SiO_2 and ATO were investigated using the GIXD measurements. As shown in Fig. 5.6a, no diffraction peak is found from the pattern. It indicates that, for the first several monolayers, the in-plane structure of CuPc molecules on SiO_2 was amorphous. On the other hand, a clear diffraction peak can be observed from the pattern of the CuPc film on ATO (indicated by the red arrow in Fig. 5.6b), revealing a crystalline structure of the first several monolayers of CuPc. Furthermore, the observed diffraction peak, which can be indexed to (1,0) [40], also discloses ordered stacking of CuPc molecules at the CuPc/ATO interface. The ordered in-plane structure and the interconnected "net" structure of CuPc on ATO thus account for the highly enhanced electrical characteristics of our devices, because the charge transport at the conducting channel is mainly located at the first several monolayers at the interface. Moreover, devices with very thin film of CuPc (5 nm) as

active layer are fabricated on both substrates, and the transfer curves are shown in Fig. 5.7. Due to the ordered structure of CuPc in the interface region of CuPc/ATO, the resultant device exhibits much higher electrical properties than that on SiO_2 as expected, and the estimated μ for ATO and SiO_2 are 1.0×10^{-2} cm^2/Vs and 1.0×10^{-3} cm^2/Vs, respectively. The obtained results give an extra confirmation on the previous arguments.

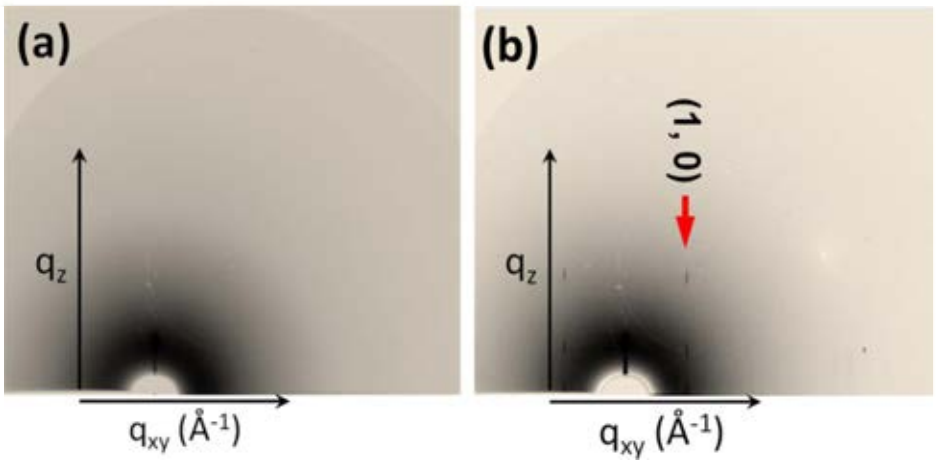

Fig. 5.6 2-dimentional GIXD patterns of CuPc thin film on (a) SiO_2 and (b) ATO with nominal thickness of 2.4 nm

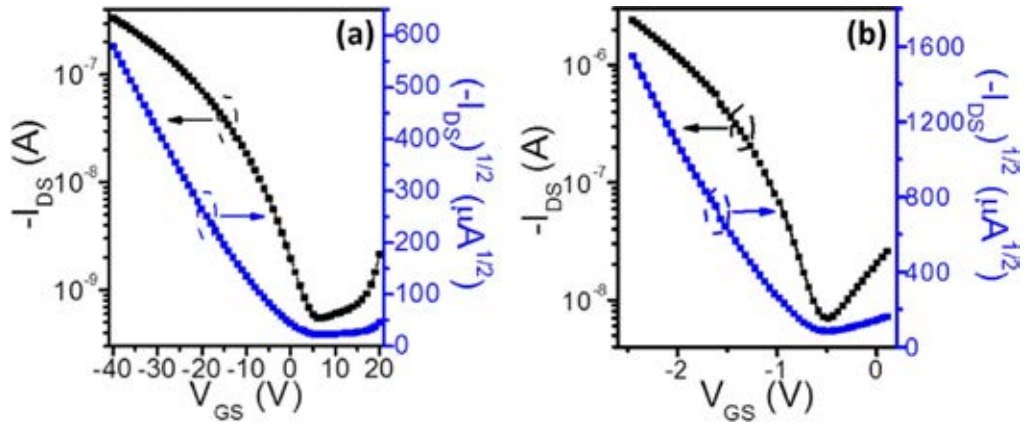

Fig. 5.7 Transfer curves of 5 nm CuPc devices on (a) SiO_2 and (b) ATO

5.3.7 XPS characterization

It is well known that metal oxide dielectrics often contain surfaces with dangling bonds that can influence negatively on the transistor performance. However, our devices based on the solution-processed ATO exhibit excellent performance. This interesting advantage of ATO is revealed by using the X-ray photoelectronic spectroscopy (XPS) characterizations, as shown in Fig. 5.8. As seen, no N atom is detected in the film, and the C atom percentage decreases drastically as the etching depth increases, indicating that the ATO precursors are completely decomposed [27]. In addition, the substrates are baked at 180 °C under high vacuum (3×10^{-4} Pa) during the deposition of CuPc molecules, therefore, it is not likely that the low surface energy of ATO results from the residual organic species or the absorbents in air. Instead, it reveals an oxygen deficient nature of the top layer Al_2O_X (x = 2.7) layer existing in ATO. The low O concentration in Al_2O_X can lower the density of surface dangling hydroxyl group, decreasing the surface energy, and subsequently benefiting the device performance. Consequently, we attribute our high mobility to the low oxygen concentration in our aluminum oxide, which will result in a low surface energy as discussed previously.

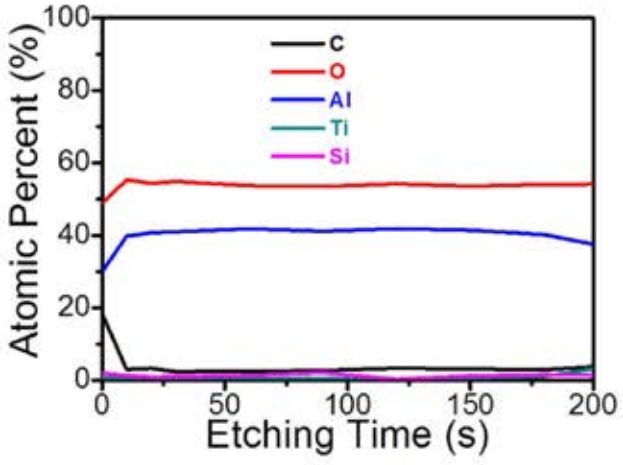

Fig. 5.8 XPS depth profile of ATO.

5.3.8 KPFM study

Furthermore, it is a common consideration that metal/organic contact is also a key factor that determines the device performance [41]. Tremendous research work has been devoted to the optimization of the energy alignment between metal electrodes and organic semiconductors, typically by inserting a modifying thin layer for better charge injection. To investigate the contact property in our devices, we applied KPFM to study the interface band structures of CuPc on different dielectrics. As shown in Fig. 5.9, the vacuum level is bending up near the CuPc/SiO_2 interface, while it keeps unchanged for the CuPc/ATO one. It implies that there are more interfacial electron traps at the CuPc/SiO_2 interface. Moreover, a negative gate voltage is applied to the 5 nm thick CuPc sample ($V_{DS} = 0$) to investigate the interfacial energy level shifting. For the CuPc on SiO_2, the vacuum level moves to -56 meV and is pinned, while for CuPc on ATO it moves to 81 meV. Therefore, from the movement of vacuum level, we can conclude that when the CuPc molecules deposited on ATO subsrate, the Fermi level aligns around 137 meV deeper to the center of HOMO than that on SiO_2 substrate. Such a deep alignment of Fermi level against the HOMO of the CuPc on ATO can improve the metal/organic contact, and benefit the charge carrier injection.

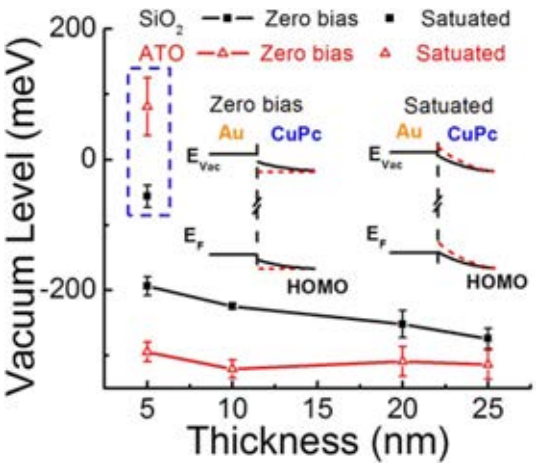

Fig. 5.9 The band diagram of vacuum level of CuPc thin films with thickness of 25 nm, 20 nm, 10 nm and 5 nm at V_{GS} = V_{DS} = 0V (Zero bias), the positions of vacuum level of 5nm CuPc films under saturated condition (V_{GS} = -2 V for ATO and V_{GS} = -40 V for SiO_2, V_{DS} = 0V) are also shown in the blue square. The insets give the schematic energy level alignment under zero bias and saturated conditions (Black solid line for CuPc on SiO_2, and red dash line for CuPc on ATO). The surface potential of the Au electrode is used as a reference.

To further study the mechanism of charge carrier transport in CuPc TFTs with the solution-processed high-k ATO as dielectric, we measure the temperature dependence of mobility. Fig. 5.10 shows the plot of μT as a function of 1000/T. As seen, the relationship between μT and 1/T can be approximately fitted into a straight line. Accordingly, the mechanism of charge carrier transport of CuPc on ATO is related to the Frohlich polaron model, with expression of temperature-dependent mobility [42]:

$$\mu_p = \frac{ea^2}{\hbar}\frac{\omega_s}{T}e^{-\Delta/T} \qquad (5.5)$$

where $\hbar$ is the reduced Planck's constant and a is the hopping length, determined by the distance between neighboring molecules. Generally speaking, the higher the dielectric constant is, the large the polarity of dielectric possesses. In organic transistors, due to the weak van der Waals force between molecules, the use of gate dielectrics with increasing polarizabilities transits the strength of interaction to be

tuned from the weak to the strong coupling regime, and the charge carriers form dielectric polarons on the surface of high-*k* dielectrics. Therefore, the charge carrier transport in the CuPc TFT on ATO mainly occurs through incoherent hopping between neighboring molecules.

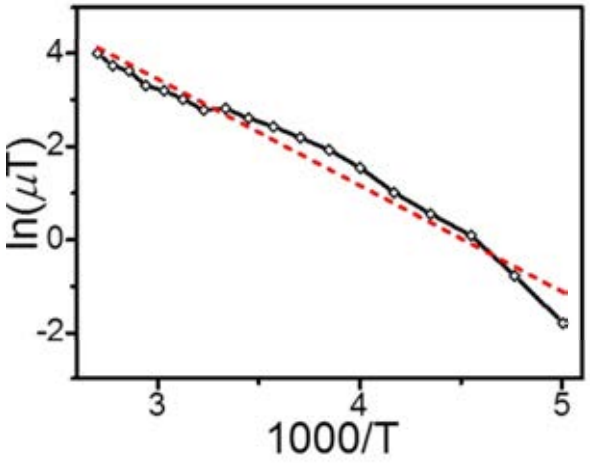

Fig. 5.10 Relationship between μT as a function of 1000/T. The dash line gives the fitting of plot.

5.3.9 Extended application to other materials

To verify the effectiveness and universality of our findings, pentacene and rubrene single crystal based devices are also studied, which have received much research interest in recent years due to their high mobility. Fig. 5.10a and b show the transfer curves of pentacene transistors on SiO_2 and ATO, respectively. As can be seen from Fig. 5.10a, the device on SiO_2 exhibits a high channel current of about 4×10^{-5} A with $V_{GS} = V_{DS} = -40$ V, and the on/off ration is on the order of 10^4. The μ, V_T, and *SS* are determined to be 0.12 cm^2/V s, -2.3 V, and 5.1 V/dec, respectively. The above obtained mobility value is in accordance with the reported one (0.11 cm^2/V s) under similar conditions [43]. As a comparison, the device on solution-processed high-*k* dielectrics can work efficiently in an operation voltage as low as -2 V (Fig. 5.10b).

The low-voltage device possesses a quite high μ of 1.1 cm^2/V s, a small V_T of -0.99 V, an excellent SS of 256 mV/dec. On the other hand, the relatively low on-state current of about 4×10^{-6} A can be attributed to the low V_{DS} (-2 V), and results in a reduced on/off ration of 3×10^3. The electric characteristics of the pentacene base TFTs on high-k ATO still outperform those on SiO_2 to a large extend. Furthermore, the observed mobility of 1.1 cm^2/V s is much higher than those fabricated on alumina prepared by sol-gel [44] and sputtering [12]. Fig. 5.10c and d give the transfer characteristics of Rubrene single crystal FETs on the two types of dielectrics, and the insets show the structure of the corresponding devices. When gated with traditional low-k SiO_2 and under an operation voltage of -30 V, the μ, V_T, SS and on/off ratio are determined to be 2.5 cm^2/V s, 4.9 V, 1.1 V/dec and 10^5, respectively. However, for device on solution-processed high-k dielectrics, the device exhibits excellent electrical characteristics under an operation voltage of only -1.5 V with μ, V_T, SS and on/off ratio values to be 7.0 cm^2/V s, -0.08 V, 101 mV/dec and 10^4, respectively. As anticipated, the solution-processed high-k dielectrics based rubrene single crystal device again possess much better performance than that of SiO_2 based device.

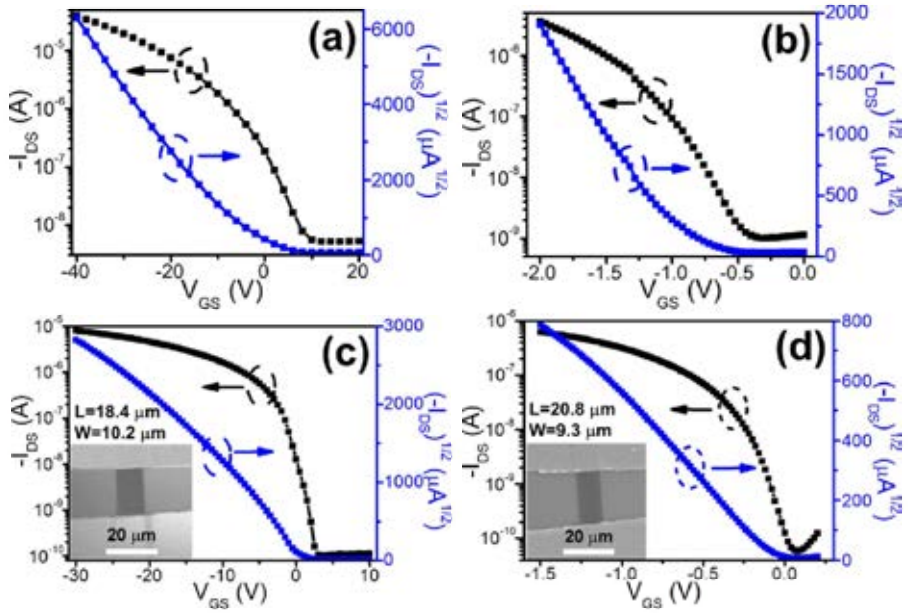

Fig. 5.11 Transfer curves of pentacene TFTs on (a) SiO_2 and (b) ATO; transfer curves of rubrene single crystal FETs on (c) SiO_2 and (d) ATO.

The application of our solution-processed ATO can also be extended to n-type organic semiconductors. Fig. 5.11a and b shows the transfer curves of $F_{16}CuPc$ devices on SiO_2 and ATO, respectively. For SiO_2 based device, the μ is determined to be 0.011 cm^2/Vs. However, for ATO based device, a much higher μ is obtained, with a value of 0.13 cm^2/Vs. Fig. 5.11c and d shows the transfer curves of C60 transistors on SiO_2 and ATO, respectively. The estimated mobility values are 0.051 cm^2/Vs for SiOs and 0.11 cm^2/Vs for ATO. As seen, our ATO can be used effectively as a gate dielectric for low-voltage high-performance OTFTs.

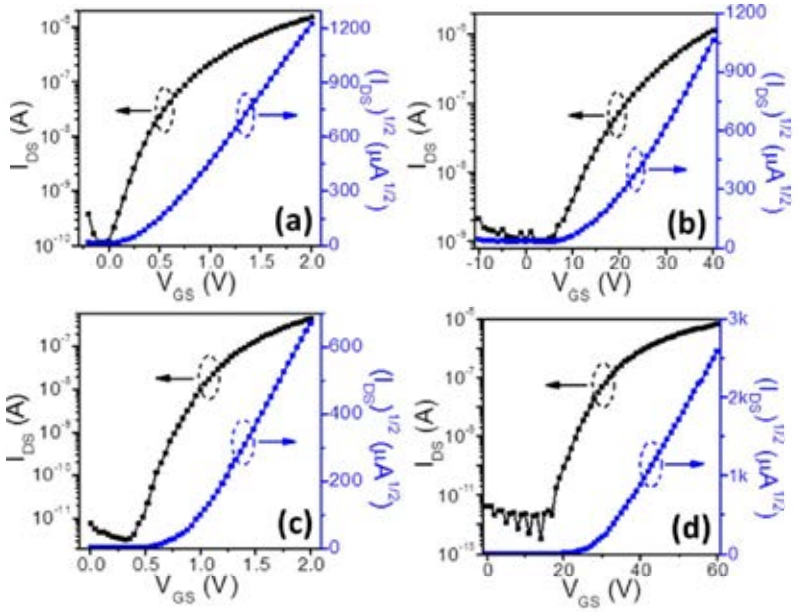

Fig. 5.12 Transfer curves of $F_{16}CuPc$ based transistors on (a) SiO_2 and (b) ATO; transfer curves of C60 based transistors on (c) SiO_2 and (d) ATO.

5.4 Conclusion

In summary, we demonstrate that the low-temperature, solution-processed high-*k* ATO can be a promising choice for fabricating low-voltage OTFTs with high performance. Detailed studies based on CuPc OTFTs reveal that the high performance is attributed to the low surface energy of ATO, which leading to an initial growth of the organic semiconductor that is favorable for the charge carrier transport. In addition, the KPFM results indicate a preferable metal/organic contact, which benefits the charge carrier injection. Moreover, the application of ATO as effective gate dielectric can also be extended to other organic materials, including both p-type and n-type ones. Our findings suggest that the low-temperature, solution-processed high-*k* ATO is applicable in fabrication of high-performance, low-voltage OFETs. In

addition, the present results may provide some clues in designing of high-*k* gate dielectrics in future low-end circuits.

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Chapter 6 Interface Engineering for High-performance Pentacene OTFTs

In this chapter, we demonstrate that by using appropriate interface engineering, the electrical performance of low-voltage pentacene TFTs can be drastically improved. The detailed studies on the effects of interface engineering are carried out, and the mechanisms behind are discussed.

6.1 Introduction

Electronics based on organic semiconductors have received much research interest in recent years [1]. As one of the most important components in organic electronics, the large area applications of organic thin film transistors (OTFTs), covering the fields of displays, sensors and radio frequency identification (RFID) tags [2-4], can be realized if the device performance can be further improved and the fabrication costs can be reduced. Great progress has been made in both design of novel organic semiconductors and device fabrication techniques in the past decades [5-8]. Among various organic semiconductors, pentacene has been one of the most intensively studied materials due to its prefered properties, i.e., good electrical properties, low processing temperature and relatively low cost. Pentacene TFTs with mobility larger than 1 cm^2/Vs have been demonstrated by several groups [9-11]. However, most of the reported high performance pentacene TFTs were fabricated by ultilizing Au as

source and drain (S/D) electrodes because of its inherently high work function (W_F), good conductivity and environmental stability. Unfortunately, the high cost of Au hampers its use in realistic applications. Consequently, finding low cost electrode materials as substitutes of Au is of great technical significance. Several research groups have already successfully used Cu as S/D electrodes in OTFTs and some promising results have been obtained [12-14]. Meanwhile, the integration of Cu is well-developed in the silicon industry. Therefore, using low-cost Cu as the S/D electrodes will further promote the development of OTFTs. However, Cu is generally believed to be unsuitable as the S/D electrodes material due to its low work function (4.2 eV) [15], which results in large hole-injection barrier when contacting with most p-type organic semiconductors, thus deteriorating device performance. As an effective solution to this issue, chemical modifications of Cu electrodes have attracted much attention in order to improve the device performance [16-18].

Another challenge for traditional OTFTs is the high gate voltages required to turn on the devices. For instance, pentacene TFTs based on SiO_2 gate dielectric usually needs an operation voltage as high as -60 V. To achieve lower driving voltage, one must increase the gate areal capacitance. Various types of dielectric materials have been explored for this purpose. Recently, we successfully demonstrated a low-temperature (~200 ^{o}C) solution-processed high-*k* ATO dielectric system, and the CuPc TFTs with this gate dielectric material showed good electrical performance under an operation voltage as low as -1.5 V [19]. However, native oxide dielectric surface usually contains hydroxyl groups (OH^-), which act as defect sites, trapping charge carriers in the channel or inducing undesired charge carriers into the channel [20-22]. This issue can be resolved by introducing a self-assembled monolayer (SAM)

at the interface between dielectrics and organic semiconductors. The SAM can simultaneously passivate the defects and modify the oxide surface, resulting in enhanced device performance [23-25]. Among diverse SAMs, phosphonic acid headed alkylate has shown great advantages of readily chemisorbed onto metal-oxide surface [26-28] with high thermal stability (~ 400 ^{o}C) [29], and other unique merits including better stability to moisture, less tendency of self-aggregation and unlimited by the densed surface hydroxyl groups [30]. Especially, as demonstrated previously, octadecylphosphonic acid (ODPA) can be easily self-assembled on the surface of aluminum oxide with high quality [2, 31].

Here we employ ODPA (as shown in the inset of Fig. 6.1a) modified solution-processed ATO (referred to as ODPA/ATO for short) as gate dielectric to fabricate low-voltage pentacene TFTs. After ODPA modification, the leakage of the dielectric layer can be effectively suppressed by more than one order of magnitude as compared to that of pristine ATO, while preserving a high capacitance density of 200 nF/cm^2. By utilizing *in-situ* modified Cu (*M*-Cu) as source-drain (S/D) electrodes via simple gradated vacuum (from 5×10^{-3} Pa to 3×10^{-4} Pa) evaporation, the resultant pentacene TFT shows an apparent mobility as high as 1.0 cm^2/Vs and a transconductance of 12 μS under an operation voltage of -3 V. On the other hand, device with conventional Au S/D electrodes possesses an apparent mobility of only 0.71 cm^2/Vs, and a markedly lower transconductance of 5.7 μS. The enhancement in device performance is thought to be arising from the optimized electrodes/pentacene interface properties. At the same time, by encapsulating the *M*-Cu with a thin layer of Au, the apparent mobility and the transconductance of pentacene TFTs further increases to 2.3 cm^2/Vs and 19 μS, respectively, which can be ascribed to the

increased conductivity of the electrode itself. Our present studies demonstrate a simple and low-cost route to realize high-performance low-voltage pentacene TFTs. It is expected that the results will shed light on the large scale implementation of OTFTs in low-end electronics in the near future.

6.2 Experimental details

Titanium oxide (TiO_x) sol (0.1 mol/L) was prepared by dissolving titanium (IV) isopropoxide (TIP) ($Ti(OC_3H_7)_4$, 99.99%, Aldrich) into a mixture of methanol and acetic acid, and aluminum oxide (Al_2O_y) sol (0.5 mol/L) was prepared by dissolving aluminum nitrate nonahydrate ($Al(NO_3)_3 \cdot 9H_2O$, 99.99%, Aldrich) into 2-methoxylethanol. Heavily n-doped Si wafers (n^{++}-Si), acting as substrates and gate electrodes, were successively cleaned by acetone, isopropanol and ethanol in ultrasonic for 10 min, and then blown dry with N_2 gas and used immediately for depostion of ATO dielectric. ATO were fabricated by spin coating TiO_x sol and Al_2O_y sol onto n^{++}-Si substrates in sequence at 5000 r/min for 40 s. After each spin coating, the substrates were baked at 200 ± 5 °C for 5 min to ensure the hydrolyzation and decomposition of the precursor and then cooled to room temperature. The as-prepared ATO substrates were immediately immersed in an ODPA (5 mmol/L in isopropanol) for 20 h, followed by a 48 h curing at 145 ^{o}C under vacuum. After that, the ODPA/ATO substrates were then cleaned by isopropanol ultrasonically for 6 min.

OTFTs were fabricated by vacuum deposition of 30-nm thick pentacene film onto the ODPA/ATO substrates at a rate of 0.1 Å/s and a pressure of 3×10^{-4} Pa. During

pentacene deposition, the substrates temperature was kept at 60 °C. Following that, 40-nm thick S/D electrodes were deposited onto pentacene layer in vacuum through a shadow mask at a rate of 0.3 Å/s. The channel length (L) and width (W) were 56 μm and 1500 μm, respectively. For Au and Cu electrodes, the deposition pressure was about 5×10^{-4} Pa. For M-Cu electrodes, a gradient deposition pressure from 5×10^{-3} Pa to about 3×10^{-4} Pa was chosen. As for Au/M-Cu electrodes, a 10-nm thick Au layer was subsequently deposited onto the 30-nm thick M-Cu electrodes without breaking the chamber vacuum.

The leakage of the dielectrics and the electrical characteristics of the pentacene TFTs were measured in ambient conditions using Keithley 4200 SCS. The frequency–dependent capacitance of the dielectrics was measured by HP 4284A in a frequency range of 20 Hz-1M Hz. The depth profile analysis of the electrodes on pentacene were characterized by XPS spectrometer (VG Scientific ESCALAB 250) through Ar^+ etching with an EX05 argon gun at ion beam voltage of 3 keV and emission current of 2 μA.

6.3 Results and discussion

6.3.1 Leakage and capacitance of dielectric

To characterize the electrical properties of the gate dielectric, n^{++}-Si/insulator/Au (MIM) sandwiched structures (inset of Fig. 6.1a) were fabricated to test the leakage current density-voltage and capacitance density (C_i)-frequency characteristics, and the results are plotted in Fig. 6.1. As shown in Fig. 6.1a, after ODPA modification, the

leakage current density can be significantly suppressed by more than one order of magnitude, from 5×10^{-6} A/cm^2 to 4×10^{-7} A/cm^2 under a bias of 2 V. The decrease in leakage current density indicates the formation of densely packed ODPA molecules on the surface of alumina in ATO. The static contact angle of DI water on ODPA/ATO is about 110°, while that on bare ATO is about 35°, further confirming the formation of high quality SAM [32]. The high hydrophobicity of ODPA/ATO surface also signifies its low surface energy, which is believed to be critical to the enhancement of device properties [26, 33, 34]. The capacitance density (C_i) of the dielectric is measured as a function of frequency from 20 Hz to 1M Hz, as shown in Fig. 6.1b. The C_i of ODPA/ATO is 200 nF/cm^2, while that of bare ATO is 250 nF/cm^2. The measured value of C_i for ODPA/ATO is in good agreement with the calculated one by assuming $k = 2.5$ and the monolayer thickness of 2.1 nm for ODPA SAM [31], using the equation $1/C_{total} = 1/C_{ATO} + 1/C_{ODPA}$. The low leakage, low surface energy, and high capacitance density of the ODPA/ATO system endows it with suitability for high-performance low-voltage OTFTs.

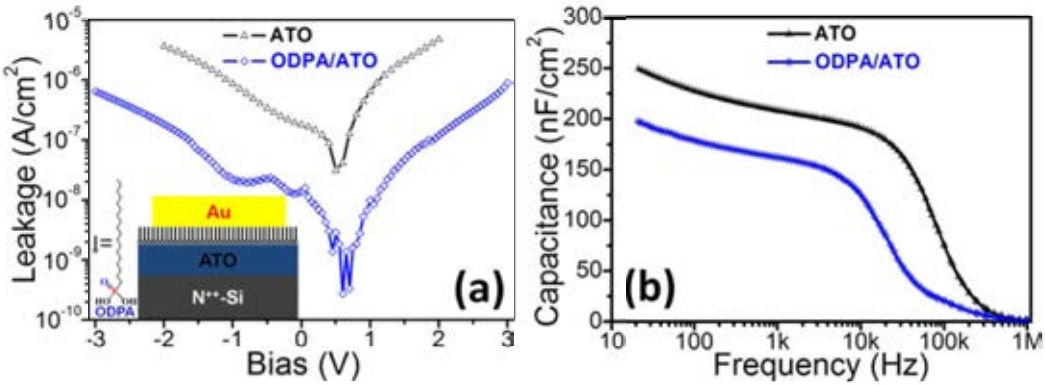

Fig. 6.1 (a) Leakage current density versus bias voltage characteristics of ATO and ODPA/ATO gate dielectrics, the inset shows the molecular structure of ODPA and the MIM device structure; (b) Capacitance density versus frequency plots of ATO and ODPA/ATO gate dielectrics.

6.3.2 Devices electrical characteristics

Fig. 6.2 shows the electrical characteristics of top-contact pentacene TFTs with Au and *M*-Cu S/D electrodes based on ODPA/ATO gate direlectrics. Owing to the high capacitance density of the ODPA/ATO (200 nF/cm^2), the devices worked very well under a low gate voltage of -3 V. All output curves exhibit clear linear and saturation regions with typical p-channel characteristics, and the S/D electrodes materials show a remarkable influence on the device performance, as shown in Fig. 6.2a. Device with Au S/D electrodes exhibits a saturation current of -7.5 μA. Interestingly, the device with *M*-Cu electrodes shows a much higher saturation current of -18 μA, which is about 1.5 times larger than that of the device with Au electrodes. Fig. 6.2b exhibits the transfer curves of the corresponding device in saturation region. For the device with Au electrodes, the on/off ratio is found to be as high as 3×10^5 due to the low leakage of the ODPA/ATO gate dieletric, and the subthreshold slop (*SS*) is 107 mV/dec. By linearly fitting the curve of $(-I_{DS})^{1/2}$ vs V_{GS} in the saturation region, one can calculate the field-effect mobility (μ) and threshold voltage (V_T). The estimated μ and V_T are 0.71 cm^2/Vs and -1.4 V, respectively. Noting that this mobility is calculated without considering the parasitic resistance in the S/D contact region, therefore, it is actually referred to the apparent mobility (μ_{app}). Interestingly, as compared with those values of pentacene TFTs previously reported by other groups, also using similar ODPA/AlO_x gate dielectrics and Au as S/D electrodes [28, 35, 36], the performance of our device is significantly higher. The improved performance may be due to the smaller roughness of the ODPA/ATO surface, with a value of root mean square (RMS) roughness of about 0.4 nm, while those reported values are in the range of 0.75 to 2.1 nm [28, 35]. Transconductance (g_m) is another important parameter of

OFETs, which is defined by $\partial I_{DS}/\partial V_{GS}$ at constant V_{DS}. The estimated g_m in the saturation region of the device with Au electrodes is about 5.7 μS. On the other hand, for the device with *M*-Cu electrodes, the on/off ratio, SS, μ_{app}, V_T and g_m are estimated to be 3×10^5, 156 mV/dec, 1.0 cm^2/Vs, -0.62 V and 12 μS, respectively. The device parameters of our pentacene TFTs are listed in Table 6.1. As clearly seen, the device with *M*-Cu electrodes exhibits a larger on-state current, higher μ_{app} and g_m, and a reduced V_T, as compared to that with Au electrodes. Because both devices were fabricated under the same condition, excepting the S/D electrodes, it is plausibly to ascribe the above observations to the interaction between electrode and organic semiconductor and/or the properties of the electrode itself.

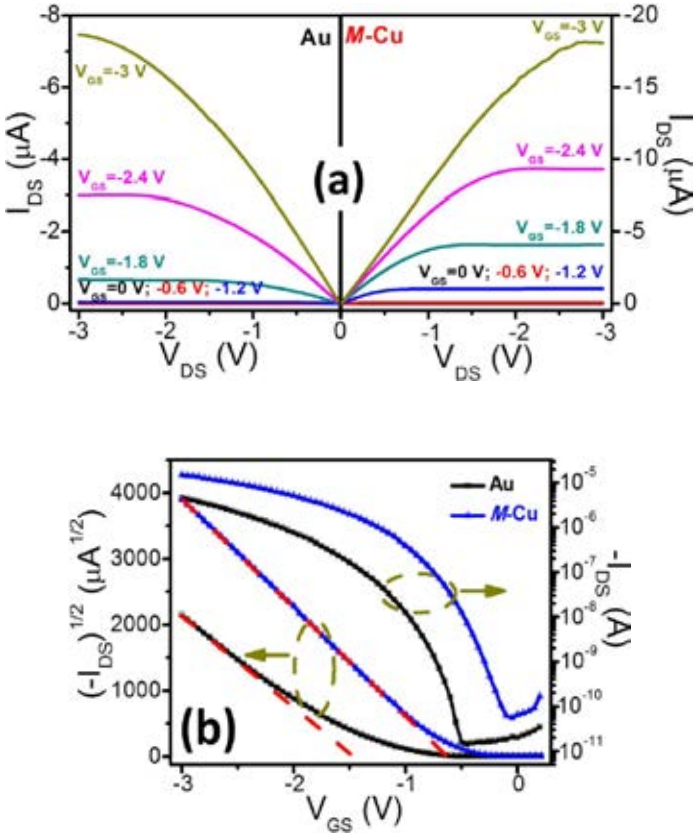

Fig. 6.2 (a) Output curves and (b) Transfer curves of devices with Au and *M*-Cu electrodes.

Table 6.1 Summary of electrical characteristics of pentacene TFTs with different S/D electrodes.

S/D electrodes	Saturation current (μA)	μ (cm^2/Vs)	on/off ratio	*SS* (mV/dec)	V_T (V)	g_m (μS)	Contact resistance (MΩ)
Au	-7.5	0.71	3×10^5	107	-1.4	5.7	0.41
M-Cu	-18	1.0	3×10^5	156	-0.62	12	0.11
Cu	-13	0.85	5×10^5	117	-0.77	7.8	0.26
Au/*M*-Cu	-28	2.0	3×10^5	73	-1.0	19	0.02

Because of its high work function, Au is the most widely used S/D electrode materials for pentacene TFTs. However, during thermal deposition, hot Au atoms usually diffuse into the pentacene film, thus resulting in high resistive grain boundaries and forming interface dipoles by doping the upper layer pentacene. Kim *et al.* have studied the behavior of contact resistance of Au electrodes at different substrate temperatures in pentacene TFTs, and the results show that Au deposited at room temperature (18 ^{o}C) exhibits a higher contact resistance than that at low temperature (-150 ^{o}C), which they ascribed to Au penetration induced degradation in pentacene films [37]. Similar results were also reported by Nakamura *et al.* who found that the degradation could even extend into the channel region [38]. The penetration of Au into pentacene also generates the deep trap states which trap charge carriers and lead to a decreased device performance [39]. On the other hand, interface dipoles between Au and pentacene were also observed by several groups [40-42]. The unfavorable interface dipoles increase the injection barrier height between Au and pentacene, giving rise to an increased contact resistance. When *M*-Cu as S/D electrodes used, Cu atoms are naturally oxidized by residual oxygen species in the chamber due to the low vacuum atmosphere (a typical base pressure of 5×10^{-3} Pa). As a result, a thin layer of CuO_X is *in-situ* formed at the initial stage of thermal

deposition instead of pure Cu. Cu_2O is a widely studied p-type semiconductor with valence band (*VB*) position locating around 5.4 eV [43], which is well aligned with the highest occupied molecular orbital (HOMO) of pentacene (5.0 eV) [44]. Meanwhile, as previously demonstrated by Yun *et al.*, the CuO layer between Cu and pentacene can facilitate the hole injection because of its low barrier height with pentancene [14]. Consequently, the *in-situ* oxidized CuO_x layer can act as an effective hole-injection layer, resulting in optimized electrode/pentacene contact, and hence improving the device performance.

6.3.3 Contact resistance

To quantify the relationship between electrical performance of devices and S/D electrodes, we estimate the contact resistance (R_C) with the transfer line method (TLM) in the linear region [45]. Fig. 6.3 shows the dependence of total resistance on channel length of devices with different electrodes, and R_C is obtained from the intercept by extrapolating the resistance line to the zero channel length. For Au electrodes, the R_C is estimated to be about 0.41 MΩ. For *M*-Cu electrodes, on the other hand, the R_C is drastically reduced, estimated to be about 0.11 MΩ. As discussed previously, when *M*-Cu is used as S/D electrodes, an efficient hole-injection interface can be created between the electrode and pentacene, which is responsible for the observed low contact resistance.

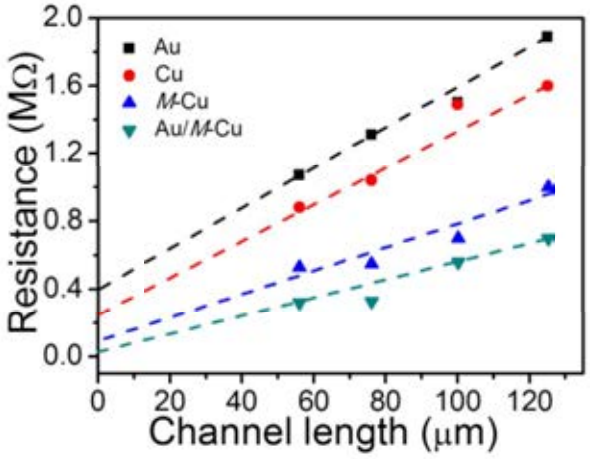

Fig. 6.3 Transfer line method (TLM) polts of pentancene TFTs with different S/D electrodes.

6.3.4 Electrode/pentacene interface structure

To verify the effect of low vacuum on the formation of modified Cu electrodes, devices with Cu S/D electrodes deposited under a higher vacuum level of 5×10^{-4} Pa are also fabricated for comparison. The obtained μ_{app} and g_m are estimated to be 0.85 cm^2/Vs and 7.8 μS, respectively, which are obviously lower than those of the device using *M*-Cu electrodes. The R_C of Cu electrodes is also studied by TLM and the obtained value is 0.26 MΩ (shown in Fig. 6.3), which is about two times as large as that using *M*-Cu electrodes. Therefore, it is obvious that the *in-situ* modification of Cu is of great importance for enhancing the performance of pentacene TFTs. It is interesting to note that, on the other hand, the contact resistance of the Cu electrodes is even lower than that of Au electrodes, which is paradoxical becasue of the lower work function of Cu than Au. Similar results are also observed by other groups [39, 46]. Ultraviolet photoelectron spectroscopy (UPS) studies reveal that the hole injection barrier in Cu/pentacene interface is about 0.95 eV [47], which is higher than

that of Au/pentacene interface (about 0.5 eV) [41]. As a result, our observed phenomenon suggests that the contact resistance is not dominated by the hole injection barrier, but dominated by the interface defects caused by severe Au penetration into pentacene.

To investigate the influence of electrode deposition on the structure of pentacene layer, very thin layers (5 nm) of Au and Cu are deposited onto the pentacene film, and Fig. 6.4 shows the correspondig AFM images. Fig. 6.4a exhitits the AFM image of 30 nm pentacene on ODPA/ATO. As seen, typical herringbone structure with terrace-like grains can be clearly observed. However, after 5 nm Au is deposited (0.2 Å/s, 5×10^{-4} Pa), the herringbone structure is decomposed, and a lot of small aggregates can be found in the interstice of grains, as shown in Fig. 6.4b. In the magnified AFM iamge given in Fig. 6.4c, no terrace is observed, further comfirming the heavy structural damage caused by Au deposition. On the other hand, under the same condition, 5 nm Cu can conformally deposite onto the the pentacene surface, and the terrace structure can be clearly discerned from the high-resolution AFM image, as shown in Fig. 6.4d and e, suggesting a much slighter structural damage caused as compared to Au. At the same time, the root mean square (RMS) roughness are 10. 8 nm, 15.8 nm and 11.6 nm for pristin pentacene, Au/pentacene and Cu/pentacene, respectively, giving additional evidence of severe stuctural damage cuased by Au deposition.

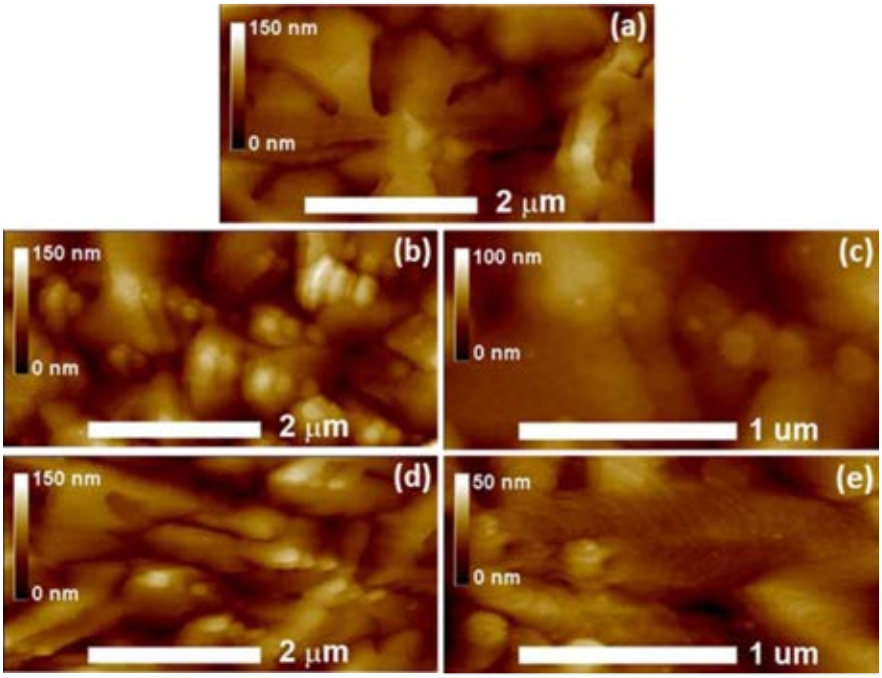

Fig. 6.4 AFM images of (a) 30 nm pentacene on ODPA/ATO; (b & c) 5nm Au and (d & e) 5 nm Cu deposited on pentacene.

6.3.5 XPS characterization

The above results clearly demonstrate that the use of *M*-Cu as S/D electrodes can effectively improve the device characteristics. In order to understand the mechanism behind, XPS depth profiles of different electrodes are characterized and the results are shown in Fig. 6.5. It is found from Fig. 6.5a that, when Au is deposited onto pentacene, a severe inter-diffusion between Au and pentacene is observed. For clarity, we define the region with carbon (C) signal varying form 15% to 85% as the interface region between electrode and pure pentancene layer. As seen from Fig. 4a, the interface has a wide range of about 25 nm in the device with Au electrodes. The severe interdiffusion usually cause structural damage to pentacene in the interface, thus give rise to a highly resistive region and generate deep trapping sites [37, 39, 48],

and consequently, a lowered electrical performance of the device is expected [38, 40, 46]. On the other hand, in the case of *M*-Cu electrodes (Fig. 6.5b), a relative pure Cu layer is observed in the inner part of electrode, and the diffusion of Cu into pentacne layer is obviously suppressed. A sharp interface layer with thickness of about 10 nm can be observed beneath the pure Cu layer, as shown in Fig. 6.4b. By contrast, when Cu is used as S/D electrodes (Fig. 6.5c), a slightly wider inter-diffusion layer is observed (13 nm) as compared to the case of *M*-Cu, indicating a stronger diffusion of Cu into pentacene.

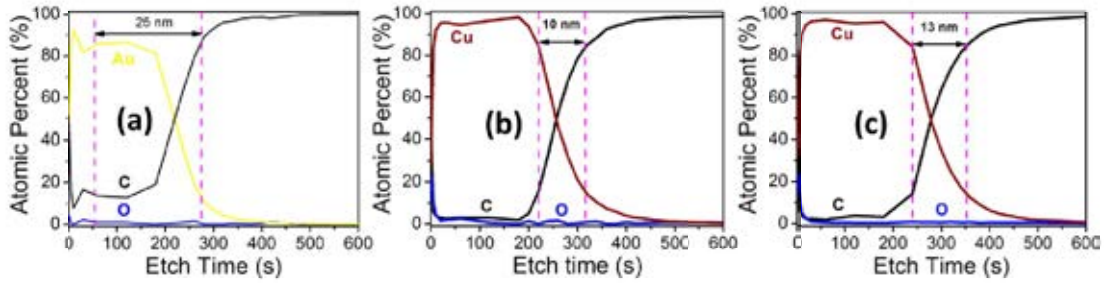

Fig. 6.5 XPS depth profiles of (a) Au, (b) *M*-Cu, and (c) Cu electrodes on pentacene. The insets plot the comparison of C1s XPS spectra obtained in interface between electrode and pentacene and in pure pentacene layer.

To give additional evidence of the high-performance of devices with *M*-Cu electrodes, the interface regions of *M*-Cu/pentacene and Cu/pentacene are studied by XPS. Fig. 6.6 shows representative high-resolution XPS spectra of Cu LMM Auger peak taken from *M*-Cu/pentacne and Au/pentacene interfaces. As can be seen from Fig. 6.6a, at the interface of *M*-Cu/pentacene, the Cu LMM Auger peak can be fitted by two peaks. The main peak at around 918.5 eV can be ascribed to Cu^0 from metallic Cu. The small peak at around 916 eV corresponds to the Cu^+ from Cu_2O, revealing the existence of Cu_2O at the interface of *M*-Cu/pentacene. Therefore, the observed sharp interface in

Fig. 6.4b may arise from the fact that, at the initial stage of the low vacuum deposition, a thin layer of CuO_X is firstly produced on the surface of pentacene by thermal oxidation of Cu with the residual oxygen species in the chamber. The observed oxidation of Cu is in accordance with that reported by others [49]. This thin layer of CuO_X provides a protection against the diffusion of Cu atoms into the pentacene layer, and suppresses the unfavorable structural degradation as well as the formation of interface dipoles. At the same time, the CuO_X layer can also act as a hole-injection layer due to its high work function [15, 50]. On the other hand, as shown in Fig. 6.6b, the only peak at around 918.5 eV can be ascribed to Cu^0 from metallic Cu, obvious signal of CuO_X is detected in the interface region of Cu and pentacene, indicating negligible oxidation of Cu when deposited at a higher vacuum condition of 3×10^{-4} Pa. Consequently, a lower density of interface defects is expected.

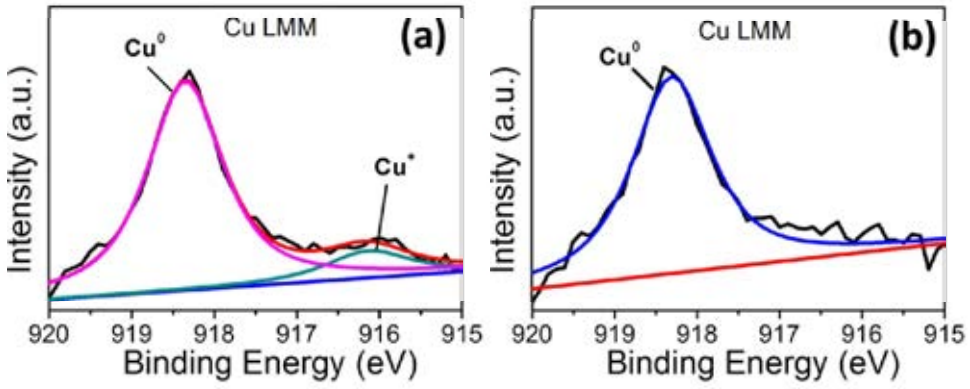

Fig. 6.6 Representative high-resolution XPS spectra of Cu LMM Auger peak taken form the interface of (a) *M*-Cu/pentacene and (b) Cu/pentacene.

6.3.6 Proposed band diagram

On the other hand, although good band alignment between Au and pentacene, interface dipoles are commonly observed phenomenon at their interface as evidenced by UPS studies [51-53]. As shown in previous studies, interface dipoles can cause a down shift of vacuum level (VL) of pentacene and redistribution of electrons from pentacene to electrode, thus acting as an opposite electric field to the charge injection, and negatively shifting the V_T of device. Owing to the higher density of interface defects and dipoles between Au and pentacene, a negatively shifted V_T is therefore anticipated, which is in good agreement with the experiment results. To better understand the mechanism, the band diagram of different electrode materials are given in Fig. 6.7. For Au electrodes (Fig. 6.7a), an typical value of interface dipole (Δ) of 0.5 eV is adopted [41]. Due to the physical and chemical damage caused in the interface of Au/pentacene, some deep trap sites are induced. As for Cu electrode (Fig. 6.7b), an interface dipole of 0.15 eV can be estimated according to the reported hole-injection barrier height of 0.95 eV [39, 47]. When M-Cu is used as the S/D electrodes (Fig. 6.7c), the thin layer of Cu_2O in the interface serves as a effective hole-injection layer. At the same time, as discussed previously, the interface dipole is suppressed.

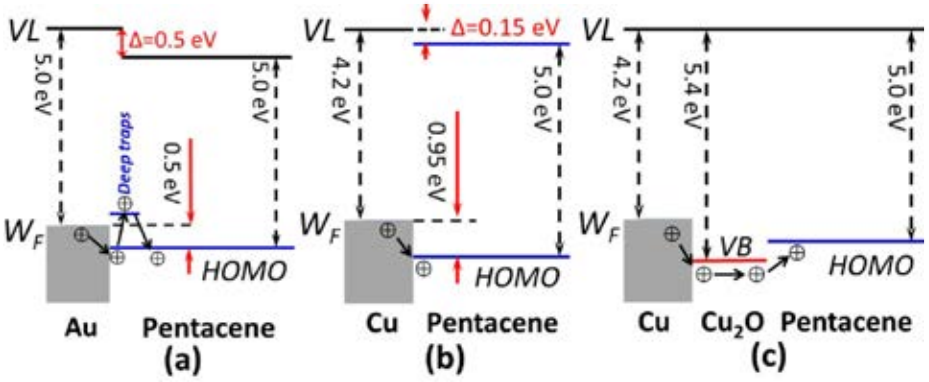

Fig. 6.7 Schematic energy diagrams of (a) Au/pentacne, (b) Cu/pentacene and (c) *M*-Cu/pentacene.

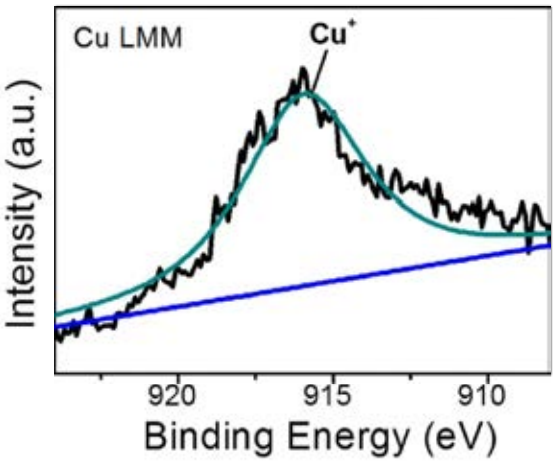

Fig. 6.8 High-resolution XPS spectra of Cu LMM Auger peak obtained from the top surface of *M*-Cu electrodes.

6.3.7 Au encapsulation

In addition to the interfacial properties of S/D electrodes and organic semiconductor, the electric conductivity of the electrode itself is another concern which can also influence the performance of OTFTs drastically [54, 55]. One major drawback associated with the use of Cu as S/D electrodes is the inevitable oxidation of Cu by oxygen species and water in air, which can be evidenced from the high-resolution XPS spectra of Cu Auger peak taken from the top surface of *M*-Cu electrodes shown in Fig. 6.8. As seen, the only peak located at around 916 eV can be assigned to Cu^{+}, indicating that the surface of *M*-Cu is totally oxidized to Cu_2O. The surface oxidized layer on Cu will result in the increased electrode resistivity over time, and hence deteriorate the device performance [56, 57]. This issue can be overcome by depositing a thin layer of Au on the top of Cu electrode, functioning as an encapsulation layer to prevent the oxidation of Cu and improve the conductivity of the

electrode. Fig. 6.9 shows the electrical characteristics of representative pentacene TFT using 10 nm Au encapsulated 30 nm *M*-Cu (Au/*M*-Cu) as S/D electrodes. As shown in Fig. 6.9a, the output curves exhibit typical p-channel feature, with a saturation current of -28 μA under $V_{GS} = V_{DS}$ of -3 V, which is about 1.5 times as large as that with *M*-Cu electrodes. Fig. 6.9b gives the corresponding transfer curves. The on/off ratio, *SS*, μ_{app}, V_T and g_m are estimated to be 1×10^6, 73 mV/dec, 2.0 cm^2/Vs, -1.0 V and 19 μS, respectively, and the highest μ_{app} achieved is about 2.3 cm^2/Vs. As seen, the electrical properties of the device are markedly improved after Au encapsulation.

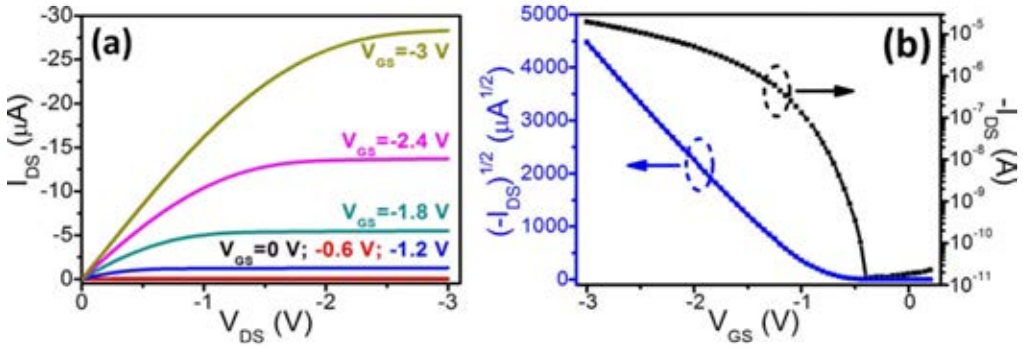

Fig. 6.9 (a) Output curves and (b) Transfer curve of device with Au/*M*-Cu electrodes.

To verify the effect of Au encapsulation on preventing the oxidation of Cu, XPS depth profiles of Au/M-Cu electrodes is recorded and the result is given in Fig. 6.10. The carbon concentration is high and then decreases drastically with prolonging the etching time, which is most probably due to the adventitious surface contamination, as can be seen from Fig. 6.10. The Au and Cu show a strong inter-diffusion, indicating good electric contact. In addition, nearly no diffusion of Au into pentacene is detected. The inset of Fig. 6.10 shows the variation of O concentration with etching time of different electrodes. As clearly seen, with the encapsulation of Au, the diffusion of O

into the electrode is effectively suppressed in Au/*M*-Cu electrode, and the surface oxidation of the underneath Cu is then prevented. As a result, the conductivity of the Au/*M*-Cu is expected to be enhanced as compared to that of *M*-Cu. Accordingly, the R_C obtained by TLM (shown in Fig. 6.3) of the device with Au/*M*-Cu electrodes is significally reduced to only 0.02 MΩ, which is much smaller than that of *M*-Cu. The reduced contact resistance is sensibly assigned to the increase in the conductivity of electrode itself. As a result, this contributes to the improved electrical performance of the obtained device. To make it more clear, we can also calculate the intrinsic mobility (μ_i) of the devices from the slop of each line in Fig. 6.3, and the calculated μ_i are 1.8 cm^2/Vs, 2.0 cm^2/Vs and 2.3 cm^2/Vs for Au, *M*-Cu and Au/*M*-Cu based divices, respectively. As expected, these values are higher than their corresponding μ_{app}.

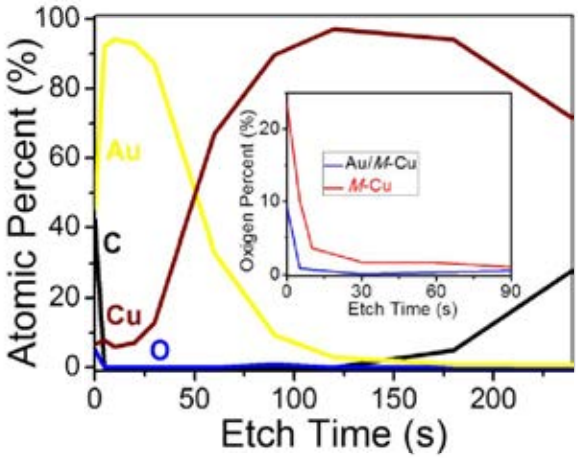

Fig. 6.10 XPS depth profiles of Au/*M*-Cu electrodes on pentacene; the inset compares the variation of O percentage with etching time on different electrodes.

6.4 Conclution

In conclusion, we have successfully demonstrated high-performance low-voltage pentacene TFTs using *M*-Cu as S/D electrodes and solution-processed ODPA/ATO gate dielectric. The fabricated devices show a significant improvement in device performance as compared with that of the devices having Au electrodes. This is plausibly ascribed to more efficient hole injection, smaller density of interface defects, consequently reduced contact resistance between the *M*-Cu electrodes and pentacene thin film. Upon encapsulation of *M*-Cu electrodes with a thin layer of Au, the electrical characteristics are further enhanced due to the suppression of the oxidation of Cu in ambient, leading to increase in the conductivity of the electrode itself. Our investigation heralds a simple and effective way to realize high-performance low-voltage OTFTs. The use of low-cost metal electrodes instead of Au can greatly faciliate the realistic applications of OTFTs in large area.

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Chapter 7 Flexible Pentacene OTFTs

Low-voltage, flexibility and low-cost are essential prerequisites for large scale application of organic thin film transistors (OTFTs) in future low-end electronics. In this chapter, low-voltage flexible pentacene OTFTs are demonstrated by using ODPA/ATO as gate dielectric and Au/M-Cu as S/D electrodes. At the same time, the mechanical flexibility and reliability of the pentacene OTFTs are also studied and discussed in detail, and the observed degradation of the device performance under strains is attributed to the damage induced in the electrodes giving rise to increased contact resistance and the phase transition from thin film phase to bulk phase of the pentacene films.

7.1 Introduction

Organic thin film transistors (OTFTs) have attracted considerable research interest over the past decades due to their potential applications in low-end electronics, such as displays, smart cards and disposable sensors [1-5]. In addition, the inherent

mechanical flexibility and low-temperature processibility of organic semiconductors stimulate the attempts of integration of OTFTs with bendable substrates, which is of great technical significance because they are fundamental building blocks of most practical electronic devices. Among various organic semiconductors, pentacene has been one of the most promising candidates due to its high field-effect mobility and good environmental stability, at the same time, flexible pentacene OTFTs have been successfully demonstrated by many groups [6-10]. Unfortunately, most of the reported devices with high performance utilize Au as source-drain (S/D) electrodes, which hampering the large scale applications of OTFTs because of the high cost of Au. Therefore, researches have been driven by the attempts in finding other low cost electrode materials, such as Cu, to replace Au. However, OTFTs with Cu as S/D electrodes usually suffer from deteriorated device properties due to its low work function (4.2 eV) [11], which resulting in large hole-injection barrier. To solve this critical issue, chemical modification of Cu electrodes have attracted much attention in order to improve the device performance [12-14].

In parallel to continual efforts in finding low-cost S/D electrode materials, the exploring of high-capacitance gate dielectrics with acceptable mechanical reliability which allowing low driving voltage of flexible OTFTs is also a key challenge to be

overcome. Furthermore, to realize printability in future organic electronic industry, it is necessary to develop low-temperature, solution-processible dielectric materials that can be compatible with the high-throughput production, such as roll-to-roll processing. The use of polymer dielectrics may achieve good mechanical flexibility and solution-processibility, however, the device performance are usually limited by the high leakage current and high driving voltage due to the low gate capacitance [7, 15-18]. In contrast, the choice of high-*k* inorganic dielectrics seems to be a promising way. Recently, we have introduced a solution-processed high-*k* ATO dielectric system, and the resultant CuPc OTFT exhibits excellent electrical characteristics under an operation voltage of -1.5 V [19]. More importantly, this dielectric material can be processed at a low temperature of ~200 ^{o}C, which is compatible with some flexible plastic substrates, such as polyimide (PI). At the same time, the unfavorable hydroxyl groups (OH^{-}) on the surface of native oxide dielectric can be easily passivated by introducing a self-assembled monolayer (SAM), which is also solution-processible [20, 21].

In this paper, we use octadecylphosphonic acid (ODPA) self-assembled onto a low-temperature, solution-processed ATO (ODPA/ATO) as gate dielectric to fabricate flexible OTFTs. The solution-processed ODPA/ATO system exhibits

excellent dielectric characteristics, with a leakage current density lower than 10^{-6} A/cm^2 under bias voltages of ± 3 V, and a high capacitance density of 180 nF/cm^2. By employing Au encapsulated *in-situ* modified low-cost Cu (Au/*M*-Cu) as S/D electrodes, the resultant flexible pentacene OTFT shows superior electrical performance with field effect mobility (μ) of 1.5 cm^2/Vs, threshold voltage (V_T) of -0.4 V, on/off ratio of 2×10^4 and subthreshold swing (*SS*) of 161 mV/dec under an operation voltage of only -2 V. The device characteristics under different mechanical strains are also examined and discussed in detail. Our results demonstrate a simple and feasible route to fabricate high-performance flexible OTFTs with solution-processed dielectric at low-cost, which is of technical importance to realize large-scale application of organic electronics.

7.2 Experimental details

125 μm polyimide substrates (provided by CEN Electronic Material Co., Ltd.) were successively cleaned by isopropanol and ethanol in ultrasonic for 10 min, and then blown dry with N_2 gas and used immediately for deposition of gate electrode. 5 nm Cr was deposited onto the PI substrates under a vacuum of 3×10^{-4} Pa, followed by

deposition of 20 nm Au without breaking the chamber vacuum. After that, the substrates were cured at 200 °C for 30 min in vacuum.

Titanium oxide (TiO_x) sol (0.1 mol/L) was prepared by dissolving titanium (IV) isopropoxide (TIP) ($Ti(OC_3H_7)_4$, 99.99%, Aldrich) into a mixture of methanol and acetic, and aluminum oxide (Al_2O_y) sol (0.5 mol/L) was prepared by dissolving aluminum nitrate nonahydrate ($Al(NO_3)_3 \cdot 9H_2O$, 99.99%, Aldrich) into 2-methoxylethanol. ATO were fabricated by spin coating TiO_x sol (5000 r/min, 40 s) and Al_2O_y sol (4000 r/min, 20 s) onto the above flexible substrates in sequence. After each spin coating, the substrates were baked at 200 ± 5 °C for 3 min to ensure the hydrolyzation and decomposition of the precursor and then cooled to room temperature. The as-prepared flexible ATO substrates were then immediately immersed in an octadecylphosphonic acid (ODPA) solution (5 mmol/L in isopropanol) for 20 h, followed by a 48 h curing at 145 °C in vacuum. Finally, the flexible ODPA/ATO substrates were washed by isopropanol ultrasonically for 6 min and blown dry by N_2 gas for use.

OTFTs were fabricated by vacuum deposition of 30 nm pentacene film onto the above flexible substrates at a rate of 0.1 Å/s and a pressure of 3×10^{-4} Pa. During pentacene deposition, the substrates temperature was kept at 60 °C. Following that, 30

nm *in-situ* modified Cu (*M*-Cu) S/D electrodes were firstly deposited onto the pentacene layer under a gradient deposition pressure from 5×10^{-3} Pa to about 3×10^{-4} Pa through a shadow mask at a rate of 0.3 Å/s, and then 10 nm Au was deposited onto the 30 nm *M*-Cu electrodes without breaking the chamber vacuum. In order to investigate the capacitance and leakage current, parallel-plate capacitors are fabricated by depositing Au electrodes on n^{++}-Si substrates with ODPA/ATO fabricated by the same procedure as that of flexible substrates.

The frequency-dependent capacitance of the dielectrics was measured by HP 4284A in a frequency range of 20 Hz-100k Hz. The leakage of the dielectrics and the electrical characteristics of the pentacene OTFTs were measured in ambient conditions using Keithley 4200 SCS. The morphologies of the pentacene thin film was characterized by atomic force microscopy (AFM, Nanoscope IIIa) in tapping mode. The two-dimensional grazing incidence X-ray diffraction (GIXD) pattern was obtained at beamline BL14B1 (λ=1.24 Å) of the Shanghai Synchrotron Radiation Facility with an incident angle of 0.15^{o}. The bending tests are conducted by placing the flexible pentacene OTFTs on glass tubes with different diameters to achieve a concave or a convex bending.

7.3 Results and discussion

7.3.1 Leakage and capacitance characterization

To characterize the electrical property of the solution-processed dielectrics, parallel plate capacitors with n^{++}-Si/insulator/Au sandwiched structure are fabricated to test the leakage current density and the capacitance density (C_i), and the representative results are plotted in Fig. 7.1. As can be seen form Fig. 7.1a, after ODPA modification, the leakage current density can be effectively suppressed by one order of magnitude under bias voltages of ±3V, indicating that the ODPA molecules assemble densely on the surface of alumina in ATO. The static DI water contact angle increases form about 35^o to about 110^o upon ODPA modification, further confirming the formation of high quality SAM [22]. The high hydrophobicity of the ODPA/ATO system also signifies its low surface energy, which is believed to be critical in enhancing the device properties [23-25]. Fig. 7.1b shows the frequency dependent capacitance density of the capacitor. A slight increase in capacitance density with decreasing frequency is observed in both ATO and ODPA/ATO, which can be due to the Maxwell-Wagner space charge polarization in the ATO layer [19, 26, 27]. The obtained C_i value is 180 nF/cm^2 for ODPA/ATO at 20 Hz, which is in good agreement with the calculated one by using the equation $1/C_{total}=1/C_{ATO}+1/C_{ODPA}$ [28]. Such a high capacitance density is

sufficient to induce adequate charge carriers at a low voltage. By taking the advantages of its low leakage, low surface energy and high capacitance density, the ODPA/ATO is expected to be a promising candidate for low-voltage high-performance OTFTs.

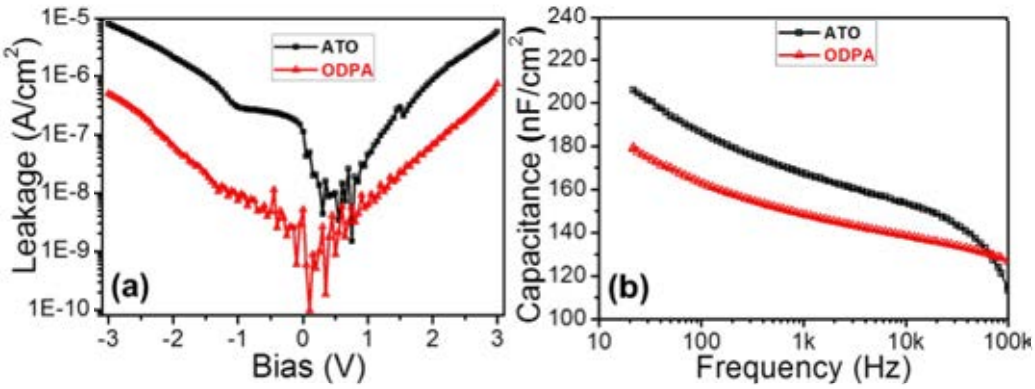

Fig. 7.1 (a) Leakage current density versus bias voltage and (b) capacitance density versus frequency characteristics of ATO and ODPA/ATO gate dielectrics.

7.3.2 Structure of pentacene thin film

Fig. 7.2a exhibits the atomic force microscopy (AFM) image of 30 nm pentacene film deposited on flexible substrate, and typical herringbone structure with feature size of ~ 2 μm can be clearly observed. In addition, in magnified image, terraces can be clearly observed, as shown in the upper right one. A step height of ~ 1.5 nm is estimated from the cross-sectional profile along the dark dash line, as shown in the

lower right image in Fig. 7.2a. This step height suggests that the pentacene molecules are oriented in an edge-on configuration with the long molecular axis parallel to the substrate normal. To further explore the crystalline structure and molecular ordering of the deposited pentacene film, the corresponding two-dimensional grazing incidence X-ray diffraction (2D GIXD) pattern is recorded and the result is given in Fig. 7.2b. As seen, the (001) reflection peak along the Q_z (out of plain) axis can be assigned to the "thin film phase" with a layer spacing of ~1.54 nm, which is approximately equal to the up-right standing molecular height [29]. Additionally, the {1, ±1}, {0, 2} and {1, ±2} in plane Bragg rod reflections at Q_{xy} (in plain) positions indicate that the pentacene crystal has a highly oriented 3D herringbone packing structure, as evidenced by many groups [29-31]. The above GIXD results are in good agreement with the AFM observations. At the same time, the "thin film phase" is believed to benefit the charge carrier transport, due to the preferred π-orbital overlap [32].

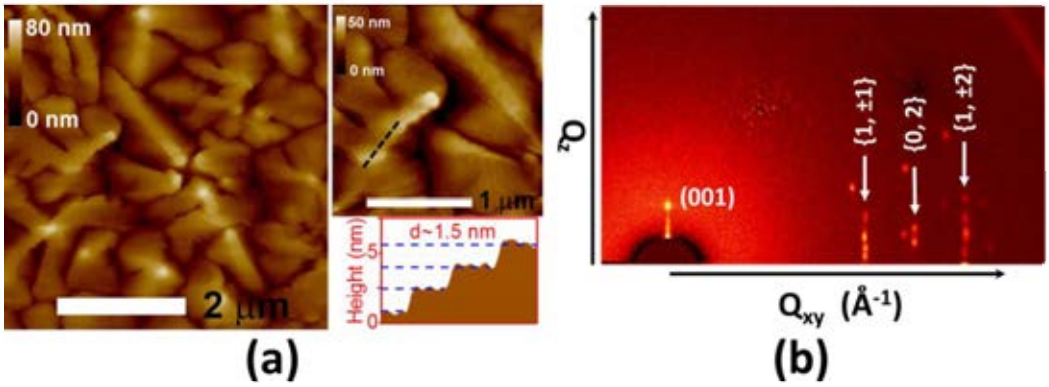

Fig. 7.2 (a) AFM images of 30 nm pentacene film deposited on ODPA/ATO and the cross-sectional profile along the dark line; (b) the corresponding 2-D GIXD pattern.

7.3.3 Electrical properties of flexible OTFTs

Besides the dielectric properties and the pentacene thin film microstructures, the choices of S/D electrode materials are also crucial in achieving high-performance devices. Au has been the most widely used S/D electrode material for pentacene OTFTs because of its inherently high work function, good conductivity and environmental stability. However, the high cost of Au hinders its use in realistic applications. Furthermore, during thermal deposition, hot Au atoms usually diffuse into the pentacene film, thus resulting in high resistive grain boundaries and forming interface dipoles by doping the upper layer pentacene, and deteriorating the device perofrmance [33-36]. In Chapter 6, we have successfully introduced the An/*M*-Cu system that can be used effectrively as the S/D electrodes to obtain high-perforamnce

pentacne OTFTs. Here, take the advantages of this system, we also employ it to fabricate flexible OTFTs. Fig. 7.3 shows the electrical characteristics of flexible pentacene OTFT using Au/*M*-Cu as S/D electrodes. Due to the high capacitance density (180 nF/cm^2) of the ODPA/ATO system, the device can work perfectly under a low operating voltage of only -2 V. As shown in Fig. 7.3a, the output curves exhibit distinct linear and saturation regions of a typical p-type feature, with a high saturation current on the order of 10^{-5} A under $V_{GS} = V_{DS} = -2$ V. No obvious leakage can be observed at zero V_{DS} due to the high quality of the ODPA/ATO system. Fig. 7.3b plots the corresponding transfer curve in saturation region, from which the electrical parameters can be extracted. The device possesses outstanding electrical characteristics, with on/off ratio of 2×10^4, field effect mobility (μ) of 1.5 cm^2/Vs, threshold voltage (V_T) of -0.4 V and subthreshold swing (SS) of 161 mV/dec. To the best of our knowledge, this obtained mobility value is among the highest ones achieved in flexible pentacene OTFTs. In comtrast, the device with 40 nm Au S/D electrodes is also fabricated and tested, and the electrical characteristics are given in Fig. 7.3c and d. As shown in Fig. 7.4c, due to the high quality of the ODPA/ATO system, no obvious leakage is detected near zero V_{DS} from the output curves of the device with Au S/D electrodes. The saturation current is about 3.6×10^{-6} A at $V_{DS} = V_{GS} = -2$ V. However, the

curves exhibit apparent "S" shape at low V_{DS}, which is an indication of contact effect, resulting from the high contact resistance. Fig.7.4d gives the corresponding transfer curve. The extracted on/off ratio, μ, V_T and *SS* are estimated to be 10^4, 0.6 cm^2/Vs, -0.7 V and 182 mV/dec, respectively. Clearly, the obtained electrical characteristics of device with Au electrodes are much lower as compared to the device with Au/*M*-Cu electrodes. At the same time, the Au/*M*-Cu can offer a hole-injection perferred interface between electrodes and pentacene, as dicussed in Chapter 6. Therefore, the high performance of our flexible pentacene OTFT with Au/*M*-Cu S/D electrodes can be ascribed to the "thin film pahse" of the deposited pentacene film and the potimized electrode/pentacene interface property.

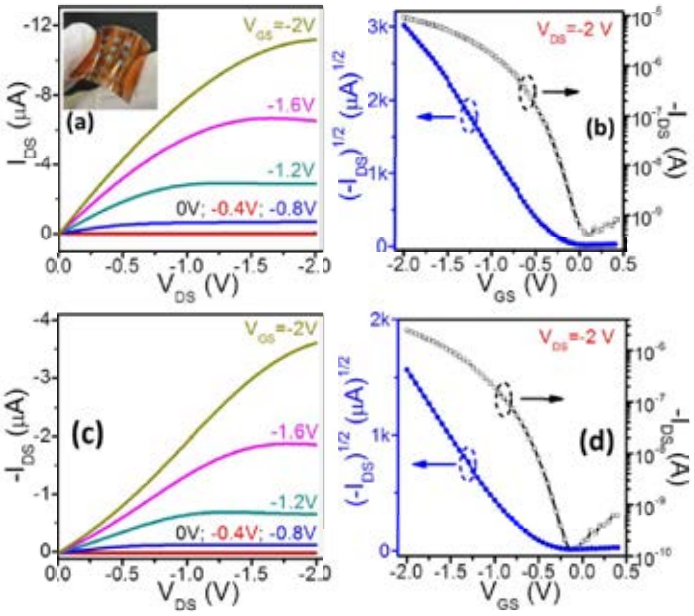

Fig. 7.3 (a) Output curves and (b) Transfer curve of flexible pentacene OTFT with Au/*M*-Cu S/D electrodes; (c) output curves and (d) Transfer curve of flexible pentacene OTFT with 40 nm Au S/D electrodes. The inset in figure (a) show the structure of the flexible device.

7.3.4 Mechanical performance characterization

To test the mechanical flexibility, another two different devices (I and II) are fabricated. The mechanical flexibility of the devices is investigated at controlled bending radii along the channel length direction, under either compressive or tensile condition. Fig. 7.4 shows the relative variation in the normalized μ and V_T of the devices as a function of strain, which defined as $d_s/2R$, where d_s is the substrate thickness and R is the bending radius [7], as illustrated in Fig. 7.4c. By convention, the values are positive with compressive strain and negative with tensile strain. As can

be seen form Fig. 7.4a, in case of compressive strains (device I), the mobility decreases gradually with increasing the strain at first, and then a rapid degradation is observed. The μ decreases to about 60% of its original value at strain of 2.7%, and the V_T shifts in a small range from -0.55 V to -0.58 V. On the other hand, as shown in Fig. 7.4b, in case of tensile strains (device II), a more drastic degradation of the mobility is observed and only about 10% is preserved at strain of -2.7%, and the V_T shifts in a larger range from -0.46 V to -0.68 V. The gate leakage current keeps almost unchanged after bending test indicating the robust integration of the ODPA/ATO with flexible substrates, and the performance of the devices can be more or less recovered after relaxation. In principle, the compressive strain may lead to smaller spacing between pentacene crystals and the tensile strain may cause larger spacing, hence the mobility is expected to increase in compressive strain and decrease in tensile strain, as having been observed by other groups [7, 37]. However, our results of compressive strain exhibit an opposite trend, and the device in compressive strain shows better mechanical stability than in tensile strain. These phenomena are worthy of studying in detail.

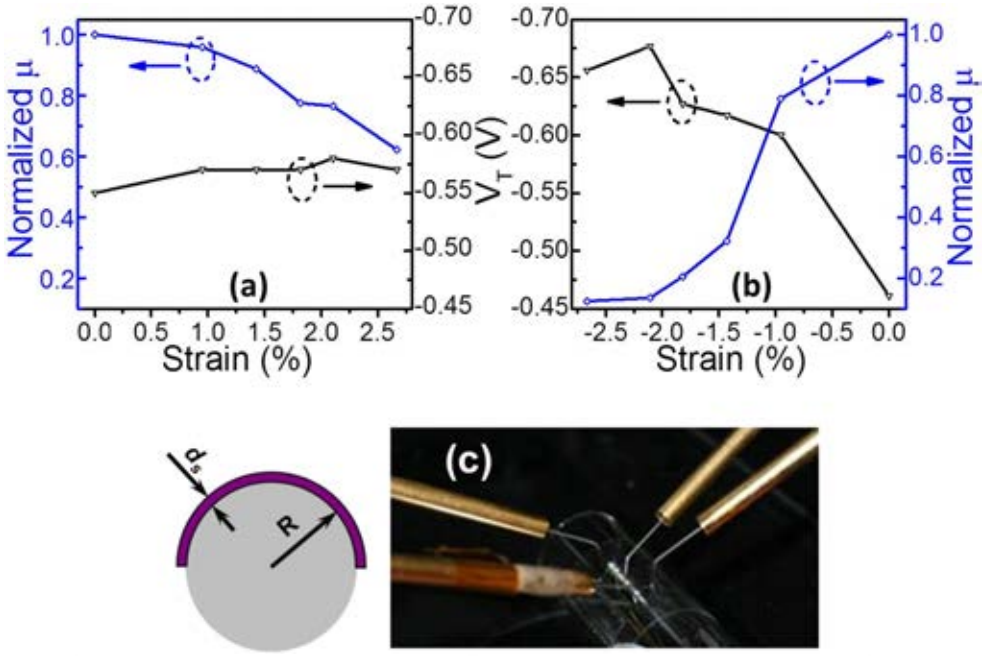

Fig. 7.4 Relative changes in the normalized mobility of the flexible pentacene OTFTs as a function of (a) compressive and (b) tensile strains; (c) gives an illustration of the testing setup.

Yang *et al.* have reported that the mechanical strain can induce phase transitions of pentacene between thin film phase and bulk phase [38]. To investigate the crystal structure variation, XRD patterns of 30 nm pentacene on flexible substrates are recorded under strains of ± 2.7%, and the results are shown in Fig. 7.5. The substrate background has been removed from the original XRD data. For the as-deposited pentacene film, the only peak indexed as $(001)_T$ can be assigned to the thin film phase of pentacene, with interlayer spacing of about 1.54 nm, which is in good agreement with the previous GIXD result [39]. However, under both compressive and tensile

strains, another peak shows up, which corresponds to the bulk phase of pentacene with interlayer spacing of 1.45 nm as denoted by $(001)_B$ in Fig. 7.5, indicating a phase transition occurs. Further investigations show that the mass fraction of the thin film phase is about 20 % in compressive strain (2.7 %), while about 14 % in tensile strain (-2.7 %). Because the bulk phase is reported to possess lower intrinsic mobility than the thin film phase [39], the remained higher thin film phase mass fraction may partly account for the better mechanical flexibility of the OTFTs under compressive strains. On the other hand, during the examination of the mechanical flexibility, in both compressive and tensile strains, some cracks along the channel width direction can be found in the S/D electrodes under magnifier, and the number of cracks increases with the absolute value of strains (not shown here). The cracks may deteriorate the contact between the S/D electrodes and the underneath pentacene, which also contribute to the decreased electrical performance of the devices with increasing the strains.

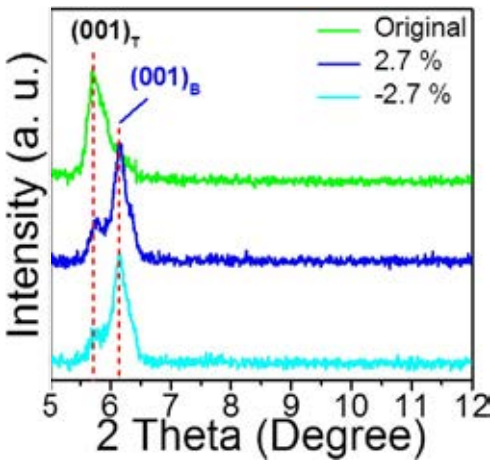

Fig. 7.5 Changes in XRD patterns of 30 nm pentacene film with different strains.

To further investigate the mechanical reliability, cyclic bending test based on the above two devices are performed in both compressive (device I) and tensile (device II) bending at a radius of 4 mm. The electric characteristics of the devices are measured in flat state immediately after bending. Fig. 7.6 shows the changes in normalized μ and V_T as a function of bending times. As can be seen from Fig. 7.6a, under a compressive strain, μ decreases drastically to about 50% of its original value with the first 500 bending cycles, and then gradually to about 40% after 2000 bending cycles. Similar trends can be observed in the variation of V_T with the bending cycles. On the other hand, under a tensile strain, both μ and V_T change gradually with bending times, as shown in Fig. 7.6b. Notably, the device performance with tensile strain shows a

lower reliability as compared to that with compressive strain, and μ decreases to about 15% of its original value after 2000 bending times.

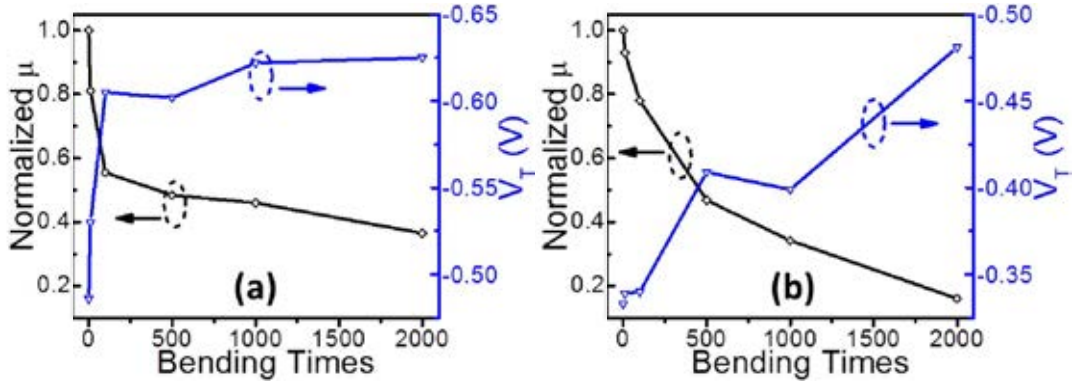

Fig. 7.6 Relative changes in normalized mobility and threshold voltage as a function of bending cycles under (a) compressive and (b) tensile strain.

Fig. 7.7 shows the evolution of the crystal structure with the bending cycles of the 30 nm pentacene film on flexible substrates under either compressive strain or tensile strain. Obvious phase transition from thin film phase to bulk phase can be observed in both strain conditions with increasing the bending cycles. In particular, as shown in the inset of Fig. 7.7a, the mass fraction of the thin film phase decreases monotonously to about 20 % with the first 500 bending cycles, and then keeps almost unchanged up to 2000 bending cycles. On the other hand, under tensile bending condition, a continuous decrease in the mass fraction of the thin film phase is observed with increasing the bending cycles, as can be seen from the inset of Fig. 7.7b. The bulk

phase has proven to show a lower mobility than the thin film phase [39], therefore, the degradation in the performance of flexible devices with bending cycles is attributed partly to the phase transition from thin film phase to bulk phase in the pentacene film.

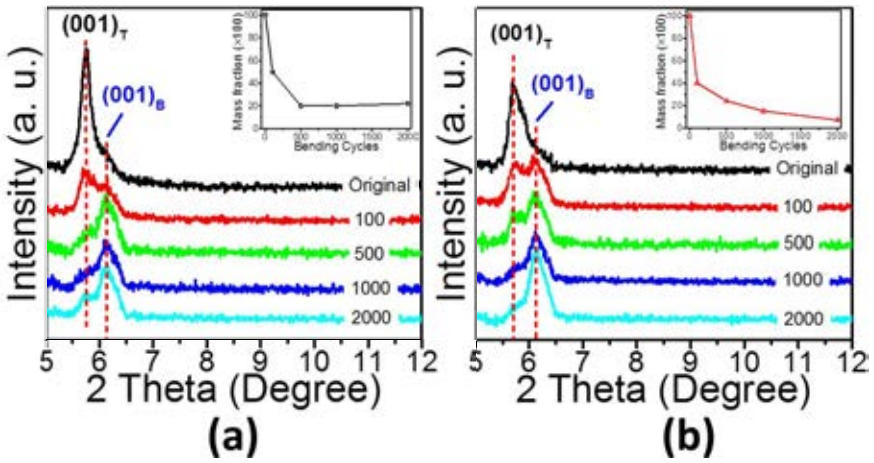

Fig. 7.7 Variation of XRD patterns of 30 nm pentacene on flexible substrates with bending cycles under (a) compressive strain and (b) tensile strain; the insets exhibit the changes of mass fraction of the thin film phase in the respective pentacene film.

7.3.5 Ambient stability study

Furthermore, as discussed previously, both compressive and tensile strains will induce cracks in the S/D electrodes, and the cracking density is believed to increase with bending cycles. As a result, the oxygen and water molecules in ambient atmosphere might be absorbed through the cracked S/D electrodes and diffuse into the

underneath pentacene film. Hu *et al.* have studied the effect of oxygen concentration to the performance of pentacene OTFTs, and they found that the charge transfer complex formed between oxygen and pentacene can lead to a decrease in mobility [40]. The polar water molecules diffused into the pentacene grain boundaries usually act as charge trapping centers, and thus reducing the mobility [41]. To quantify the effect of oxygen and water in ambient to the electrical performance of flexible pentacene devices, one control device are fabricated and stored in the ambient atmosphere for 12 h, which is much longer than the time required to test the mechanical reliability of device I and II, and the electrical performance of the control sample is given in Fig. 7.8. The obtained μ for the as-prepared control sample is about 1.1 cm^2/Vs, and after stored for 12 h, the μ increases to about 1.2 cm^2/Vs. The increased μ can be due to the further oxidation of Cu in the interface of S/D electrode and pentacene in the ambient atmosphere, which acting as a hole-injection layer, thus enhancing the performance of the device [42]. Form the above results, it is clear that the degradation of the device performance under strains is not caused by the absorption and diffusion of oxygen and water molecules through the cracks in the electrodes.

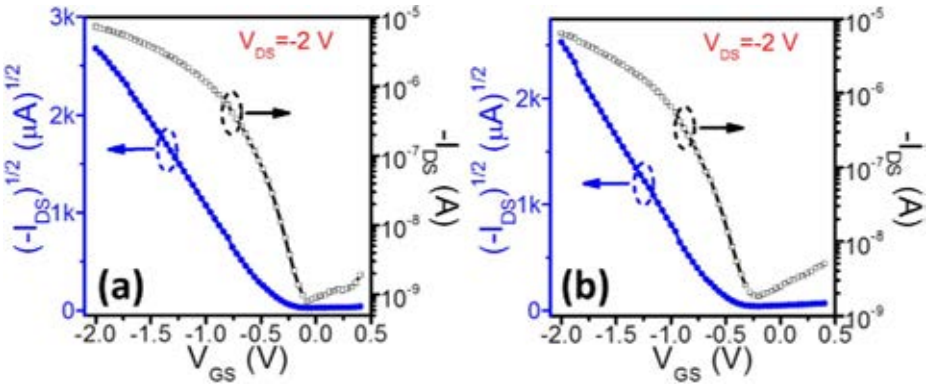

Fig. 7.8 Transfer curves of the control sample stored in ambient atmosphere for (a) 0 h and (b) 12 h.

7.3.6 Study on the electrode structure

Fig. 7.9 shows the microscopic images of the S/D electrodes during the compressive bending cycling test. From Fig. 7.9, it is clear that the cracking density increases mainly in the first 500 bending cycles, and then keeps almost unchanged up to 2000 bending cycles. The cracks in the electrodes can deteriorate the contact with the pentacene layer, and consequently, an increased contact resistance with cracking density can be expected. As a result, together with the variation of phase structure of pentacene film with compressive bending cycles, it is easy to understand the degradation of device performance. In order to quantify the contribution from the two parts, S/D electrodes are deposited after 1000 compressive bending cycles of the 30 nm pentacene film on flexible substrates, and the results show that only 30% degradation on the mobility is

obtained. Therefore, the cracks in the electrodes are responsible for the 20% degradation in mobility of the device with 1000 bending cycles under compressive strain.

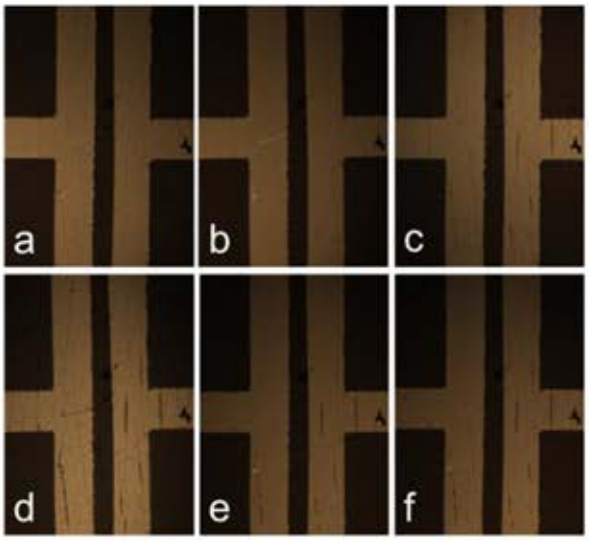

Fig. 7.9 A series of microscopic images of the S/D electrodes during the cyclic bending test under compressive stress: (a) before bending, (b) 10, (c) 100, (d) 500, (e) 1000 and (f) 2000 cycles.

Because the Young's moduli of Au (~80 GPa) and Cu (~135 GPa) are much larger than that of pentacene (~15 GPa) [7, 43], the strain of the Au/*M*-Cu film is smaller than that of the underneath pentacene layer under a tensile stress. The unmatched Young's moduli will induce a delamination of the electrodes form the pentacene layer during bending cycles, thus causing a poor contact. As a result, except for the cracks in the S/D electrodes and the pentacene film, the delamination of electrodes from

pentacene layer also contributes to the degradation of device performance. Furthermore, the cracks in the S/D electrodes will accelerate the delamination, and the delamination is thought to extend with bending cycles. Our proposed mechanism is well proven by the microscopic images taken on the S/D electrodes with tensile bending cycles, as shown in Fig. 6.10. As seen, the density of cracks increases with bending times. In addition, the gap in the crack area also increases with bending cycles, which can be due to the delamination of the electrodes from pentacene layer along the crack. Therefore, the device is expected to show lower reliability under tensile strain than compressive strain. At the same time, one can differentiate the contribution of each part by deposition of S/D electrodes after bending cycles, and the results reveal that, with 1000 bending cycles in tensile strains, the phase transition causes a 50% degradation of the mobility, and the damage in electrodes is responsible for the other 20%. Encapsulation of the flexible OTFTs with protection layers is proven to be an effective way to enhance their flexibility and reliability [29]. The relevant research is in progress, and the results will be reported elsewhere.

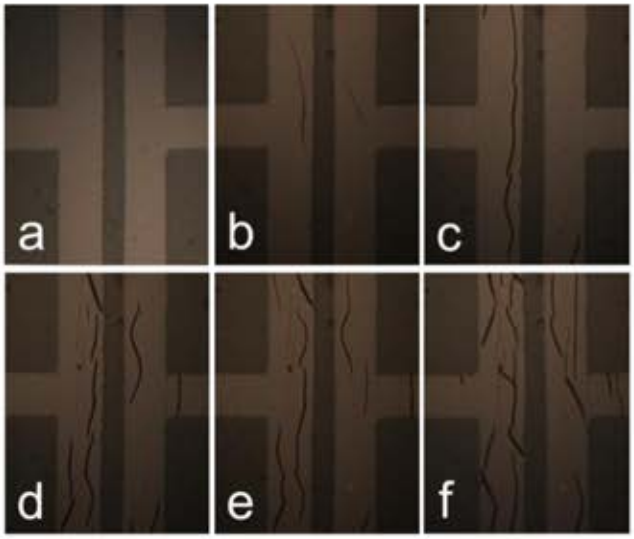

Fig. 7.10 A series of microscopic images of the S/D electrodes during the cyclic bending test under compressive stress: (a) before bending, (b) 10, (c) 100, (d) 500, (e) 1000 and (f) 2000 cycles.

7.3.7 Study on the operational stability and lifetime

The operational stability of flexible OTFTs is of great importance for their realistic applications. To evaluate such characteristics, of the, it is necessary to investigate the cyclic sweeping and bias-stress effects of our device. Fig. 7.11a shows the influence of cyclic sweeping on the electronic characteristics of flexible pentacene OTFT with Au/*M*-Cu S/D electrodes. As shown, with increasing the sweeping cycle to 100 times (due to the limit of the testing program in our equipment), the transfer curves nearly overlap with each other. The inset of Fig. 7.11a shows the change in normalized μ and V_T as a function of cycling times. As seen, the mobility shows a slightly variation of

less than 5%, and the threshold exhibits a negative shift of about -0.02 V, indicating a good cycle sweeping stability of the flexible pentacene OTFT. Fig. 7.11b shows the evolution of transfer characteristics of the flexible device stressed at V_{DS} = -1 V and V_{GS} = -2 V in ambient. The devices are measured at V_{DS} = V_{GS} = -2 V. It can be found from Fig. 7.11b that the on state currents decrease gradually upon prolonging the stress time, and degradation up to 60% of its original value is observed after 1000 s stress. The inset of Fig. 7.11b plots the changes of normalized μ as a function of bias time of the device. As shown in the inset, the mobility decreases monotonously to about 70% of its original value with prolonging bias time, and the V_T increase negatively from ~ 0.4 V to ~ 0.47 V. The degradation in device performance can be due to the fact that the bias stress will lead to increased defect states and time-dependent charge trapping in the channel of OTFTs, which has been well documented by other groups [44-47].

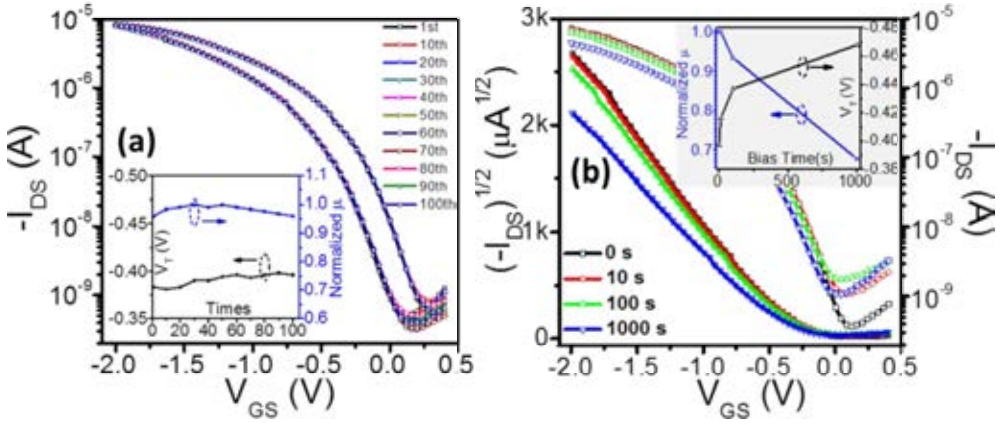

Fig. 7.11 (a) Cyclic sweeping stability and (b) bias stress stability of flexible pentacene devices; the insets give the variations of normalized mobility and threshold voltage.

The ambient lifetime of the device is also critical in the practical applications. Due to the strain induced degradation in flexible pentacene TFT performance as having been discussed in previous section, it is inappropriate to study the lifetime of flexible device. Instead, the lifetime study is conducted based on the device fabricated on n^{++}-Si substrate by the procedures as that of flexible device, and the results is given in Fig. 7.12. As seen, the mobility decreases monotonously with storing time and degrades from about 2.1 cm^2/Vs to about 0.5 cm2/Vs after 50 days. The decrease in device performance can be combination effects of O_2, H_2O [40, 41] and the oxidation of Cu in the interface region of Cu/pentacene, which resulting in an increase in electrode resistivity[48]. Interestingly, the threshold voltage shift drastically from -1.5 V to about -1.1 V in the first week, and then keeps almost unchanged with time,

indicating a good V_T stability of our device.

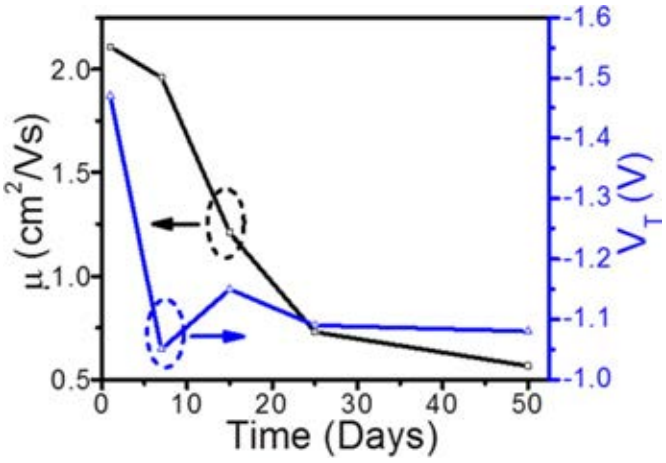

Fig. 7.12 Variation of mobility and threshold voltage as a function of storing time in ambient.

7.4 Conclusion

Low-temperature, solution-processed gate dielectric system (ODPA/ATO) has been successfully integrated onto flexible PI substrates. The high quality ODPA/ATO system shows a low leakage current density of 10^{-6} A/cm^2 and a high capacitance density of 180 nF/cm^2. Pentacene film grown on the flexible substrates possesses a highly ordered "thin film phase", which is benefit to the charge carrier transport. By using Au/*M*-Cu as S/D electrodes, the resultant flexible pentacene OTFT exhibits an outstanding electrical characteristics, with on/off ratio of 2×10^4, μ of 1.5 cm^2/Vs, V_T of -0.4 V and *SS* of 161 mV/dec, under an operation voltage of only -2 V. The

mechanical flexibility and reliability of the devices are also studied and discussed in detail. The degradation of the device performance with strains can be assigned to the damage induced in the electrodes resulting in increased contact resistance and the phase transition from thin film phase to bulk phase of the pentacene films. Our present study suggests a simple and effective way to fabricate low-voltage, high-performance flexible OTFTs at low-cost, which is of technical importance in the large scale application of the organic electronics. Future work will focus on the improvement of the device mechanical flexibility and the reliability.

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Chapter 8 Summary and Perspectives

8.1 Summary

The low-voltage operation of OTFTs is a prerequisite for OTFTs in future large scale low-end applications. Therefore, the exploration of new dielectric materials that can be used effectively as gate dielectrics and allow low-voltage operation of OTFTs is of great scientific and technological importance. This thesis focuses on fabrication and characterization of low-voltage OTFTs based on a newly developed dielectric material, and improved the device performance through interface engineering. A brief summary is given below.

In Chapter 4, a low-temperature, solution-processed high-*k* ATO system was introduced. The ATO exhibited excellent dielectric properties, including low leakage, smooth surface and high dielectric constant (*k*). It was found that the capacitance of ATO increased with decreasing the frequency, which could be explained by an electric double layer model. Upon using the ATO as gate dielectric, CuPc based OTFTs showed outstanding electrical performance under an operation voltage of only -1.5 V. The above results suggested that the low-temperature, solution-processed high-*k* ATO

could be used as an effective dielectric to realize low-voltage circuits.

In Chapter 5, we showed that, when compared with traditional low-*k* SiO_2, the CuPc OTFTs on high-*k* ATO exhibited even better electrical characteristics, which was contradictory to the previously reported results by other groups due to the commonly observed broadening of density of states (DOS) at the interface of high-*k* dielectric and organic semiconductor [1]. Characterization on the CuPc film morphologies and crystal structures revealed that both ATO and SiO_2 gave similar results. However, the initial growth of CuPc exhibited obvious difference. When deposited on ATO, the CuPc showed a Volmer-Veber growth mode with an interconnected rod-like structure. On the other hand, a Stranski-Krastanov mode with small isolated islands structure was observed when deposited on SiO_2. We proposed that the above distinctions resulted from the different surface energies of dielectrics. In addition, GIXD study revealed that, in the initial growth stage, the CuPc tended to form a crystallized structure on ATO, whereas an amorphous CuPc appears on SiO_2. Furthermore, by using the KPFM technology, we were able to observe a preferable metal/organic contact on the ATO, which benefits the charge carrier injection at the contact. At the same time, the application of ATO as an effective gate dielectric could also be extended to other organic semiconductors, including both p-type and n-type

ones. Our findings suggested that the high-*k* ATO is applicable in fabrication of high-performance, low-voltage OTFTs.

Following the detailed characterization of ATO dielectric layer and the resultant device performance, Chapter 6 dedicated to improving the OTFTs properties through interface engineering. For the dielectric/organic semiconductor interface, it was shown that, by modifying the surface of ATO using ODPA SAM, the leakage of dielectric was obviously suppressed by more than one order of magnitude without sacrificing the high gate capacitance, and a highly hydrophobic ODPA/ATO surface was obtained. At the same time, for the S/D electrode/organic semiconductor interface, we showed that by using low cost *M*-Cu as S/D electrodes as a substitute of high cost Au, a significantly enhanced device performance of pentacne OTFT was observed. The above results could be ascribed to more efficient hole injection, smaller density of interface defects, resulting in the reduced contact resistance between the *M*-Cu electrode and pentacene thin film. On the other hand, upon encapsulation of the *M*-Cu electrodes with a capping layer of Au in the aim of suppressing unfavorable surface oxidation of copper, the electrical characteristics of the pentacene OTFT were further improved, which was thought to result from the increased conductivity of the electrode itself. Our investigation suggested a facile and effective way to realize

high-performance low-voltage OTFTs, and the use of low-cost metal electrodes instead of Au could also greatly promote the realistic applications of OTFTs in the near future.

Basing on the encouraging results achieved in previous chapters, we finally took a step forward to fabricate low-voltage flexible OTFTs, as demonstrated in Chapter 7. The ODPA/ATO showed good compatibility with Au coated flexible PI substrate. It was shown that the pentacene film deposited on the flexible substrate possessed a charge carrier transport favored thin film phase, as evidenced from the GIXD results. By employing Au/M-Cu as S/D electrodes, the obtained flexible pentacene OTFT showed excellent electrical characteristics under an operation voltage of -2 V. In addition, the mechanical flexibility was studied, and the electrical performance showed decreases under both compressive and tensile strains. The degradation of the device performance was ascribed to the phase transition from thin film phase to bulk phase of the pentacene films, as revealed by XRD characterization, and the damage induced in the electrodes resulting in the increased contact resistance. Our present studies suggested a promissing way to fabricate low-voltage flexible OTFTs at low cost, which is of technical importance in the large scale application of the organic electronics.

8.2 Future work

Following up the work presented in this thesis and the exciting results reported by other research groups, there are a few feasible research directions that can be done in the near future work.

In Chapters 6 and 7, we have achieved high-performance, low-voltage pentacene OTFTs. However, for practical applications, the reliability of OTFTs should be sufficient. On the one hand, organic semiconductors usually suffer from environmental instabilities when exposed to atmospheric species and light, which will result in degradation in device performance. On the other hand, after a prolonged working period, a shift of the threshold voltage is commonly observed, which can be attributed to the trapping of charge carriers in localized states in the gate dielectric, in the organic semiconductor, or at the dielectric/semiconductor interface [2]. Therefore, systematic studies should be conducted to probe the reliability of our fabricated devices, including bias stability and ambient lifetime, and then find ways to improve the reliability.

At the same time, we have shown that the *M*-Cu can effectively enhance the device

performance, which can be ascribed to the existence of a thin layer Cu_2O at the interface of Cu and pentacene. Hence, there should be a critical thickness of the Cu_2O layer that can make the device work efficiently. Such issue should also be clarified in the future work.

In Chapter 7, we showed that the electrical performance of our flexible pentacene OTFTs suffered from degradation under stress, which is due to the phase transition occurred in pentacene film and damage in S/D electrodes. Encapsulation of the flexible OTFTs with protection layers is proven to be an effective way to enhance their flexibility and reliability [3]. Accordingly, future work should focus on improving the flexible device mechanical stability through encapsulation.

In this thesis, the work is mainly focused on p-channel OTFTs. In order to realize complementary logic circuits, both p- and n-channel OTFTs are required. In particular, ambipolar OTFTs can simplify the design of such logic circuits [4]. Therefore, it is important to fabricate high-performance, low-voltage n-channel OTFTs as a first step. Secondly, high performance ambipolar OTFTs are expected to be demonstrated by combining the obtained n- and p-channel devices, as well as through optimizing the fabrication procedure and the device structure.

On the other hand, most reported n-type organic semiconductors are usually found to exhibit either low mobility and/or poor ambient stability. Fortunately, solution-processed metal oxide semiconductors, such as Al-doped zinc tin oxide (AZTO) [5], gallium tin zinc oxide (GSZO) [6] and indium oxide [7] exhibit mostly n-type semiconducting behavior with the advantages of high electron mobility and excellent environmental stability. Therefore, by integrating p-type organic semiconductor with n-type metal oxide semiconductors, fabrication of high-performance ambipolar transistors will show a bright future.

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Publications

Journal papers:

(1) **Yaorong Su**; Chengliang Wang; Weiguang Xie; Fangyan Xie; Jian Chen; Ni Zhao; Jianbin Xu, *Low-Voltage Organic Field-Effect Transistors (OFETs) with Solution-Processed Metal-Oxide as Gate Dielectric*, Acs Applied Materials & Interfaces 2011, 3, 4662-4667.

(2) **Yaorong Su**, Mingdong Wang, Fangyan Xie, Jian Chen, Weiguang Xie, Ni Zhao, Jianbin Xu, *In-situ Modification of Low-cost Cu Electrodes for High-performance Low-voltage Pentacene Thin Film Transistors (TFTs)*, accepted by Organic Electronics.

(3) **Yaorong Su**, Weiguang Xie, Yun Li, Yi Shi, Ni Zhao, Jianbin Xu, *Low-temperature, Solution-processed High-k Dielectric for Low-voltage, High-Performance Organic Field-Effect Transistors (OFETs)*, accepted by Journal of Physics D: Applied Physics.

(4) **Yaorong Su**, Jiaolong Jiang, Ning Ke, Ni Zhao, Jianbin Xu, *Low-voltage Flexible Pentacene Thin Film Transistors (TFTs) with Solution-processed*

Dielectric and Modified Copper Source-drain Electrodes, submitted to Journal of Materials Chemistry C, *under review*.

Conference presentations:

(1) MRS Spring Meeting, 2011, **Poster**, *Low voltage CuPc organic thin film transistor with double layer high-k metal oxide gate dielectrics*.

(2) E-MRS 2011 Spring & Bilateral Meeting, **Poster**, *Low-voltage n-Type $F_{16}CuPc$ Organic Thin Film Transistors (OTFTs) with High Electron Mobility.*

(3) International Symposium on Electrical/Optic Functional Molecules (ISEOFM2012), **Poster**, *Solution-processed High-k Dielectrics as a new choice for High Performance, Low-voltage Organic Field-Effect Transistors (OFETs).*

(4) The Third China Printed Electricals Symposium, 2012, **Poster**, *High-Performance, Low-Voltage Flexible Pentacene Thin Film Transistors (TFTs) with Solution-Processed Dielectric and Low-cost Source-Drain (S/D) Electrodes*.

(5) AOE symposium, The University of Hong Kong, 2012, **Oral**, *Solution-processed Dielectrics for Low-voltage Organic Thin Film Transistors (OTFTs) and Interface Engineering*.

(6) MRS Fall Meeting, 2012, **Oral**, *In-situ Modified Low-cost Copper Source-drain (S/D) Electrodes for Low-voltage, High Performance Pentacene Thin Film Transistors (TFTs).*

(7) MRS Spring Meeting, 2013, **Poster**, *Low-voltage Flexible Pentacene Thin Film Transistors (TFTs) with Solution-processed Dielectric and in-situ Modified Cu as Source-drain (S/D) Dlectrodes.*