Jitter Reduction Techniques

for Digital Audio

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TABLE OF CONTENTS

ABSTRACT

The existing techniques such as: analogue phase-locked loop (APLL) circuit and first in first out (FIFO) technique for jitter reduction are not satisfactory when the low frequency jitter (wander) exists. This thesis presents several techniques for achieving better performance of jitter reduction that can be used in digital audio. The following techniques are presented:

It is shown that using the all digital phase-locked loop (ADPLL) circuit can reduce the jitter and / or wander significantly. It is because the ADPLL can set the cut-off frequency or locked range extremely low (i.e.: lock range $\leq$ 1.314mHz for 44.1kHz in practice) . This locked range is difficult to achieve in the analogue phase-locked (APLL) loop circuit due to very long initial lock-on time.

We have made circuit comparisons between the ADPLL and APLL. The frequency against voltage stability and frequency against temperature stability of APLL circuit are not better than that of the ADPLL circuit.

We study the design of extremely stable power supply circuit to get better voltage regulation with a low noise, low dc offset Op-amp as a voltage comparator and use current feedback Op-amp as a current buffer to provide dynamic current to the load. We also study the design of extremely stable discrete transistor oscillator circuit to minimize the master clock jitter level successfully, and the design of temperature compensated circuit for crystal oscillator in order to minimize the master clock temperature drift.

In addition, the jitter occurring in digital audio chain is presented and discussed. Jitter reduction techniques can be applied to the circuit level (especially discussed in this thesis), board level, and system level.

Finally, we suggested that further analysis of jitter should be obtained by using high quality measurement instrument, i.e.: Audio precision system two, real-time modular oscilloscope mainframe (HP 54720D 8GSa/s) plus the time-interval measurement software (M1TM) or digitizing oscilloscopes (HP 54750A) with the clock jitter analyzer software HP E1725B Option 243 TIA.

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LIST OF SYMBOLS AND GLOSSARY

1. **AES/EBU INTERFACE:** A digital interface standard for professional audio equipment interconnection.
2. **DYNAMIC RANGE:** The difference, usually expressed in dB, between the highest and lowest amplitude portions of a signal, or between the highest amplitude signal which a device can linearly handle and the noise level of the devices.
3. **ECPD:** Edge-controlled phase detector.
4. **JITTER:** The undesirable cycle-to-cycle variation in the period of a reference clock, such as are used in digital audio converters. Jitter can cause modulation sidebands and noise if converters operate from a jittered clock. Excessive jitter in an interface can cause digitally-interfaced equipment to malfunction.
5. **SPDIF:** Sony Philips Digital Interface; a digital interface for consumer audio equipment. Sometimes also referred to as the EIAJ interface. The SPDIF is similar to the professional AES/EBU interface, but is normally an unbalanced coaxial signal of lower amplitude. Most of the status byte definitions are different between SPDIF and AES/EBU.
6. **STEREOPHILE:** USA. audio magazines.
7. **THD+N:** Total harmonic distortion plus noise. Measured by attenuation the fundamental signal with a narrow-band notch filter, then measuring the remaining signal which consists of harmonics of various order wide-band noise, and possibly interfering signals . This is the common harmonic distortion method implemented in most analyzers.
8. **EXORPD:** exclusive-or phase detector.

Chapter 1

1 INTRODUCTION

The growth of digital audio, such as CD has been rapidly increased since its introductions to the consumer market more than ten years. It was discovered that the effect of *timing jitter* or *sampling jitter* was the major factor for degradation of the digital audio sound quality. Stereophile (USA. audio magazines) has reported an interesting correlation between source material and measured jitter. For example, using the CBS test disk as the source, with sine-wave signals of 1KHz (0dB) , 1KHz (-90dB) , and digital silence and using the Meitner jitter analyzer, Stereophile found a direct correlation between some of the signals and the observed jitter. In particular, they found that very low-amplitude signals (-90dB) exhibit jitter-spectrum frequencies that match the test signals and their harmonics. The mathematical derivation of the effects of jittered sampling and the clock jitter on DAC are reported in [70,71,72] .

There is a variety of system timing failure mechanisms attributable to *sampling jitter* or *clock jitter*. Some are caused by an excessively short clock period, some others by large instantaneous changes in the period, and others by an accumulation of jitter in a phase-locked loop (PLL) circuit or oscillator over multiple cycles. Still others attributed more to the spectrum of the modulation than to the actual magnitude of the modulation. PLLs are a prime example of a device sensitive to the latter class of failures.

In the present thesis, we will address three aspects of jitter: what is the jitter, why does jitter occur in digital audio and jitter reduction techniques.

In Chapter 1, we describe what is the jitter.

In Chapter 2, we describe the cause and effect of jitter in digital audio.

In Chapter 3, we investigate and propose various methods for jitter reduction. by the hardware circuit design. Also we propose to use all digital phase locked loop (ADPLL) circuit, which incorporates with the digital audio interface chip to reduce the jitter. Some computer simulated results and experimental results are also given.

In Chapter 4, we describe the application circuit block diagram of jitter reduction.

Finally, in Chapter 5, we summarize the contributions of the thesis and discuss the directions for future development.

1.1 What is the jitter ?

Jitter is simply defined as the time variations in the sample period [65]. In practice, the long-term phase variations ***below 10 Hz*** are called ***Wander----*** *low frequency jitter* , and those ***above 10 Hz*** are called ***Jitter*** [1] , [2].

Jitter amplitude is defined as the variation in time from the ideal sample period Δ.

Jitter frequency is defined as the rate of change from ideal sample time.

Jitter is the time-base error or timing uncertainty of the data or clock signals. It is caused by the variation of time delays in the circuit paths from component to component in the signal path. The industrial standards of sampling frequencies are 32kHz for MD player, 44.1kHz for CD player and 48kHz for DAT (digital audio tape). An error of a few nano-second in the sampling time can cause major degrade in the system **dynamic range** and the **signal to noise (S/N)** [8] of the digital to analog converter (DAC) analog output. The plot of distortion against jitter is in Section 7.1.3 figure 12.

Jitter has the following characteristics:

- The variations in the time base of a system is regular and periodic (possibly sinusoidal). In an analog signal system it is called **Wow & flutter** . The variation can cause spurious tones at low signal levels which block our perception of critical ambient decay and thus truncate the dynamic range of the reproduction.
- The variations are random / Gaussian distributed (incoherent, white noise) and its presence tends to mask the low level musical material.
- The effect of Jitter can be a combination of the above three degradations.

For the clock jitter it can be modeled as a frequency modulation (FM) process. It is caused by noise or changes in temperature of the active components (ie: CMOS chips). This modulation causes the timing to vary slightly at the positive and negative going edges of the signal.[7] , [19]. One notable result is that the level of the noise or the sidebands is proportional to the slope of the input signal, i.e.: the worst case occurs at the highest frequency full-scale input (a full-scale 20kHz sinusoid).

Chaper 2

2 WHY DOES JITTER OCCUR IN DIGITAL AUDIO ?

2.1 Poorly-designed Phase Locked Loop (PLL)

Poorly-designed Phase Locked Loop (PLL) circuit especially the phase detector circuit has **Dead Zone** region (undetectable phase difference range) and the **counting dividers** that can increase jitter level [59].

The minimum peak-to-peak phase error caused by this dead zone is equal to

$$2\pi \bullet T_{deadzone} \bullet \frac{1}{\sqrt{T_{period}}} \qquad (2.1)$$

The dead-zone [73] occurs when the loop is in a locked mode and the output of the charge pump does not change for small changes in the input signals at the phase detector .

A 0° phase difference between the phase lock loop's phase detector two input terminals (one input is the reference input and the other input is the voltage control oscillator output or the counting dividers output) or cause a **race condition** in the integrated circuit. This race condition which can cause an **undetermined state** in the phase-detector logic is called **Dead Zone**. In this condition, the phase detector output is sensitive to **circuit-loading effects** that can cause non-linearity in the phase-versus-output-voltage transfer function.

This non-linearity produces

1. higher reference sidebands;
2. loop instability;
3. longer loop settling time;
4. higher phase noise or phase jitter ;
5. erratic operation when the VCO is locked in phase with the input signal. The race condition depends on the rise, fall and propagation time of the integration circuits .

The width of the dead zone (non-linear distortion zone) depends on the rise, fall and propagation times . These intervals decrease with the higher-speed digital-logic families (i.e. **54/74ACT series**) , and a high speed phase detector **(AD9901)** has a smaller dead zone than a lower speed counter part **(HC4046)** .

With proper interfacing together with a PLL circuit using a no dead zone high speed phase detector **(AD9901)** with a moderate cut-off frequency (of about 1kHz cut-off frequency) can reduce jitter [48]. For further jitter reduction, the All digital phase lock loop (ADPLL) circuit must be used . ADPLL will be discussed in detail in section 3.3.

However, time jitter in phase-locked loop circuit's pulse-synchronized and counting dividers can increase jitter level [59] in-side the PLL cut-off frequency.

The triggering effect encountered in these types of frequency dividing circuit is released when the input waveform u(t) reaches a predetermined level. The superimposed spurious signals and changes of the triggering level itself, due to the ambient temperature shift the time of the triggering.

In the first approximation, the first two terms of the Taylor expansion may be sufficient for its evaluation.

$$\mathbf{u(\,t_k\,) = u(\,kT\,) + u'(\,kT\,)\,(\,t_k - kT\,)} \qquad \mathbf{(\,2.2\,)}$$

where **kT** is the ideal time of the **k**-th triggering and $\mathbf{t_k}$ is the actual time.

The amount of the time jitter ($\Delta\mathbf{T_k}$) is

$$\begin{aligned}\Delta T_k &= (\,t_k - kT\,) \\ &= \left[u(t_k) - u(kT)\right]\frac{1}{\left[u'(kT)\right]} \\ &= -\left[ui(tk)\right]\frac{1}{\left[u'(kT)\right]}\end{aligned} \qquad \mathbf{(\,2.3\,)}$$

where $\mathbf{u_i(\,t\,)}$ is the interfering signal.

From the above equation, the smallest spurious time jitter ΔT_k requires placing of the triggering level at the steepest part of the input waveform.

A frequency dividing chain begins with a shaping circuit which is driven by a **sinewave**

$$u(t) = V_s \sin\omega t ;$$

$$u'(t)_{max} = \omega V_s ;$$

$$\Delta Tk = -ui(t_k)\frac{1}{\omega \bullet V_s} \qquad (2.4)$$

The individual dividing circuits are driven by pulses or nearly rectangular waves with steep leading or trailing edges. The actual triggering slope may be expressed approximately by

$$u'(t) = V_s \frac{1}{t_{lead}}; \qquad (2.5)$$

where $t_{lead} << T$

$$\Delta Tk = -ui \bullet tk \bullet t_{lead} \bullet \frac{1}{V_s}; \qquad (2.6)$$

That means the time jitter introduced in a pulse-synchronized or counting divider may be kept at a very low level, even in long chains of dividing circuits [66].

2.1.1 Digital data problem

The digital audio data is SPDIF format that have the similar property of non-return-to-zero (NRZ) data format. In the NRZ format, each bit has a duration of T_b (bit period), is equally likely to be ZERO or ONE, and is statistically independent of other bits. The quantity $r_b = \frac{1}{T_b}$ is called the **bit rate** and measured in bits/s. The various SPDIF signals pulse width are shown in below table:

item	sampling frequency (kHz)	one period (1T) pulse width(ns)	two periods (2T) pulse width(ns)	Maximum frequency f=1/T (MHz)	three periods (3T) pulse width or preamble pulse width(ns)
1.	32	244	488	4.098	732
2.	44.1	177	354	5.650	531
3.	48	163	326	6.135	488

NRZ data has two attributes that make the task of clock recovery difficult. First, due to the lack of a spectral component at the bit rate in the NRZ format, a clock recovery circuit may lock to spurious signals or simply not locked at all. The spectrum of NRZ data has nulls at frequencies that are integer multiples of the bit rate, for example, if the data rate is 11.2896Mb/s, the spectrum has no energy at 11.2896MHz. The fastest waveform for a 11.2896Mb/s stream of data is obtained by alternating between ONE and ZERO every 88.577ns. The result is a 5.6448MHz square wave, with the absence of all the even-order harmonics. From another point of view, if an NRZ sequence with rate r_b is multiplied by A sin (2 π m r_b t), the results has a zero average for all integers m, indicating that the waveform contains no frequency components at m (r_b).

It is also helpful to know the shape of the NRZ data spectrum. Since the auto-correlation function of a random binary sequence is [74].

$$R_x(\tau) = 1 - \frac{|\tau|}{T_b} \qquad |\tau| < T_b \qquad (2.7)$$

$$= 0 \qquad |\tau| < T_b \qquad (2.8)$$

the power spectral density equals

$$P_x(\omega) = T_b \left[\frac{\sin(\omega T_b / 2)}{\omega T_b / 2} \right]^2 \qquad (2.9)$$

It is showed that this function vanished at $\omega = 2m\pi \frac{1}{Tb}$ .In contrast, return-to-zero (RZ) data has finite power at such frequencies.

Second, the data may exhibit long sequences of consecutive ONEs or ZEROs, demanding the clock recovery circuit (CRC) to " remember " the bit rate during such a period. This means that, in the absence of data transitions, the CRC should not only continue to produce the clock, but also incur negligible drift in the clock frequency.

2.2 Sampling jitter or clock jitter (Δt_i)

In sampled-data systems, a time jitter in the sampling clock (Sampling jitter or clock jitter) leads to non-uniform sampling, which adds noise to the sampled signal.

$$e(t_i) = A\{\sin[\omega(t_i + \Delta t_i)] - \sin(\omega t_i)\}$$
$$\approx A\omega\Delta t_i \cos(\omega t_i) \qquad (2.10)$$

where

$e(t_i)$ is the error that is made for the ith sample of a sinusoidal input

Δt_i is the timing error or jitter

A clock jitter in Nyquist-rate analogue to digital converters (ADCs) thus leads to a loss in the signal to noise ratio (SNR) and hence in the converter resolution [4]. Sampling jitter or clock jitter at the analog-to-digital (ADC) or digital- to-analog (DAC) conversion process causes distortion in signal reproduction. It is induced on the system clock electronically and mechanically.

The system clock of DAC is used to control the timing of the DAC (either internal or external). The DAC output current pulse edge is depend only on jitter in the latch clock (digital filter output pin----word clock (WCKO)). Typical clock jitter measured on various players ranged from **200 to 700ps** [4 , 6].

The mathematical derivation of the effects of jittered sampling instants for a sinusoidal input signal is presented in [71].

$$S_{\varepsilon base} = \frac{A^2}{4}(2\pi f_{in})^2 S_\zeta(f - f_{in} + \frac{k}{T}) \qquad (2.11)$$

where

k is a,

$S_{\varepsilon base}$ is the lowest frequency image of the sampled data in the continuous time spectral,

$(2\pi f_{in})^2 S_\zeta(f)$ is the power spectral density of sampling a sinusoid with a jittered clock

The clock jitter of general PCM are reported in [72].

$$\frac{S}{N} = 10\log\left(\frac{1}{4\pi^2 \bullet f^2 \bullet \sigma^2{}_j}\right) \qquad (2.12)$$

The clock jitter of ΣΔ DAC are reported in [72].

$$\frac{S}{N} = 10\log\left(\frac{1}{16m \bullet f_b{}^2 \bullet \sigma^2{}_j}\right) \qquad (2.13)$$

where

1. S/N is the maximum signal-to- noise ratio due to the clock jitter,
2. m is the oversampling ratio,
3. f_s is the Nyquist sample rate,
4. f_b is the useful bandwidth available from the Nyquist sample rate with the relation of $f_s=2\ f_b$,
5. σ^2_j is the variance of the timing errors Δt_i (jitter).

From the above equation, it shows that the noise caused by jitter is frequency dependent in this case, and that the signal-to -noise ratio is $\frac{4m}{\pi^2}$ and a low sampling ratio is favorable for low clock jitter sensitivity. As an example, clock jitter with a standard deviation of 1ns reduces the dynamic range of a modulatior with m=64 and fb =3.4kHz to 79dB (but for the general PCM system, equation would yield 93dB). If a crystal oscillator is used, the jitter is usually sufficiently low.

The jitter noise spectrum of multi bits DAC are reported in [73].

$$E_{multi}(f) = f_s \sum_{n=1}^{N=1} [A_n - A_{n-1}] t_{jn} \exp\left(\frac{-i2\pi nf}{f_s}\right) \qquad (2.14)$$

The jitter noise spectrum of pulse-width modulation (PWM) DAC are reported in [73].

$$E_{PWM}(f) = f_s \sum_{n=1}^{N=1} A t_{jn} \exp\left(\frac{-i2\pi nf}{f_s}\right) \qquad (2.15)$$

where

A is the full-scale output level,

t_{jn} is the jitter of one bit PWM time-domain DAC,

f_s is the sampling frequency.

2.3 Waveform distortion

Waveform distortion (for example : square wave becomes round edges , **ringing** or triangle, fast rise times becomes slow) is due to **impedance mismatch** and / or reflections in the signal path. This distortion can cause mis-interpretation of the actual **zero crossing point** of the waveform. Severe ringing will affect the data transfer if it exceeds the device's input noise margin. Severe waveform distortion can cause an audible errors for example clicks or tics in the sound. The amplitude of the ringing depends on the degree of mismatch at either end of the transmission line or cable while the ringing frequency depends on the electrical length of the line.

Especially, this deviation can be found at the master clock (**MCK**) waveform from the digital interface chip output signal to the digital filter and the digital filter word clock waveform (**BCKO**) output signal to the digital to analogue converter (DAC) chip .

Waveform distortion can be improved by matching the printed circuit board wire impedances and using the high speed switching diode (**1N4148**) or schottky diode (**BAT85**) or more high speed switching schottly diode in parallel with a lowpass filter resistor element for making faster settling time [25 , 38 , 43] and lowering the square wave overshoot level.

Different types of switching diodes are linked below for ease of comparison:

	1N4148	BAT85
	silicon switching diode	schottky switching diode
Switching time (ns)	50	20
Forward voltage (V)	0.6	0.2
Reverse voltage (V)	50	30

Different types of TTL /CMOS logic line drivers or inverters are linked below for ease of comparison:

	74HCU04	74HC04	74HCT04	74HC244	74HCT244
function	Hex inverters	Hex inverters	Hex inverters	Octal buffer and line driver	Octal buffer and line driver
output current rating (mA)	+/-20	+/-25	+/-25	+/-35	+/-35
output impedance (ohms)	250	200	200	143	143

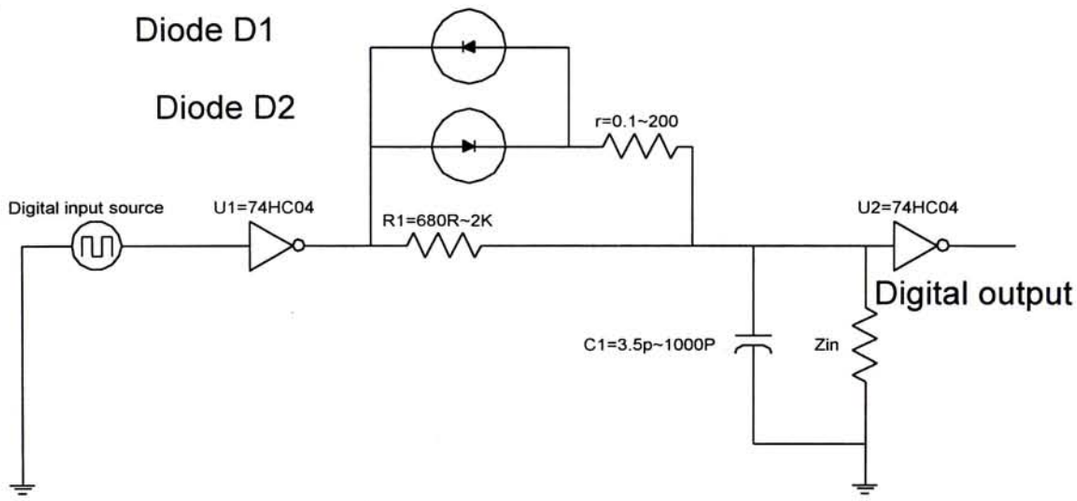


Fig. 2.1: show that using back-to-back high-speed switching diode is to reduce the settling time between two chips.

D1 and D2 are used to decrease the settling time between U1 and U2. The use of schottky type switching diode will have better transient response. Zin is the input impedance of the U2 and C1 (range from 3.5pF to 1000pF) is its input capacitance. R1 is used to adjust the time constant and waveform sharpening.

The capacitor C1 is charged faster through the low forward biased diode impedance during the initial portion of a large input step change. When the difference between the input and output voltage becomes less than the forward biased diode

drop, the diode turns off and C1 reacts with R1 alone. That means the circuit behaves like a normal single pole RC filter.

Assuming the diode resistance is negligible, the improvement in settling time depends on the ratio of the input step voltage to the forward biased diode voltage.

Improvement in settling time only occurs when the voltage step is much larger than the diode drop. Small step charge approaches the forward biased diode voltage, this simple method offers no improvement. By reducing the threshold to below one diode drop, the settling time can be improved for smaller inputs.

The calculation below will show the setting time improvement through the value of r (range from 0.1Ω to 200Ω).

$$fc = 2\pi RC \qquad (2.16)$$

$$\theta = -\tan^{-1}\left(\frac{f}{fc}\right) = -45° \qquad (2.17)$$

$$Vo = Vi\left(1 - e^{-\left(\frac{t}{RC}\right)}\right) \qquad (2.18)$$

$$\frac{Vo}{Vi} = 1 - e^{-\left(\frac{t}{RC}\right)} \qquad (2.19)$$

$$t = -RC \bullet In\left(1 - \frac{Vo}{Vi}\right) \qquad (2.20)$$

For example: R1=100 and C=100pf , using 74HCU04 as a output line driver.
time constant T1 =R1C =100 x100x 10^{-12}=10ns.

The calculation below will show the setting time improvement through the value of r (range from 0.1Ω to 200Ω) but without including the output impedance of the logic chip.

- set r1=10 and R1=100Ω

  T2= (R1// r1) C=(100 // 10) 100 x 10^{-12} = 9.09 x 100 x 10^{-12} =909ps

  Time constant is shorter 11 time.

- set r1=1 and R1=100Ω

  T3= (R1// r1) C=(100 // 1) 100^{-12} = 0.99 x 100 x 10^{-12} =99ps

  Time constant is shorter 101 time.

- set r1=0.1 and R1=100Ω

  T4= (R1// r1) C=(100 // 0.1) 100^{-12} = 0.0999 x 100 x 10^{-12} =9.99ps

  Time constant is shorter 1001 time.

From the above calculation , we know that the settling time is improved from **10ns into 9.09ps** in theory.

For example: R1=100 and C=100pf , using 74HCU04 as a output line driver, and its output impedance is 5/20m=250 ohms,

time constant T1 =(R1+ ro) C =(100+ 250) x 100 x 10^{-12}=35ns.

The calculation below will show the setting time improvement through the value of r (range from 0.1Ω to 200Ω) but with including the output impedance of the logic chip.

- set r1=10 and R1=100Ω

  T2= [(R1// r1) + 250] C=(100 // 10)100x 10^{-12} = 259 x 100^{-12} =25.9ns

  Time constant is shorter 1.35 time.

- set r1=1 and R1=100Ω

  T3= [(R1// r1) + 250] C =(100 // 1) 100-12 = 250.99 x 100^{-12} =25ns

  Time constant is shorter 1.39 time.

- set r1=0.1 and R1=100Ω

  T4= [(R1// r1) + 250] C=(100 // 0.1) 100-12 = 250.0999 x 100^{-12} =25.00999ps

  Time constant is shorter 1.4 time.

From the above calculation , we know that the settling time is improved from **35ns into 25ns** in practice.

This method can also apply to the analog PLL' low pass filter section. The large signals , which occur when the PLL loop is out of lock, pass through the back-to-back diodes and see a relatively small time constant while smaller signals, which occur in the locked stage , see the full filter time constant. The filter-corner frequency is higher for larger input changes. It is noted that the non-linear diode characteristic must be properly matched to the shunting resistance to produce a transition at the desired current level. Also, there is the potential problem of large spikes from the phase detector causing the diodes to conduct in normal operation and thus defeating the filtering action.

2.4 Logic induced jitter

Logic induced jitter [2,16] is the delay variations in logic gates. The effects of power supply voltage variation on modulating CMOS gate delay may be elaborated under two extreme cases:

a/ Global voltage variation----slow effect

The variation of CMOS logic amplitude with the power supply voltage is the crucial point of logic induced jitter. This effect can pull-down the delay time of the inverter.

b/Local voltage variation----fast effect

If the V_{dd} voltage changes, the logic gate's output node is then not influenced by its going low. If it goes high, the output node and the V_{dd} power-bus are connected by the P-FET channel resistance then the V_{dd} voltage variation will be **coupled** more or less directly to the gate output node.

From the paper or literature reveal that the HC4046 PLL IC can achieve **1ns** of absolute jitter and using re-clocking circuit [3] can further reduce the absolute jitter from **10ns to 500ps** [2].

The delay of a digital logic gate is sensitive to the power supply variations as the voltage changes., the propagation delay (t_{pd}) through a logic gate will vary as the voltage changes. CMOS logic, which has a power supply sensitivity of 5.6-128ns/V or 5.6-128ps/mV per logic gate , is commonly used in practice.

Most high end CD transports use CMOS logic gate to re-clock the signal. **Re-clocking** can be used to reduce the delay variation (jitter) to the logic gate but it depends on the master clock quality and the type of logic gate . Different type of logic families against power supply sensitivity are linked below for ease of comparison:

	logic	**Propagation delay time t_{pd} (ns)**	**Power supply sensitivity (ns/V)**
1.	74HC00	20-115	23.75 (MAX.)
2.	74HCT00	22-25	3 (MIN.)
3.	74F00	1.5-5.3	3.8
4.	74AC00	1.5-8.5	7
5.	74ACT00	1.5-9.5	8
6.	74AC11000	1.5-7.4	5.9
7.	74ACT11000	1.5-12.3	10.8
8.			
9.	74HC04	20-120	25 (MAX.)
10.	74HCT04	23-25	2 (MIN.)
11.	74AC04	1-7.5	6.5
12.	74ACT04	1-9	8
13.	74F04	3.5-10.5	7
14.	74HCU04	17-100	20.75
15.	74AC11004	1.5-7.1	5.6
16.	74ACT11004	1.5-9.7	8.2
17.			
18.	74HC74	37-220	45.75 (MAX.)
19.	74HCT74	31-35	4 (MIN.)
20.	74AC74	2.5-10.5	8
21.	74ACT74	4-13	9
22.	74F74	3.5-10.5	7
23.	74AC11074	1.5-9	7.5
24.	74ACT11074	1.5-12.5	11
25.			
26.	74HC86	21-125	26 (MAX.)
27.	74HCT86	48	*
28.	74AC86	1-9.5	8.5
29.	74ACT86	1-10.5	9.5
30.	74F86	3-7.5	4 (MIN.)
31.	74AC11086	1.5-7.6	6.1
32.	74ACT11086	1.5-9.6	8.1
33.			
34.	74HC112	35-205	42.5
35.	74HCT112	*	*
36.	74F112	*	*
37.	74AC112	*	*
38.	74ACT112	*	*

39.			
40.	74HC123A	34-135	25.25
41.	74HC163	43-255	53
42.	74HC221	34-135	25.25
43.			
44.	74HC244	25-145	30 (MAX.)
45.	74HCT244	32-35	3 (MIN.)
46.	74AC11244	1.5-7.3	5.8
47.	74ACT11244	1.5-9.9	8.4
48.			
49.	74LS297	20-30	*
50.	74HC297	37-220	45.75
51.	74HCT297	44	*
52.	74AC297	*	*
53.	74ACT297	*	*
54.			
55.	74HC393	26-150	31
56.	74HCT393	38	*
57.			
58.	74HC423A	34-135	25.25
59.	74HC590A	30-175	36.25
60.			
61.	74HC4017	49-290	60.25
62.	74HC4020	32-190	39.5
63.	74HC4024	26-150	31
64.	74HC4040	32-190	39.5
65.	74HCT4040	60	*
66.	74HC4060	105-615	127.5
67.	74HC4538	59-347	72

2.4.1 Digital noise mechanisms

Digital integrated circuit induces noise on the supply rails or on the substrate. Noise induced on the ground plane or signal path will cause delay variations.

Depending on the mechanisms, digital noise can be classified into three types,

a/Induced noise: noise voltage induction from one circuit node of a chip to the other circuit node on the same chip.

***b/Power-bus noise*:** *Discharge current spike* of on-chip or off-chip circuit creates power bus *voltage fluctuation* affects all, or a significant part of the circuits on the chip.

c/*Communication noise*: Noise voltage is also induced on the transmission lines and wires that connect the chips together. The behavior of communication noise and induced noise are different in respect of the node's impedance level, logic amplitude, mechanisms of noise induction, and the effects of noise.

2.4.2

Different types of D-type flop-flip chips are linked below for ease of comparison:

	type of logic families		Propagation delay t_p (ns)	max. clock frequency (MHz)	Re-mark
1.	74HC74	CMOS	30-220	6-35	
2.	74AC74		9.4-10.5	95-100	
3.	74AC11074		1.5-11.3	100-125	center pin power supply logic
4.	74HCT74	TTL	15-70	6-36	
5.	74ACT74		9.4-10.5	95-100	
6.	74ACT11074		1.5-9.4	100-125	center pin power supply logic
7.	74F74		3.8-9.2	100	
8.	74ABT273		2.5-7	150-200	only have buffer , flip-flop and transceiver function
9.	MC10H131	ECL	0.8-1.8	250	

It is noted that **74AC11074** and **74AC11074** dual D-type flip-flop are center-powered and center-grounded . This configuration can reduce internal inductance and the possibility of the supplies being modulated by the output signal. This device has a high output drive capability .

2.4.3 Ground bounce [25]

$$V_{(gnd\ bounce)} = L_{gnd} \bullet \frac{d}{dt} I_{discharge} \qquad (2.21)$$

Slight variations in the ground potential for the IC chips has a great effect on the transition detection. For example, the DIP flip-flop packages with very fast output drivers connected to heavy capacitive loads will induce double-clocking error.

	type of logic families	Ground bounce level (p-p) with 20pF load	Jitter level (p-p)
1.	74HCT74	470mV	~332ps
2.	74F174	400mV	~283ps

It is noted that 5mVrms or $14mV_{p-p}$ ground noise may cause ~10ps jitter to a standard TTL gate. But emitter couple logic (ECL) has much higher resistance to Vcc noise or ground bounce in the power planes and common mode noise on the signal itself. Less injected noise means more constant transition time, and less jitter.

2.5 Power supply high frequency noise

Some circuits, especially the oscillator circuit, are very sensitive to power supply noise within certain frequency range. This effect usually results from insufficient power supply filtering inside the oscillator. **Resonance** in power supply filter causes poor power supply rejection (PSRR) at this frequency.

If the oscillator has poor power supply immunity, or if it must work in a noisy system, a provision of additional power supply filtering with damping resistor can solve this problem [25].

A filter with 20dB attenuation frequency is

$$F_{20dB} = 3.2 \bullet \frac{1}{\sqrt{LC}} \qquad (2.22)$$

Power supply is often a dominant source of jitter [60,61,62]. Therefore it is better to

1. decouple and bypass all IC power supply pins (**Decoupling** is " the art and practice of breaking coupling between portions of systems and circuits to ensure proper operation.". **Bypassing** is " the practice of adding a low-impedance path to shunt transient energy to ground at the source. Decoupling the receiver section (RX) and the transmitter section (TX) of a chip is useful. The TX section is typically noisy because it has to switch heavy loads. The RX section is typically highly sensitive because it has to detect small voltage changes) ;
2. separate analog and digital power supply by using π **type low-pass power filter** consisting of a capacitor and an inductor (Typically, ferrite inductors are used for power filtering. The **ferrites** acts as shorts at DC, allowing power to drive the remain circuit. The ferrites'impedance increases with frequency, filtering out high-frequency noise from the digital power and ground planes. Board designers should choose capacitance and inductance value for high impedance at frequency of 50MHz or higher. Typically, a 10uF capacitor is used where digital and analog power planes are connected. A 0.22uF capacitor is used at the power and ground pins);

3. separate functionality and speed;
4. separate power and ground planes;
5. separate power and ground traces;
6. minimize loop area and return current paths;
7. isolate noisy return current paths from more sensitive analog circuits
8. minimize interference from clocks.

The above precautions will maximize the power supply performance.

2.6 Interface Jitter

Interface Jitter at the SPDIF (Sony-Philips Digital Interface), AES/EBU interface, bandwidth limit of an interconnection wire (due to capacitance increases with wire length) between the CD transport and digital to analogue converter and bandwidth limitation of the input coupling transformer cause transmission error [5 , 7 , 51 , 52 , 53, 58]. The coupling transformer is used for *power line isolation.* A typical coupling transformer can have a high pass of about 50kHz which will induce 1ns of jitter.

The use of wide bandwidth transformer [48] or high speed **(62.5 / 125μm) ST optical glass fiber transmission system** has provided to minimize the effect of interface jitter [44,45,46]. Since the optical cable is not conductive, no ground loops are present, which eliminates the hum that the potential difference between grounds in connected equipment may generate. The bandwidth of an optical cable is also wider than that of a wire cable. An optical cable does have a maximum length, but this is based on the attenuation of the signal in the cable, i.e.: its efficiency.

The high speed optical glass fiber system has **125MHz** bandwidth but the **Toslink optical plastic fiber optic transmission** system only has **6MHz** bandwidth. There is some difference in the optical drivers. The Toslink parts include the driver circuitry. The ST transmitter is simply the photo-diode, so external driver circuit must be used. The output of the optical receiver is a TTL level. The maximum bandwidth of the Toslink is only 6MHz which can create the jitter at the sampling frequency 48KHz significantly. It is because the maximum rate of transition is 6.134MHz that is out of the Toslink transmission bandwidth.

Optical high speed ST transmitter circuit diagram is shown in Fig. 2.2. The SPDIF signal input to the inverter **(74F04)** of U1. The output of U1 drives three inverters that are U2,U3,U4. Their output are joined together with three resistors of R1,R2and R3 (the function of resistor is to isolation the driver and equalize the output current) and then couple to the high speed ST optical transmitter **(HFBR-1412**. The buffer chips U2,U3,U4 are used to supply current to the LED

transmitter. This circuit is proposed by the HP data book and typically produce rise/fall times of **3ns** and a total jitter including pulse-width distortion of less than **2ns**. This circuit is recommended for applications requiring low edge jitter or high-speed data transmission at signal rates of up to 125MBd. Also, this circuit uses " **current-peaking technique** " to reduced the typical rise/fall times of the LED and a small pre-bias voltage to minimize propagation delay differences that cause pulse-width distortion. The detail of resistor value calculation in this circuit can be found in the HP data sheet.

Optical high speed ST receiver circuit diagram is shown in Fig. 2.3. The optical pulses come from the ST transmitter circuit though the AT&T glass fiber cable (**62.5 / 125μm**) to the ST optical high speed receiver **(HFBR-2416).** Its output is connected to U1 **(74HCU04)** though the capacitor C1.C1 serves as an ac-couple between the optical high speed receiver and inverter. U1 acts as a linear amplifier to amplify the optical pulse to the suitable level. The R1 resistor (Its value can be within 10k ohms to 470k ohms) across the inverter U1 provides bias such that operation is within the linear operation region of the gate. R2 is the loading resistor or the impedance of the U2. U2 buffers U1 and provides the wave-shape function.

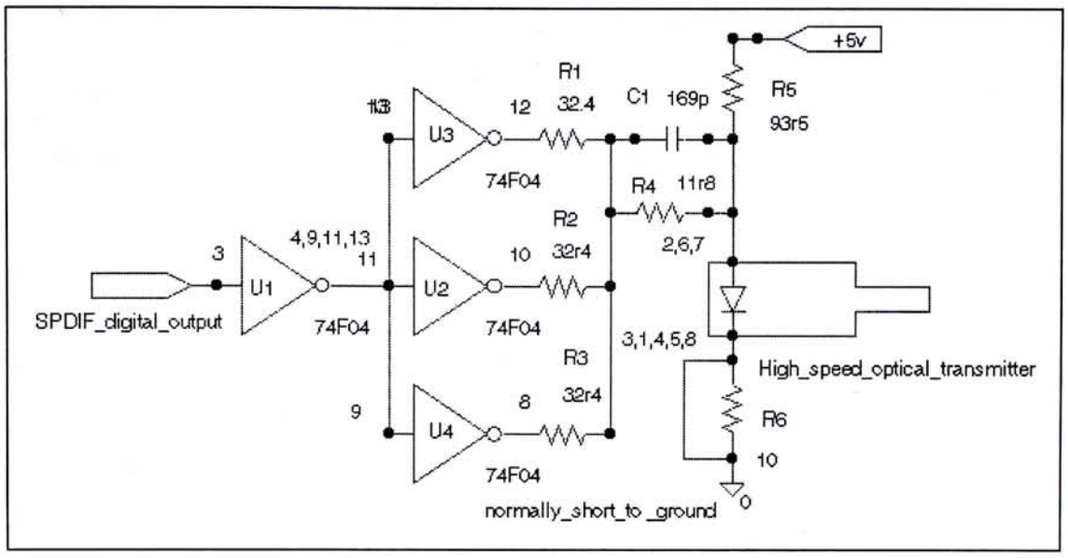


Fig. 2.2 Optical high speed ST transmitter circuit diagram

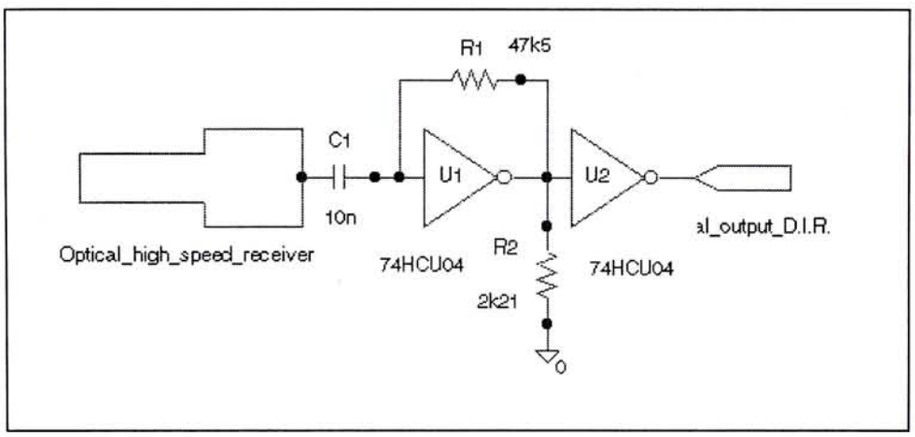


Fig. 2.3 Optical high speed ST receiver circuit diagram

2.7 Crosstalk

Crosstalk, interference or signal coupling or the high frequency can increase jitter. It is advisable to avoid parallel PCB traces to minimize digital crosstalk between clocks and control lines.

In practice, PCB layout and interconnect guidelines should be followed. This may include terminating MCLK (master clock) or the bit clocks if excessive overshoot or undershoot is evident.

2.8 Inter-Symbol-Interference (ISI)

On a long cable, high frequency roll-off can cause sufficient jitter to move a transition into an adjacent bit period. This is called **Inter-Symbol-Interference (ISI)** [67] and the effect becomes worse in signals, which have greater asymmetry, i.e.: short pulses alternating with long ones. This effect can be reduced by the application of equalization, which is typically a high frequency booster, or by choosing a channel code which has restricted asymmetry. Usually this kind of jitter has strong pattern dependency. A few ns jitter is likely to occur for cable up to 100m long [6]. By adding pre-distortions like overshoot or undershoot to the transmitted data to compensate the cable capacitance effect -is called **cable capacitance compensation method** (i.e.: application of this method in the 1.544Mb/s PCM systems) [6].

2.9 Baseline wander

The received signal voltage is compared with the midway voltage, known as the **baseline** or **slicing level**, using a comparator. If the signal voltage is above the baseline , the comparator outputs a high level; if below, a low level results. Slicing a signal which has suffered losses works well if the duty cycle is even. If the duty cycle is odd, timing errors will become worse. With the opposite duty cycle the slicing fails in the opposite direction. If the signal is DC free, correct slicing can continue even in the presence of serious losses. If a signal with sloping edges is sliced, the time at which the waveform crosses the slicing level will be changed. This causes jitter [67].

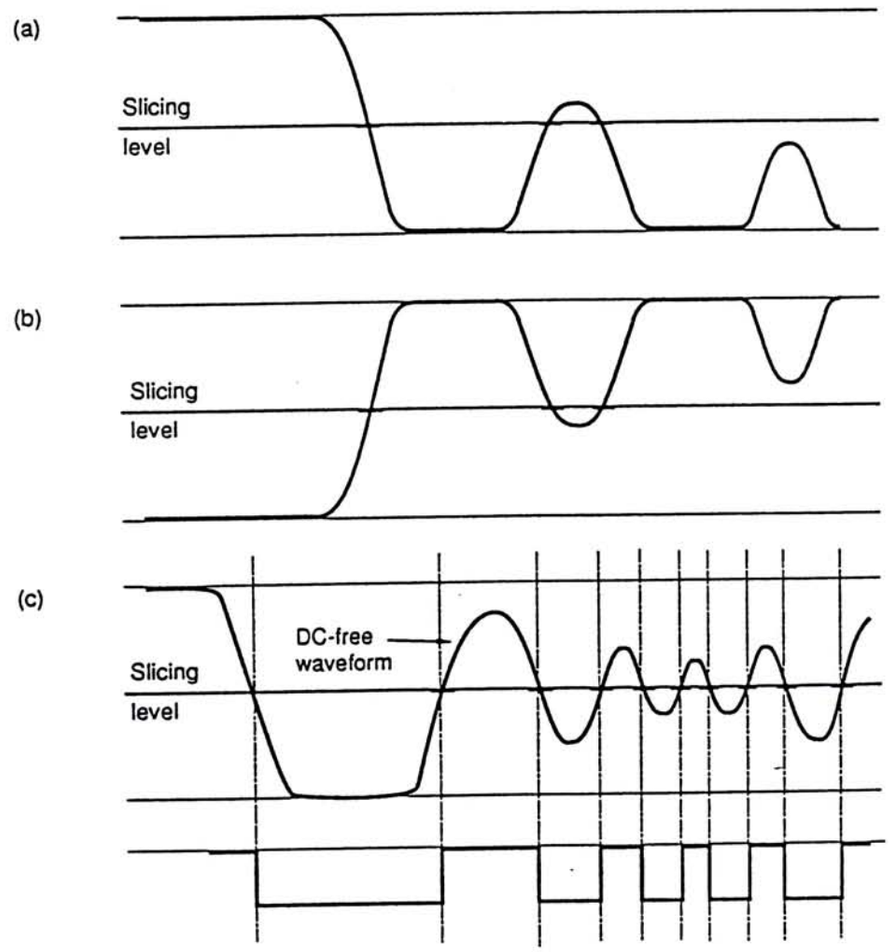


Fig.2.4. Slicing a signal which has suffered losses works well if the duty cycle is even. If the duty cycle is uneven, as at (a), timing errors will become worse until slicing fails. With the opposite duty cycle. The slicing fails in the opposite

direction as at (b). If the signal is DC free, correct slicing can continue even in the presence of serious losses, as (c) shows (note: this figure is quoted from [67] pp.64).

2.10 Noise jitter

When noise is present on a sloping signal edge, it can change the time at which the slicer judges the transition to have occurred. Differential signals are often used in interfacing to reduce sensitivity to noise because the receiver subtracts the anti-phase signal from the in-phase signal. As a result the noise is canceled but the signals are enhanced [67].

2.11 FIFO jitter reduction chips

The problem of First In First Out---- FIFO jitter reduction chips or Sample Rate Converter ----SRC chips (**AD1890**, **AD1891**, **AD 1893** [19] , **SM5844AP** [20] and **TDA1373H** [21]) :

A FIFO using RAM buffer is supposed to eliminate all the incoming jitter but it does not seem effective at frequency below 10 Hz [25].

If the same power supply is applied to the Crystal oscillator, at the output of the FIFO, and the input of the FIFO, any variation in loading at the input to the FIFO is **micro-cosmically** transmitted to the output of the FIFO *through the power supply rail.* (Note: Crystal oscillators and PLL should be powered from independent supplies. Using battery supplies will give better results.) .

At any time, data is transferred between two digital domains which are under the control of independent clocks, then clock jitter occurs.

For example, suppose we have two devices, A and B, which have their clocks independently synchronized their clocks to a common reference. Let the common reference frequency be fs and the clock frequency in each section is 256 fs. Data from device A, through the FIFO, into device B. Theoretically, once the FIFO gets started, it stays filled at a constant level because the input and output rates are the same.

In practice, the two clocks are hardly the same. The common timing reference signal comes along only once every 256 clock period, leaving plenty of time for the two clocks to diverge between reference edges. In practice, jitter between the two clocks makes the FIFO to gyrate wildly. The greater the ratio of clock to reference frequency, the worse this effect becomes. *Enough jitter will cause the FIFO to either overflow or run empty.* The maximum deviation in the FIFOs corresponds to the maximum phase difference between the two clocks.

Megabytes of RAM would be required to store the digital data otherwise the Jitter and /or Wander still occurs [18].

FIFOs are sensitive to wander. These FIFOs operate open loop and are dependent on inherent synchronization between the write and read clock. Therefore, they are sensitive to the variations of phase from 10 Hz all the way down to dc [1].

Chaper 3

3 JITTER REDUCTION TECHNIQUES [14 , 15 , 17]

3.1 Why using two-stage phase-locked loop (PLL) circuit?

The first stage recovers the clock and data and then feeds its recovered clock to the second stage. The VCO on the digital interface receiver (DIR.) chip like CS8412-CP will range from 3MHz to 13 MHz over a control voltage range of less than 5V and with a gain of about 2MHz/ Volt.

The second stage PLL acts as a " **jitter attenuator** " (Like low-pass filter on the jitter spectrum, passes the unjittered clock signal and attenuates any fluctuations in the input signal clock frequency which occurs faster than a certain rate, ie: the cut-off frequency of the low-pass filter.) and has a much simpler task than the first stage.

Analog PLL or All digital PLL circuit may be used in the second stage. In fact, PLL circuit function is to maintain frequency stability and not to track frequency variation. It is noted that the use of high speed, low-gain phase detector, with low-gain VCO (i.e.: VCXO , its gain is about 100ppm/ Volt), and loop filter with cut-off frequency setting as low as possible and no frequency multiplication, no input hysteresis needed, not expected to track clock variations .

It is noted that the second stage cannot track input frequencies beyond VCXO range[65]. It is desirable to make the PLL'cutoff frequency as low as possible. Using the all digital PLL circuit can fulfill this job by setting the very low cut-off frequency ≤ **1.314mHz** to eliminate the extrinsic jitter and low frequency jitter wander (see section 3.4).

There are three application methods of this stage:

- **First method:** The two-stage PLL circuit only supplies the PLL de-jittered master clock signal (MCK') into the next stage and leaves the DIR. output signal----SDATA, FSYNC, SCK into the next stage (Suggested by the application notes of crystal semiconductor company (65)).
- **Second method:** The two-stage PLL circuit supplies the PLL de-jittered master clock signal (MCK') , FSYNC', SCK' into the next stage and sends the DIR. output signal----SDATA, into the next stage.
- **Third method:** The two-stage PLL circuit supplies the PLL de-jittered master clock signal (MCK') , FSYNC', SCK' into the next stage and sends the DIR output signal----SDATA, into the next stage which uses another ADPLL circuit to synchronic all the following chips, hence the master clock **skew effect** will be neglected (see section 7.1.2).

3.1.1 The PLL circuit components[14]

PLL circuit consists of the phase detector, analog low pass filter (LPF) of either single-ended or differential, voltage-controlled oscillators (VCO) and external divide-by-N counter.

An ideal phase detector (PD) produces an output signal whose dc value is linearly proportional to the difference between the phases of two periodic inputs ($\Delta\phi$). The PD generates an output pulse whose width is equal to the time difference between consecutive zero crossings of the two inputs. Because two frequencies are not equal, the phase difference exhibits a " beat " behavior with an average value of zero. There are many type of PD (below listed is common available from the hardware market):

1. Excusive Or gate phase detector (EX-OR-PD) with commercial available chip are CDHC4046A'PC1 and CD4046A'PC1.
2. Phase frequency comparator (PFC-PD) with commercial available chip are MC4044, CDHC4046A'PC2 and CD4046A'PC2.
3. R-S flip-flop phase detector (RS-PD) with commercial available chip are CDHC4046A'PC3 and CD4046A'PC3.

In the locked condition, the low-pass filter suppresses high-frequency components in the PD output, allowing the dc value to control the VCO frequency. The VCO then oscillates at a frequency equal to the input frequency and with a phase difference equal to $\Delta\phi$. Thus, the LPF generates the proper control voltage for the VCO.

The external divide-by-N counter is to **frequency multiplication** of periodic signals. If the input of the PLL frequency is Fs, the PLL output frequency can be scaled to N x Fs. For example: the Fs is 44.1KHz and the N is 256, then the PLL output frequency can be scaled to 256 x 44.1k =11.2896MHz).

3.1.2 The PLL timing specifications

A set of specifications is used to describe the operation of a PLL [69]. The critical parameters are as follows:

1. Duty cycle

   The duty cycle of a clock refers to the percentage of time the clock signal is high compared to the percentage of time it's low. For instance, if a 50Mhz clock is low for 9ns and high for 11ns, it is said to have a 45%/55% duty cycle. The incoming clock must meet a duty cycle specification in order for the PLL to lock onto the clock. This specification is called $\mathbf{t_{induty}}$. Additionally, the clock that the PLL generates will meet a specification for duty cycle. This specification is called $\mathbf{t_{outduty}}$.

2. Clock deviation

   There is a tolerance allowed relative to the expected frequency , for example, if 20MHz is entered and 20.5 kHz is allowable. The $\mathbf{f_{clkdev}}$ specification shows how far from the expected frequency the input clock may deviate. If the input clock deviates from the expected frequency by more than $\mathbf{f_{clkdev}}$, then the PLL may lose lock onto the input clock.

3. Clock stability

   If the incoming clock is not a clean, regular signal, the PLL may not be able to lock onto it. The $\mathbf{t_{inclkstb}}$ specification specifies how regular the incoming clock must be . The $\mathbf{t_{inclkstb}}$ parameter is measured on adjacent clocks and shows how much the period of the clock can vary from clock cycle to clock cycle. For instance, if clock cycle n is 20ns, and clock cycle n+1 is 20.1ns, the clock stability would be 0.1ns.

4. Lock time

   Before the PLL begins to operate, it must lock onto the incoming clock. The PLL will take certain amount of time to lock onto the clock. This time is referred to as the lock time. During this time, the PLL will output an unstable clock. Therefore, it is recommended that the circuit be reset after the Lock signal is asserted.

5. Jitter

Jitter refers to instability in the PLL's output. The low and high times of the PLL-generated clock may vary slightly from clock cycle to clock cycle, The $\mathbf{t_{jitter}}$ specification shows how much the PLL-generated clock may change from cycle to cycle.

3.2 Analog phase-locked loop (APLL) circuit used in second stage

The APLL circuit block diagram used in digital audio is shown in Fig.3.1. Analog ADPLL consists of the phase detector, analog low pass filter of either single-ended or differential, VCO and external divide-by-256 or 384 counter. The input f_s or F_{sync} signal comes from the digital audio receiver chips. The output signal of the APLL circuit is then connected either into the digital filter chips or first in first out chips (see the section 6 of appendices 6.1).

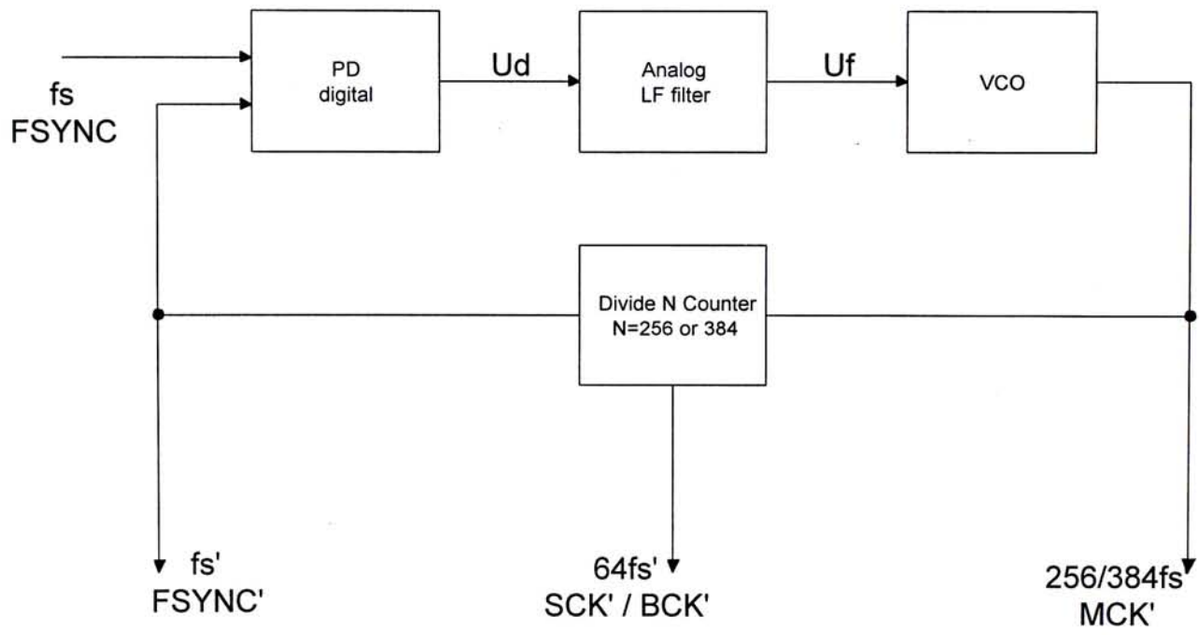


Fig.3.1. Analog PLL circuit block diagram

The using of single-ended analog loop filter circuit techniques can reduce jitter :

1. Biasing current can be added to the output of the phase detector. This current moves the phase detector off the **phase-distortion zone,** but bias current raises the reference sideband levels in a PLL by increasing the output pulse width of the detector in the locked condition.
2. A pulse is added at the phase detector output when the input signals are at 0 degree phase. This pulse biases the phase detector off the **phase-distortion zone**, but this pulses also increase the reference side-band levels.

The use of second order differential analog loop filter circuit techniques can further reduce jitter :

1. The differential circuit can minimize phase detector distortion at the 0° phase shift condition. This configuration (with filtering) averaged the distortion at 0 degree to produce a smooth transition. At 0° input-signal phase difference, the up and down outputs produce negative-going spikes. One capacitor integrates the spikes from the up output and the other capacitor integrates the spikes from the down output. Each capacitor separately stores the DC average of several spikes from the up and down outputs of the detector. The differential comparison of the DC average by the op-amp produces the filtered output. But the effects of the op-amp propagation delays and bandwidth must be minimized.
2. The differential circuit decreases the reference side-band levels by reducing the effects of the op-amp bias current.
3. A single-ended phase/ frequency-detector (i.e.: **MC 4044, MC 4344 and MC 145151-2** and so on) connection produces considerable distortion at 0° phase. This problem is avoided by employing a differential connection with output filtering.

3.3 All digital phase-locked loop (ADPLL) circuit used in second stage

The ADPLL circuit block diagram used in digital audio is shown in Fig.3.2. ADPLL consists of a **ripple cancellation circuit** with **edge-controlled phase detector (ECPD)** as a phase detector and **HC / HCT 297, HC / HCT 297** as a digital PLL filter chip, external divide-by-256 or 384 counter and high speed inverter.

Different types of phase detectors are linked below for ease of comparison:

	edge-controlled phase detector	exclusive-or phase detector
	ECPD	EXORPD
loop phase error	+/-180°	+/-90°
phase detector gain (K_d)	2	4
advantage	no duty cycle requirement	1. less sensitive to noise ; 2. narrow phase-error range
disadvantage	1. wider phase-error range; 2. more sensitive to noise	1. square wave input signal; 2. input signal must have a 50% duty cycle

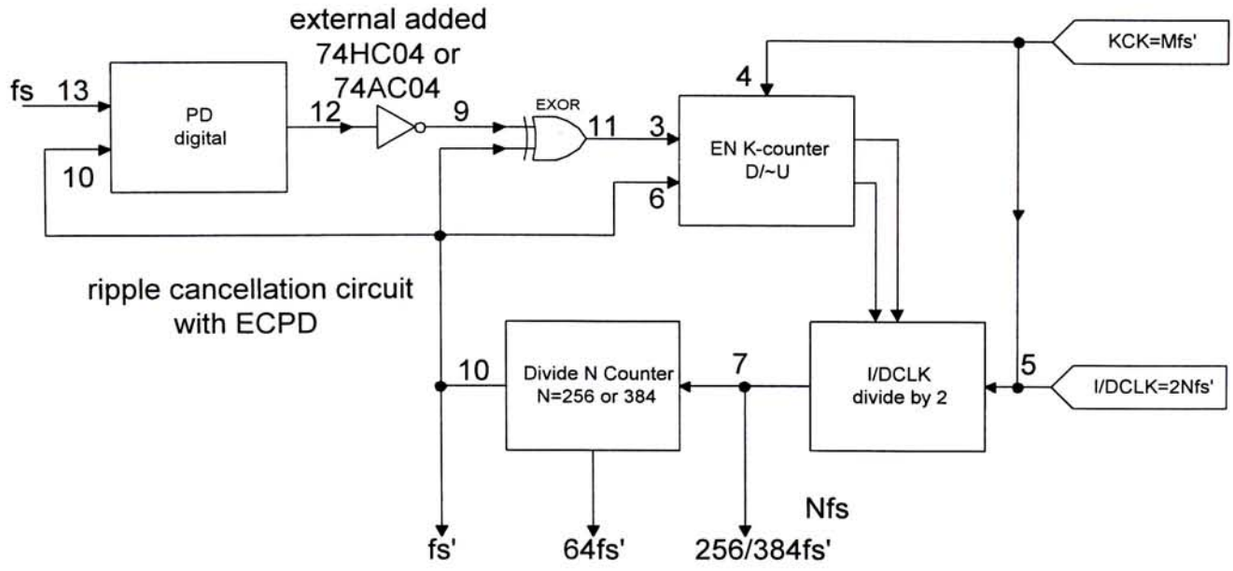


Fig.3.2. All digital PLL circuit block diagram

The global working of such a PLL [9,10] is as follows:

The K-counter counts up or down when the output of the phase detector is high or low , with a step equal to

$$\Delta \mathbf{k} = \mathbf{M}\, \mathbf{k}_d\, \theta_e \qquad (3.1)$$

where $\theta_e = \theta_i - \theta_o$

is the phase error between the input signal and the output signal of the VCO. Without carry or borrow pulses, the I/D counter divides its own input frequency by two to get **50% duty cycle** clock signal. When a carry pulse is generated at the I/D counter circuit . The output frequency of the divided by N-counter circuit is

$$f_{out} = f_{s'} = f + \mathbf{M} \bullet \mathbf{k}_d \bullet \theta_e \bullet f_s \bullet \frac{1}{2\mathbf{kN}} \qquad (3.2)$$

In this circuit, the **ripple cancellation techniques** is included in order to minimize ripple. The K-counter is disabled when the DPLL is in locked condition with zero phase error. While these circuits act to minimize ripple, they also have the effect of narrowing the locked range of the loop. Without using this ripple cancellation techniques, the K-counter should continue to function, producing periodic carry and borrow pulses, even if the loop is locked with zero phase error. If K is too small, the K counters will recycle too often, producing repeated carry pulses followed by repeated borrow pulses. This will result in a **duty cycle error** called **ripple** in the DPLL output. This ripple may be reduced to a value of 1/N cycles at the divide-by-N counter output by making K sufficiently large, specifically, K> M/4 for DPLL circuit utilizing the EXOR phase detector and K> M/2 for ECPD circuit, so that the phase correction pulses will cancel in the lower order bits of the divider-by-N counter.

When the ripple cancellation circuits is implemented, the K-counter is disabled when the DPLL is in a locked condition with zero phase error. While these circuits act to minimize ripple. They have the effect of narrowing the lock range of the loop. The loop phase error limit is reduced by a factor of n nd and the phase detector gain, K_d is reduced by 0.5. This results in an adjusted locked range from

$\Delta f \max = Mfs/2KN\,(Hz)$ into $\Delta f \max = Mfs/(1+0.5K)4KN\,(Hz)$.

3.4 ADPLL design

Here is the ADPLL design:

- Assume the all digital PLL is in a locked condition .
- Take the input to all digital PLL frequency is f_s = 44.1kHz and output master clock frequency = 256f_s' as an example. The symbol ['] is the PLL output frequency.
- $f_s = f_s' =$ **44.1kHz** ,
- master clock =256f_s ,
- I/D clock = K clock = 512f_s=**22.5792MHz.**
- M =**512** ,
- N =256,
- Kd = **2** (for ECPD),
- Kmin = 8 ,
- Kref = 2^7 = 128 ,
- Kmax = 2^{17} = 131072
- Note: K_d = 4 (for EXOR).

A/ The locked range Δf_s min. (theoretical calculation)

$$= \frac{M \bullet f_s}{2K_{min} \bullet N} = \frac{512 \bullet 44.1K}{2 \bullet 8 \bullet 256} = 5512.5Hz. \qquad (3.3)$$

The recommenced locked range Δf_s ref. (theoretical calculation)

$$= \frac{M \bullet f_s}{2K_{ref} \bullet N} = \frac{512 \bullet 44.1K}{2 \bullet 128 \bullet 256} = 344.53Hz.$$

The locked range Δf_s max. (theoretical calculation)

$$= \frac{M \bullet f_s}{2K_{max} \bullet N} = \frac{512 \bullet 44.1K}{2 \bullet 131072 \bullet 256} = 336.46mHz.$$

B/ The locked range Δf_s min. (practical calculation)

$$= \frac{fs}{K\,\min \bullet N} = \frac{44.1K}{8 \bullet 256} = 21.533Hz. \qquad (3.4)$$

The recommenced locked range Δf_s ref. (practical calculation)

$$= \frac{f_s}{K_{ref} \bullet N} = \frac{44.1K}{128 \bullet 256} = 1.346Hz.$$

The locked range Δf_s max. (practical calculation)

$$= \frac{f_s}{K_{max} \bullet N} = \frac{44.1K}{131072 \bullet 256} = 1.314mHz.$$

C1/ The phase error resolution (phase error in divide-by-256 counter)

$$= \pm\frac{1}{2N} \bullet 360° = \pm\frac{1}{2 \bullet 256} \bullet 360° = \pm 0.7°. \qquad (3.5)$$

C2/ The phase error resolution (phase error in divide-by-384 counter)

$$= \pm\frac{1}{2N} \bullet 360° = \pm\frac{1}{2 \bullet 384} \bullet 360° = \pm 0.469°.$$

D1/ The ripple (phase error in divide-by-256 counter)

$$= \frac{1}{N} = \frac{1}{256} = 3.90625ms / cycles \qquad (3.6)$$

when $f_s = f_s'$.

D2/ The ripple (phase error in divide-by-384 counter)

$$= \frac{1}{N} = \frac{1}{384} = 2.604ms / cycles$$

when $f_s = f_s'$.

E/ The settling time Ts min.

$$= \frac{K_{min} \bullet N}{K_d \bullet M \bullet f_s} = \frac{8 \bullet 256}{2 \bullet 512 \bullet 44.1k} = 45.35\mu s. \qquad (3.7)$$

where T_s is the duration of one reference cycle.

The settling time T_s ref.

$$= \frac{K_{ref} \bullet N}{K_d \bullet M \bullet f_s} = \frac{128 \bullet 256}{2 \bullet 512 \bullet 44.1k} = 725.62\mu s.$$

The settling time T_s max.

$$= \frac{K_{max} \bullet N}{K_d \bullet M \bullet f_s} = \frac{131072 \bullet 256}{2 \bullet 512 \bullet 44.1k} = 743.04ms.$$

F/ The PLL filter quality factor $Q_{min.}$ is

$$= \pi \bullet K_{min} \bullet \frac{1}{k_d} = \pi \bullet 8 \bullet \frac{1}{2} = 12.566 \ (\text{if } M = 2N) \qquad (3.8)$$

The PLL filter quality factor $Q_{rec.}$ is

$$= \pi \bullet K_{ref} \bullet \frac{1}{k_d} = \pi \bullet 128 \bullet \frac{1}{2} = 201.062 \ (\text{if } M = 2N)$$

The PLL filter quality factor $Q_{max.}$ is

$$= \pi \bullet K_{max} \bullet \frac{1}{k_d} = \pi \bullet 131072 \bullet \frac{1}{2} = 205887.4 \ (\text{if } M = 2N)$$

The conventional analog VCO cannot obtain this value (205887.4), but the system clock (K_{CK} and I/D_{CLK}) of ADPLL circuit must be temperature compensated to avoid the system **clock drift**.

The phase error lock range data in chapter 3.4.A and 3.4.B indicate that the locked ranges were reduced from the theoretical limits by the phase resolution factor 0.5N and loop propagation delays along with the factor of $1/(1+0.5K)$ mentioned in earlier section (3.3) for ripple cancellation circuits.

Phase error resolution in chapter 3.4.C1 and 3.4.C1 can be best understood by recalling that the phase of the I/D circuit output is adjusted by half-cycles. This means that the phase of the output signal, f_s', will have an uncetainty or resolution of +/- 0.5N cycles. For a +/-0.5N phase resolution, the output frequency f_s' will have an uncertainty Δf of 21.533 Hz for K_{min}. To increase the divided by N number and decrease the input frequency (pre-scale by N) can solve this problem.

The input to the PLL frequency can be 32kHz / 44.1kHz / 48kHz / 64kHz / 88.2kHz / 96kHz if the ADPLL system clock can be change dynamically.

3.4.1

Different of K counter value of ADPLL are listed for comparison with M=512, N=256, Kd=2 :

		$K_{min} = 8$	$K_{ref} = 128$	$K_{max} = 131072$
1.	**lock range (Hz) in theoretical calculation**	5512.5	344.53	0.336
2.	**lock range (Hz) in practical calculation**	21.533	1.346	0.001314
3.	**phase error resolution**	**±0.7°**	**±0.7°**	**±0.7°**
4.	**ripple**	3.90625 ms/cycles	3.90625 ms/cycles	3.90625 ms/cycles
5.	**settling time**	45.35μs	725.62μs	743.04ms

3.4.2 Computer simulated results and experimental results of the ADPLL

Computer simulated results of the ADPLL are shown below:

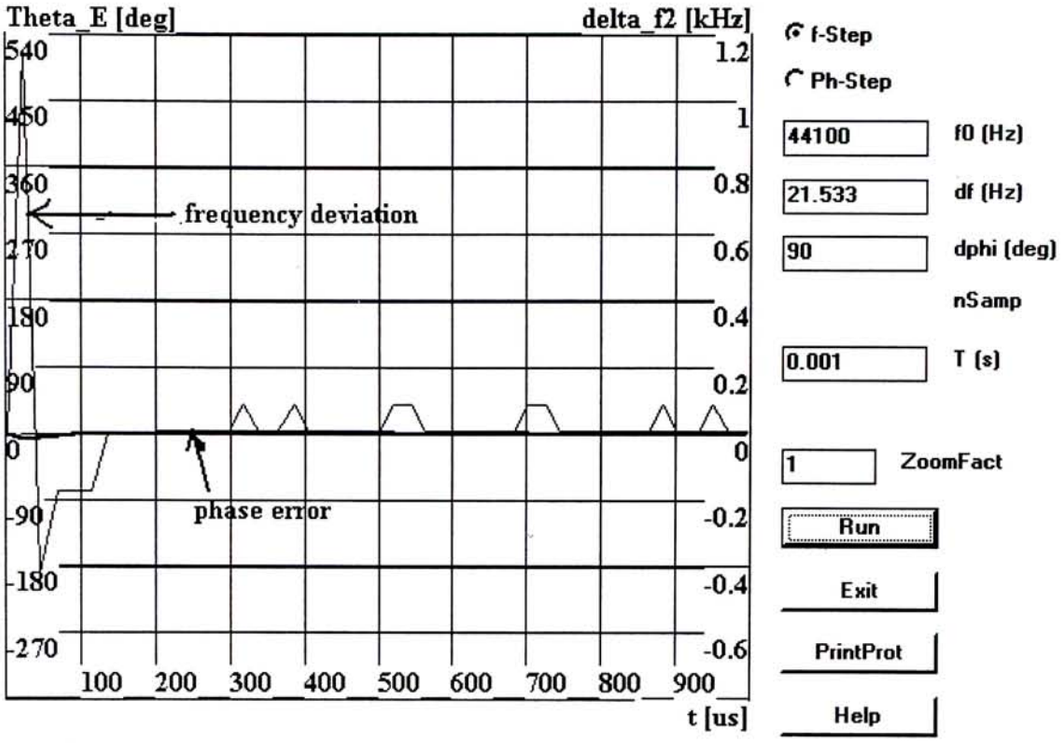


Fig.3.3. Simulated results for a ADPLL circuit with Kmin

The **thick line** is the phase error,

the **thin line** is the deviation Δf_s or Δf of the output frequency from the center frequency f_s'.

Fig 3.3 shows the outcome of the simulation.

A Linear system would settle to within 5 percent of its final state in about three time constants. The curve for the frequency is quite jittery, but the settling time is well in that range. The ADPLL maintains locked condition after 145us with time constant of 1ms. The difference frequency curve looks noisy indeed. The frequency of the output signal does not asymptotically approach the reference but oscillates around that value (within 200Hz) . This is the most typical property of the ADPLL. The instantaneous frequency f_s' of the output signal can take only a number of discrete values.

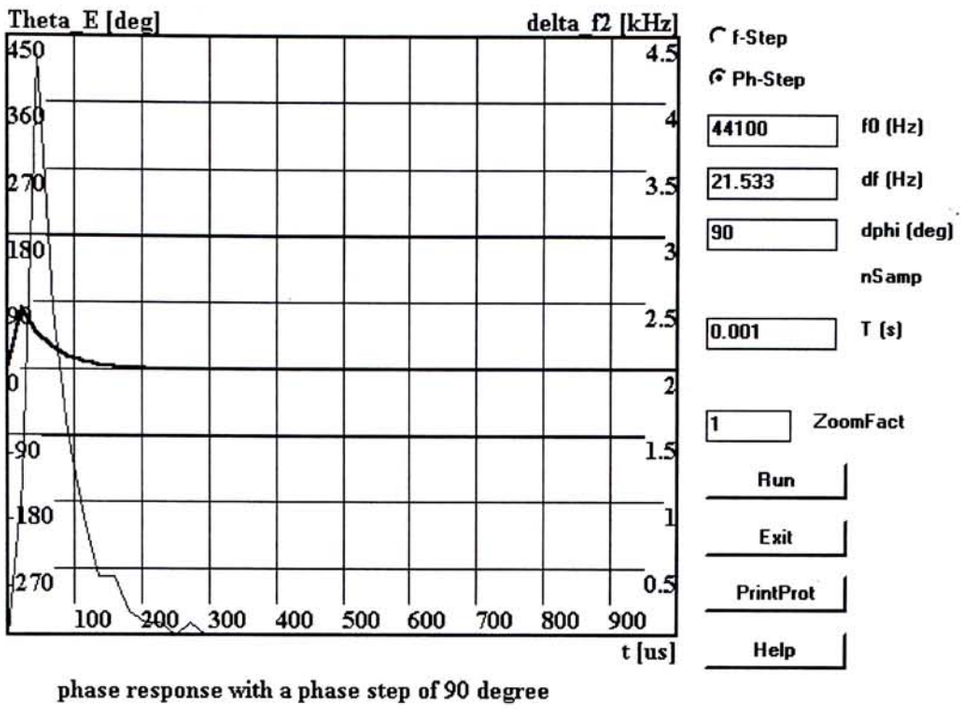


Fig.3.4. Simulated results for a ADPLL circuit with Kmin

The **thick line** is the phase error,

the **thin line** is the deviation Δf_s or Δf of the output frequency from the center frequency f_s'.

Fig 3.4 shows that how the ADPLL reacts onto phase steps. Applying a phase step of 90° causes the output frequency to be increased in a cycles after occurrence of the step, but the loop settles to zero phase error very quickly.

The ADPLL maintains locked condition after 300us with time constant of 1ms. The frequency of the output signal oscillates within 4500Hz .

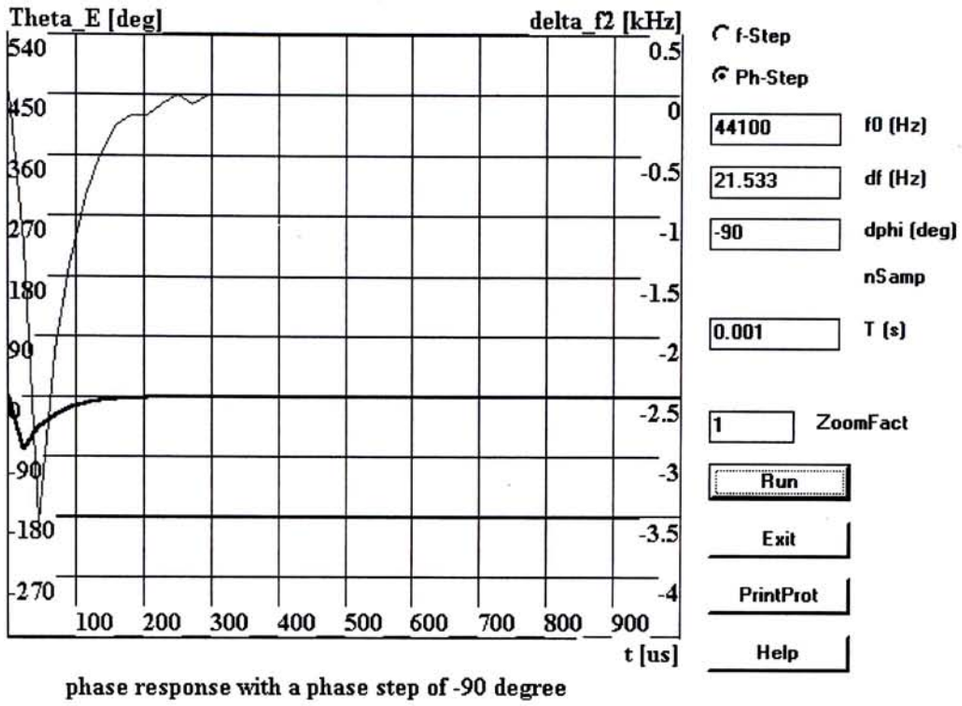


Fig.3.5. Simulated results for a ADPLL circuit with Kmin

The **thick line** is the phase error,

the **thin line** is the deviation Δf_s or Δf of the output frequency from the center frequency f_s'.

Fig 3.5 shows that how the ADPLL reacts onto negative phase steps. When the polarity of the phase step is inverted, the output frequency is reduced during a few cycles, until the ADPLL is locked again with zero phase error. The steady-state error approaches 0 as predicted by the theory.

The ADPLL maintains locked condition after 300us with time constant of 1ms. The frequency of the output signal oscillates within 3500Hz.

Fig.3.6. Simulated results for a ADPLL circuit with Kmin

The **thick line** is the phase error,

the **thin line** is the deviation Δf_s or Δf of the output frequency from the center frequency f_s'.

Fig 3.6 shows how the ADPLL is unable to get into locked condition. When the phase error is over its limit of stability ie: higher than **90°**steps, the system can no longer maintain locked condition, the loop locks out momentarily. When the phase error becomes about **180°** , the gain of the control system reverses, and the output frequency is corrected in the wrong direction. This experiment shows that the reasonable hold range is only slightly less than the predicted one.

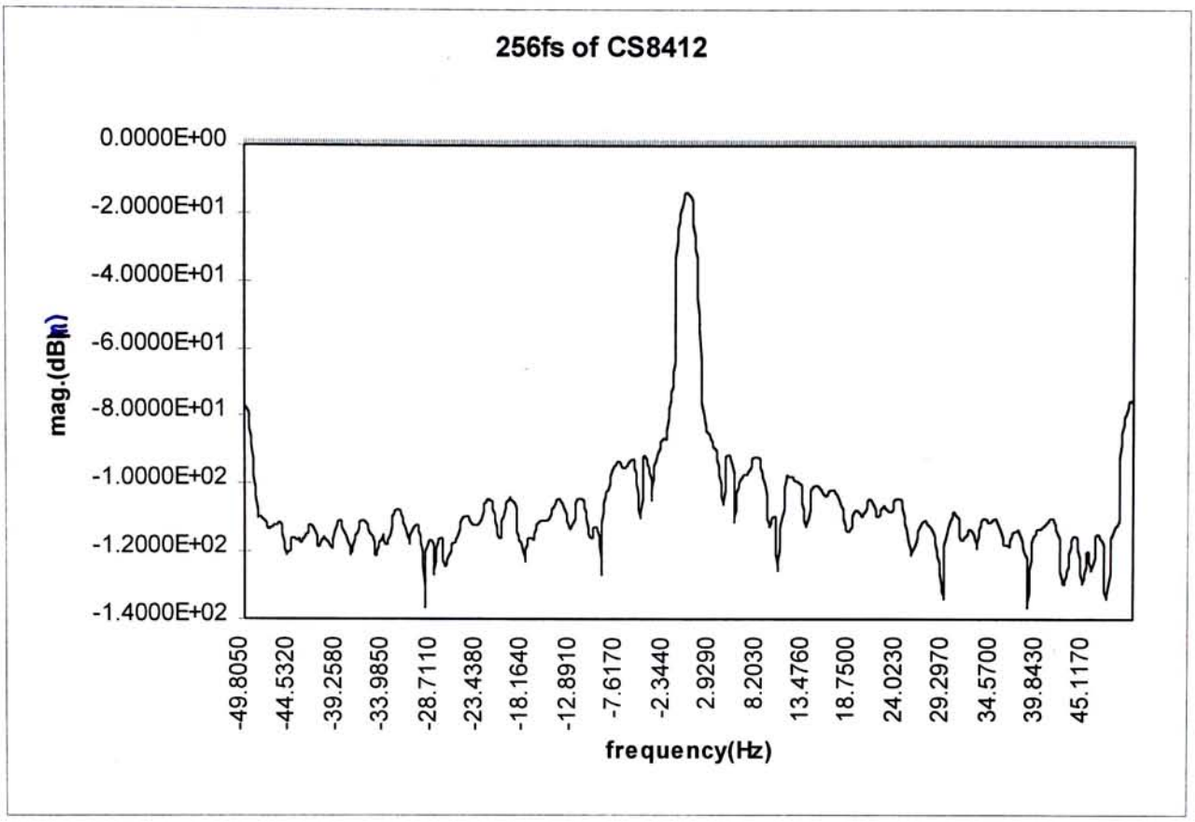


Fig.3.7. Experimental results for a DIR. Chip----CS8412 MCK output spectrum (11.2896MHz) by using ADPLL as a second order PLL..

From the above figure, it can be shown that the quality factor of the CS8412-CP MCK output spectrum (11.2896MHz----256f_s) by using ADPLL as a second order PLL clock. is higher than the Fig.3.8. The side band is +/-49.805Hz.

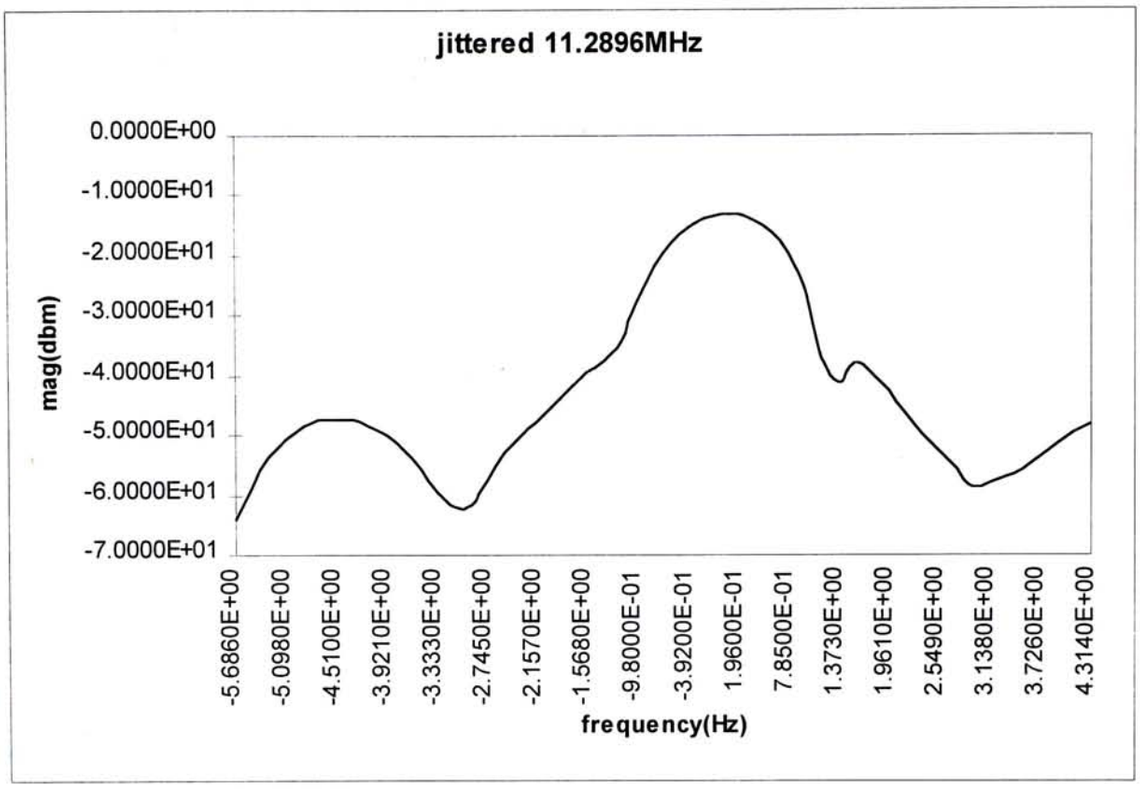


Fig.3.8. Experimental results for a DIR. Chip----CS8412 MCK output that are used in the Audio Alchemy V3.0 (11.2896MHz)

From the Fig.3.8, it can be shown that the quality factor of the jittered CS8412-CP MCK (11.2896MHz----256f_s) is lower than the Fig.3.7. The side band is +/-4.51Hz.

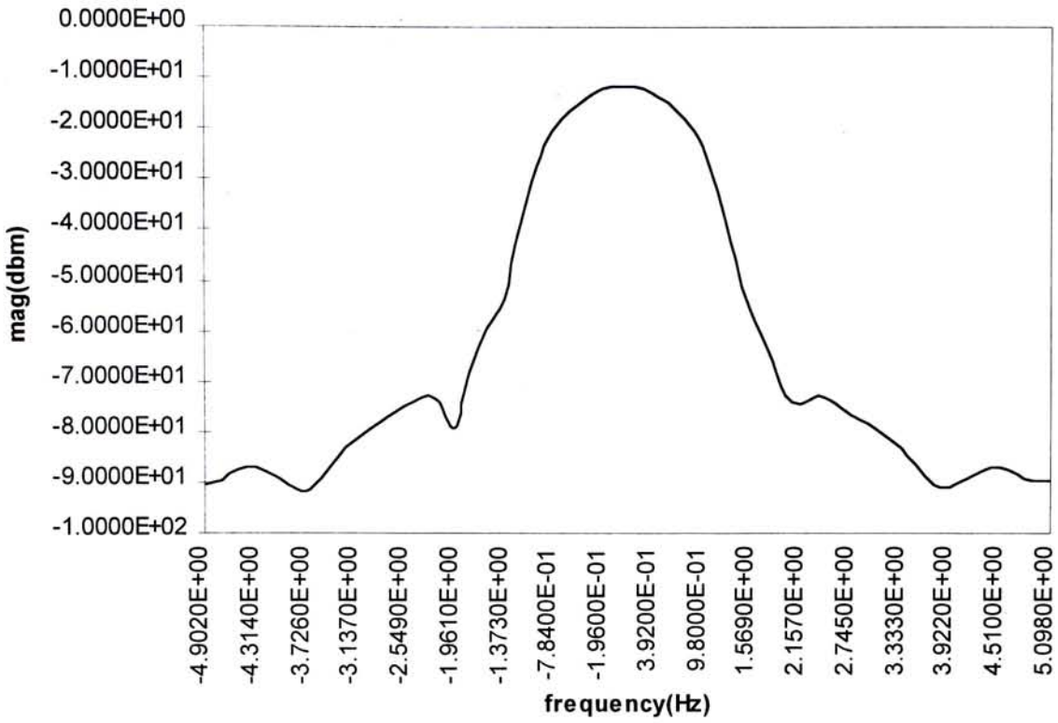


Fig.3.9. Experimental results for a DIR. Chip----YM3623A output that are used in the Stax talent DAC (16.9344MHz).

From the Fig.3.9, it can be shown that the quality factor of the jittered YM3623A MCK (16.9344MHz----384f_s) is litter bit lower than Fig.3.8.

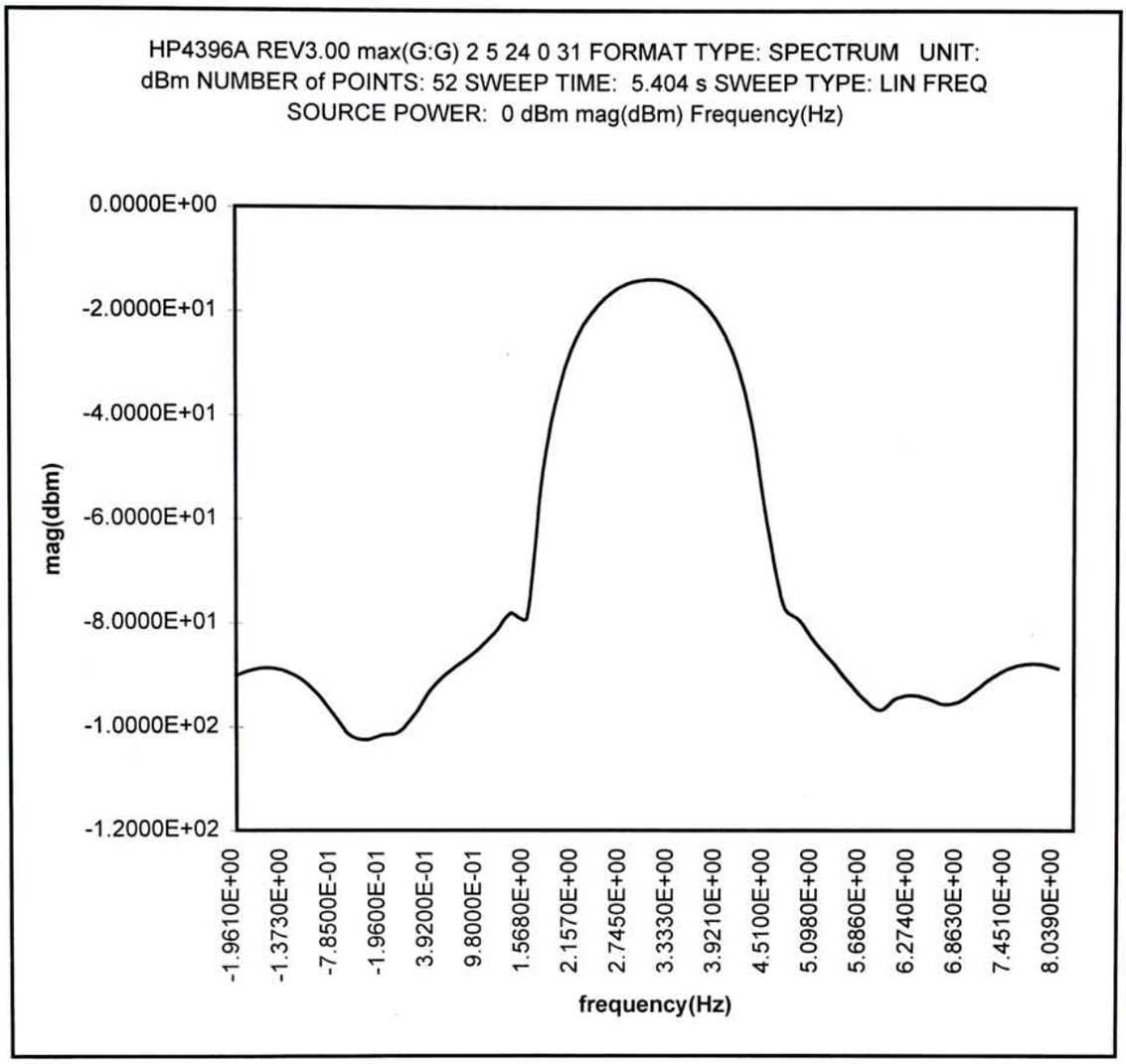


Fig.3.10. Experimental results for a discrete oscillator output with 11.2896MHz

From the Fig.3.10, it can be shown that the discrete oscillator output spectrum (11.2896MHz----$256f_s$) as a master clock of the ADPLL have the highest quality factor. The side band is +/-1.373Hz.

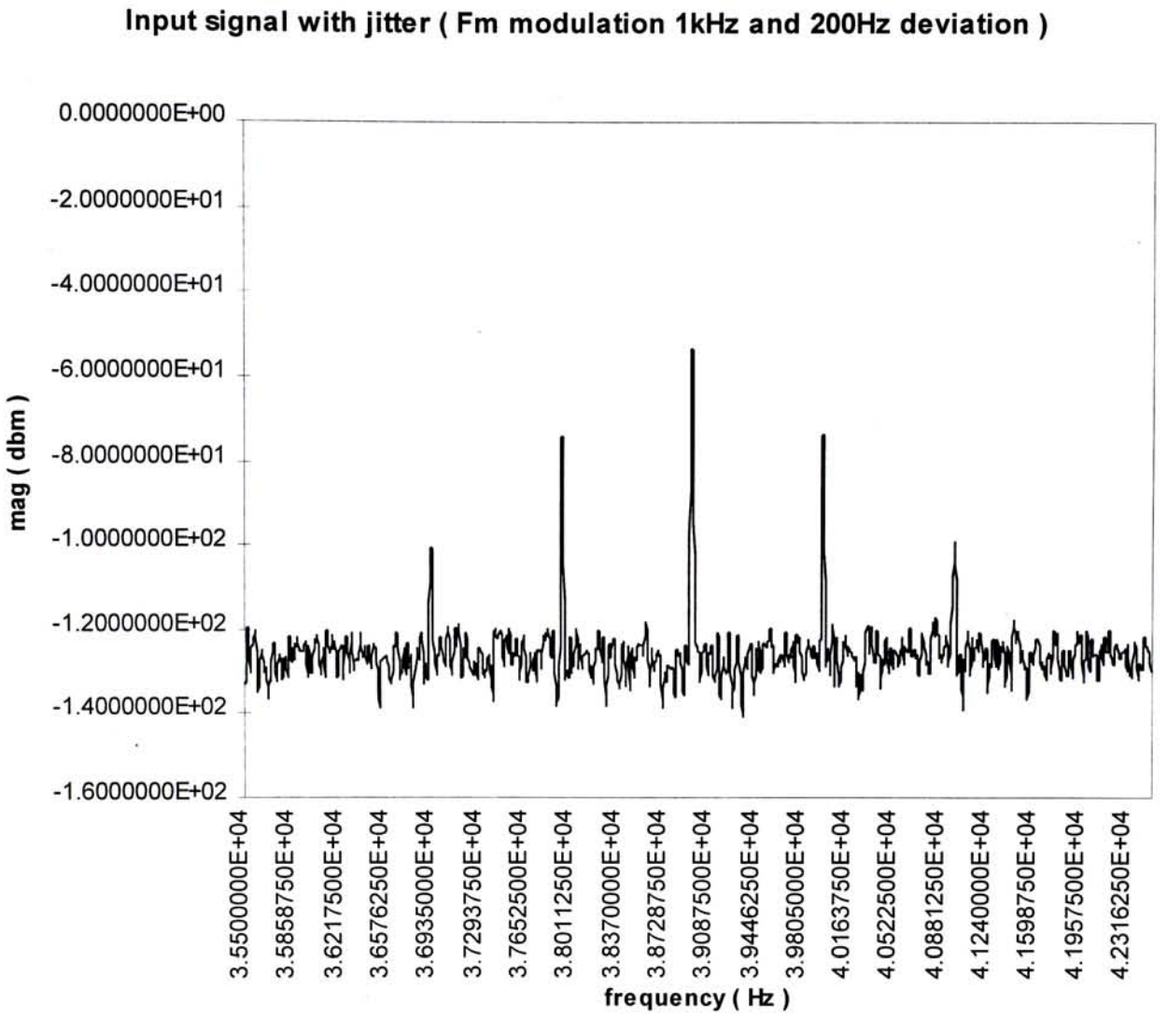


Fig.3.11. Experimental results for input the jitter signal into the ADPLL circuit

From the above diagram, it can be shown input the jitter signal (with frequency modulation of 1KHz and 200Hz deviation) into the ADPLL circuit spectrum.

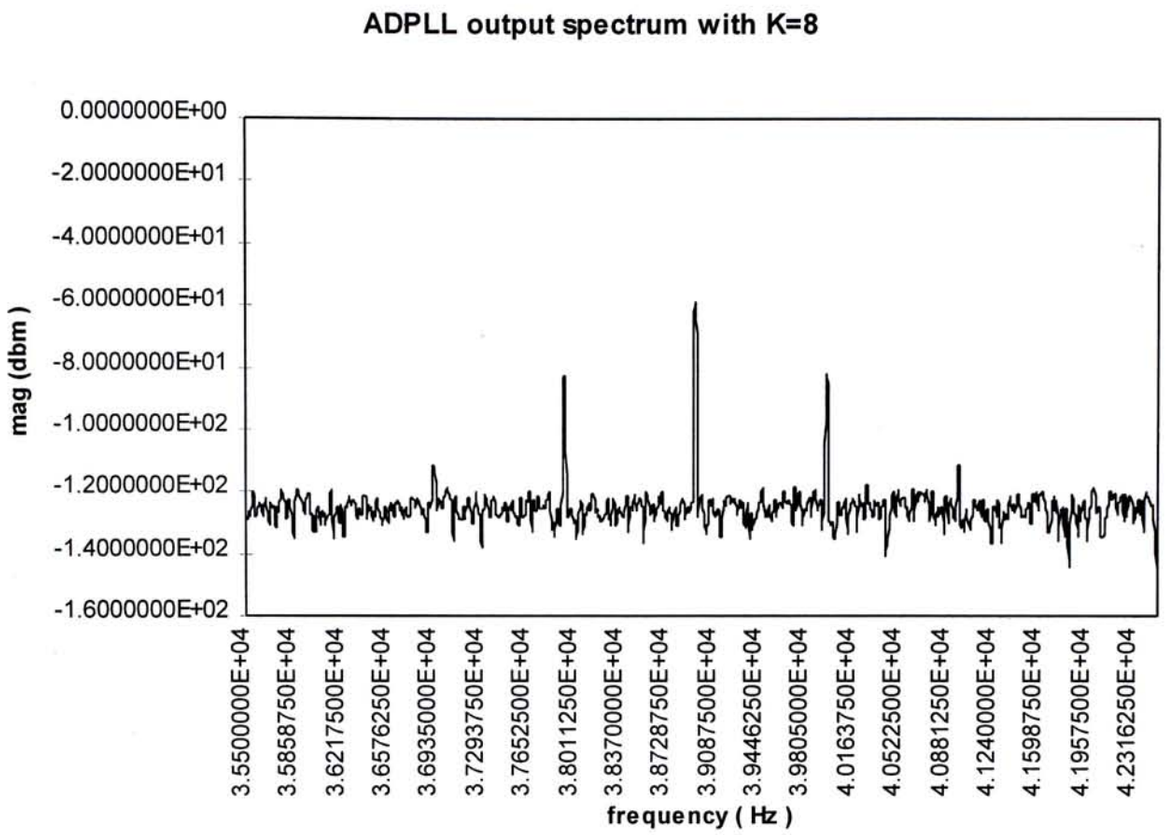


Fig.3.12. Experimental results for the output spectrum of the ADPLL circuit with input jitter signal from Fig.3.11.

From the above diagram, it can be shown input the jitter signal (with frequency modulation of 1KHz and 200Hz deviation) into the ADPLL circuit spectrum. The result is that the sideband have been suppressed but it is not so effective with the K=8 (min.).

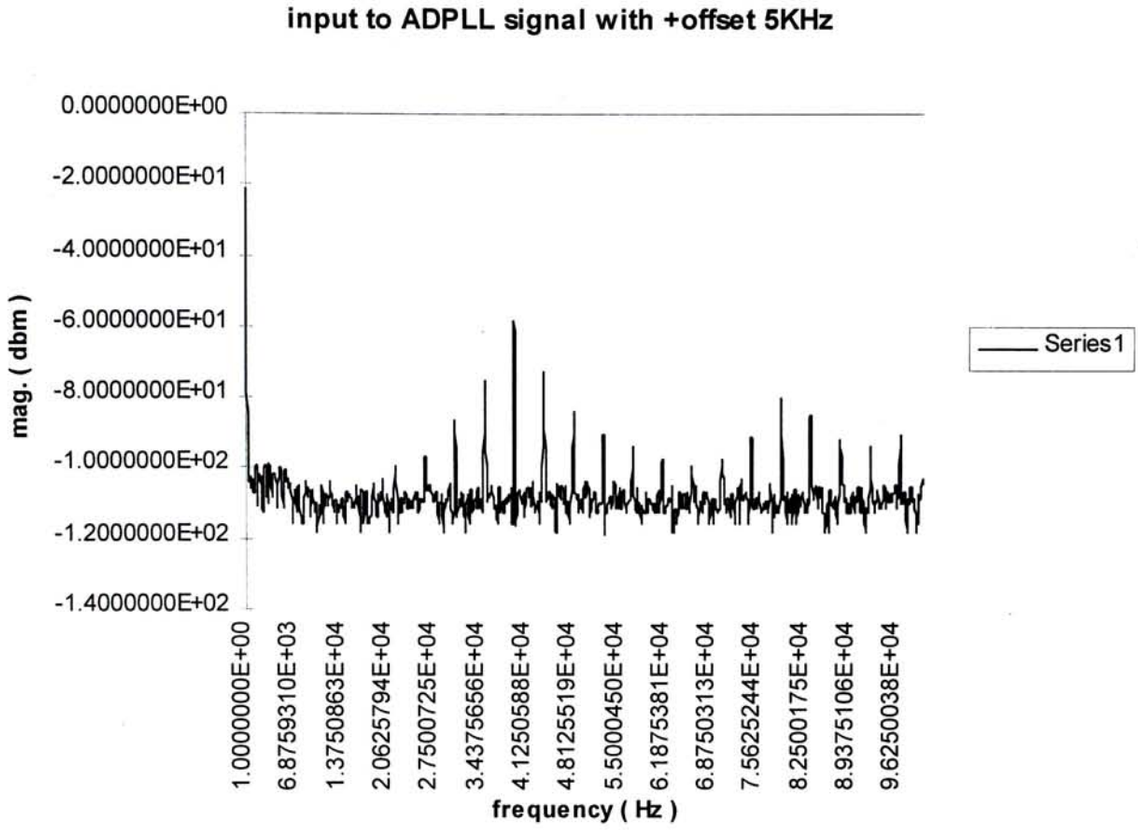


Fig.3.13. Experimental results for the output spectrum of the ADPLL circuit with input signal positive offset with 5 KHz.

From the above diagram, it can be shown output center frequency (f_s') of the ADPLL circuit is nearly the same as the input signal but the sideband's harmonic content is very high with the K=8 (min.) .

All the experimental results are base on the use of S type input HP4396A network analysis, Rev:3.00, number of points is 801, the sweep time is 1.22s with linear frequency sweep, RBW is 100Hz and VBW is 100Hz.

3.4.3 PLL design notes

1. The lower the PLL cut-off frequency, the more the wideband jitter and / or low frequency jitter (wander) the digital interface link can be tolerated and can prevent jitter accumulation in a cascaded system.
2. **Gain peak (GP) or jitter peaking** occurs near the 3dB cut-off frequency $\mathbf{f}_{3dB}$. As a result, some high-frequency jitter components are actually amplified as they appear at the output or create the problem of jitter will be amplified instead of being attenuated in this region. This will aggravate the jitter **accumulation** problem in a cascaded system. To solve this problem, the loop is overdamped to reduce the GP value, but low GP value corresponds to less jitter attenuation at mid-frequency (~ 10 f_{-3dB}), long acquisition time and awkwardly large capacitor value in the loop filter.
3. For the analog VCO , **M2SC12M288-D300** is for 256 fs, **M2SC18M432-D300** is for 384 fs and **M2SC24M576-D300** is for 512 fs. They have two features:

- Build in three sampling frequencies controller .
- 100 times more stable than VCOs with LC or TTL-IC configuration (according to the data sheet).

4. For the analog low-pass filter design see the novel design of [42]. This voltage-mode second-order filter circuit offers the below advantages:

- it uses two high speed current feedback (CFAs) ICs (**AD844JN**);
- it uses five passive elements only: namely two capacitors and three resistors;
- it can realize all the filter functions; namely lowpass, highpass, bandpass, notch and all-pass, without changing the locations or the number of resistors and capacitors used;
- it enjoys independent tuning of the natural frequency, ω_o , and the bandwidth, ω_o/Q_o;
- it enjoys orthogonal tuning of the natural frequency, ω_o , and the quality factor or damping factor , Q_o;
- it has low-impedance output and, can therefore, be easily cascaded to produce higher order filters.

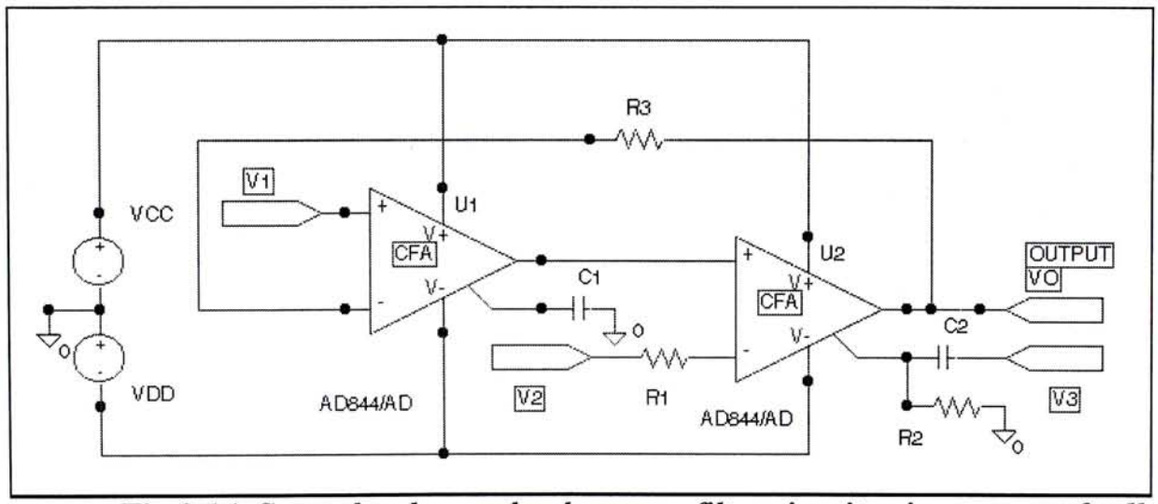


Fig.3.14. Second order analog low-pass filter circuit using current feedback Op-amps

Fig 3.14 shows the circuit diagram of using current feedback Opamp as a second order analog low-pass filter to get better performance. Signal input is at V1 terminal and Vo is the output terminal. U1 and U2 are the current feedback Opamps AD844JN.

The transfer function of fig3.14 can be expressed as

$$Vo = \frac{s^2 C_2 C_1 V_3 - s G_1 C_1 V_2 + G_1 G_3 V_1}{s^2 C_2 C_1 + s G_2 C_1 + G_1 G_3} \qquad (3.9)$$

a/ A second order low-pass filter can be obtained with $\frac{Vo}{V_1}$ if $V_2=V_3=0$ (grounded).

$$\frac{Vo}{V_1} = \frac{G_1 G_3}{s^2 C_2 C_1 + s G_2 C_1 + G_1 G_3} \qquad (3.10)$$

$$f = \frac{1}{2\pi\sqrt{C1C2R1R3}} \qquad (3.11)$$

$$QUALITY\_FACTOR = Q = R2\sqrt{\frac{C2}{C1R1R3}} \qquad (3.12)$$

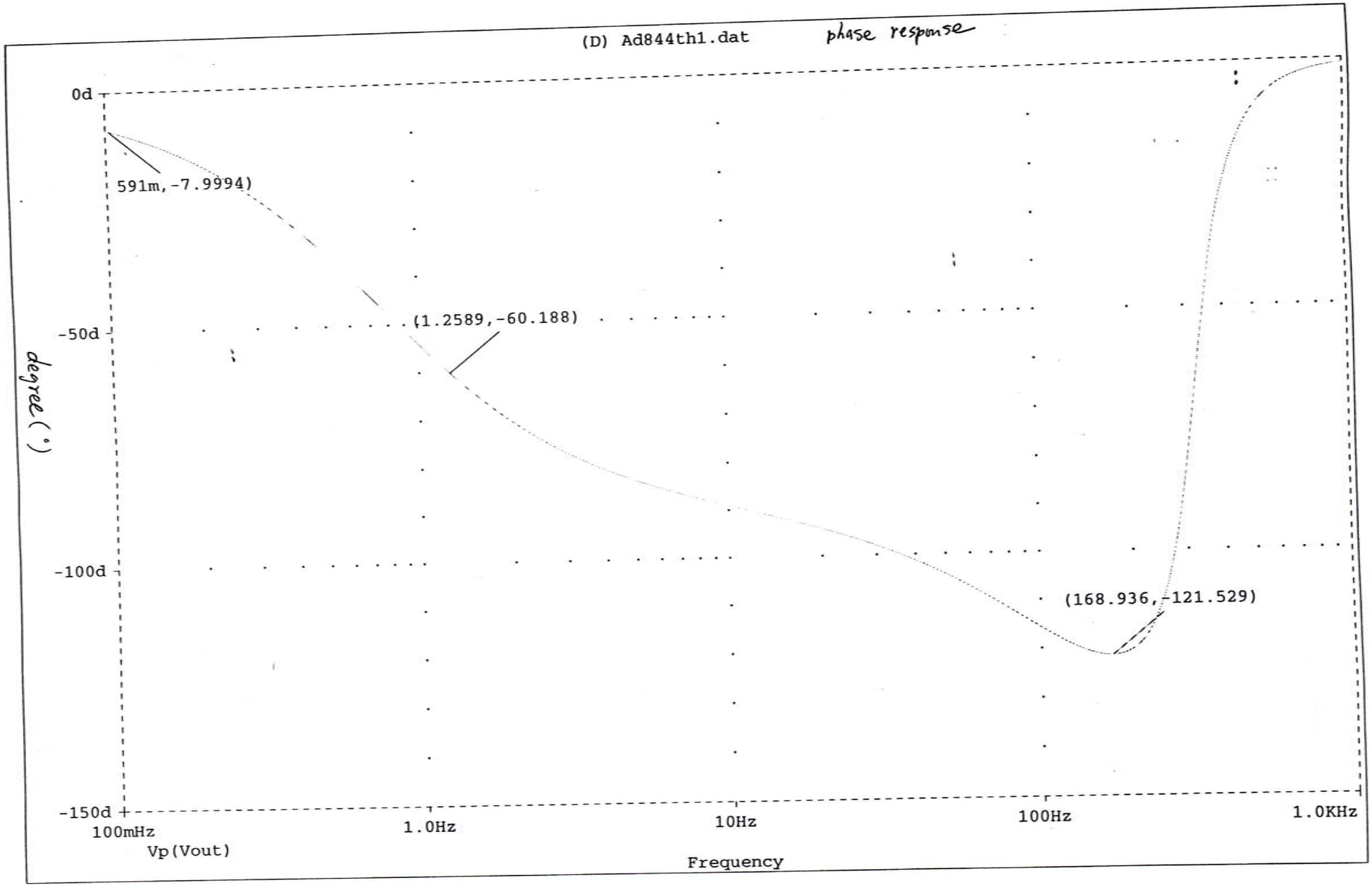
For example:

R1=R3=16k, C1=C2=10uF, R2=1100,

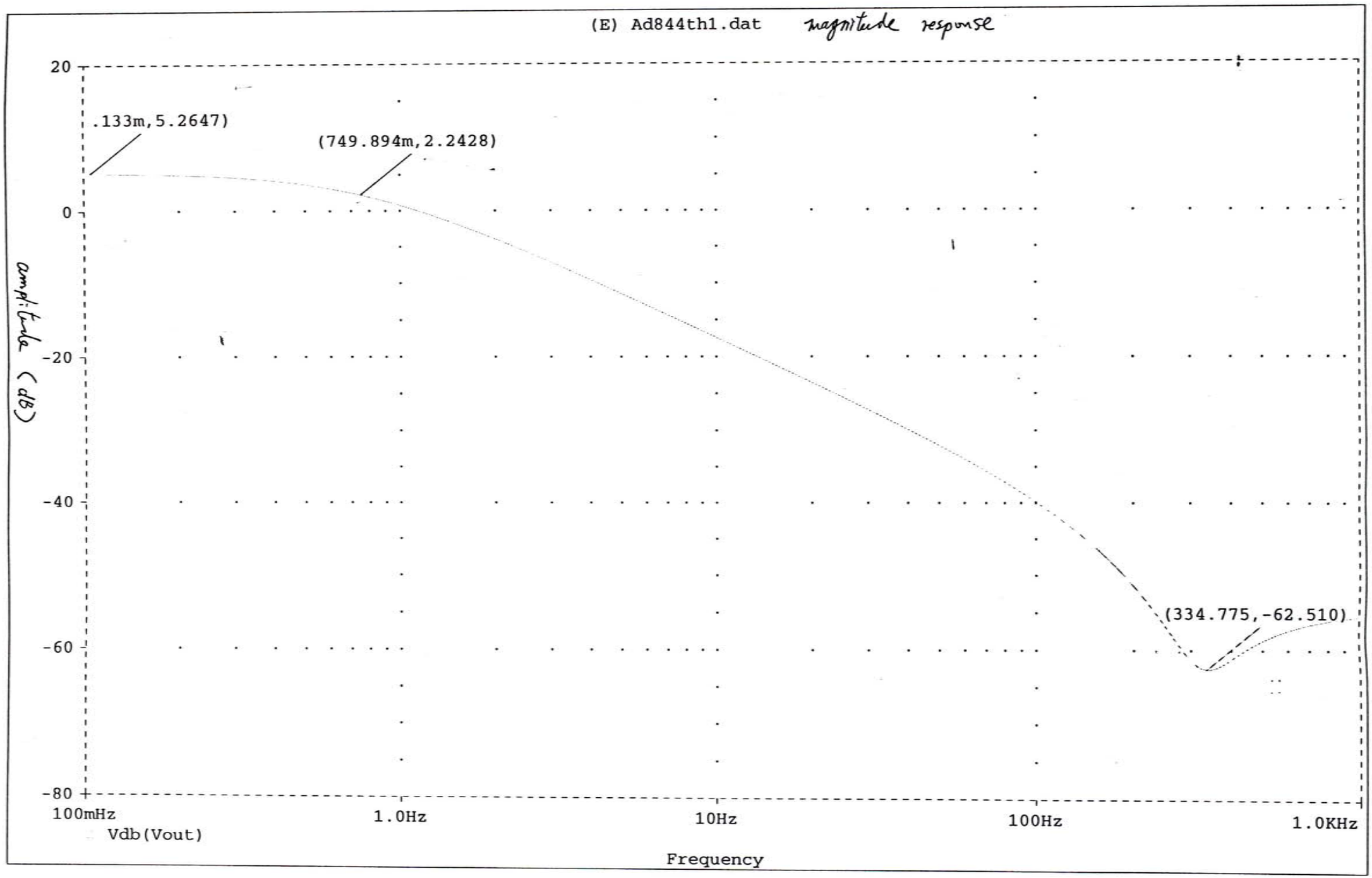
the cut-off frequency is 0.9947Hz

and the quality factor is 0.06875.

The computer simulation results are as follows. These results (-3dB cut-off frequency is 0.74989 Hz) are similar to the hand-calculation result.


(D) Ad844th1.dat
phase response
0d
-50d
-100d
-150d
591m,-7.9994)
(1.2589,-60.188)
(168.936,-121.529)
degree (°)
100mHz
1.0Hz
10Hz
100Hz
1.0KHz
Vp(Vout)
Frequency

61


(E) Ad844th1.dat
magnitude response
20
0
-20
-40
-60
-80
.133m,5.2647)
(749.894m,2.2428)
(334.775,-62.510)
amplitude (dB)
100mHz
1.0Hz
10Hz
100Hz
1.0KHz
Vdb(Vout)
Frequency

62

5. For the external divide-by N counter

a/ For divide-by 256, using 74AC393, or 74HC590.

b/ For divide-by 384, using 74HC590 plus 74F163 or 74AC112 plus 74AC393.

The below circuits show the divide-by 256 and 384 counter connection.

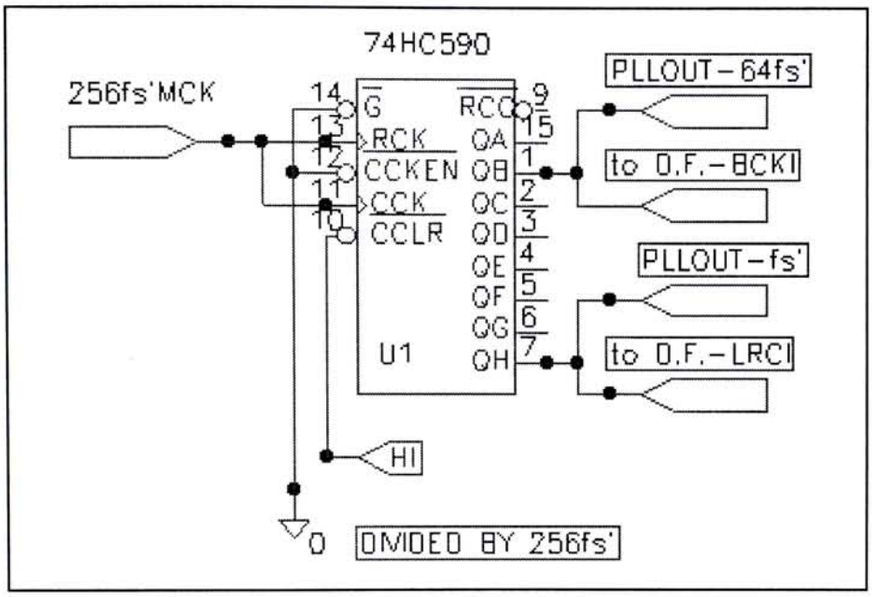


Fig.3.15 Divided by 256 counter connection circuit

The input frequency $256f_s$'MCK is divided by the 74HC590 256 times to get the $1f_s$'and $64f_s$'.

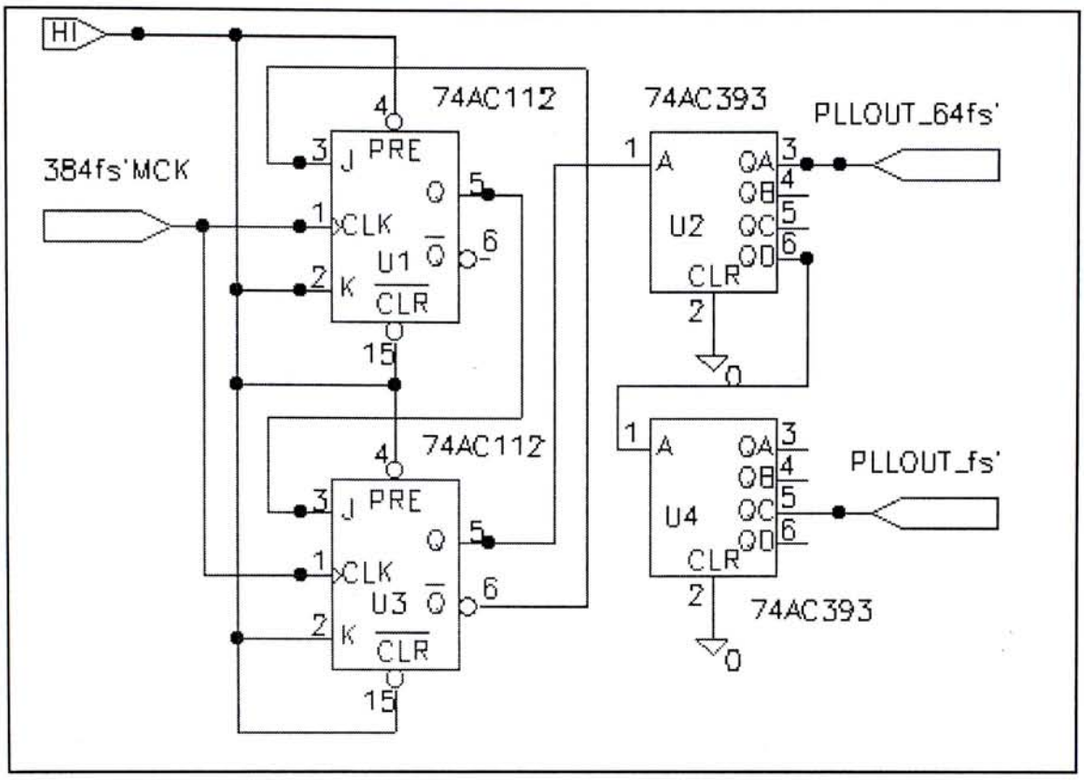


Fig.3.16 Divided by 384 counter connection circuit (1)

The input frequency $384f_s$'MCK is divided by the 74AC112 3 times to get the 128 f_s'and then its output is divided by the 74AC393 128 times.

3.5 Different arrangement of the all digital phase-Locked Loop (ADPLL) with 74ACT297 and the analogue phase-Locked Loop (APLL) with M2SC18M432-D300 as a VCO are listed for comparison:

		ADPLL	APLL
1.	PLL circuit components	ACT297----Pd, external divide-by N counter and external discrete oscillator as a digital VCO.	74HC4046 or AD9901----Pd, M2SC12M288-D300 for 256 fs, M2SC18M432-D300 for 384 fs---- analog VCO, plus external divide-by N counter
2.	Frequency compensation	All digital design avoid compensation	Require analog compensation
3.	Frequency tuning step	discrete	continuous
4.	PLL order	Can be cascadable for higher order	High order PLL create complex design problem [6]
5.	Locking frequency	DC to 17.5MHz (typ.) for HCT 297; DC to 35MHz (typ.) for ACT 297	Cannot lock to DC 19MHz (typ.) /21MHz for 74HC4046, 200MHz for AD9901 with no Dead Zone (undetectable phase difference range which results in increased jitter)[12,13].

6.	Frequency voltage stability $\Delta f (V_{CC})$	Depend on the power supply design, can be achieve 0.6-1000ppm (usually is 50ppm)	for M2SC18M432-D300.is +/- 100ppm , the typical value of VCXO is 20-30ppm.
7.	Frequency temperature stability $\Delta f (T_a)$	Depend on the crystal specification and the temperature compensated circuit, can be achieve < 2-1000ppm (usually is 50ppm)	for M2SC18M432-D300 is +/- 500ppm, the typical value of VCXO is 20-30ppm.
8.	Initial lock-on time	Very fast (for N=256, **923.888μs**/ cycles)	Longer than the ADPLL
9.	Power supply effect	Not effected by V_{cc} and temperature variations but depends solely on accuracies of the K-clock, I/D-clock and loop propagation delays.	A PLL contains analog components, which may be sensitive to noise generated by digital components. When the outputs of high-speed digital components switch, they may generated voltage fluctuations on the board's'' power and ground planes. While this poses no problem to digital components as long as the fluctuation is within the digital noise margin, any voltage fluctuation may affect the operation of an analog component. Also the phase noise of the VCO must be very low for jitter reduction circuit

10.	Feature a/	Very narrow lock range can be achieve≤ 1.314mHz for 44.1kHz , practically.	Very difficult to get the narrow cut-off frequency range ~ 3Hz
	b/	Can incorporate ripple cancellation circuit to minimize ripple	Cannot incorporate ripple cancellation circuit
	c/	By setting the very low cut-off frequency ≤ 1.314mHz to eliminate the extrinsic jitter and low frequency jitter wander.	Difficult to design the cut-off frequency < 0.5Hz but can be used higher order loop filter to get the deep attenuation but suffer from the gain peak problem [6].
	d/	Need power on **reset**	No need to reset
	e/	The lock range can be ***dynamically*** change	Difficult to change the lock range

3.6 Discrete transistor oscillator

Discrete transistor oscillator circuit using **Colpitts**-transistor [27] is in parallel-resonant mode. It has the advantage over the **Pierce**-transistor that is in series-resonant mode for multi-frequency circuit. Note: CMOS oscillator normally uses the Pierce oscillator circuit.

Phase noise from the **LC type oscillator** exhibits a higher level of sideband noise, extending out much further on either side [63].

Good crystal oscillator (for example: 20MHz) may show a level of sideband noise that is down to **-120dBc** at only **10Hz** offset from the carrier. Most crystal oscillators will achieve jitter less than **10 picoseconds** peak-to-peak if the noise of the oscillator power supply is low enough. It is usually advisable to decouple the oscillator with 10 ohms and a bypass capacitor.

For any VCO , **white noise** at the VCO input will modulates the VCO frequency and adds jitter to it [60].

For a white noise density of $\mathbf{e}_{n(\,vco\,)}$, k is given by

$$k_{vco} = \frac{1}{\sqrt{2}} \bullet K_o \bullet \frac{1}{\omega o} \bullet e_{n(vco)} \qquad (3.15)$$

where $\mathbf{K}_0$ is the VCO scale factor [rad / V . sec] and ω_0 is the VCO center frequency [rad /. sec].

3.7 Discrete transistor oscillator circuit operation

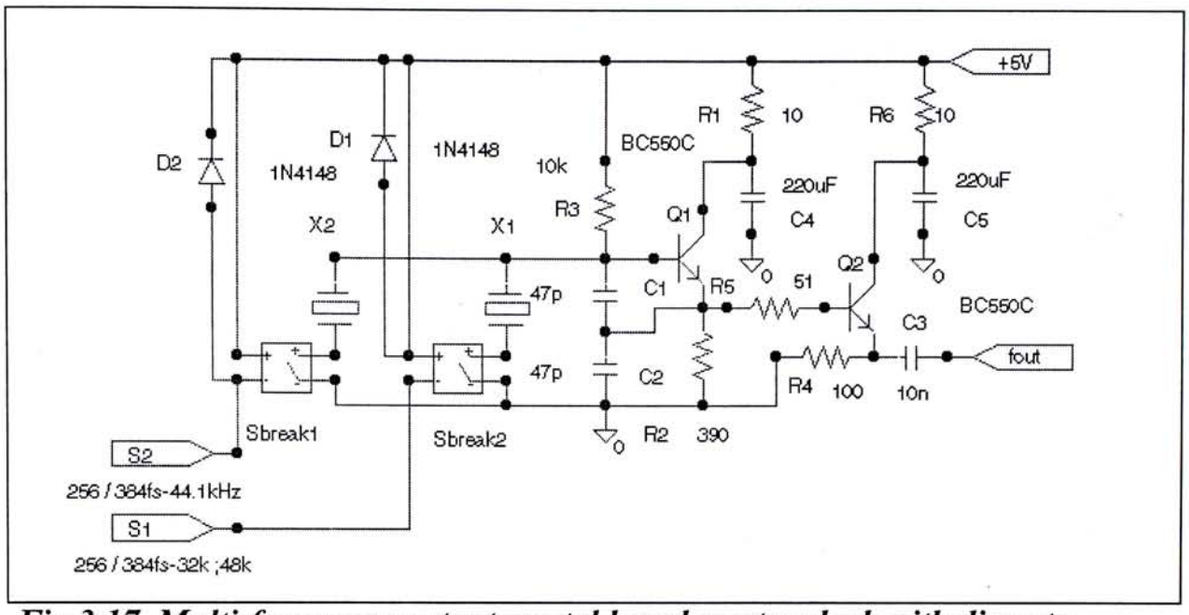


Fig.3.17 Multi-frequency output crystal based master clock with discrete transistor circuit diagram.

The operation of the above circuit is given below:

Q1 is the Colpitts-transistor oscillator circuit element and Q2 is the output buffer. C1 should be fixed within 1pF to 100pF. The oscillation frequency is very sensitive to the value of C1 but not to C2. The time constant R2C2 should be inversely proportion to the oscillation frequency

$$R2 \bullet C2 \approx 0.5 \bullet \frac{1}{fo} . \qquad (3.16)$$

The ratio of C1 to C2 is not critical but usually the value of C2 is about 5 ~ 10 time of C1. S1 and S2 are used to select the output frequency of this oscillator (f_{out}) where the Sbreak1 and Sbreak2 are the relays. They can be SPST or DPST. C3 serves as an ac-couple between the discrete transistor oscillator circuit and outside circuit in order to avoid the baseline wander. R1-C4 and the R6-C5 are the power supply low-pass filter. D1 and D2 discharge the reverse dV/dt voltage generate by the relay coils during the switching transient.

Design of the bench work sample one is shown on the below table. The value of X1 is 22.5796MHz and the value of X2 is 33. The f_{out} signal amplitude is 0v and 2.5 voltages. Therefore, the fout must be added most stage i.e. the use of

Smith trigger (74ACT14) circuit is to increase the voltage output level to +5 voltages.

Design of the bench work sample two is shown on the below table. The f_{out} signal amplitude is 0v and 5 voltages.

	Sample 1	Sample 2
supple voltage (V)	+5	+12
C1 (pF)	5	47
C2 (pF)	47	47
R2 (ohms)	390	470
R3 (ohms)	10k	20k
R4 (ohms)	390	390
R5 (ohms)	51	51
Output voltage (v)	0-2.5	0-5

For higher performance, the master clock f_{out} must be connected to the high speed voltage comparator to square up the f_{out} [23].

Further enhancement uses technique that described below [22]. Critical clock source f_{out} passes through the narrow band-pass filter with high Q characteristic to generate the pure sine wave and then using fast, low jitter comparator chip (**AD9696KN or LT1016**) or high speed TTL logic or high speed CMOS logic or ECL logic for example the ECL to TTL translator **10124** or **10125** to square up the pure sine wave. Therefore, the $\mathbf{f_{out}}$ will have a **50% duty cycle** characteristic provided that the band-pass filter has high Q characteristic.

The experimental result is shown in Fig.3.10.

3.8

The advantage and disadvantage of using external discrete oscillator

Advantage of using external discrete oscillator:

1. the parameters of source and load resistance, gain and amplitude of the crystal, can be controlled,
2. the precise frequency stability can be controlled,
3. delay time is shorter because the oscillator circuit uses one or two transistors only and low power dissipation is due to shorter delay time[26],
4. frequency sensitivity to power supply voltage changes is reduced since most of the CMOS-IC's have higher sensitivity to power supply regulation than the transistor circuit,
5. short-term stability can be up to **+/- 0.1ppm**,
6. lower phase noise than the CMOS oscillator circuits [24].

Disadvantage of using external discrete oscillator**:**

1. frequency shifting with temperature changes,
2. high-gain transistor should be used to get higher input impedance at the transistor base input terminal so as to minimize crystal loading effect by the transistor,
3. voltage swing across the crystal is large large (from +5 to -1Vdc) [24].

3.9 Background of using high-precision oscillators

The accuracy of frequency and time-interval of phase-locked loop circuit vitally depends on the time base or reference element selected (capacitor and resistor). There are three types of oscillators that are usually used in the high-precision application:

1. **RTXO**: Room-temperature crystal oscillators are designed for minimum frequency-change over a change in temperature.
2. **TCXO**: Temperature-compensated crystal oscillators use external components to offset temperature effects. TCXO time base have temperature characteristics which are typically five times better than an RTXO (5×10^{-7} for a **0° to 50°C** change).
3. **OTBXO**: Oven time base-compensated oscillators have crystal and temperature-sensitive elements enclosed within a temperature-controlled environment. A heating element maintains a constant temperature, The best stability is achieved when the operation point is **15° to 20°** above the highest temperature to which the unit will be exposed. After warm-up, the frequency remains very stable, typically $< 7 \times 10^{-9}$ over a **0° to 50°C** variation.

3.9.1 The temperature compensated circuit for crystal oscillator operation

In this thesis we propose the use of the temperature compensated circuit for crystal oscillatoar by hardware circuit design in the circuit level. The temperature compensated crystal circuit diagram is shown in Fig 3.18 and the operation is described below.

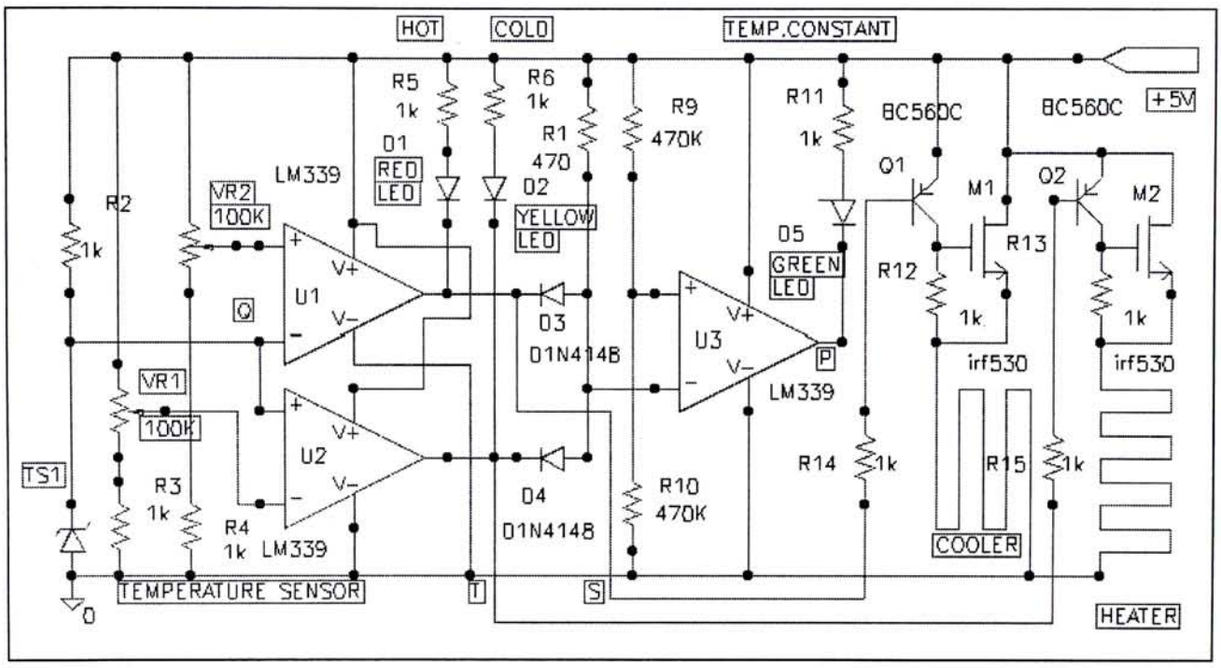


Fig.3.18 Temperature compensation circuit diagram

The small size temperature sensor employ IC LM45B or LM56B [28 to 31] for highly linear output. U1, U2 and U3 are the window comparators to compare the temperature sensor voltage output with the temperature set by the variable resistor VR1 and VR2.

D1 , D2 and D5 are the LEDs to indicate the circuit temperature state. Q1, M1 and the load----semiconductor thermo-electric device [32] are for cooling the crystal and the Q2 . The surface of M2 serves as a heater element for heating the crystal.

If the voltage at point Q goes lower than that preset by the VR1, the output of U2 goes low , then the yellow light emitting diode D2 will be turned on, indicating a bath that is too cold.

If the voltage at point Q goes above that preset by VR2, the output of U1 goes low and red LED D1 will be turned on, indicating a bath that is too hot.

For input voltages between these limits both U1 and U2 outputs will be high . Diode D3 and D4 will then be turned off and the inverted input to U3 will be pulled above the half power supply voltage (i.e. 2.5 V) appeared on the non-inverting input; the green LED D5 is turned on, indicating a bath that is at the correct temperature.

		$V_Q < V_{VR1}$	$V_Q > V_{VR2}$	$V_{VR2} < V_Q < V_{VR1}$
1.	V_{u1}	High	Low	High
2.	V_{u2}	Low	High	High
3.	V_Q	High	High	Low
4.	Led	yellow LED D2 turn on indicating in cold condition	Red Led D1 turn on indicating in hot condition	Green Led D5 turn on indicating in balance condition

Note:

1.V_Q is the voltage at point Q

2.V_{u1} is the voltage output of the comparator U1

3.V_{u2} is the voltage output of the comparator U2

4.V_{VR1} the voltage at VR1

5.V_{VR2} the voltage at VR2

To calibrate the temperature chamber, the lower and upper temperature limits are selected , for example from 32°C to 36 °C . Measuring the voltage at point Q when the temperature sensor is in water at a temperature corresponding to the lowest limit, say 32°C . The voltage at point Q is noted, then adjust the preset VR1 anti-clockwise until the voltage measured at pin 6 of the Op-amp U2 has the same value. When the temperature is raised to the upper limit, say 36 °C, the voltage at point Q is again noted and this value is estabished on pin 5 of Op-amp U1 by adjustment anti-clockwise of VR2.

These measurements must be made with a high impedance digital voltmeter, an analogue instrument will almost certainly be unsuitable.

3.9.2 The temperature compensated circuit design notes:

1. Thermo-electric device (using the **Peltier effect**) , when supplied with a suitable electric current, can cool down or heat up the crystal. In this circuit its function is to keep the crystal cool.
2. Because the crystal used in this circuit Fig.3. is AT cut , which has the cubic or S-shaped frequency variation with temperature . The more stable region at low temperature is around **5 °C to -20°C** and at high temperature it is around **75 °C** (depend on the angle of cut) [31]. For the AT cut crystal , the point of inflection occurs at around **27°C to 31°C**. But for the strain compensated cut (**SC cut**) , it offers improved resistance to shock and superior aging effect but exhibits more spurious resonance .
3. For the **AT cut** crystal , its has the sensitive characteristic with the *mechanical vibration* .
4. Another simple design of the oven control circuit can be found in [28].

3.10 The discrete voltage reference circuit operation

In this thesis we propose the use of the discrete ultra-low noise, low temperature offset< 30ppm, voltage reference circuit design diagram is shown in Fig 3.19 and the operation is described below..

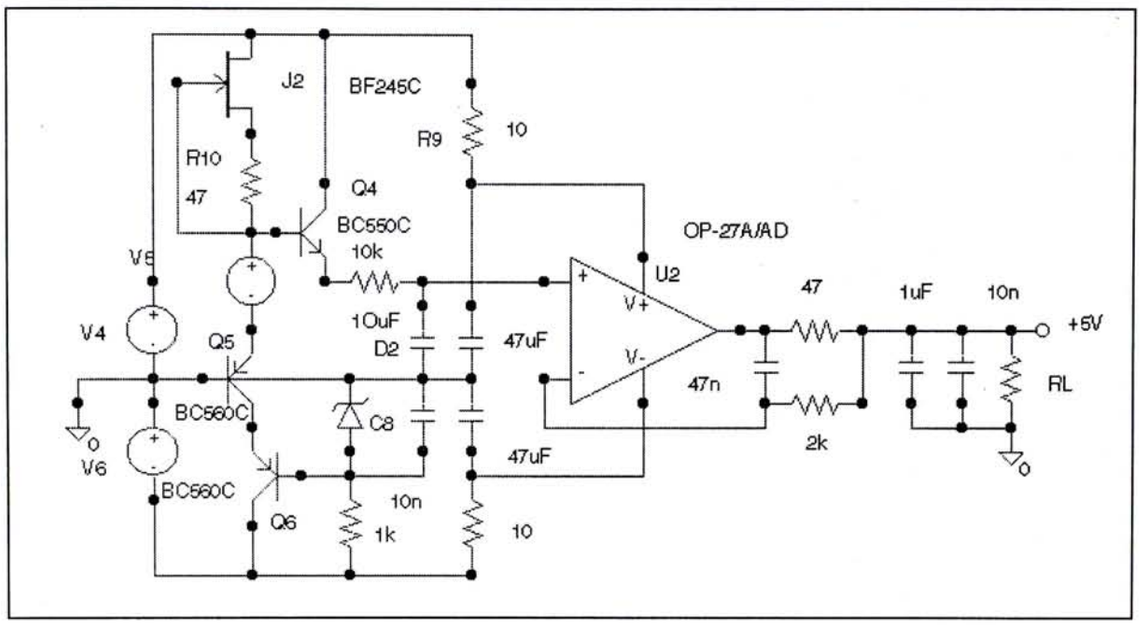


Fig.3.19 Discrete ultra-low noise, low temperature offset < 30ppm, differential voltage reference circuit diagram.

V4 and V6 are the input supply unregulated rail voltages. Jfet J2 is the current source to bias the voltage reference V_{ref} [39 , 40 , 41]. The choice of voltage reference mainly depends on the cost against the performance. Q4 is the voltage reference buffer which is temperature compensated by Q5. D2 is a zener to fix the Q5 Vce voltage to above 2.1V and C8 is used to bypass the noise generated by the zener. Q5 is used to bypass the positive power supply current (Iref.) and source major current ($i_C=\beta$ X Iref) to the negative power supply. That means the β **X Iref** current draw from the negative power supply. β is the current gain of Q5 . Q6 forms the **cascode** transistor pairs with Q5 to minimize the **Miller effect**. Therefore, the noise current from the ground to the voltage reference Vref will be divided-by the current gain (β) of Q5. This is the ***ground noise current bypass technique*** with the additional negative power supply.

The advantage of the circuit shown in Fig.3.19 is that *low dc errors is obtained due to the capacitor leakage is minimum.*

The negative power supply of the U2 can be connected to negative power supply rail or power ground. Load resistor RL biases U2 to Class A operation (around 5mA) and keeps the output resistance more constant. The voltage reference bypass capacitor is set at about 1uF and it must have low leakage current and ultra low impedance at high frequency [34,35].

The output of the voltage references shown in Fig.3.20 is connected to the current feedback Op-amps' (for example **AD811** or **AD844**) non-inverted inputs and the outputs of which are connected to the inverted inputs through 470 ohms resistor. The output of each current feedback Op-amps must be connected to an isolated resistor (0.1 ohms to 47 ohms) in order to isolate the capacitive loads, all major power supply sensitive ICs, (e.g. the PLL circuit (VCO)), master clock circuit (fig.3.17) , digital interface IC, digital filter chips and the DAC. Current feedback Op-amp is used to isolate the voltage reference and the load which provides faster or dynamic current to the load.

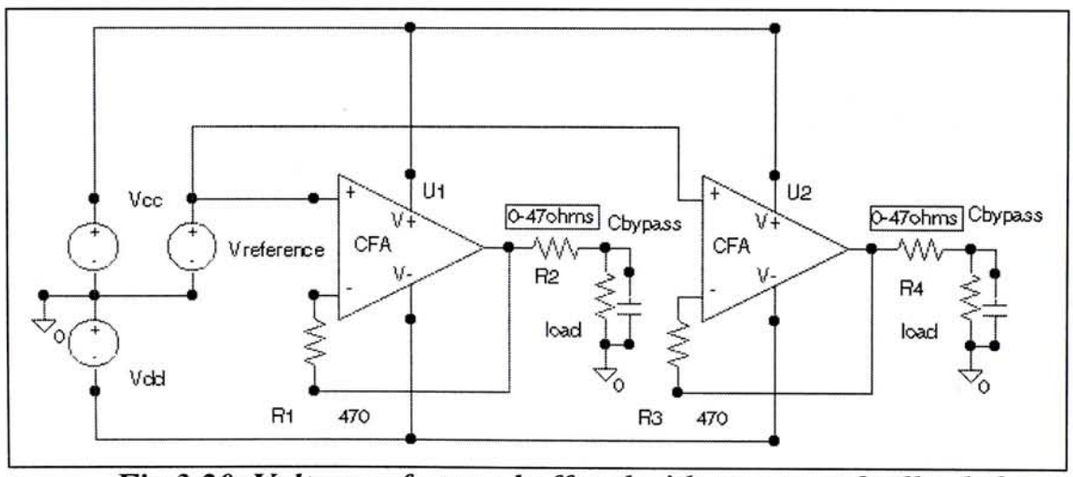


Fig.3.20. Voltage reference buffered with a current feedback Op-amps for multi-power supply.

Another analog power supply circuit design for DAC can be found in [33].

The layout technique of the power supply and the power supply bypass can be found in [37,38].

3.10.1 Comparing the different types of Op-amps that can be used as a voltage comparator:

Different types of high performance Op-amp that used in U2 of Fig.3.19 are listed below for ease of comparison.

		AD797BN	OP27AJ	OP177AJ
1.	input offset voltage max.(μV)	60	25	10
2.	input voltage noise 0.1 Hz to 10Hz (nV p-p)	50	180	424
3.	input voltage noise 10 Hz to 1MHz (μV rms.)	1.2		
4.	CMMR min.(dB)	114	114	130
5.	PSSR min.(dB)	114	100	120
6.	output current min.(mA)	30	30	22.5
7.	supply current max.-no load.(mA)	10.5	9.3	2
8.	Gain bandwidth product (MHz)	80	8	0.4

3.10.2 Precaution of separate CMOS chips Vdd and Vcc

A CMOS chip usually has two power supply connections: digital V_{dd} and analog V_{cc} . If separate power supplies are used, there is a possibility of a latch-up condition when the power supplies are turned on at different times,. To avoid this problem, the analog power supply and digital power supply must be connected with two back to back switching diodes (Fig 3.21.).

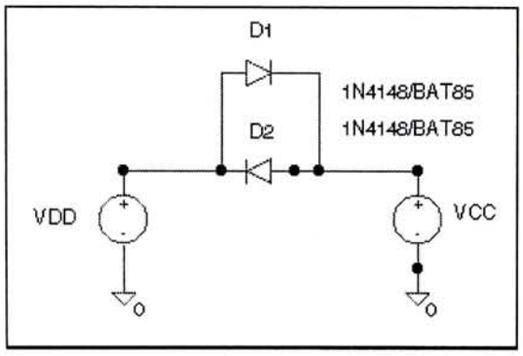


Fig.3.21. Avoid CMOS latch up circuit connection diagram

3.11 Board level jitter reduction method

Jitter can be reduced by better layout and a better noise decoupling scheme. For example, the passage of high frequency signals over short transmission lines (e.g.: PCB traces) will not generate jitter. However, the emissions and cross-talk triggered by such signals do contribute to a lot of noise, which ultimately gets injected into the receivers and the transmitters of the same board and causes jitter. The key to reducing emissions and cross-talk is to lay out high-speed traces with a *constant impedance* across their lengths.

Wide traces **(>10mil)** are recommended because the variations in line width caused by etching errors and bending will have less impact than thiner ones. Greater distance between neighboring traces and between a trace and a board edge is also recommended.

3.12 Digital audio interface chips

The function of digital audio interface transmitter chip (DIT) (i.e.: CS8401, CS8402 and YM3437) is to encode and transmit audio data according to the AES / EBU, IEC 958, S / PDIF and EIAJ CP-340 interface standards.

Digital audio interface receiver chips (DIR) (i.e.: CS8412, CS8414 , AES20, AES21, YM3623 and YM3436D) have the following characteristics for clock-data recovery [65]:

1. Lock quickly onto an input signal.
2. Track frequency variations.
3. Operate at multiple frequencies.
4. Recover data and clock signal over wide dynamic range.
5. Recover data correctly in the presence of jitter.
6. Hysteresis in data recovery.
7. Produce high-frequency master clock ($256f_s$ or $384f_s$) .

Commercially available low jitter clock specification is that typical low jitter slaving clock Apogee CC768 have output jitter < 30ps rms. (typ.) and < 100ps peak to peak (typ.).

The latest digital audio interface chip (**CS4224/6**) use the following method for reducing **data dependent jitter**. Please refer to the data sheet of CS4224/6 and Chapter 7.1.4 to get more detail information.

The receiver frequency and phase locking is accomplished by using timing cues derived from the preamble (a timing reference for synchronizing the PLL) preceding the **Z preamble** (please refer to Chapter 7.1.4 to get more detail information.) or **channel " B " data frames**. These occur at the input word rate (IWR) between 32kHz to 50 kHz. The Z preamble occurs once every 192 frames in place of the X preamble in order to mark the beginning of a new channel status block. Since this edge is quite distant in time from any data dependent edges, this method greatly reduces susceptibility to inter-symbol interference which can result in data-dependent clock jitter [64]. Usually, each preamble has two bit boundaries with no transition which enables the receiver to recognize the data as a preamble.

Further reduction of jitter may be achieved through a two-stage PLL. The first or one stage PLL is inside the DIR. chip and the second or two stage PLL is an addition circuit that added externally either in the form of analog PLL or ADPLL.

3.12.1 Different brand of the digital interface receiver (DIR) chips and clock modular are listed for comparison:

	CS8412-CP/ CS8414-CP	AES 20 / AES 21	TDA1373H	CC768
Branch name	crystal semiconductor	Ultra-analogue	Philips	Apogee
Function	DIR	DIR	DIR + sampling rate converter	low jitter slaving clock
Output jitter (ps)	200 rms.	40 rms. Per 1/3-octave bandwidth	no specific	<30 rms. (typ.), < 100p-p (typ.)
jitter attenuation (dB)	25kHz at 100Hz (typ.) 55 at 1kHz (typ.) >80 at 20kHz (typ.)			15 at 100Hz (typ) 55 at 1kHz (typ) >80 at 20kHz (typ)
pull-in time (30-54kHz)				0.7
pull-in range (kHz)				30-54
tracking rate (kHz/sec)				36
VCO freq. Range (MHz)				23-42

Chaper 4

4. APPLICATION CIRCUIT BLOCK DIAGRAMS OF JITTER REDUCTION AND CLOCK RECOVERY

Block diagram 4.1 and 4.2 are for the outboard digital-to-analogue converter's circuit design. DIR's Fsync pin is used as a PLL input reference for both block diagrams.

The different is that the block diagram 4.1 use the **Fsync'** pin and **Sck'** pin of 2nd PLL to the digital filter chips but block diagram 4.2 use the Fsync pin and Sck pin of the DIR. chip to the digital filter chips.

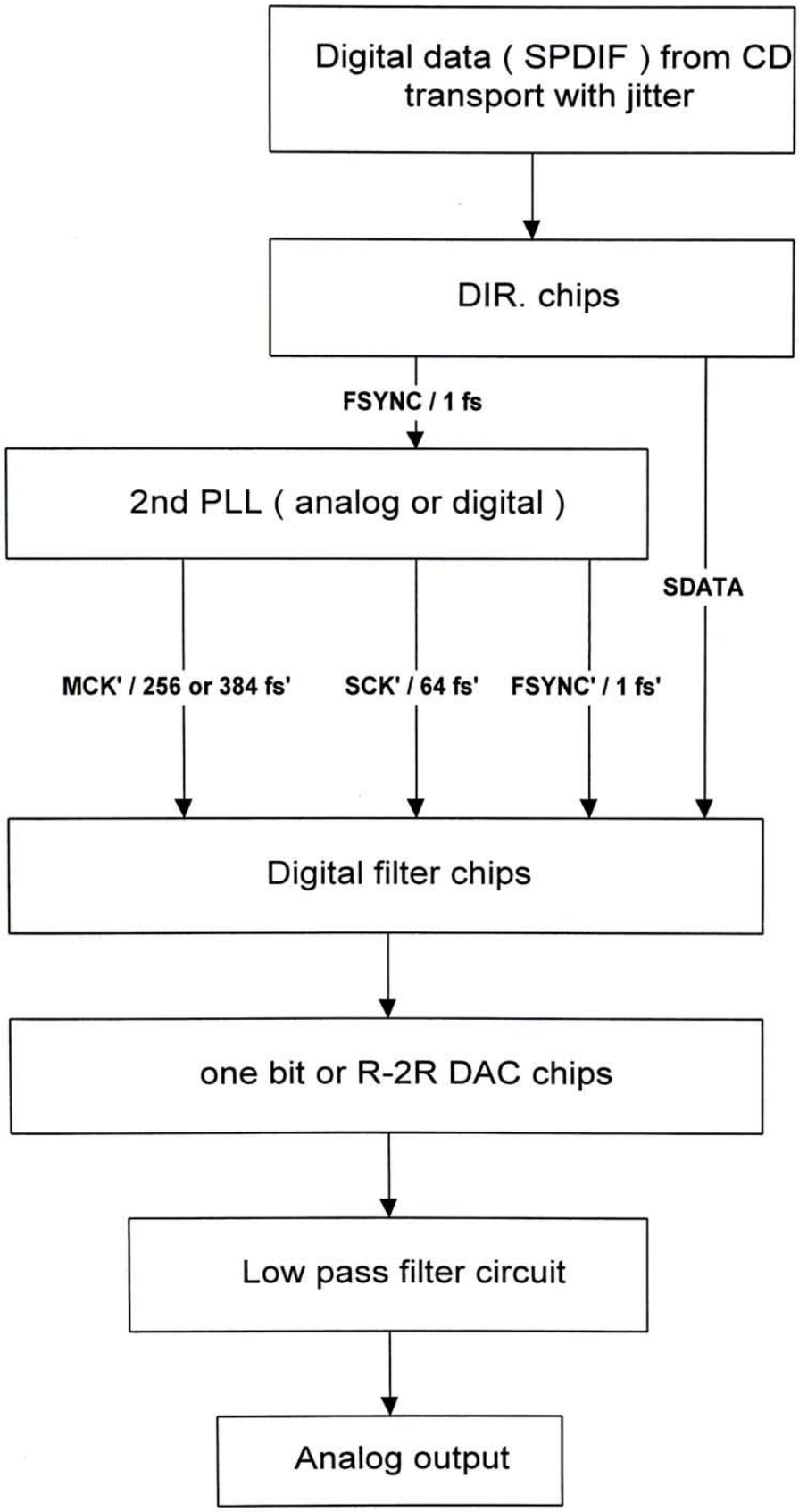
The block diagram 4.1 design idea comes from a Japanese digital audio designer. And the block diagram 4.2 design idea comes from a Crystal semiconductor digital audio designer [65].

Block diagram 4.3 and 4.4 are for the outboard digital-to-digital jitter reduction unit's circuit design DIR's F_{sync} pin is used as a PLL input reference for both block diagram.

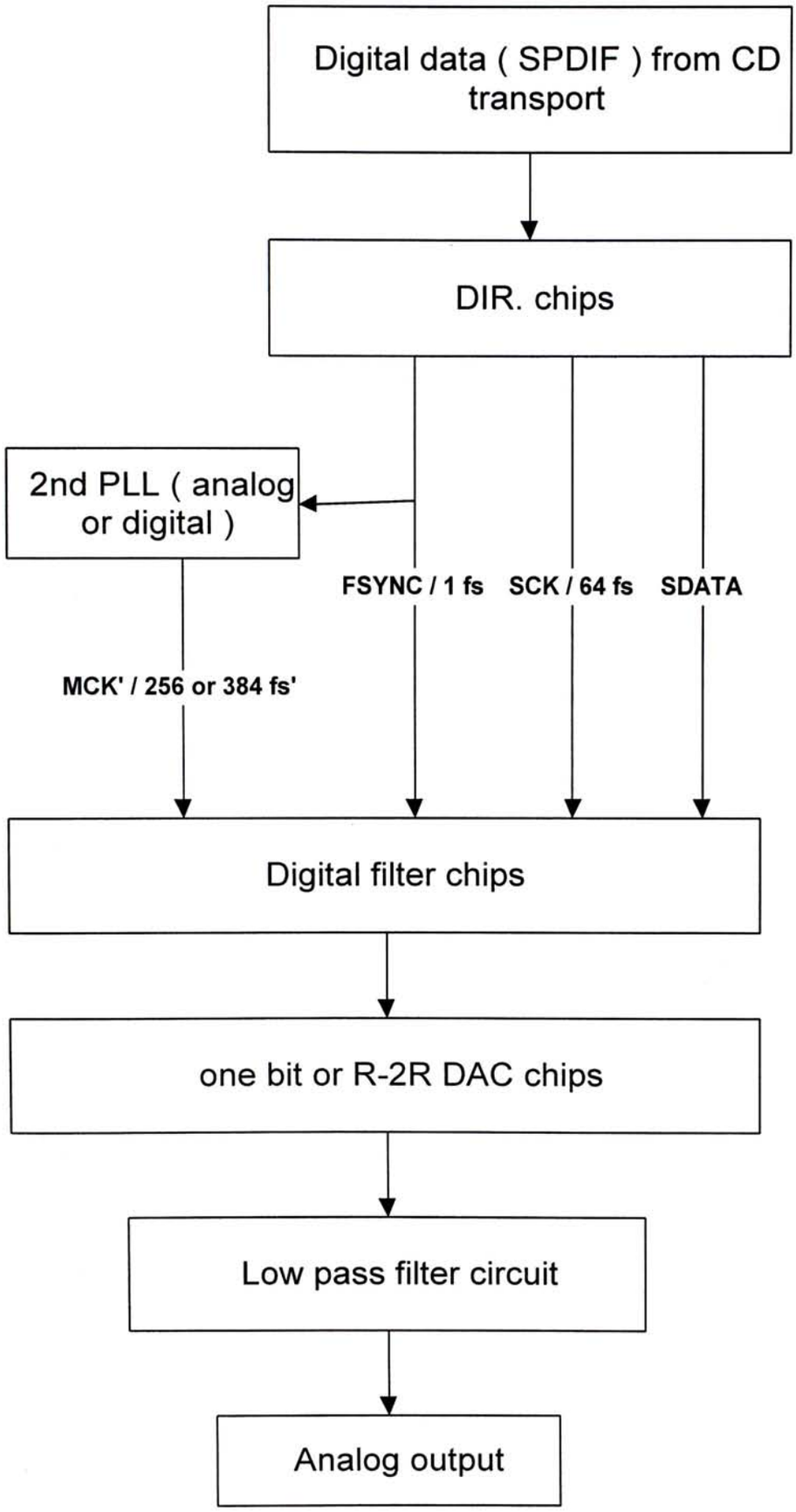
The different is that the block diagram 4.3 use the **F_{sync}'** pin and **S_{ck}'** pin of 2nd PLL to the digital filter chips but block diagram 4.4 use the Fsync pin and S_{ck} pin of the DIR. chip to the digital filter chips.

The block diagram 4.3 design idea comes from a Japanese digital audio designer. And the block diagram 4.4 design idea come from a Crystal semiconductor digital audio designer [65].

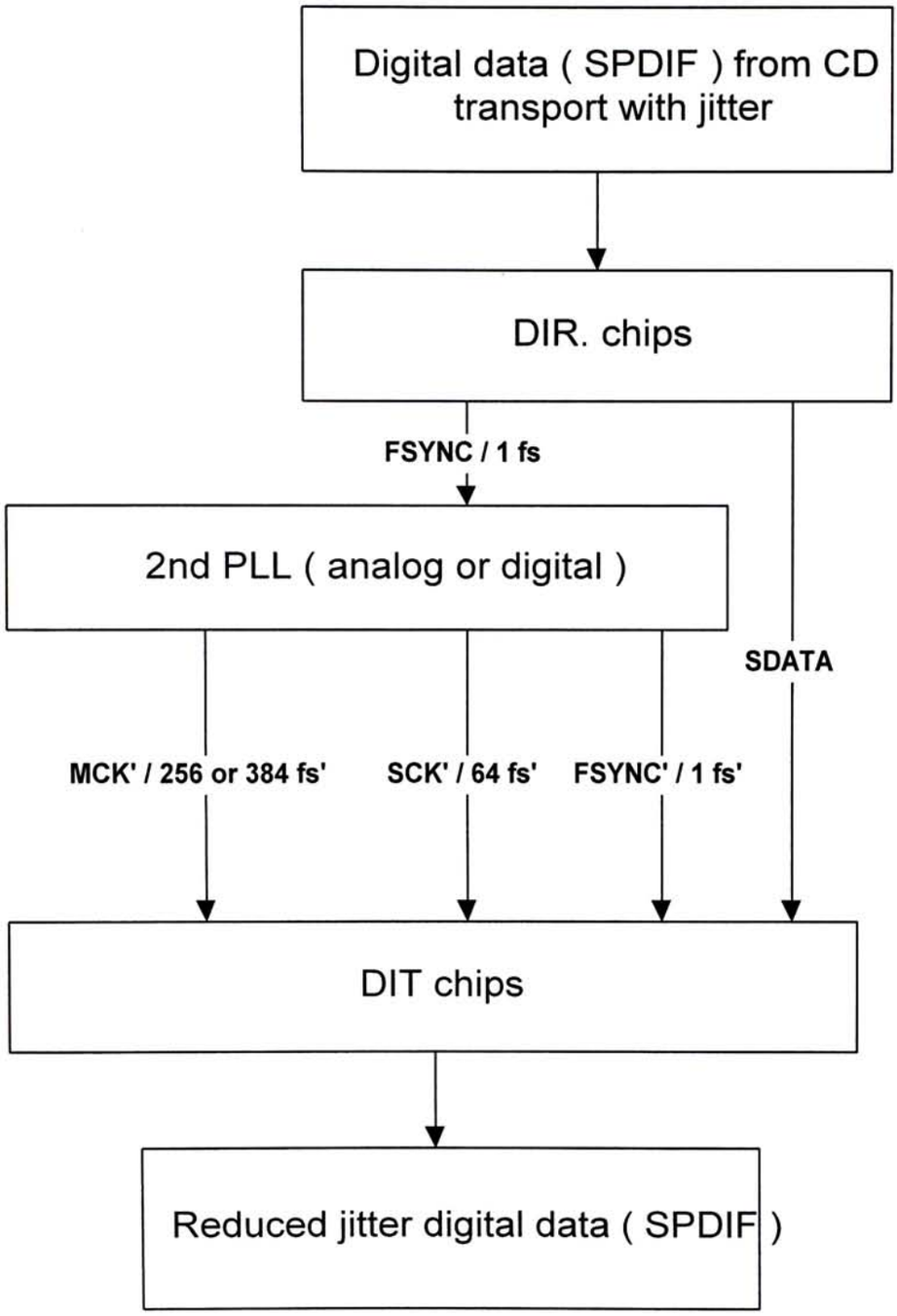
4.1 SECONDARY PLL APPLICATION CIRCUIT BLOCK DIAGRAMS



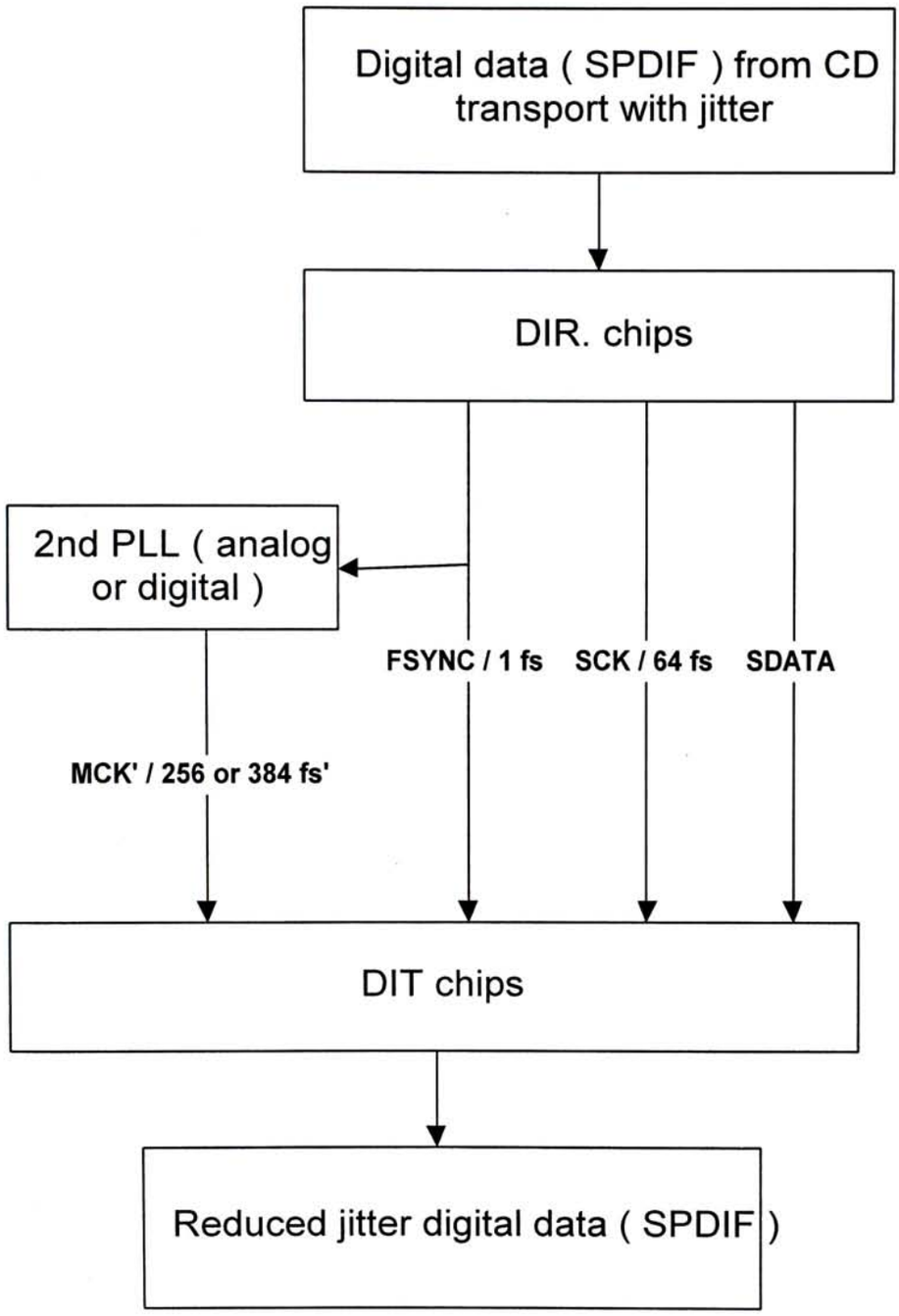
4.2 SECONDARY PLL APPLICATION CIRCUIT BLOCK DIAGRAMS



4.3 SECONDARY PLL APPLICATION CIRCUIT BLOCK DIAGRAMS



4.4 SECONDARY PLL APPLICATION CIRCUIT BLOCK DIAGRAMS



Chaper 5

5. CONCLUSIONS

5.1 Summary of the research

Jitter reduction is very important in digital audio. In this thesis we have investigated various methods for jitter reduction. The main contributions, together with the corresponding publication, of this thesis are summarized as follows:

We have addressed three aspects of jitter: what the jitter is , why jitter occurs in digital audio and jitter reduction techniques in the hardware circuit design level.

In Chapter 1, we have described what is the jitter and its characteristics. We have also clearly defined the jitter and wander.

In Chapter 2, we have described and studied the cause and effect of jitter in digital audio and proposed various methods for jitter reduction. For example, in Section 2.3, the proposed method can reduce the settling time from 10ns into 9.09ps in theory and from 35ns into 25ns in practice.

In Chapter 3, we have investigated and proposed various methods for jitter reduction by the hardware circuit design.

A proposed all digital phase locked loop (ADPLL) circuit, which is the first one to use this circuit design in this application, which incorporates with the digital audio interface chip to reduce the jitter, has been implemented. For all digital phase locked loop circuit, it is proved work by computer simulation. With this circuit, experiments were successfully carried out to measure the clock jitter spectrum in the digital audio interface chips and ADPLL circuit. But sadly speaking, the performance is not as good as the analogue PLL circuit due to the limitation of the ADPLL circuit's phase resolution.

It has been shown that using the all digital phase-locked loop (ADPLL) circuit can reduce the jitter and / or wander significantly. This is because the ADPLL can set the cut-off frequency or locked range extremely low (i.e.: locked range $\leq$ 1.314mHz for 44.1kHz in theoretical). This locked range is difficult to achieve in the analogue phase-locked (APLL) loop circuit due to very long initial lock-on time.

We have also made circuit comparisons between the ADPLL and APLL. The frequency against voltage stability and frequency against temperature stability of APLL circuit are not better than that of the ADPLL circuit.

We have suggested that for further reduction of the jitter and / or wander in the digital audio chain, the power supply performance and the master clock quality must be considered, and the design of extremely stable discrete transistor oscillator circuit in order to minimize the master clock jitter level successfully, and the design of temperature compensated circuit for crystal oscillator in order to minimize the master clock temperature drift.

We have also studied the extremely stabled power supply circuit design to obtain better voltage regulation with a high performance Op-amp as a voltage comparator, and used current feedback Op-amp to provide dynamic current to the load. This circuit design is the first one to integrate all the best chips together in the digital audio application. But sadly speaking, the performance is not so good. It is because the voltage reference's temperature drift is not as good as the data sheet quoted. In practical measurement, we find that the voltage reference's temperature drift is out of specification which makes this circuit not fulfill the extremely low temperature drift requirement.

Jitter affects the reliability of data communication systems in unpredictable ways. Circuit designers have to be very careful to reduce all possible sources of jitter and be highly determined to eliminate them in the design stage but not in the debugging stage .

5.2 Suggestions for further development

Several methods for jitter reduction by the hardware circuit design have been investigated and studied in this thesis. They can be used for practical applications after further development.

Future work should be focused on improving the proposed circuit design. For the ADPLL circuit design: The phase resolution of the ADPLL must be improved to reduce the jitter level. The ADPLL circuit's locked range needs to be improved by setting of the digital ADPLL's K-clock frequency higher than that of the I/D clock. The ADPLL circuit's jitter suppression capability needs to be improved by the use of higher order digital ADPLLs circuit [11].

For the extremely stabled power supply circuit design: Further study of the temperature drift of the voltage reference must be done.

In addition, we also need further study in details about the *enclosure* and the *physical layout* of the circuits.

We believe that these jitter reduction techniques will become popular in the high-end internal or external Digital to Analog converter circuit , CD player , VCD player , LD player and DVD player after further refining the circuit design performance.

5.3 Instrument listing that used in this thesis

1. HP4396A network / spectrum analyzer 100k~1.8G, 2Hz~1.8G
2. HP5381A 80MHz frequency counter
3. TDS320 two channel oscilloscope 100Mhz 500Ms/s
4. COR5501U Kikusui digital oscilloscope 100Mhz
5. HM8130 Hameg programmable function generator
6. A2-D Neutrik audio measurement system
7. GPC-3030 GW dual tracking with 5V fixed power supply

Chaper 6

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Chaper 7

7 APPENDICES

cycle in an auxiliary counting decade, whereupon the information is transferred directly into the 'tens' stage of the main counter.

With more complicated recognition and presetting logic Frank [3.14] was able to reduce N_{min} to 3 without sacrificing the resolution capabilities of the counter on the one hand and still retaining slower flip-flops (power saving) at higher decimal places on the other hand.

3.6 PHASE INSTABILITY IN FREQUENCY DIVIDERS

The coherence condition requires that in any arbitrary time interval $(t - t_1)$ the number of input periods is N-times the number of output periods. Thus in the ideal case when neglecting the phase noise due to the dividing process

$$\frac{(1/2\pi)\,[\varphi_i(t) - \varphi_i(t_1)]}{(1/2\pi)\,[\varphi_0(t) - \varphi_0(t_1)]} = N \tag{3.10}$$

The above equation may be fulfilled for any arbitrary time interval $(t - t_1)$ only if

$$\varphi_0(t) = \frac{\varphi_i(t)}{N} \tag{3.11}$$

In the case of simple phase modulation of the input signal, (3.11) may be written as

$$\varphi_0(t) = \frac{\omega_i t + \Delta\varphi_i \sin \nu t}{N} \tag{3.12}$$

It is clear that the phase modulation index $\Delta\varphi_i$ is reduced in proportion to the division ratio N, but the modulation frequency remains unchanged. When differentiating (3.11) the same conclusion can also be drawn for the case of frequency modulation.

With a discrete spurious signal present at the input (with respective amplitudes $V_{sp} \ll V_i$) the resulting output phase modulation index is, according to (9.11) and (3.12),

$$\Delta\varphi_0 \approx \frac{1}{N} \cdot \frac{V_{sp}}{V_i} \tag{3.13}$$

In the case of narrow-band input noise eq. (9.12) gives for the input and output phase jitter

$$\varphi_{ni}(t) = \frac{n_s(t)}{V_i} \tag{3.14}$$

$$\varphi_{n0}(t) = \frac{\varphi_{ni}(t)}{N} = \frac{1}{N}\,\frac{n_s(t)}{V_i} \tag{3.15}$$

where $n_s(t)$ is the component of the noise voltage $n(t)$ which is in quadrature to the input signal.

The variance of (3.15) is

$$\overline{\varphi_{n0}^2(t)} = \frac{\overline{\varphi_{ni}^2(t)}}{N^2} = \frac{1}{N^2} \cdot \frac{\overline{n^2(t)}}{V_i^2} = \frac{1}{N^2}\,\frac{1}{2(\mathrm{SNR})_{in}} \tag{3.16}$$

If the frequency divider behaves as a perfect limiter it suppresses the amplitude noise completely and

$$(\mathrm{SNR})_{out} = 1/\overline{\varphi_{n0}^2(t)} = 2N^2(\mathrm{SNR})_{in} \tag{3.17}$$

or

$$(\mathrm{SNR})_{out} = (\mathrm{SNR})_{in} + 20 \log N + 3 \quad \text{(dB)} \tag{3.18a}$$

$$\approx \mathrm{SNR}_{in} + 20 \log N \quad \text{(dB)} \tag{3.18b}$$

In other words the ideal dividing process improves the signal-to-noise ratio by a factor $2N^2$ or approximately by $20 \log N$ (dB).

In actual dividing circuits the theoretical value given by (3.17) is not achieved because of the additive noise contributed by the dividing circuit itself.

(A) Regenerative Frequency Dividers

The output phase is given by (3.4)

$$\varphi_0 = \frac{\varphi_i + \varphi_a - \varphi_b}{N}$$

In a general case all the terms on the right-hand side are not constants and may contribute to additional output phase instability

$$\Delta\varphi_0(t) = \frac{\Delta\varphi_i(t) + \Delta\varphi_a(t) - \Delta\varphi_b(t)}{N} \tag{3.19}$$

where $\Delta\varphi_i(t)$ is in respect of the degradation of the input (SNR) due to the mixer, and $\Delta\varphi_a(t)$ and $\Delta\varphi_b(t)$ of the filter phase instabilities (see Section 2.4(C)) and also of the noise generated in the amplifier and multiplier.

The additional output phase instability may be further enhanced by intermodulation in the mixer (see Section 4.4), particularly when the division factor N is low.

Appendix A PLL Basics

A.1 INTRODUCTION

Transferring data between ASIC chips at frequencies above 40 MHz requires special on-chip circuitry in current sub-micron technologies. Phase locked loops can provide skew management in ASIC devices to help compensate for clock tree insertion delays and process, temperature and voltage variations allowing maximum multi-chip system performance.

This application note is written to help designers of multi-chip ASIC systems maximize system performance by managing clock distribution and optimizing clock skew and data path relationships. It contains equations relating measurable timing and skew parameters to maximum frequencies of operation. It explains techniques available to minimize critical parameters which contribute to clock skew.

A.2 BACKGROUND

A.2.1 REGISTER-TO-REGISTER DATA TRANSFER BETWEEN ASIC CHIPS

When determining the maximum frequency at which data can be transferred from one ASIC device to another, a designer must carefully consider both the delay of the data path and the skew of the clock. The data path is the delay from a register in the sending ASIC (including clock to Q) to the D input of a register in the receiving ASIC (including the setup and hold times), see Figure A.1. The clock skew or Tskew is the difference between a rising edge on ClkA in ASIC1 and ClkB in ASIC2.

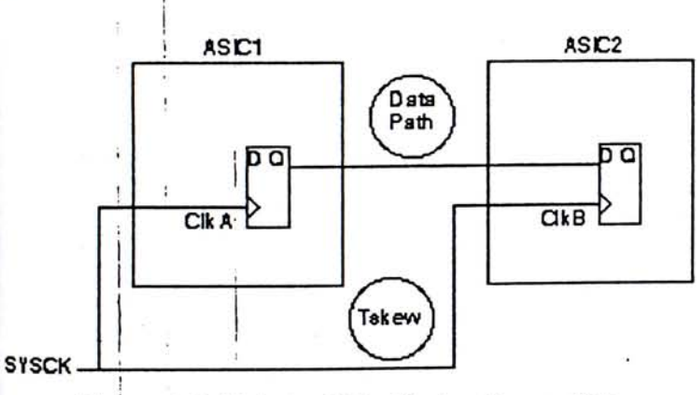

Figure A.1 Chip-to-Chip Timing Parameters

Tskew in this document refers to clock skew in both the positive and negative directions. Positive skew is when the rising edge of ClkB occurs later than a rising edge of ClkA. Positive skew affects data transfer from a hold time standpoint. Negative skew is when the rising edge of ClkB occurs earlier than a rising edge on ClkA. Negative skew affects data transfer from a setup time standpoint. A complete analysis of clock skew is performed in Appendix B.

A.2.2 SETUP AND HOLD TIME CONSIDERATIONS

To insure error-free data transitions between ASIC1 and ASIC2, the data path from the sending flip- flop in ASIC1 to the receiving flip flop in ASIC2 must not be so long that a set-up time violation is realized on the receiving flop- flop. The same data path must also be long enough to avoid a hold-time violation on the receiving flip-flop. This setup and hold time relationship must take into consideration clock skew between the rising edge of ClkA, which initiates the data transfer and the rising edge of ClkB which clocks in the transferred data.

A.2.3 INSERTION DELAY AND THE EFFECT OF THE CLOCK TREE

Insertion delay is defined as the delay from the rising edge of the external system clock to the rising edge of the clock on any given flip- flop on the ASIC. In Figure A.2, it's the delay from SYSCK to ClkA or ClkB. Insertion delay is made up of the clock input buffer and clock tree delays. The insertion delay in one ASIC can be very different from the insertion delay in another ASIC, depending on the size of the ASIC and the number of elements that must be clocked by the clock tree. Differences in insertion delays between ASIC devices directly contribute to clock skew (Tskew). In the example circuit (Figure A.2): if ASIC1 has an insertion delay of 5 ns and ASIC2 an insertion delay of 10 ns, then a rising edge in ASIC 1 will be skewed by at least 5 ns from a rising edge in ASIC 2.

A.2.4 PTV VARIATIONS

Process, Temperature and Voltage (PTV) variations can increase the difference in insertion delays. Most ASIC technologies use a multiplier to adjust delays due to PTV. In the H4C technology, a worst-case multiplier (WCM) and a best-case multiplier (BCM) are used. The WCM modifies a typical delay to represent worst-case conditions. The WCM is greater than one. The BCM is less than one and modifies a typical delay to represent a best-case condition. The "process spread" is the difference between a best-case delay and a worst-case delay for a given data path. The process spread can be found by dividing the WCM by the BCM (WCM/BCM). Choosing a technology with a minimum process spread will allow higher overall performance.

A.2.5 MAXIMUM FREQUENCY OF OPERATION

An equation can be derived that relates setup and hold times, insertion delay and process spread to determine the maximum frequency at which data can be safely transferred from chip-to-chip. A full derivation of this equation is provided in Appendix E. The equation in terms of the minimum period is,

$$MinPer = Tskew\ (WCM/BCM + 1) + WCM\ (Tsu + Th + TDm) \quad (A.1)$$

where,

MinPer Minimum clock period in ns (1/max frequency of operation).

Tskew Total skew (positive and/or negative) between rising edges of ClkA and ClkB (see Figure A.2).

WCM Worst Case Multiplier.

BCM Best Case Multiplier.

Tsu Setup delay of flip flop in receiving ASIC (ASIC2 in Figure A.2).

Th Hold delay of flip flop in receiving ASIC (ASIC2 in Figure A.2).

TDm Data path delay margin

Two things become apparent in looking at Equation (A.1). First, Tskew is the dominant parameter affecting the maximum frequency at which data can be transferred between ASIC devices. Secondly, the process spread for the chosen technology is also very important. Clearly, Tskew and the process spread must be minimized to allow maximum performance.

To address the problem of clock skew, a Phase Locked Loop (PLL) can be added to each ASIC device to reduce the effects of insertion delay differences and help manage the skew from chip-to-chip. The PLL will synchronize the rising edge on SYSCK such that it will be simultaneous with a rising edge on flop ck, see Figure A.3. If the PLL is used on each ASIC device, all flop ck signals on every ASIC will be simultaneous within the error of the PLL. The PLL will compensate for differences in insertion delays from ASIC-to-ASIC as well as PTV variations.

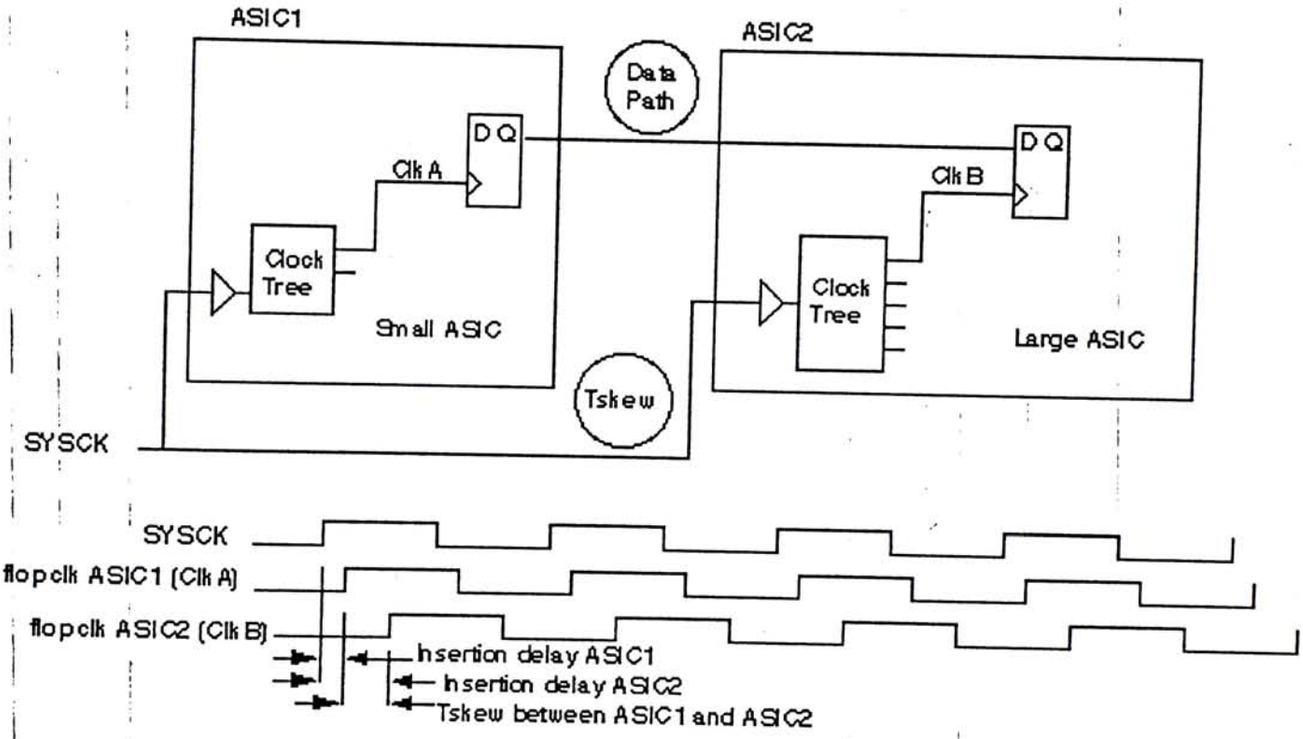

Figure A.2 Effect of Clock Tree on T_{skew}

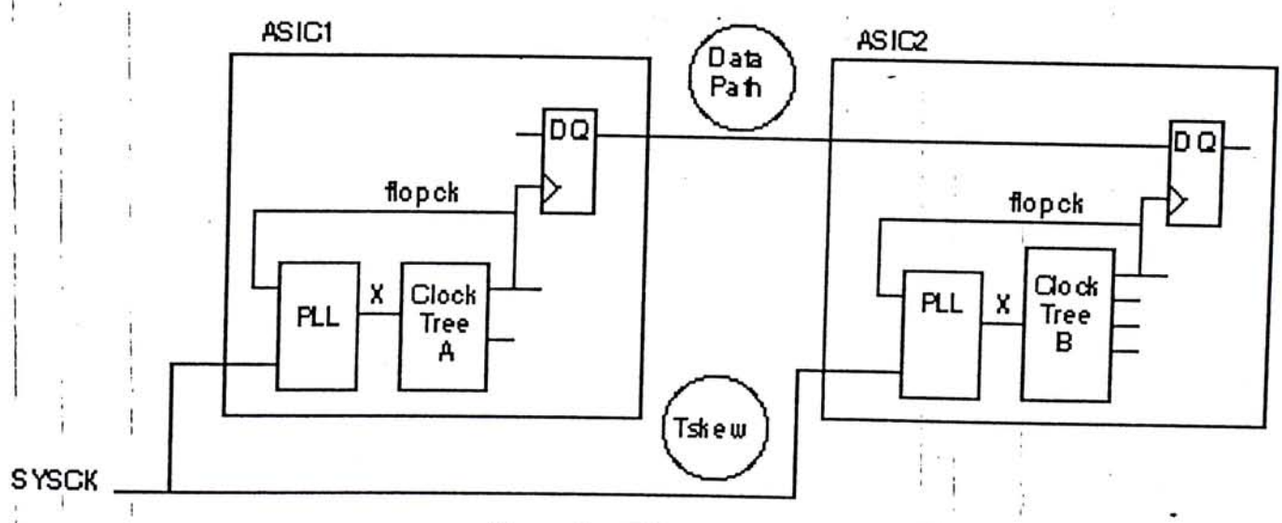

Figure A.3 PLL Solution

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precision
Beaverton, Oregon

AUDIO.TST®

SYSTEM ONE & TWO NEWSLETTER

Volume 11 Number 1
January 1996

re Have We Been?

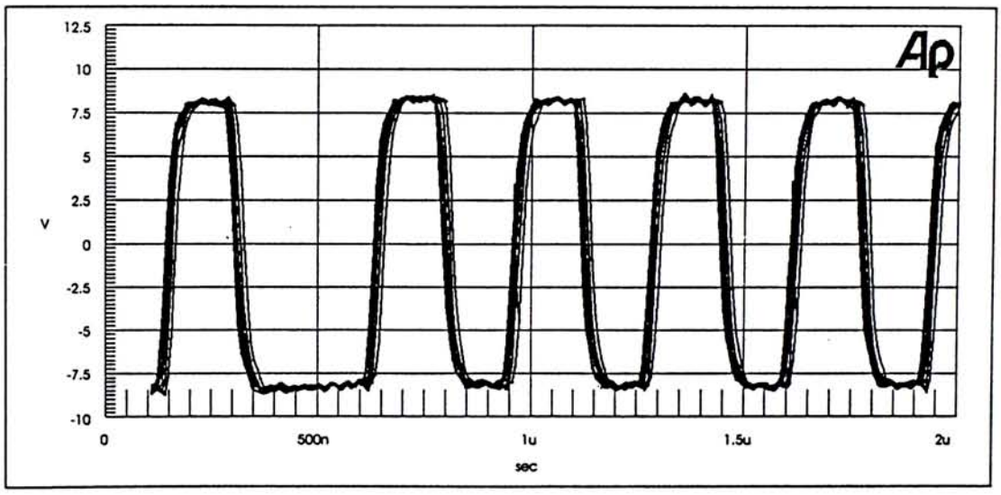
ou might have thought that we lost your name ur AUDIO.TST mailing list. Actually, the last is- this newsletter (and the only one we hed in 1995) was March 1995. What's our ex- Heavy involvement in the new product ing has consumed a great deal of time from one, including those who contribute to D.TST. We also wanted to give you some inter- articles using the new capabilities of APWIN ystem Two, learn the new software and instru- and we have had to wait in line for product y like our customers.

'e've tried to partially make it up with a bonus –16 pages, up from our usual 12. And our Year's resolution is to get back on track with evious four-time-per-year schedule.

This Issue

Digital Audio Transmission

Why Jitter is Important



Digital Audio holds the promise of perfect repeatability, no degradation over time or distance and infinite generation copies without degradation. Or does it? Convert the analog audio to ones and zeros and you can store, transmit, copy, and reproduce with perfect integrity...or can you? What is all of this talk about jitter? A digital bit stream is either high or low, a one or a zero — how can the imbedded audio degenerate?

The audio industry collectively has a wide range and depth of experience with the symptoms and causes of analog signal degradation. We all know how easy it is to develop various types of distortion, deviate from a flat frequency response or add noise. We may even have developed an intuitive feel for how signal degradation is proportional to the magnitude of the problem with the hardware: Increase the level of an external noise source and you hear the noise increase in the audio. Overdrive an amplifier and you can hear the distortion increase. Experienced audio engineers and technicians develop an intuitive sense relating circuit problems to audible effects and measured results.

Unfortunately, digital audio does not have the same obvious cause/effect relationship as analog audio. And it is a myth that the digital bit stream itself is impervious to degradation; impairments to the digital signal will definitely

adverse effects on the imbedded
o signal. These will show up as
o signal degradation just as do
e caused by conventional analog
nalies.

et's look at what are the typical im-
nents that can happen to a digital
o signal, what they are caused by,
what effects they cause in the im-
ded audio.

udio Precision's new System Two
a powerful digital audio data im-
nent simulation and measurement
bility integrated with a sophisti-
d audio measurement capability.
IN software allows any settable pa-
ter (such as a digital audio data im-
nent) to be swept while plotting
measurable parameter (such as
o level or distortion). This combina-
provides a powerful tool to evalu-
nd quantify just how a variety of
al impairments can modify the im-
ded audio. It is relatively easy to il-
ate the proportionality of digital bit
m degradation to measurable
o degradation.

er

One of the most often talked about
lem parameters of digital audio
e days is jitter. Jitter is phase modu-
n of the digital transitions of the
stream. The edges of the pulses do
nappen precisely at the time of a
retically perfect clock signal.

et's investigate how jitter can cause
o signal degradation. We can artifi-
y inject calibrated amounts and
s of jitter on a digital audio bit
m and measure the resulting audio
rtion and noise. This jitter can be
e frequency, broad-band noise jit-
r band-limited noise jitter. We can
vary the rise and fall time of the
al transitions to simulate what hap-
with long cables and see how this
ase in rise/fall time adds jitter. And
an add other digital errors such as
nal mode and common mode
e to see their effects.

ital Audio Transmission

o understand how impairments of
digital audio signal affect the imbed-
audio, we need to understand the digital audio transmission technique itself.

Most audio signals start as analog, often from a microphone which is inherently analog. At some point, the signal is converted to a digital format. For program audio (music), the resolution is typically 16 to 18 bits for each of the two channels of the stereo pair. ("Business audio", used for telephone and other voice applications, uses a much lower resolution, typically 8-bits and is a single channel.) The sample rate is typically high enough to cover the complete audio bandwidth, usually defined as 20 Hz to 20 kHz. This requires a sample rate just over twice the highest frequency of interest. For standardization, two sample rates have been defined: the consumer audio industry uses 44.1 kHz while the professional (studio recording and broadcast) industry uses 48 kHz. The seemingly unusual number of 44.1 k was chosen to be mathematically convenient in relation to television scan rates to allow the digital audio to be synchronized to the video and easily multiplexed with video.

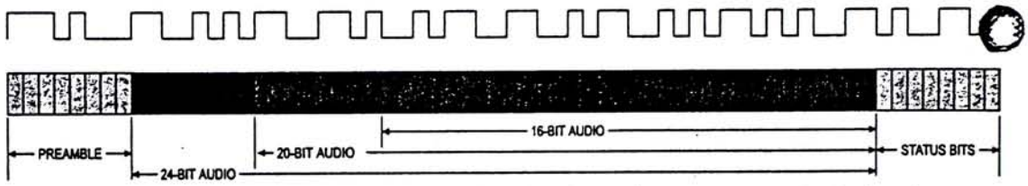
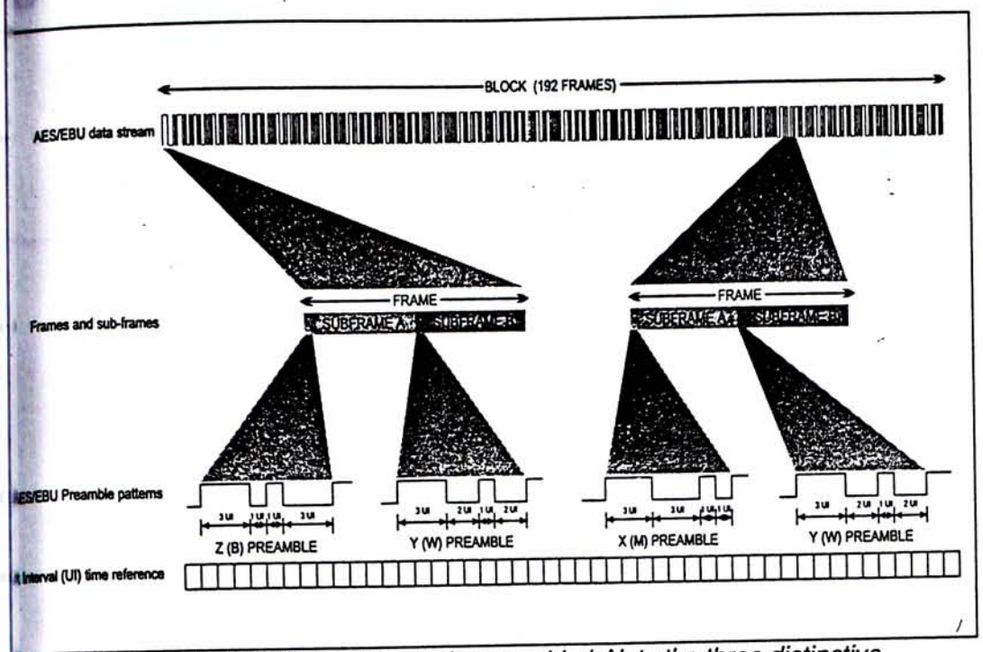


Figure 1. One sub-frame of digital audio showing the various components that make up the 32-bit data stream.

This digital audio transmission technique has been standardized by several international organizations. In the broadcast and professional audio area, the Audio Engineering Society (AES) and the European Broadcasting Union (EBU) have collaborated on individual specifications that define what is commonly known as the AES/EBU Digital Audio Interface. On the consumer audio side, Sony and Phillips have defined a lower cost variant suitable for consumer audio equipment. This format is commonly referred to as the SPDIF (Sony Phillips Digital Interface) format. These standards define the digital audio bit stream (which is the same for both), the connector, and the digital signal levels. The AES/EBU format typically uses a three-conductor XLR-style connector. The SPDIF is typically an RCA or a BNC coaxial connector or an optical connector (often called a TOSLINK, a name trademarked by Toshiba, a manufacturer of such connectors). New variants of the standards now allow additional connector types so the format can no longer be recognized solely by the connector.

Let's look at the data format for these standards. It is serial with the two audio channels of the stereo pair time multiplexed. Supplementary information, called status bits, is also carried along with the audio for supervisory and administrative purposes. To allow for improvements in converter technology, 24 bits have been reserved for each audio channel. Typically, 16 to 20 of these are used for the program audio. The unused data bits can be used for other purposes. 4 bit precede the audio as a preamble to enable the receiver to synchronize and 4 more bits are added following the audio for the supplementary administrative information. This gives a total of 32 bits per channel (4 preamble + 24 audio + 4 administrative) which form a sub-frame. The next sub-frame is an identical pattern but for the second channel. These two sub-frames in sequence become a frame. 192 such frames in sequence are defined as a block.

One of the original objectives of the AES/EBU format was to allow the digital signal to be able to be routed around a facility in the same way as an audio signal. This is why the XLR connector and a balanced signal format were chosen. The plan was to allow normal microphone cable and signal routing equipment to be used. (We'll see later how cable quality is important). The format chosen to send the data is



ure 2. How the AES/EBU data pattern is assembled. Note the three distinctive amble patterns that identify the start of a 192 frame block, the start of a frame and the rt of a sub-frame.

led Manchester or bi-phase coding ich has the property of not caring out polarity. Therefore, if a cable or itch inadvertently swaps polarity (exanges pins 2 and 3 on the XLR), the ta is preserved intact. It also has the operty of carrying very little DC as e logic transitions, on average, are mmetrical about the centerline. This ows the signal to pass through transrmers.

Let's look at how the audio bit eam is assembled. For convenience, e'll use a new time unit called the Unit terval (UI) rather than nanoseconds. UI is the smallest interval possible in e data stream. There are 128 UI's per ame. Stated this way, a UI is indeendent of sample rate; it is 162.76 sec at 48 kHz and 177.15 nsec at 44.1 Hz. The UI will be used frequently in escribing parameters of the digital ata.

All data pulses are either one or two I in duration with the exception of the reamble which contains three-UI-wide ulses. The 3-UI preamble is distinctive order to establish synchronization nd, being the lowest frequency compoent, is the most robust. There are three ariations of the 3-UI preamble to niquely identify the start of sub-frame , start of sub-frame B, or start of the lock of 192 frames respectively. Figure 2 shows the make up of a complete block with its frames, sub-frames, and the distinctive preambles.

Real-life data patterns

So much for the theoretical shape of the data bit stream, what does the signal look like in reality? We used the time domain (oscilloscope mode) of System Two to capture a typical data pattern as shown in figure 3 below. The three different pulse widths (1,2, and 3 UI) are clearly evident. This particular view shows some overshoot and rise and fall time are relatively fast. Contrast this with the view shown in figure 4 which shows increased rise and fall time caused by the distributed reactance of a typical long cable. Note that the slower transition times give rise to base line shift, that is a variance of the instantaneous DC level. The consequence of this

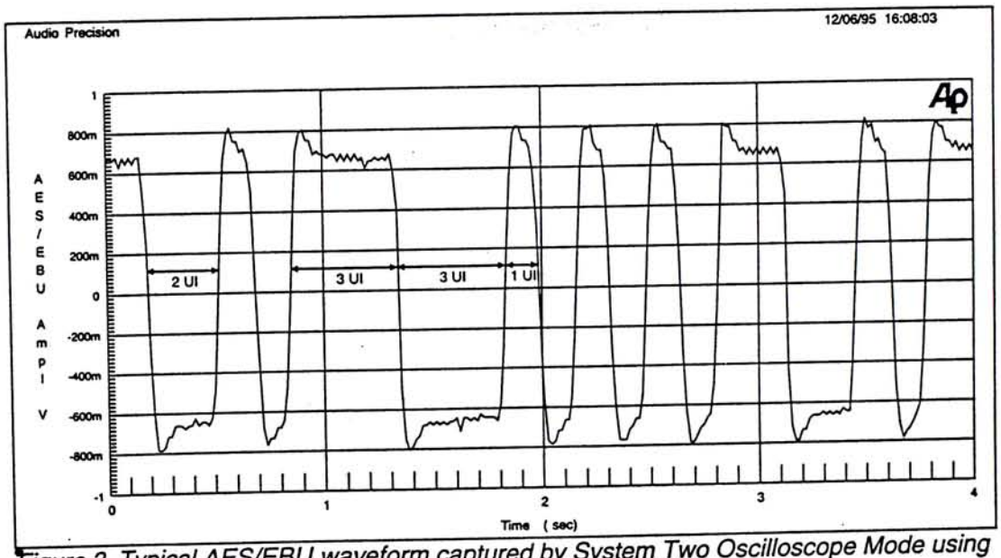


Figure 3. Typical AES/EBU waveform captured by System Two Oscilloscope Mode using APWIN. Note the 1, 2, and 3 UI pulse widths.

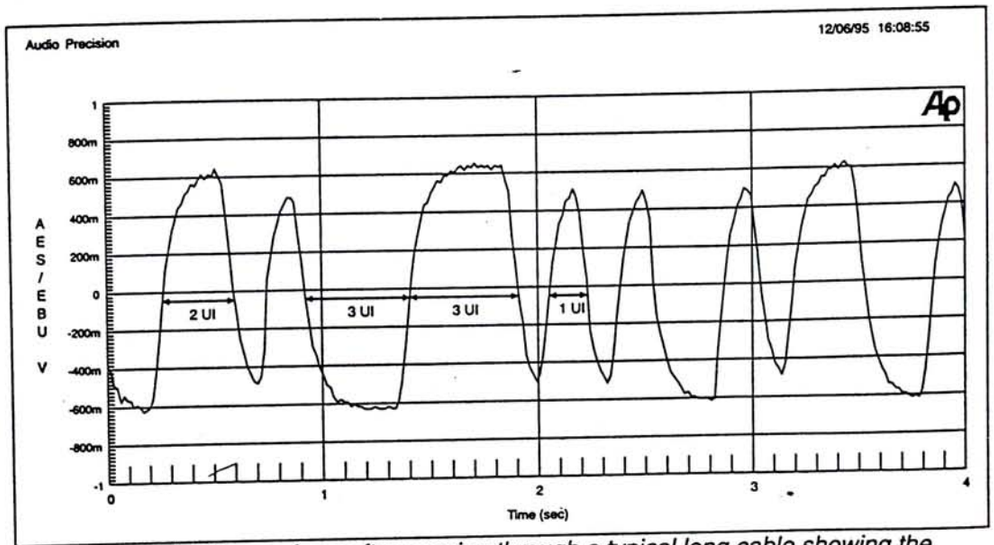
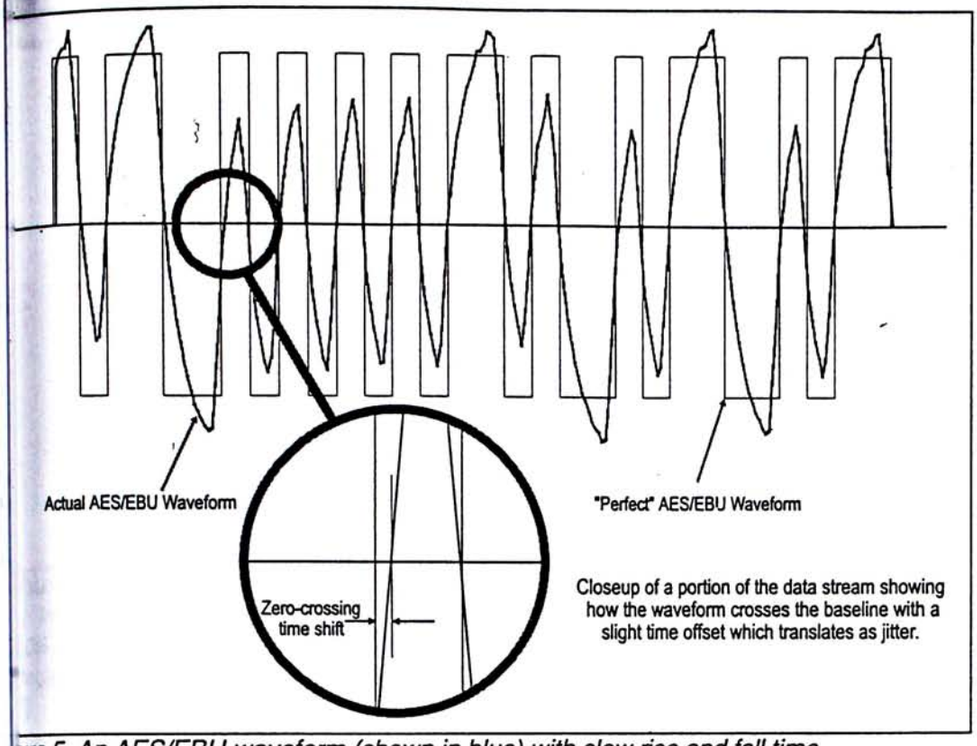


Figure 4. AES/EBU waveform after passing through a typical long cable showing the slower rise and fall time caused by cable capacitance.



ure 5. An AES/EBU waveform (shown in blue) with slow rise and fall time erimposed over the theoretical waveform with zero rise and fall time (shown in black). e expanded view shows how the zero cross transitions have n shifted along the time axis resulting in jitter on the recovered ck signal.

shifting of the zero cross point along time axis. Since clock information is ived from the zero cross transition, shift shows up as time variance or ase modulation. Figure 5 illustrates point clearly. Here we have shown actual waveform in blue superimsed over the theoretically perfect veform in black. If you look at the exnded portion, the time shift is clearly dent.

Why is jitter on this data stream and sequently the recovered clock impor- t? The receiving device may use the overed clock signal to create the ck for the converter used to convert digital audio signal to analog. Alugh there is some filtering between interface clock and the converter ck, there is not total isolation. The de- n of the phase lock loop (PLL) circuit d to recover the data stream and ck will determine the transfer func- n or jitter rejection capability of the rice. Jitter on the converter clock will distortion and noise to the recovd audio. Even if the device does not a converter but just passes the sigon in the digital domain, it will still s on some degree of jitter which can affect an eventual converter later in the path.

Figure 6 is a plot of the jitter level versus time on an AES/EBU signal. The AES/EBU signal has had 0.5 UI of sine wave jitter at 5 kHz intentionally added at the generator to illustrate how an impairment is carried with the data. This impairment is clearly evident in this time waveform of the received signal jitter. We will show how this jitter imbedded in the digital bit stream can "leak" into the actual audio signal recovered by the D to A converter.

For our evaluation, we used a commercial signal processing device that had both stereo analog audio inputs and outputs and digital audio inputs and outputs. This allowed us to evaluate both the transmit and receive paths of the digital circuits and exercise all converters.

To qualify our measurement setup, we ran an FFT spectrum analysis of the residual distoration and noise of the digital to analog converter of the device under test with System Two as the digital source with no simulated jitted injected. This indicated that the highest distoration components were below -80 dB relative to full scale. Broadband noise was below -100 dB showing no jitter components. See figure 7.

Let's start by using the digital to analog converter path. We used the digital

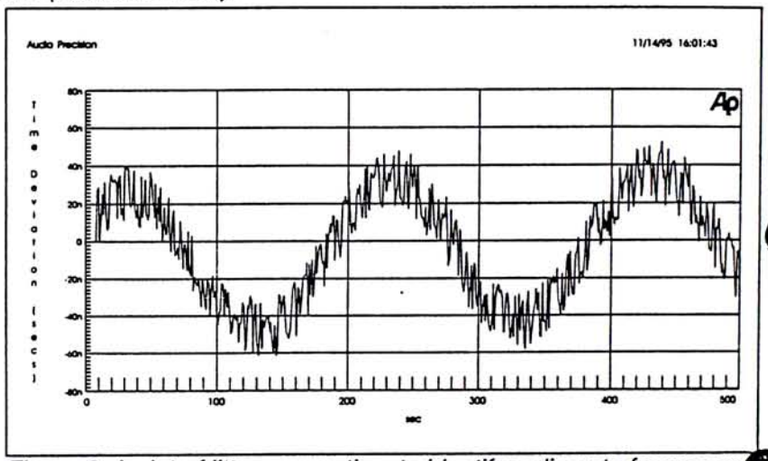
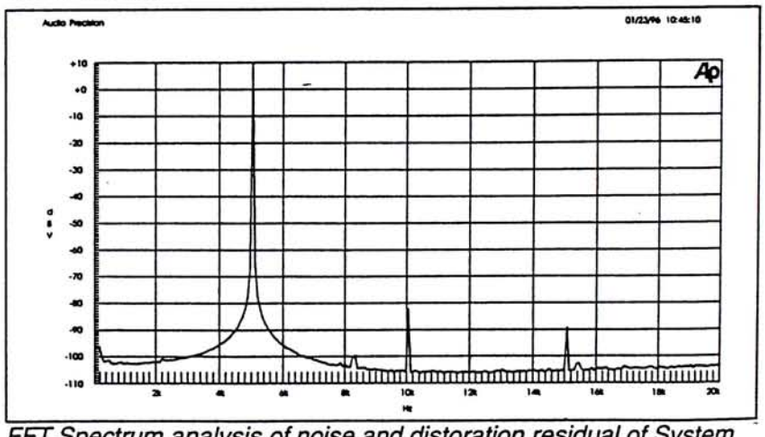


Figure 6. A plot of jitter versus time to identify a discrete frequency component of the jitter. The jitter signal has been recovered from an AES/EBU signal that has had a 5 kHz sinusoidal jitter signal at 0.5 UI added.



FFT Spectrum analysis of noise and distoration residual of System Two and the digital to analog converter of the device under test. The fundamental is 5 kHz. The second and third harmonic products from the converter show as spikes at 10 kHz and 15 kHz. Residual noise is below -100 dB and there are no other components showing jitter induced artifacts.

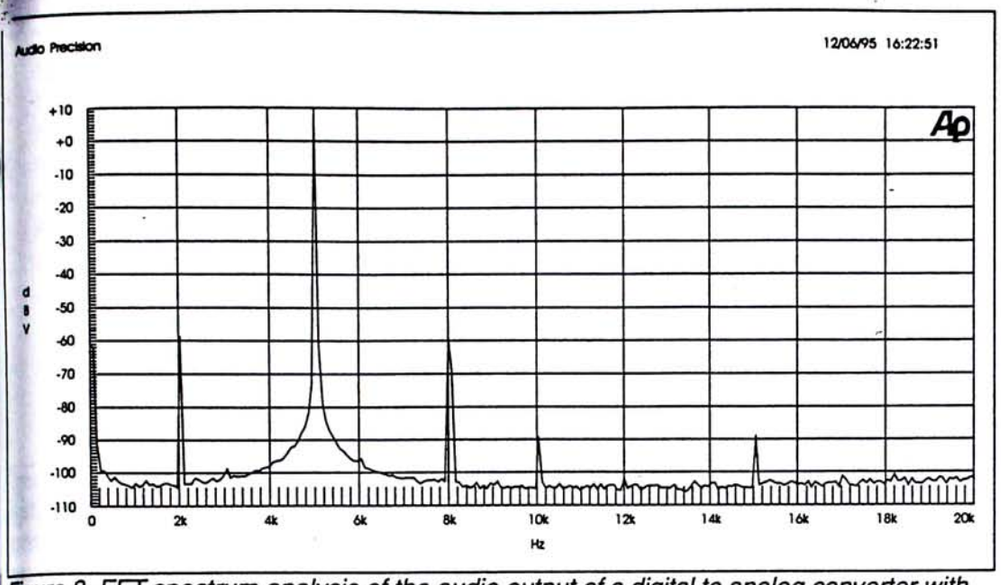


Figure 8. FFT spectrum analysis of the audio output of a digital to analog converter with a 5 kHz audio signal encoded in the AES/EBU digital data stream sent to the converter. A 35 nsec 3 kHz sinewave jitter signal has been added to the digital signal. This has produced sidebands offset from the audio signal at 2 kHz and 8 kHz at approximately -60 dB.

domain capabilities of System Two as our source and the analog audio measurement capabilities to evaluate the results. We added both a discrete frequency jitter and random noise jitter to the AES/EBU data, sent this impaired signal to the digital input of the signal processing device, and measured the audio output from the device. We performed an FFT spectrum analysis to clearly show what had been added to the test signal.

Our test signal was a 5 kHz sine wave generated by System Two in the digital domain. We ran three tests for comparison. Our jitter signals were generated by System Two's data impairment simulation function. For the first test, we injected sine wave jitter into the digital bit stream. We used a 3 kHz sine wave with an amplitude of 35 nsec (approx. 0.22 UI). Figure 8 shows the spectrum analysis of the audio. The induced jitter has produced sidebands at 2 kHz and 8 kHz (5 kHz - 3 kHz and 5 kHz + 3 kHz). The magnitude of these sidebands is approximately 60 dB below full scale.

For the next two tests, we selected band-limited random noise as the jitter signal. System Two allows control of the amount and bandwidth of the injected signal. First, we added 0.25 UI of jitter with a 3 kHz low pass roll off. Next we added added 1 UI of random noise with a 2 kHz roll off. Figure 9 shows the spectrum analysis of the recovered audio. The noise added to the audio by the jitter is clearly evident. Again it is clear that jitter injected on the data bit stream shows up in the recovered audio signal.

Other Data Impairment Sources

Remember how we showed that slow rise and fall times can induce jitter? And we have shown how jitter shows up as spurious signals on the recovered audio. To show the sensitivity of the converters in the device under test to this impairment, we set up System Two's data impairment facility to provide slower transmit rise and fall times. We set up a sweep to vary the rise/fall times from nominal (approx. 16 nsec) to 400 nsec. We plotted this data impairment against THD+N of the recovered audio at the output of the converter. The resulting graph is shown in figure 10. With this particular set up, THD+N starts to increase as the rise/fall times approach 80 nsec and increases smoothly until approximately

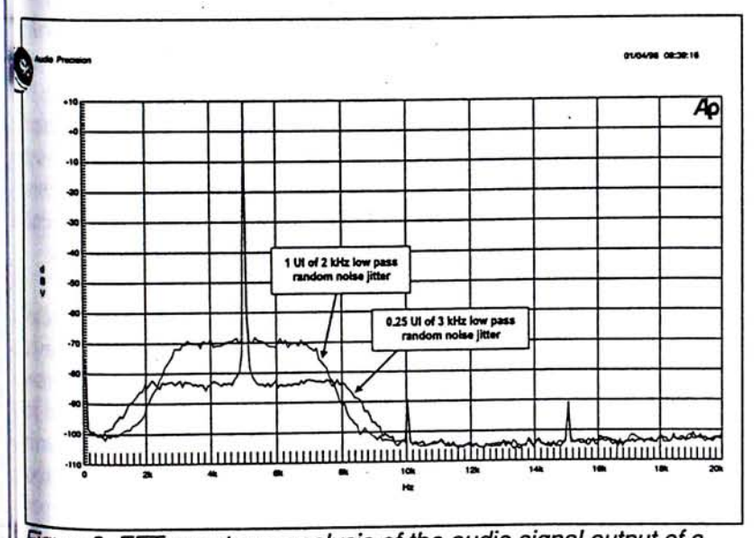


Figure 9. FFT spectrum analysis of the audio signal output of a digital to analog converter stimulated with an AES/EBU signal that has had random jitter intentionally added. The jitter signal in one case is random noise with a 3 kHz low pass filter. In the second case, 1 UI of 2 kHz low pass filtered jitter has been added. Note how this digital data stream jitter has been added to the audio signal showing the correlation between digital data impairments and audio signal degradation.

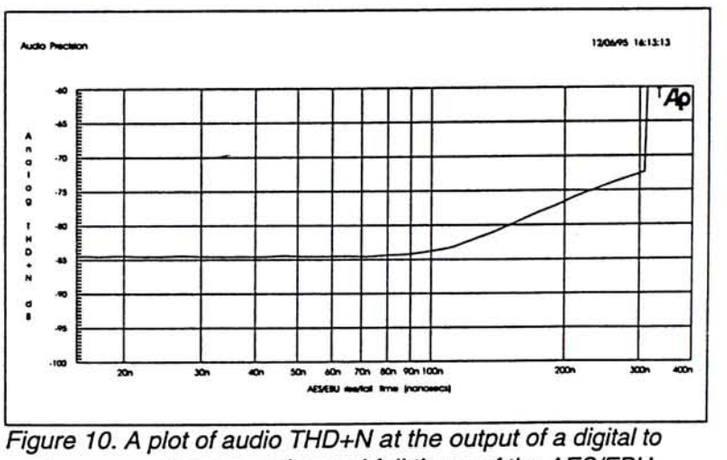


Figure 10. A plot of audio THD+N at the output of a digital to analog converter versus rise and fall times of the AES/EBU data stream. The digital audio signal is 10 kHz. This graph illustrates that in this particular situation, THD+N increases proportionally as the digital rise and fall time increase above 100 nsecs.

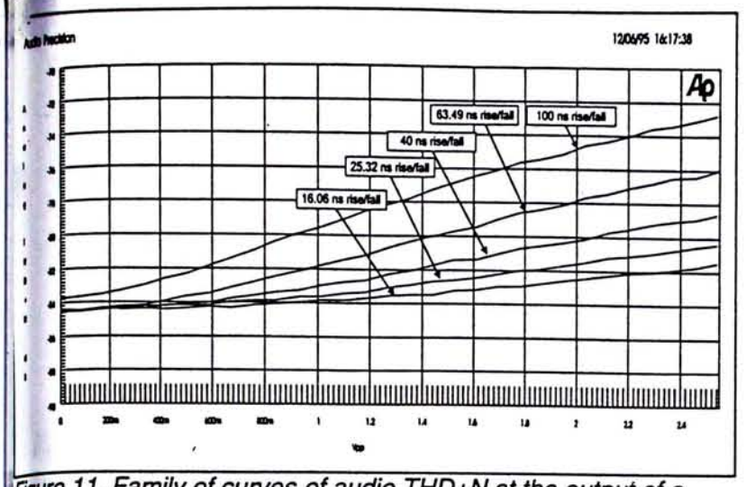


Figure 11. Family of curves of audio THD+N at the output of a digital to analog converter versus the amplitude of broadband normal mode noise added to the AES/EBU digital signal at the input of the converter for various rise/fall times. These curves illustrate the combining effect of two data impairments on the digital data stream. For fast rise and fall times, the addition of broad band noise has little effect on the THD+N of the audio signal, contributing only about 2 dB to the distortion in this case. With slower rise and fall time, such as would be true with the bandwidth limitations caused by cables, increasing broadband noise can have a significant effect of audio THD+N, in this case increasing the distortion by about 10 dB as broadband noise increases to approximately 2.5 Vpp.

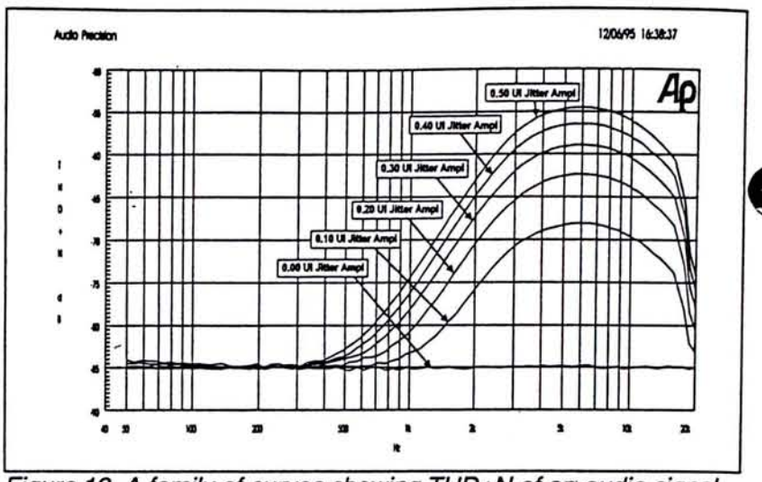


Figure 12. A family of curves showing THD+N of an audio signal at the output of a digital to analog converter versus jitter frequency for various amounts of jitter added to the digital data stream. The jitter signal is a sine wave varied from 0 to 0.5O UI. Note that at low jitter frequencies, the jitter on the digital bit stream has little effect on the distortion but at approximately 6 kHz for this particular device, the jitter can increase the THD+N by from 15 dB to over 30 dB. The audio stimulus source is a digital sine wave at a fixed frequency of 10 kHz and fixed amplitude of -6 dBFS.

300 nsec. At this point, the AES/EBU receiver was unable to handle the digital signal. A "typical" XLR AES/EBU cable of about 100 meters (≈300 feet) in length will have rise and fall times of about 150 nsec.

Multi-dimension tests

A powerful measurement technique varies two stimulus parameters while measuring a third to produce a family of curves. This generates a three dimension result: X versus Y versus Z. This presents a wealth of data in a single snapshot making it easy to spot trends, determine safe operating areas, etc.

The next three tests we ran are an example of such tests, called nested sweeps in APWIN. For the first test, we wanted to see the effect and interaction of both increased noise and increased rise/fall time to the D to A converter of our device under test. We added varying amounts of broadband noise to the digital AES/EBU signal by sweeping the injected normal-mode noise parameter and ran this sweep for five values of rise and fall time while plotting audio THD+N. In this way, we can see the interaction of these two impairments on the imbedded audio. Figure 11 shows the family of curves that this test produced. We can see that for fast rise/fall times, the induced noise has little audio degradation effect, adding only about 2 dB of THD+N for up to 2.5 Vpp of injected noise on the data stream. However, with 100 nsec of rise/fall time, increased noise has a more dramatic effect now showing about a 10 dB increase in distortion with the same 2.5 Vpp increase in noise.

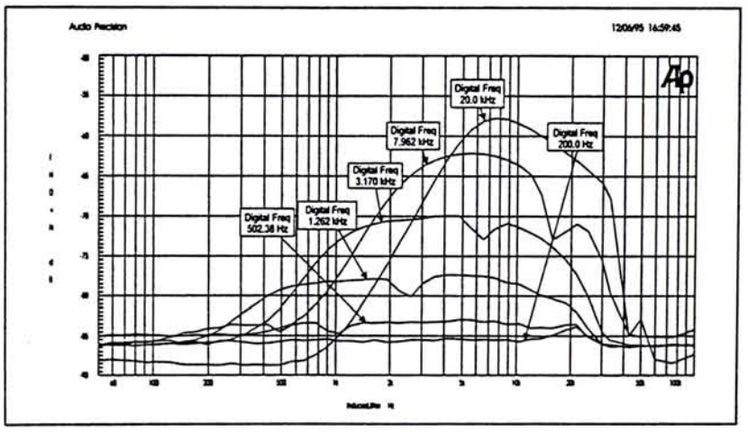


Figure 13. Family of curves of audio THD+N at the output of a digital to analog converter versus jitter frequency for various digital audio signal frequencies from 200 Hz to 20 kHz. Sinusoidal jitter swept from 50 Hz to 100 kHz at .25 UI has been added to the AES/EBU digital data stream that is input to the D to A. This shows that at low audio signal frequencies, the jitter contribution to THD+N is minimal but as the audio frequency and/or the jitter frequency increases, the converter THD+N is more susceptible to jitter.

For our second multi-dimension test, we plotted THD+N versus injected sinewave jitter frequency for six different amplitude values of jitter (see figure 12). These curves give us some indication of how the AES/EBU phase locked loop in the device under test behaves. At low jitter frequencies below about 500 Hz, injected jitter has little effect on the imbedded audio. We see a peak in the distortion when the jitter is about 6 kHz showing that the PLL has least jitter rejection at this frequency. 0.50 UI of sine wave jitter at 6 kHz has increased distortion by about 30 dB.

Our third multi-dimension test plotted audio THD+N versus injected jitter frequency for six values of audio fre-

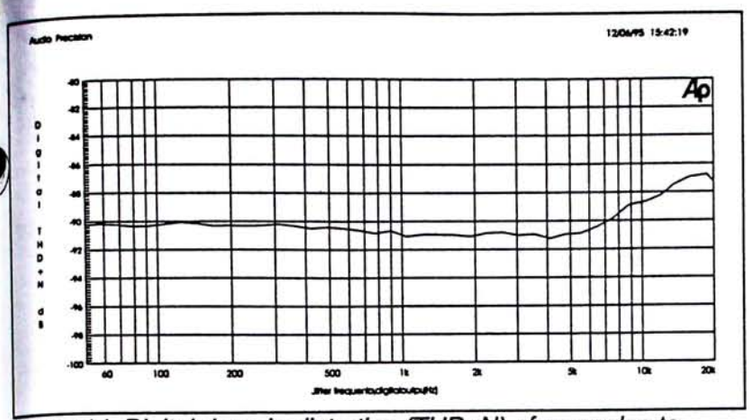


Figure 14. Digital domain distortion (THD+N) of an analog to digital converter versus jitter frequency. The audio source at the input of the A to D is a 1 kHz sine wave at 0 dBu. The jitter amplitude is a 0.35 UI sine wave that is swept form 20 Hz to 20 kHz. This graph shows greater susceptibility to interface jitter at higher frequencies.

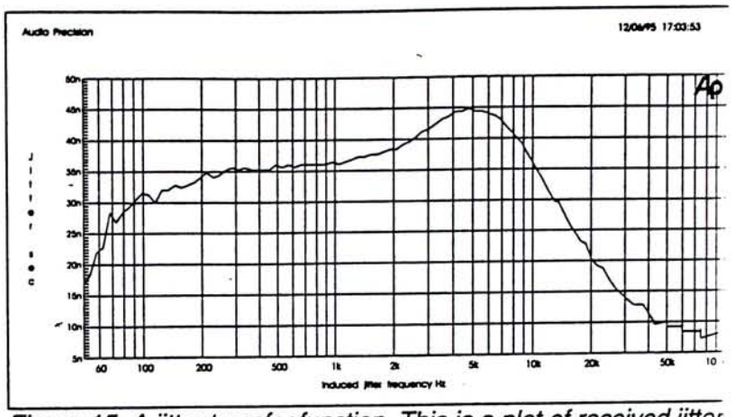


Figure 15. A jitter transfer function. This is a plot of received jitter amplitude versus injected jitter frequency. This illustrates the ability of a digital domain device to reject jitter at its input and not pass it on to its output. This measurement was made by connecting the AES/EBU input of the test device to System Two with ≈40 nsec of sinusoidal jitter added to the output. This sine wave is swept from 50 Hz to 100 kHz and the jitter is measured and plotted at the output of the device under test. This particular device has jitter gain at 5 kHz.

quency (see figure 13). We used 0.25 UI of sine wave jitter which we swept from 50 Hz to 100 kHz while plotting THD+N of the recovered audio signal. We ran this sweep for six frequency values of digital audio test signal. What this shows is for lower audio frequencies, injected jitter has little effect. But at higher audio frequencies, injected jitter at mid-band frequencies can have a pronounced effect. We see a peak at 8 kHz of injected sine wave jitter when the audio frequency is 20 kHz. Here we see an increase of THD+N of over 25 dB. At lower and higher jitter frequencies, or at lower audio frequencies, there is far less contribution from the injected jitter. With a 200 Hz sine wave, there is virtually no audio degradation.

Analog to Digital Converter Measurements.

To see the effect on the analog to digital converter, we ran the test shown in figure 14. Here we generated a 1 kHz analog sine wave to feed to the audio inputs of the device under test. We then fed the AES/EBU reference input of the DUT with the digital output of System Two. It is possible to slave the A to D clock of the device under test to this external AES/EBU reference. We added 0.35 UI of sine wave jitter to the digital data stream and swept the jitter frequency from 20 Hz to 20 kHz while plotting THD+N at the AES/EBU output of the DUT. This illustrates how jitter from the reference input can find its way to the sample clock of the A to D converter and add distortion to the digital audio signal. The graph shows a rise in THD+N at higher frequencies caused by the jitter but good jitter rejection at mid-band and lower frequencies.

AES/EBU Jitter Transfer Function

A useful picture of the behavior of an AES/EBU interface with injected jitter is shown by the jitter transfer function. This is produced by plotting jitter amplitude of the AES/EBU output of a device versus jitter injected at the AES/EBU input of the device. It is a digital domain measurement and can illustrate the behavior of the clock recovery circuits of the interface.

We swept approximately 35 nsec of injected sine wave jitter over the 50 Hz to 100 kHz range while plotting received jitter amplitude. The resulting curve shows about unity jitter gain at 5 kHz and increasing rejection at higher and lower frequencies. Note that this peak shows up in the THD+N versus frequency plots of figures 12 and 13.

Conclusion

The comprehensive analog and digital domain generation and measurement capability of System Two coupled with the flexible test configuration and data presentation features of APWIN form a powerful tool to evaluate the operation, quantify the performance and ensure compatibility of digital audio equipment. A digital audio interface may have marginal parameters that allow operation in some applications but not others. The numerous simulated data impairment features of System Two in conjunction with its many measurement functions allow thorough evaluation of devices to real-world situations. The ability to sweep certain parameters while plotting others can clearly show what error margins are present in the device under test.

Ap

Most of the content of this article was taken from an AES Workshop presentation on AES/EBU Interface Jitter given by Dr. Richard Cabot in New York in October 1995.

CRYSTAL
Semiconductor Corporation

AES/EBU Interface

Application Note

Overview of Digital Audio Interface Data Structures

Clif Sanchez & Roger Taylor

The following information is provided for convenience, but by no means constitutes the entire specification. Also included is information from the IEC 958 and the new AES3-199x and TC84 documents. The AES3-199x and TC84 documents have not received approval as of the printing of this data sheet. To guarantee conformance, a copy of the actual specification should be obtained from the Audio Engineering Society or ANSI (ANSI S4.40-1985) for the AES3 document, and the International Electrotechnical Commission for the IEC 958 document.

The AES/EBU interface is a means for serially communicating digital audio data through a single transmission line. It provides two channels for audio data, a method for communicating control information, and some error detection capabilities. The control information is transmitted as one bit per sample and accumulates in a block structure. The data is biphase encoded, which enables the receiver to extract a clock from the data. Coding violations, defined as preambles, are used to identify sample and block boundaries.

Frames Sub-frames and Blocks

An audio sample is placed in a structure known as a sub-frame. The sub-frame, shown in Figure 1, consists of 4 bits of preamble, 4 bits of auxiliary data, 20 bits of audio data, 3 bits called validity, user, and channel status, and a parity bit. The preamble contains biphase coding violations and identifies the start of a sub-frame. The audio sample word length can vary up to 24 bits and is transmitted LSB first. If the word length is greater than 20 bits, the sample occupies both the audio

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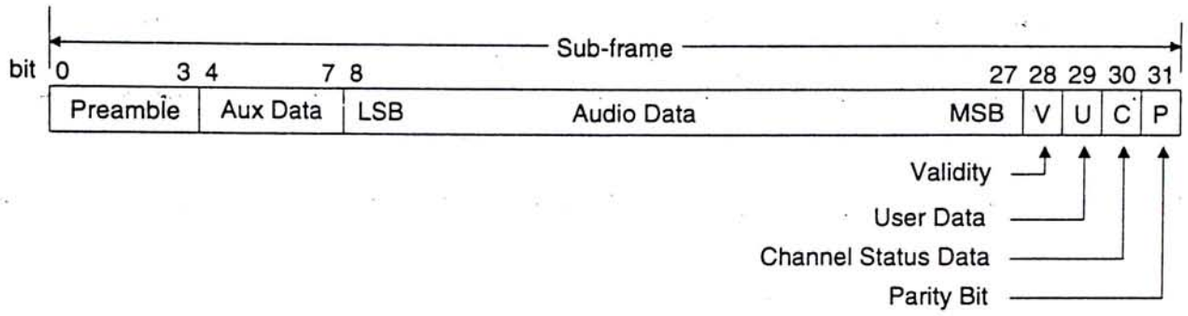


Figure 1. Sub-frame Format

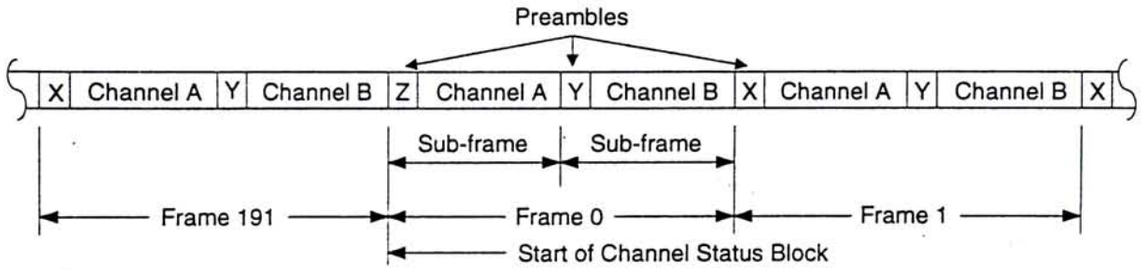


Figure 2. Frame/Block Format

and auxiliary data fields. If it is 20 bits or less, the auxiliary field can be used for other applications such as voice. The parity bit generates even parity and can detect an odd number of transmission errors in the sub-frame. The validity bit, when low, indicates the audio sample is fit for conversion to analog. The user and channel status bits are sent once per sample and, when accumulated over a number of samples, define a block of data. The user bit channel is undefined and available to the user for any purpose. The channel status bit conveys, over an entire block, important information about the audio data and transmission link. Each of the two audio channels has its own channel status data with a block structure that repeats every 192 samples.

As shown in Figure 2, two consecutive sub-frames are defined as a frame, containing channels A and B, and 192 frames define a block. The preambles that identify the start of a sub-frame are different for each of the two channels with another unique one identifying the beginning of a channel status block.

Modulation and Preambles

The data is transmitted with biphase-mark encoding to minimize the DC component and to allow clock recovery from the data. As illustrated in Figure 3, the 1's in the data have transitions in the center, and the 0's do not, after biphase-mark encoding. Also, the biphase-mark data switches polarity at every data bit boundary. Since the value of the data bit is determined by whether their is a transition in the center of the bit, the actual polarity of the signal is irrelevant.

Each sub-frame starts with a preamble. This allows a receiver to lock on to the data within one sub-frame. There are three defined preambles:

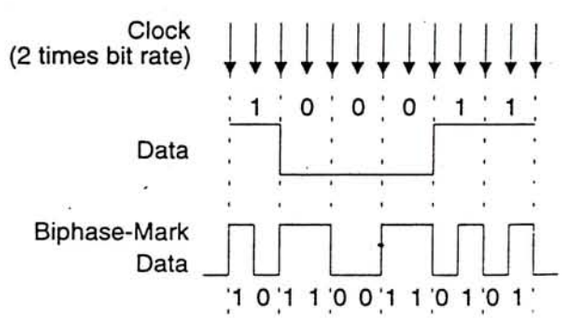


Figure 3. Biphase-Mark Encoding

	Biphase Patterns	Channel
X	11100010 or 00011101	Ch. A
Y	11100100 or 00011011	Ch. B
Z	11101000 or 00010111	Ch. A & C.S. Block Start

Table 1. Preambles

one for each channel and one to indicate the beginning of a channel status block (which is also channel A). To distinguish the preambles from arbitrary data patterns, the preambles contain two biphase-mark violations. Biphase-mark data is required to transition at every bit period, but each preamble violates that requirement twice. In Figure 3 each bit boundary, indicated by the dashed lines, contains a transition in the biphase

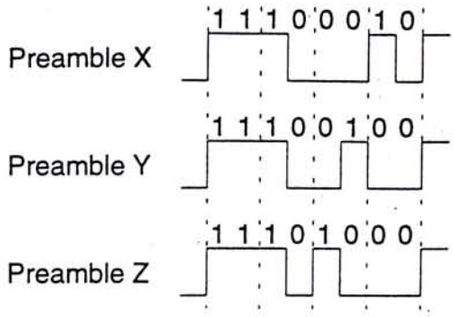


Figure 4. Preamble Forms

data. Each preamble shown in Figure 4 has two bit boundaries with no transition, which enables the receiver to recognize the data as a preamble. Table 1 lists the preamble biphase-mark data pat-

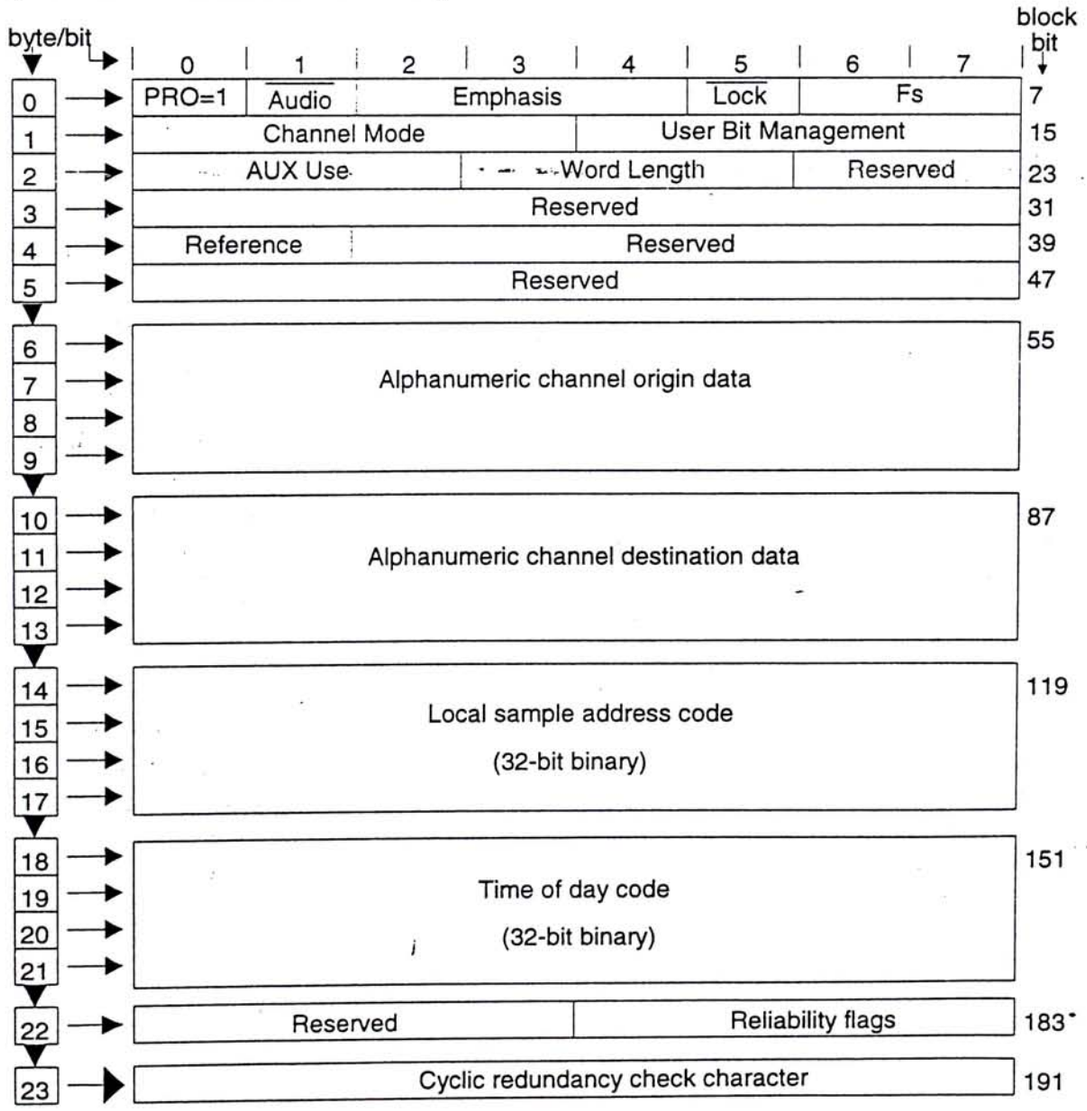


Figure 5. Professional Channel Status Block Structure

terns and what each designates. Since biphase-mark encoding is not polarity conscious, both phases are shown in the table. Preambles "X" and "Y" indicate a sub-frame containing channels A and B respectively. Preamble "Z" replaces preamble "X" once every 192 frames to indicate the start of a channel status block.

There are two channel status blocks, one for channel A and one for channel B. Since there are 192 frames in a block, each channel has a channel status block 192 bits long. These 192 channel status bits in a block can be arranged as 24 bytes. The blocks have one of two formats, professional or consumer. The first bit of the channel status block defines the format with 0 indicating consumer and 1 indicating professional.

Channel Status Block - Professional Format

Setting the first bit of channel status high designates the professional or broadcast format. The channel status block structure for the professional format is illustrated in Figure 5 and shows bit 0 of byte 0, PRO, to contain a one. Tables 2 and 3 list the bits in each byte and their meaning. The areas designated "reserved" in the figures and tables, are currently not specified and must be set to 0 when transmitting. Most of the professional format data was obtained from the AES3-1985 document, and information from AES3-199x. Since the AES specification is currently being updated, the accuracy of this data is not guaranteed.

BYTE 0	
bit 0	PRO = 1
0	Consumer use of channel status block
1	Professional use of channel status block
bit 1	$\overline{\text{Audio}}$
0	Normal Audio
1	Non-Audio
bits 2 3 4	Encoded audio signal emphasis
0 0 0	Emphasis not indicated. Receiver defaults to no emphasis with manual override enabled
1 0 0	None. Rec. manual override disabled
1 1 0	50/15 µS. Rec. manual override disabled
1 1 1	CCITT J.17 . Rec. man. override disabled
X X X	All other states of bits 2-4 are reserved
bit 5	$\overline{\text{Lock}}$: Source Sample Frequency
0	Locked - default
1	Unlocked
bits 6 7	Fs: Sample Frequency
0 0	Not indicated. Receiver default to 48 kHz and manual override or auto set enabled
0 1	48 kHz. Man. override or auto disabled
1 0	44.1 kHz. Man. override or auto disabled
1 1	32 kHz. Man. override or auto disabled

BYTE 1	
bits 0 1 2 3	Channel Mode
0 0 0 0	Mode not indicated. Receiver default to 2-channel mode. Manual override enabled
0 0 0 1	Two-channels. Man. override disabled
0 0 1 0	Single channel. Man. override disabled
0 0 1 1	Primary/Secondary (Ch. A is primary). Manual override disabled
0 1 0 0	Stereophonic. (Ch. A is left) Manual override disabled.
0 1 0 1	Reserved for user defined applications
0 1 1 0	Reserved for user defined applications
1 1 1 1	Vector to byte 3. Reserved
X X X X	All other states of bits 0-3 are reserved.
bits 4 5 6 7	User bits management
0 0 0 0	Default, no user info indicated
0 0 0 1	192 bit block structure Preamble 'Z' starts block
0 0 1 0	Reserved
0 0 1 1	User defined application
X X X X	All other states of bits 4-7 are reserved.

Table 2. Professional Channel Status bytes 0-1

BYTE 2	
bits 0 1 2	AUX: Use of auxiliary sample bits
0 0 0	Not defined. Maximum audio word length is 20 bits
0 0 1	Used for main audio. Maximum audio word length is 24 bits
0 1 0	Single coordination signal. Max. audio word length is 20 bits
0 1 1	User defined application
X X X	All other states of bits 0-2 are reserved

bits 3 4 5	Source word length Max. audio based on bits 0-2 above	
	Max audio 24 bits	Max audio 20 bits
0 0 0	Not Indicated	Not Indicated (default)
0 0 1	23 bits	19 bits
0 1 0	22 bits	18 bits
0 1 1	21 bits	17 bits
1 0 0	20 bits	16 bits
1 0 1	24 bits	20 bits
X X X	All other states of bits 3-5 are reserved	

bits 6 7	
X X	Reserved

BYTE 3	
bits 0-7	Vectored target byte
XXXXXXX	Reserved

BYTE 4	
bits 0 1	Digital audio reference signal per AES11-1990
0 0	Not reference signal (default)
0 1	Grade 1 reference signal
1 0	Grade 2 reference signal
1 1	Reserved
bits 2-7	
XXXXXX	Reserved

BYTE 5	
bits 0-7	
XXXXXXX	Reserved

BYTES 6 - 9
Alphanumeric channel origin data
7-bit ISO 646 (ASCII) data with odd parity bit. First character in message is byte 6. LSB's are transmitted first.

BYTES 10 - 13
Alphanumeric channel destination data
7-bit ISO 646 (ASCII) data with odd parity bit. First character in message is byte 10. LSB's are transmitted first.

BYTES 14 - 17
Local sample address code (32-bit binary)
Value is of first sample of current block. LSBs are transmitted first.

BYTES 18 - 21
Time-of-day sample address code (32-bit binary)
Value is of first sample of current block. LSBs are transmitted first.

BYTE 22	
bits 0 1 2 3	
X X X X	Reserved
bit 4	Channel status bytes 0 to 5
0	Reliable
1	Unreliable
bit 5	Channel status bytes 6 to 13
0	Reliable
1	Unreliable
bit 6	Channel status bytes 14 to 17
0	Reliable
1	Unreliable
bit 7	Channel status bytes 18 to 21
0	Reliable
1	Unreliable

BYTE 23
CRCC: Cyclic redundancy check character
CRCC for channel status data block that uses bytes 0 to 22 inclusive. Generating polynomial is $G(x) = X^8 + X^4 + X^3 + X^2 + 1$ with an initial state of all ones.

Table 3. Professional Channel Status Bytes 2-23

Channel Status Block - Consumer Format

Setting the first bit of channel status low designates the consumer format. The channel status block structure for the consumer format is illustrated in Figure 6 with the bit descriptions in Tables 4 and 5. All areas listed as "reserved" must be transmitted as a 0. The data for this format was obtained from the EIAJ CP-340 and the IEC 958 with some information from TC84 which is a proposed amendment to IEC 958 and has not received approval yet. As with the professional format, since this format is currently changing, the accuracy of the data listed cannot be guaranteed.

In the consumer format, bit 0 must be 0. If bit 1 is set to 1 defining the data as non-audio, then bits 3-5 are redefined (see Table 4, byte 0). Bits 6 and 7 of byte 0 define the mode, and only one mode is presently defined, mode = 00. This mode defines the next three bytes as listed in Figure 6. Most of byte 1 defines the category code. The first 3 to 5 bits define the general category. Under the laser-optical category is compact disk (cat. code 1000000). This format defines some of the U channel bits and the CD subcode port. More information can be obtained from the CP-340 or IEC 958 documents.

Currently the standards committees are trying to define a minimum implementation as well as levels of implementation of channel status data.

A scheme for providing copy protection is also currently being developed. It includes knowing

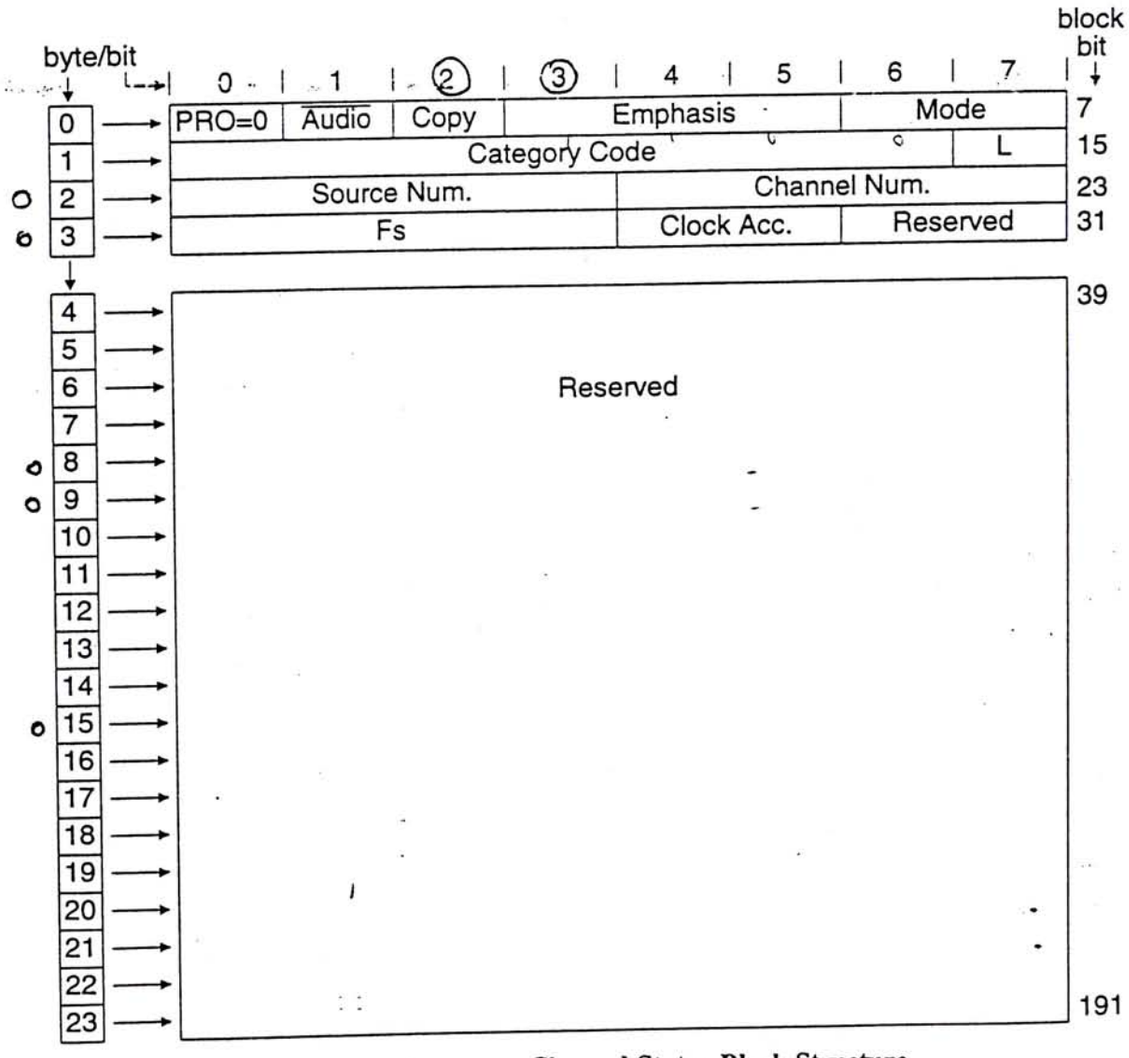


Figure 6. Consumer Channel Status Block Structure

BYTE 0		
bit	0	PRO = 0 (consumer)
	0	Consumer use of channel status block
	1	Professional use of channel status block
bit	1	$\overline{\text{Audio}}$
	0	Digital Audio
	1	Non-audio
bit	2	Copy / Copyright
	0	Copy inhibited / copyright asserted
	1	Copy permitted / copyright not asserted
bits	3 4 5	Pre-emphasis - if bit 1 is 0 (dig. audio)
	0 0 0	None - 2 channel audio
	1 0 0	50/15 µs - 2 channel audio
	0 1 0	Reserved - 2 channel audio
	1 1 0	Reserved - 4 channel audio
	X X 1	Reserved - 4 channel audio
bits	3 4 5	if bit 1 is 1 (non-audio)
	0 0 0	Digital data
	X X X	All other states of bits 3-5 are reserved
bits	6 7	Mode
	0 0	Mode 0 (defines bytes 1-3)
	X X	All other states of bits 6-7 are reserved

BYTE 1 - Category Code 001		
bits	3 4 5 6	Broadcast reception of digital audio
*	0 0 0 0	Japan
*	0 0 1 1	United States
*	1 0 0 0	Europe
*	0 0 0 1	Electronic software delivery
	X X X X	All other states are reserved

BYTE 1 - Category Code 100		
bits	3 4 5 6	Laser Optical
	0 0 0 0	CD - compatible with IEC-908
*	1 0 0 0	CD - not comp. with IEC-908 (magneto-optical)
	X X X X	All other states are reserved

BYTE 1								
bits	0	1	2	3	4	5	6	Category Code
	0	0	0	0	0	0	0	General
*					0	0	1	Experimental
					X	X	X	Reserved
*	0	0	0	1	X	X	X	Solid state memory
*	0	0	1	X	X	X	X	Broadcast recep. of digital audio
	0	1	0	X	X	X	X	Digital/digital converters
*	0	1	1	0	0	X	X	A/D converters w/o copyright
*					1	X	X	A/D converters w/ copyright (using Copy and L bits)
*	0	1	1	1	X	X	X	Broadcast recep. of digital audio
	1	0	0	X	X	X	X	Laser-optical
*	1	0	1	X	X	X	X	Musical Instruments, mics, etc.
	1	1	0	X	X	X	X	Magnetic tape or disk
	1	1	1	X	X	X	X	Reserved

bit	7	L: Generation Status.
		Only category codes: 001XXXX, 0111XXX, 100XXXX
*	0	Original/Commercially pre-recorded data
*	1	No indication or 1st generation or higher
		All other category codes
*	0	No indication or 1st generation or higher
*	1	Original/Commercially pre-recorded data

The subgroups under the category code groups listed above are described in tables below. Those not listed are reserved.

The Copy and L bits form a copy protection scheme for original works. Further explanations can be found in the proposed amendment (TC84) to IEC-958.

BYTE 1 - Category Code 010		
bits	3 4 5 6	Digital/digital conv. & signal processing
	0 0 0 0	PCM encoder/decoder
*	0 0 1 0	Digital sound sampler
*	0 1 0 0	Digital signal mixer
*	1 1 0 0	Sample-rate converter
	X X X X	All other states are reserved

Table 4. Consumer Channel Status Bytes 0 and 1

BYTE 1 - Category Code 101	
bits 3 4 5 6	Musical Instruments, mics, etc.
* 0 0 0 0	Synthesizer
* 1 0 0 0	Microphone
X X X X	All other states are reserved

BYTE 1 - Category Code 110	
bits 3 4 5 6	Magnetic tape or disk
0 0 0 0	DAT
* 1 0 0 0	Digital audio sound VCR
X X X X	All other states are reserved

BYTE 2	
bit 0 1 2 3	Source Number
0 0 0 0	Unspecified
1 0 0 0	1
0 1 0 0	2
1 1 0 0	3
0 0 1 0	4 to
0 1 1 1	14 (binary - 0 is LSB, 3 is MSB)
1 1 1 1	15
bit 4 5 6 7	Channel Number
0 0 0 0	Unspecified
1 0 0 0	A (Left in 2 channel format)
0 1 0 0	B (Right in 2 channel format)
1 1 0 0	C to
0 1 1 1	N (binary - 4 is LSB, 7 is MSB)
1 1 1 1	O

BYTE 3	
bits 0 1 2 3	Fs: Sample Frequency
0 0 0 0	44.1 kHz
0 1 0 0	48 kHz
1 1 0 0	32 kHz
X X X X	All other states of bits 0-3 are reserved
bits 4 5	Clock Accuracy
0 0	Level II, ±1000 ppm (default)
0 1	Level III, variable pitch
1 0	Level I, ±50 ppm - high accuracy
1 1	Reserved
bits 6 7	
X X	Reserved

BYTES 4 - 23
Reserved

* - Data from draft of IEC 958 proposed amendment (from TC84). Has not received approval yet.

Table 5. Consumer Channel Status Bytes 1-23

the category code and then utilizing the Copy and L bits to determine if a copy should be allowed. Digital processing of data should pass through the copy and L bits as defined by their particular category code. If mixing inputs, the highest level of protection of any one of the sources should be passed through. If the copy bit indicates no copy protection (copy = 1), then multiple copies can be made. If recording audio data to tape or disk, and any source has copy protection asserted, then the L bit must be used to determine whether the data can be recorded.

The L bit determines whether the source is an original (or prerecorded) work, or is a copy of an original work (first generation or higher). The actual meaning of the L bit can only be determined by looking at the category code since certain category codes reverse the meaning.

If the category code is CD (1000000) and the copy bit alternates at a 4 to 10 Hz rate, the CD is a copy of an original work that has copy protection asserted and no recording is permitted.

Appendix 9
Quartz crystals

(Reproduced by courtesy of SEI Ltd, a GEC company.)

The properties of a quartz crystal operating near to a frequency of resonance can be represented by an equivalent circuit consisting of an inductance (L_1) a capacitance (C_1) and a resistance (R_1), shunted by second capacitance (C_0). The elements L_1, C_1 and R_1 have no physical existence and are introduced to provide an electrical model of a vibrating crystal plate. The commonly used simplified equivalent circuit is shown as Figure 1.

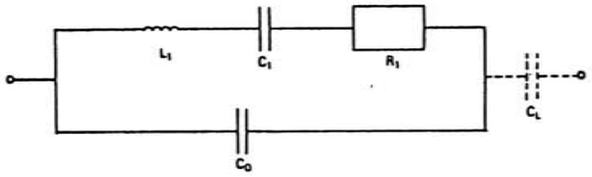


Figure 1.

The L_1, C_1, R_1 branch is known as the motional arm where L_1 is a function of the vibrating mass, C_1 represents the compliance and R_1 represents the sum of the crystal losses. C_0 is the sum of the capacitance between the crystal electrodes plus the capacitance introduced by the crystal terminals and the metal enclosure.

The crystal impedance varies rapidly in the immediate vicinity of the crystal resonance frequencies as shown in Figure 2. There are two zero phase frequencies, one at series resonance (f_s) and one at parallel or anti-resonance (f_a).

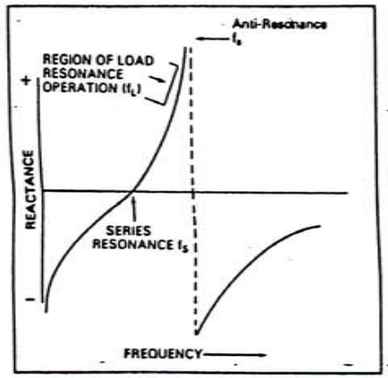


Figure 2.

Series Resonance. When a crystal is operating at series resonance its impedance at f_s is near to zero but a low active resistance remains which is known as the equivalent series resistance (ESR). The ESR value (expressed in ohms) is a measure of crystal activity and is used as an acceptance criterion. (See Appendix B).

Parallel or Anti-Resonance. When a crystal is operating at parallel resonance its impedance reaches its peak at f_a, as shown in Figure 2. Often the load circuit causes the reactive impedance to resonate in parallel or in series with the oscillator's load capacitance C_L. When a crystal is operating in this condition (f_L) the value of C_L should be precisely specified and to avoid instability the value of the load capacitance should be several times greater than the value of C_0. (Typical range of values for C_L = 20pF to 60pF.)

The frequency temperature characteristics of AT-Cut high frequency crystals show a cubic characteristic which, dependent upon the crystal plate design or mode of vibration, has an inflexion point which may be between +27°C and +31°C. By careful control of the crystal cutting angle the two turning points of the curve can be positioned to provide a minimum total deviation of the crystal frequency over a specified temperature range. The frequency/temperature characteristics for the AT-Cut, shown in Figure 3, are substantially valid for most fundamental and overtone types.

Typical frequency/temperature variations

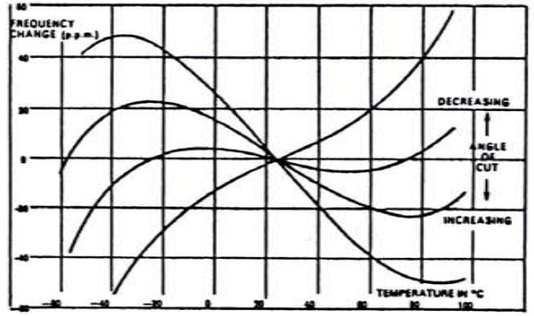


Figure 3.

7.2 IC specification used in these research project

APPLICATION INFORMATION

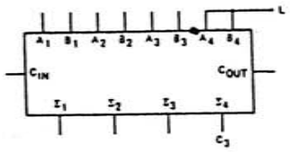


Fig. 7 3-bit adder.

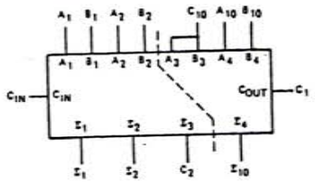


Fig. 8 2-bit and 1-bit adder.

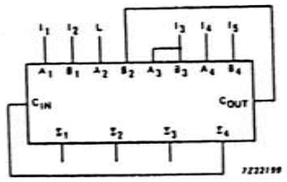


Fig. 9 5-input encoder.

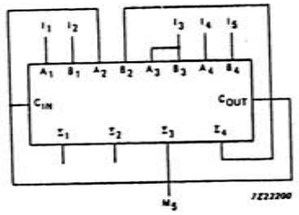


Fig. 10 5-input majority gate.

Note to Figs 7 to 10

Figure 7 shows a 3-bit adder using the "283". Tying the operand inputs of the fourth adder (A_3, B_3) LOW makes Σ_3 dependent on, and equal to, the carry from the third adder. Based on the same principle, Figure 8 shows a method of dividing the "283" into a 2-bit and 1-bit adder. The third stage adder (A_2, B_2, Σ_2) is used simply as means of transfering the carry into the fourth stage (via A_2 and B_2) and transfering the carry from the second stage on Σ_2. Note that as long as A_2 and B_2 are the same, HIGH or LOW, they do not influence Σ_2. Similary, when A_2 and B_2 are the same, the carry into the third stage does not influence the carry out of the third stage. Figure 9 shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs Σ_0, Σ_1 and Σ_2 produce a binary number equal to the number inputs (I_1 to I_5) that are HIGH. Figure 10 shows a method of implementing a 5-input majority gate. When three or more inputs (I_1 to I_5) are HIGH, the output M_5 is HIGH.

DIGITAL PHASE-LOCKED-LOOP FILTER

FEATURES

- Digital design avoids analog compensation errors
- Easily cascadable for higher order loops
- Useful frequency range:
  DC to 55 MHz typical (K-clock)
  DC to 35 MHz typical (I/D-clock)
- Dynamically variable bandwidth
- Very narrow bandwidth attainable
- Power-on reset
- Output capability: standard/bus driver
- I_{CC} category: MSI

SYMBOL	PARAMETER	CONDITIONS	TYPICAL HC	TYPICAL HCT	UNIT
t_{PHL}/t_{PLH}	propagation delay I/D_{CP} to I/D_{OUT}	C_L = 15 pF, V_{CC} = 5 V	15	18	ns
	ϕA_1, ϕB to $XORPD_{OUT}$		13	13	
	ϕB, ϕA_2 to $ECPD_{OUT}$		19	19	
f_{max}	maximum clock frequency K_{CP}		63	68	MHz
	I/D_{CP}		41	40	
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	18	19	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

GENERAL DESCRIPTION

The 74HC/HCT297 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT297 are designed to provide a simple, cost-effective solution to high-accuracy, digital, phase-locked-loop applications. These devices contain all the necessary circuits, with the exception of the divide-by-n counter, to build first order phase-locked-loops.

Both EXCLUSIVE-OR (XORPD) and edge-controlled (ECPD) phase detectors are provided for maximum flexibility. The input signals for the EXCLUSIVE-OR phase detector must have a 50% duty factor to obtain the maximum lock-range.

Proper partioning of the loop function, with many of the building blocks external to the package, makes it easy for the designer to incorporate ripple cancellation (see Fig. 7) or to cascade to higher order phase-locked-loops.

(continued on next page)

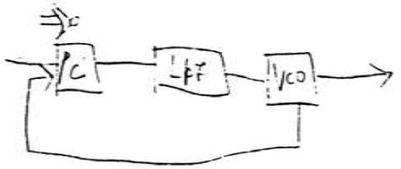
Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z).

16-lead mini-pack; plastic (SO16L; SOT162A).



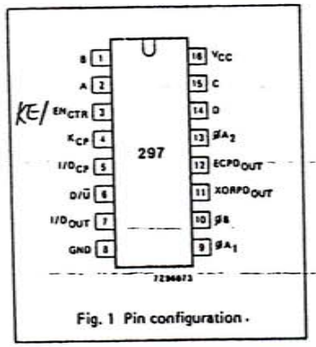


Fig. 1 Pin configuration.

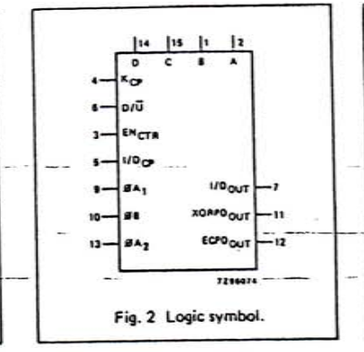


Fig. 2 Logic symbol.

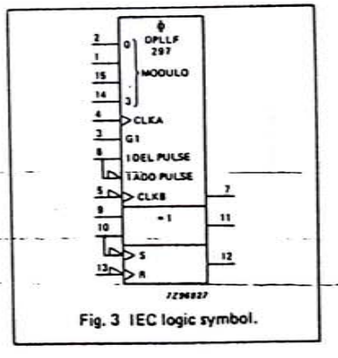


Fig. 3 IEC logic symbol.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
2, 1, 15, 14	A, B, C, D	modulo control inputs
3	EN_{CTR}	K-counter enable input
4	K_{CP}	K-counter clock input (LOW-to-HIGH, edge-triggered)
5	I/D_{CP}	increment/decrement clock input (HIGH-to-LOW, edge-triggered)
6	$D/\overline{U}$	down/up control
7	I/D_{OUT}	increment/decrement bus output
8	GND	ground (0 V)
9, 10, 13	ϕA_1, ϕB, ϕA_2	phase inputs
11	$XORPD_{OUT}$	EXCLUSIVE-OR phase detector output
12	$ECPD_{OUT}$	edge-controlled phase detector output
16	V_{CC}	positive supply voltage

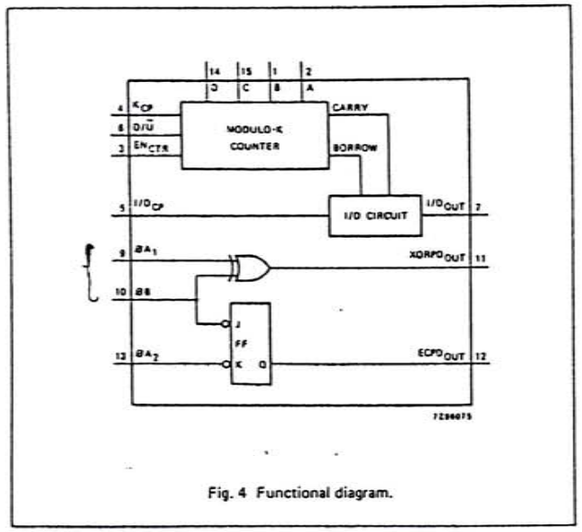


Fig. 4 Functional diagram.

K-COUNTER (DIGITAL CONTROL) FUNCTION TABLE

D	C	B	A	MODULO (K)
L	L	L	L	inhibited
L	L	L	H	2^2
L	L	H	L	2^4
L	L	H	H	2^5
L	H	L	L	2^6
L	H	L	H	2^7
L	H	H	L	2^8
L	H	H	H	2^9
H	L	L	L	2^{10}
H	L	L	H	2^{11}
H	L	H	L	2^{12}
H	L	H	H	2^{13}
H	H	L	L	2^{14}
H	H	L	H	2^{15}
H	H	H	L	2^{16}
H	H	H	H	2^{17}

EXCLUSIVE-OR PHASE DETECTOR FUNCTION TABLE

ϕA_1	ϕB	$XORPD_{OUT}$
L	L	L
L	H	H
H	L	H
H	H	L

EDGE-CONTROLLED PHASE DETECTOR TABLE

ϕA_2	ϕB	$ECPD_{OUT}$
H or L	↓	H
↓	H or L	L
H or L	↑	no change
↑	H or L	no change

H = HIGH voltage level
L = LOW voltage level
↓ = HIGH-to-LOW transition
↑ = LOW-to-HIGH transition

GENERAL DESCRIPTION

The length of the up/down K-counter is digitally programmable according to the K-counter function table. With, A, B, C and D all LOW, the K-counter is disabled. With A HIGH and B, C and D LOW, the K-counter is only three stages long, which widens the bandwidth of capture range and shortens the lock time of the loop. When A, B, C and D are all programmed HIGH, the K-counter becomes seventeen stages long, which narrows the bandwidth or capture range and lengthens the lock time. Real-time control of loop bandwith by manipulating the A to D inputs can maximize the overall performance of the digital phase-locked loop.

The "297" can perform the classic first-order phase-locked-loop function without using analog components. The accuracy of the digital phase-locked-loop (DPLL) is not affected by V_{CC} and temperature variations but depends solely on accuracies of the K-clock, I/D-clock and loop propagation delays.

The phase detector generates an error signal waveform that, at zero phase error, is a 50% duty factor square wave. At the limits of linear operation, the phase detector output will be either HIGH or LOW all of the time depending on the direction of the phase error ($\phi_{IN} - \phi_{OUT}$). Within these limits the phase detector output varies linearly with the input phase

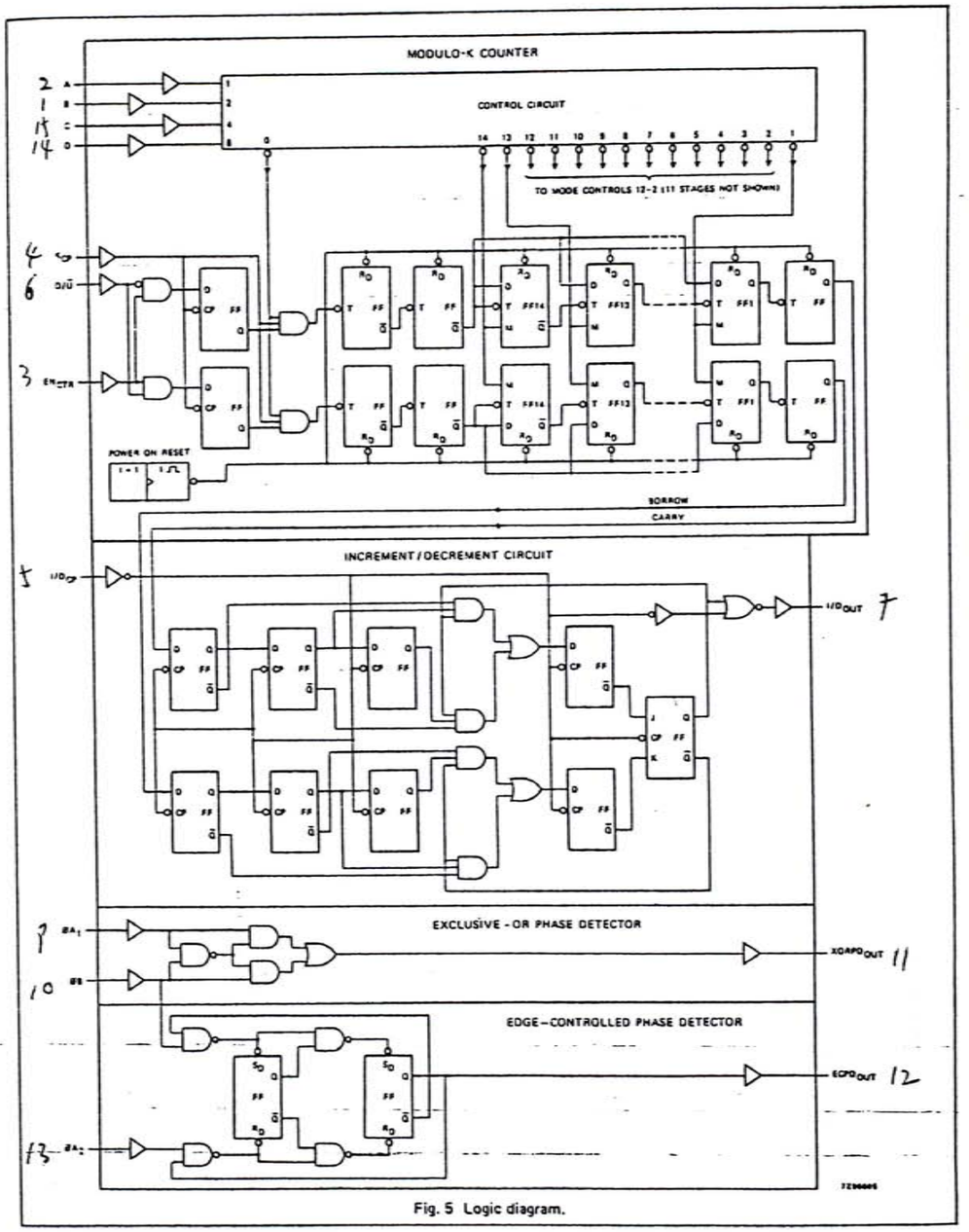


Fig. 5 Logic diagram.

GENERAL DESCRIPTION

error according to the gain k_d, which is expressed in terms of phase detector output per cycle or phase error. The phase detector output can be defined to vary between ± 1 according to the relation:

$$\text{phase detector output} = \frac{\%\,\text{HIGH} - \%\,\text{LOW}}{100}$$

The output of the phase detector will be $k_d\phi_e$, where the phase error $\phi_e = \phi_{IN} - \phi_{OUT}$.

EXCLUSIVE-OR phase detectors (XORPD) and edge-controlled phase detectors (ECPD) are commonly used digital types. The ECPD is more complex than the XORPD logic function but can be described generally as a circuit that changes states on one of the transitions of its inputs. The gain (k_d) for an XORPD is 4 because its output remains HIGH ($XORPD_{OUT}$ = 1) for a phase error of 1/4 cycle.

Similarly, k_d for the ECPD is 2 since its output remains HIGH for a phase error of 1/2 cycle. The type of phase detector will determine the zero-phase-error point, i.e., the phase separation of the phase detector inputs for a ϕ_e defined to be zero. For the basic DPLL system of Fig. 6 ϕ_e = 0 when the phase detector output is a square wave.

The XORPD inputs are 1/4 cycle out-of-phase for zero phase error. For the ECPD, ϕ_e = 0 when the inputs are 1/2 cycle out-of-phase.

The phase detector output controls the up/down input to the K-counter. The counter is clocked by input frequency Mf_c, which is a multiple M of the loop centre frequency f_c. When the K-counter recycles up, it generates a carry pulse. Recycling while counting down generates a borrow pulse. If the carry and the borrow outputs are conceptually combined into one output that is positive for a carry and negative for a borrow, and if the K-counter is considered as a frequency divider with the ratio Mf_c/K, the output of the K-counter will equal the input frequency multiplied by the division ratio. Thus the output from the K-counter is $(k_d\phi_e Mf_c)/K$.

The carry and borrow pulses go to the increment/decrement (I/D) circuit which, in the absence of any carry or borrow pulses has an output that is 1/2 of the input clock (I/D_{CP}). The input clock is just a multiple, 2N, of the loop centre frequency. In response to a carry or borrow pulse, the I/D circuit will either add or delete a pulse at I/D_{OUT}. Thus the output of the I/D circuit will be $Nf_c + (k_d\phi_e Mf_c)/2K$.

The output of the N-counter (or the output of the phase-locked-loop) is thus: $f_o = f_c + (k_d\phi_e Mf_c)/2KN$.

If this result is compared to the equation for a first-order analog phase-locked-loop, the digital equivalent of the gain of the VCO is just $Mf_c/2KN$ or f_c/K for M = 2N.

Thus the simple first-order phase-locked-loop with an adjustable K-counter is the equivalent of an analog phase-locked-loop with a programmable VCO gain.

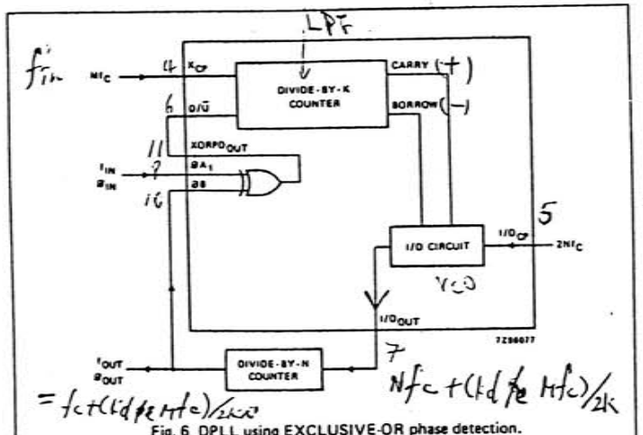


Fig. 6 DPLL using EXCLUSIVE-OR phase detection.

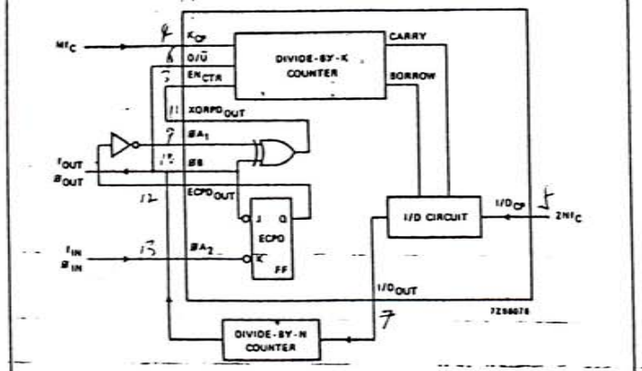


Fig. 7 DPLL using both phase detectors in a ripple-cancelation scheme.

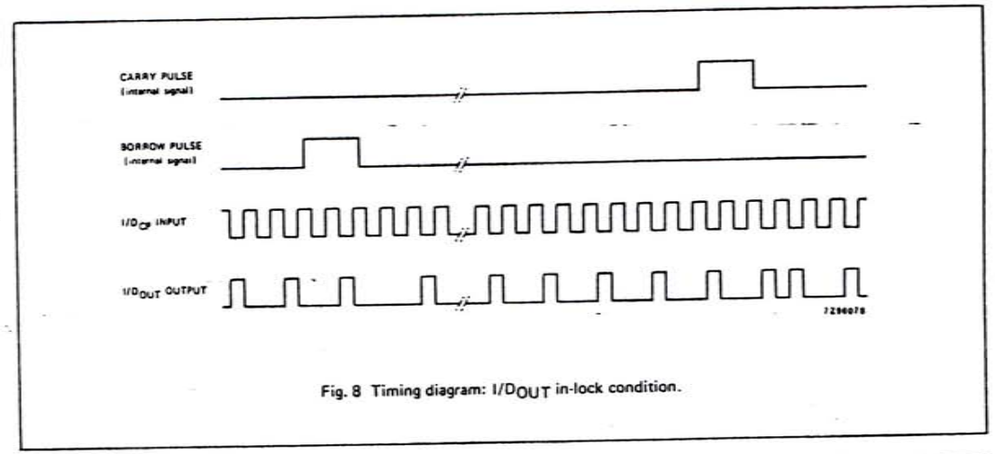


Fig. 8 Timing diagram: I/D_{OUT} in-lock condition.

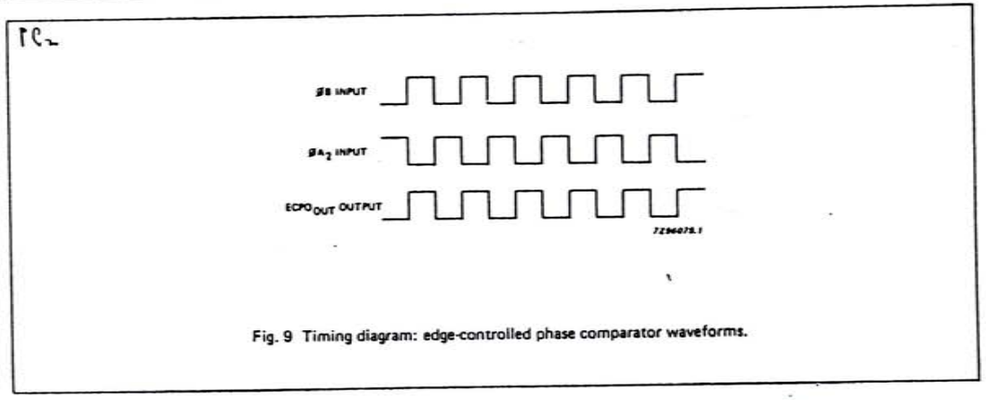


Fig. 9 Timing diagram: edge-controlled phase comparator waveforms.

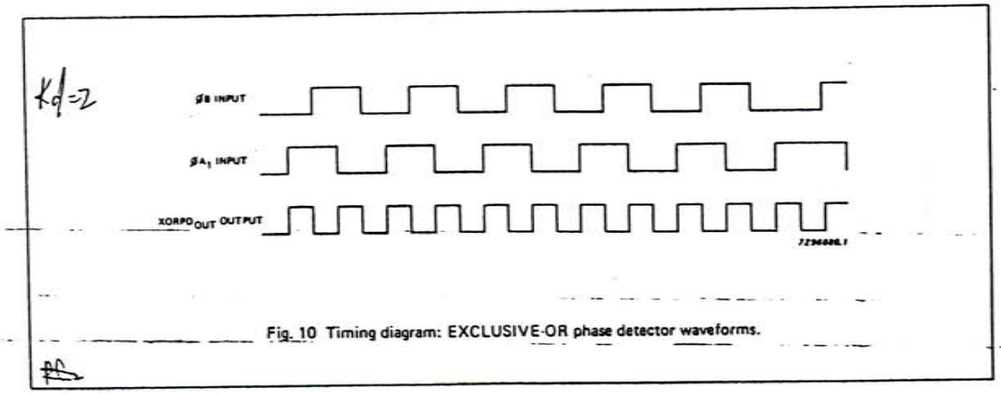


Fig. 10 Timing diagram: EXCLUSIVE-OR phase detector waveforms.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard/bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C) 74HC +25 min.	+25 typ.	+25 max.	−40 to +85 min.	−40 to +85 max.	−40 to +125 min.	−40 to +125 max.	UNIT	TEST CONDITIONS V_{CC} V	TEST CONDITIONS WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay I/D_{CP} to I/D_{OUT}		50 18 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 11
t_{PHL}/t_{PLH}	propagation delay ϕA_1, ϕB to $XORPD_{OUT}$		44 16 13	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig. 12
t_{PHL}/t_{PLH}	propagation delay ϕB, ϕA_2 to $ECPD_{OUT}$		61 22 18	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig. 13
t_{THL}/t_{TLH}	output transition time: bus driver output; I/D_{OUT} (pin 7)		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 11
t_{THL}/t_{TLH}	output transition time: standard outputs; $XORPD_{OUT}$, $ECPD_{OUT}$ (pins 11, 12)		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 12 and 13
t_W	clock pulse width K_{CP}	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 14
t_W	clock pulse width I/D_{CP}	100 20 17	28 10 8		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig. 11
t_{su}	set-up time $D/\overline{U}$, EN_{CTR} to K_{CP}	120 24 20	33 12 10		150 30 26		180 36 31		ns	2.0 4.5 6.0	Fig. 14
t_h	hold time $D/\overline{U}$, EN_{CTR} to K_{CP}	0 0 0	−19 −7 −6		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig. 14
f_{max}	maximum clock pulse frequency K_{CP}	6.0 30 35	19 57 68		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 14
f_{max}	maximum clock pulse frequency I/D_{CP}	4.0 20 24	12 37 44		3.2 16 19		2.6 13 15		MHz	2.0 4.5 6.0	Fig. 11

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard/bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
EN_{CTR}, $D/\overline{U}$	0.3
A, B, C, D, K_{CP}, ϕA_2	0.6
I/D_{CP}, ϕA_1, ϕB	1.5

AC CHARACTERISTICS FOR 74HCT

GND = 0 V, $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C) 74HCT +25 min.	+25 typ.	+25 max.	−40 to +85 min.	−40 to +85 max.	−40 to +125 min.	−40 to +125 max.	UNIT	TEST CONDITIONS V_{CC} V	TEST CONDITIONS WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay I/D_{CP} to I/D_{OUT}		21	35		44		53	ns	4.5	Fig. 11
t_{PHL}/t_{PLH}	propagation delay ϕA_1, ϕB to $XORPD_{OUT}$		16	32		40		48	ns	4.5	Fig. 12
t_{PHL}/t_{PLH}	propagation delay ϕB, ϕA_2 to $ECPD_{OUT}$		22	44		55		66	ns	4.5	Fig. 13
t_{THL}/t_{TLH}	output transition time bus driver output I/D_{OUT} (pin 7)		5	12		15		18	ns	4.5	Fig. 11
t_{THL}/t_{TLH}	output transition time standard outputs $XORPD_{OUT}$, $ECPD_{OUT}$ (pins 11, 12)		7	15		19		22	ns	4.5	Figs 12 and 13
t_W	clock pulse width K_{CP}	16	8		20		24		ns	4.5	Fig. 14
t_W	clock pulse width I/D_{CP}	25	13		31		38		ns	4.5	Fig. 11
t_{su}	set-up time $D/\overline{U}$, EN_{CTR} to K_{CP}	24	13		30		36		ns	4.5	Fig. 14
t_h	hold time $D/\overline{U}$, EN_{CTR} to K_{CP}	0	−8		0		0		ns	4.5	Fig. 14
f_{max}	maximum clock pulse frequency K_{CP}	30	62		24		20		MHz	4.5	Fig. 14
f_{max}	maximum clock pulse frequency I/D_{CP}	20	36		16		13		MHz	4.5	Fig. 11

AC WAVEFORMS

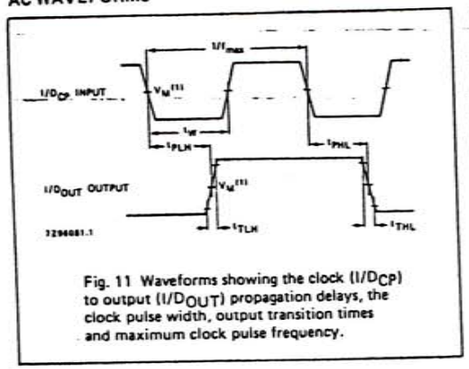


Fig. 11 Waveforms showing the clock (I/D_{CP}) to output (I/D_{OUT}) propagation delays, the clock pulse width, output transition times and maximum clock pulse frequency.

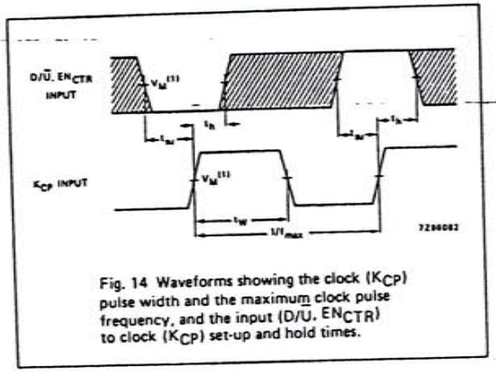


Fig. 14 Waveforms showing the clock (K_{CP}) pulse width and the maximum clock pulse frequency, and the input (D/$\overline{U}$, EN_{CTR}) to clock (K_{CP}) set-up and hold times.

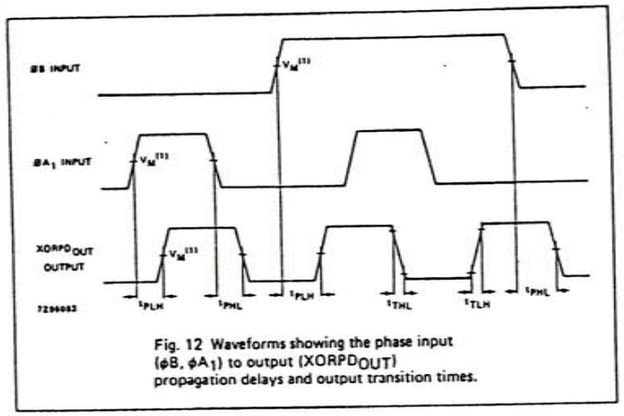


Fig. 12 Waveforms showing the phase input (ϕB, ϕA_1) to output ($XORPD_{OUT}$) propagation delays and output transition times.

Note to Fig. 14

The shaded areas indicate when the input is permitted to change for predictable output performance.

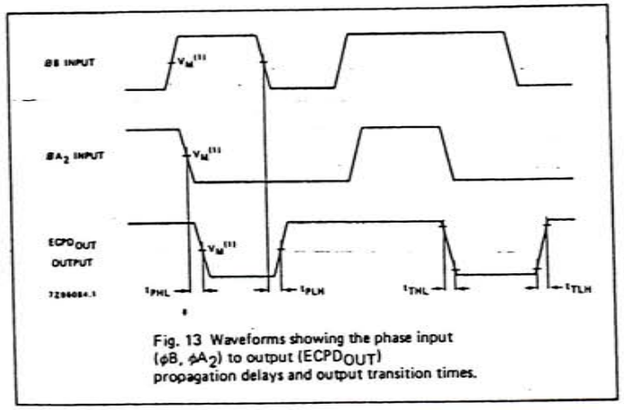


Fig. 13 Waveforms showing the phase input (ϕB, ϕA_2) to output ($ECPD_{OUT}$) propagation delays and output transition times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

8-BIT UNIVERSAL SHIFT REGISTER; 3-STATE

FEATURES

- Multiplexed inputs/outputs provide improved bit density
- Four operating modes: shift left
  shift right
  hold (store)
  load data
- Operates with output enable or at high-impedance OFF-state (Z)
- 3-state outputs drive bus lines directly
- Can be cascaded for n-bits word length
- Output capability:
  bus driver (parallel I/Os)
  standard (serial outputs)
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT299 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT299 contain eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift-right, shift-left, parallel load and hold operations. The type of operation is determined by the mode select inputs (S_0 and S_1), as shown in the mode select table.

All flip-flop outputs have 3-state buffers to separate these outputs (I/O_0 to I/O_7) such, that they can serve as data inputs in the parallel load mode. The serial outputs (Q_0 and Q_7) are used for expansion in serial shifting of longer words.

(continued on next page)

SYMBOL	PARAMETER	CONDITIONS	TYPICAL HC	TYPICAL HCT	UNIT
t_{PHL}/t_{PLH}	propagation delay CP to Q_0, Q_7	C_L = 15 pF; V_{CC} = 5 V	20	19	ns
	CP to I/O_n		20	19	ns
t_{PHL}	$\overline{MR}$ to Q_0, Q_7 or I/O_n		20	23	ns
f_{max}	maximum clock frequency		50	46	MHz
C_I	input capacitance		3.5	3.5	pF
$C_{I/O}$	input/output capacitance		10	10	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	120	125	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

20-lead DIL; plastic (SOT146).
20-lead mini-pack; plastic (SO20; SOT163A).

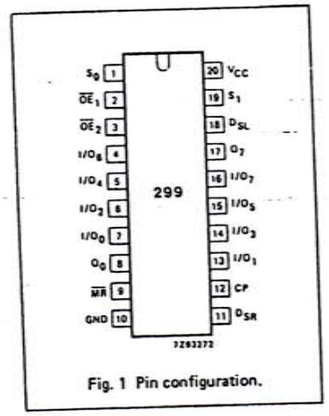


Fig. 1 Pin configuration.

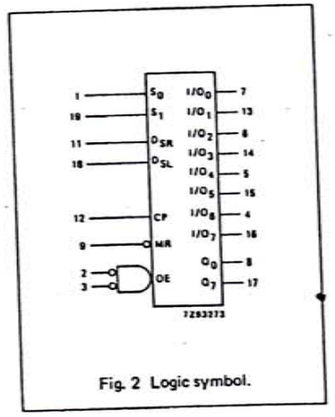


Fig. 2 Logic symbol.

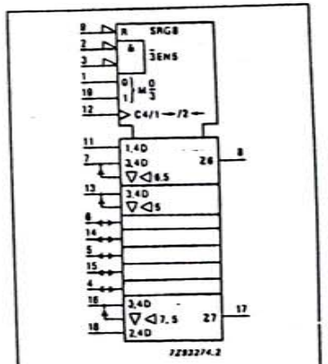


Fig. 3 IEC logic symbol.

CRYSTAL
Semiconductor Corporation

CS8411 CS8412

Digital Audio Interface Receiver

Features

- Monolithic CMOS Receiver
- Low-Jitter, On-Chip Clock Recovery
  256×Fs Output Clock Provided
- Supports: AES/EBU, IEC 958,
  S/PDIF, & EIAJ CP-340
  Professional and Consumer Formats
- Extensive Error Reporting
  Repeat Last Sample on Error Option
- On-Chip RS422 Line Receiver
- Configurable Buffer Memory (CS8411)

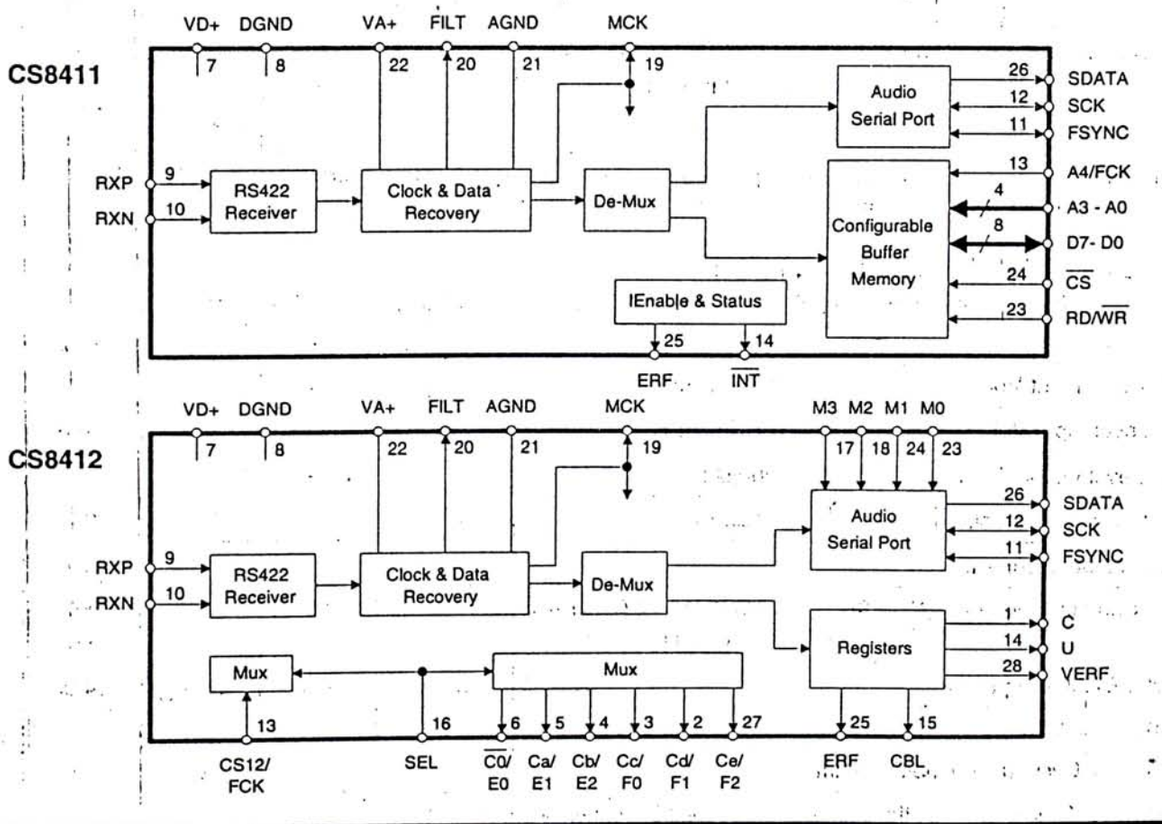
General Description:

The CS8411/12 are monolithic CMOS devices which receive and decode audio data according to the AES/EBU, IEC 958, S/PDIF, & EIAJ CP-340 interface standards. The CS8411/12 receive data from a transmission line, recover the clock and synchronization signals, and de-multiplex the audio and digital data. Differential or single ended inputs can be decoded.

The CS8411 has a configurable internal buffer memory, read via a parallel port, which may be used to buffer channel status, auxiliary data, and/or user data.

The CS8412 de-multiplexes the channel, user, and validity data directly to serial output pins with dedicated output pins for the most important channel status bits.

5



Preliminary Product Information This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

YAMAHA LSI

YM3436D

Digital audio Interface Receiver (DIR2)

■ OUTLINE

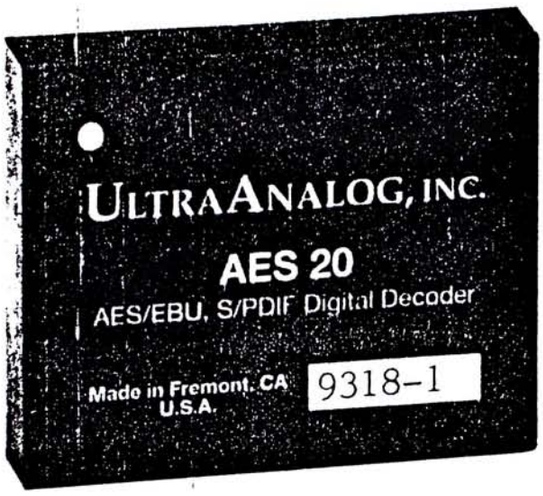
The YM3436D(DIR2) receives and demodulates the digital audio interface format signals, conforming with the EIAJ CP-340 or AES/EBU. Comparing to the YM3623B(DIR), external synchronization and error processing functions are further improved and it is made applicable more widely by using the channel status and user data outputs.

■ FEATURES

- Capable to accept the A/D input and asynchronous input as well as the digital audio interface signal input.
- As a phase comparator and VCO are built in, a PLL circuit synchronized with the external input can be formed easily (fs=32kHz~48kHz)
- Capable to demodulate the digital audio interface signal and output 24-bit 2-channel audio data and control data.
- As a clock master, it supplies various kinds of clock signals to the other LSIs.
- The built-in asynchronous buffer enables the output phase to be retained even on clock switching. Also capable of easy interface between the equipments where full synchronization is impossible such as when several digital audio interface signals are received simultaneously.
- Detects transmission errors and reception errors and executes error processing of data hold and muting.
- Executes decoding and output of the validity flag, channel status, user data as control data. Especially, the channel status conforms with both Consumer use and Professional use formats. Also, information can be read out microprocessor interface.
- 5V power supply, Si-gate CMOS, 44-pin QFP.

YAMAHA CORPORATION

YM3436C CATALOG
CATALOG No. : LSI-2134365
1993. 07



ULTRAANALOG, INC.
Advancing the Analog Art.

AES20/AES21

Ultra-Low Jitter AES/EBU Receiver

vision 2, see Note 4, page 5.

Features

- 1 kHz jitter attenuation corner frequency
- AES/EBU and S/PDIF formats
- Internal low-jitter D flip-flop
- Transformer isolated (AES 20 only)
- 16, 18, 20 and 24 bit data output formats
- 28 to 55 kHz sampling rates

Description

The UltraAnalog AES20/AES21 is complete AES/EBU and S/PDIF ceiver. It is designed to provide the ter performance required by today's gh-resolution digital-to-analog and nalog-to-digital converters, perfor- ance not yet possible in monolithic rcuits. In a 2.05" L x 1.65" W x 0.46" H 2 x 41 x 12 mm) shielded module, the AES20/AES21 provides the following functions:

- data extraction,
- control and user bits extraction,
- actual incoming frequency measurement,
- error detection and reporting,
- low jitter clock generation and regeneration.

In addition, the AES20 has impedance matched, transformer isolated inputs for both AES and S/PDIF signals, therefore reducing the number of required external components.

Necessity for Low-Jitter Clock Recovery

In any system using a receiver, the recovered clock is going to be used as the master clock for a D/A converter or an A/D converter. It is necessary for this master clock to have as little jitter as possible. The jitter of a repetitive signal, such as a clock, can be defined as follows:

The jitter of a repetitive signal is the sequence of the timing differences between this signal and a perfectly timed signal with the same frequency and average phase.

This definition can be modified to include only the signal edges actually contributing to the system performance. For an 8 times oversampling D/A converter for example, it would be the clock edges causing the analog output voltage to change.

The jitter is a sequence of time error values. Like for any such sequence, a spectrum can be computed on the jitter. This spectrum is used to determine the impact of the clock jitter on the system performance. In the case of an 8 times over-sampling D/A converter, for instance, the conversion error signal caused by the clock jitter can be shown to be made of pulses, each equal to the product of a clock edge timing error by the voltage change associated with this clock edge. (See Fig. 1.) The resulting train of pulses is then filtered by the low-pass filters and the rest of the chain to produce an audible signal. (See Note 1 below.*)

*NOTE 1: In the time domain, the pulses have the following value:

$$u(kT) = [v(kT) - v((k-1)T)]\, p(kT)$$ with: $V(kT)$ = DAC voltage at time kT, $p(kT)$ = timing error at time kT

In the frequency domain, the pulse spectrum is:

$$U(\omega) = \sum_{k=-\infty}^{+\infty} u(kT)\, e^{-j\omega kT} = \frac{T}{2\pi} \int_{-\frac{\pi}{T}}^{\frac{\pi}{T}} X(\omega)\, P(\omega-\omega_1)\, d\omega_1$$

with: $X(\omega)$ = Fourier transform of $V(kT) - V((k-1)T)$, $P(\omega)$ = Fourier transform of $p(kT)$

Semiconductor Corporation

CS8401A CS8402A

Digital Audio Interface Transmitter

Features

- Monolithic Digital Audio Interface Transmitter
- Supports: AES/EBU, IEC 958, S/PDIF, & EIAJ CP-340 Professional and Consumer Formats
- Host Mode and Stand Alone Modes
- Generates CRC Codes and Parity Bits
- On-Chip RS422 Line Driver
- Configurable Buffer Memory (CS8401A)
- Transparent Mode Allows Direct Connection of CS8402A and CS8412 or CS8401A and CS8411A

General Description

The CS8401/2A are monolithic CMOS devices which encode and transmit audio data according to the AES/EBU, IEC 958, S/PDIF, & EIAJ CP-340 interface standards. The CS8401/2A accept audio and digital data, which is then multiplexed, encoded and driven onto a cable. The audio serial port is double buffered and capable of supporting a wide variety of formats.

The CS8401A has a configurable internal buffer memory, loaded via a parallel port, which may be used to buffer channel status, auxiliary data, and/or user data.

The CS8402A multiplexes the channel, user, and validity data directly from serial input pins with dedicated input pins for the most important channel status bits.

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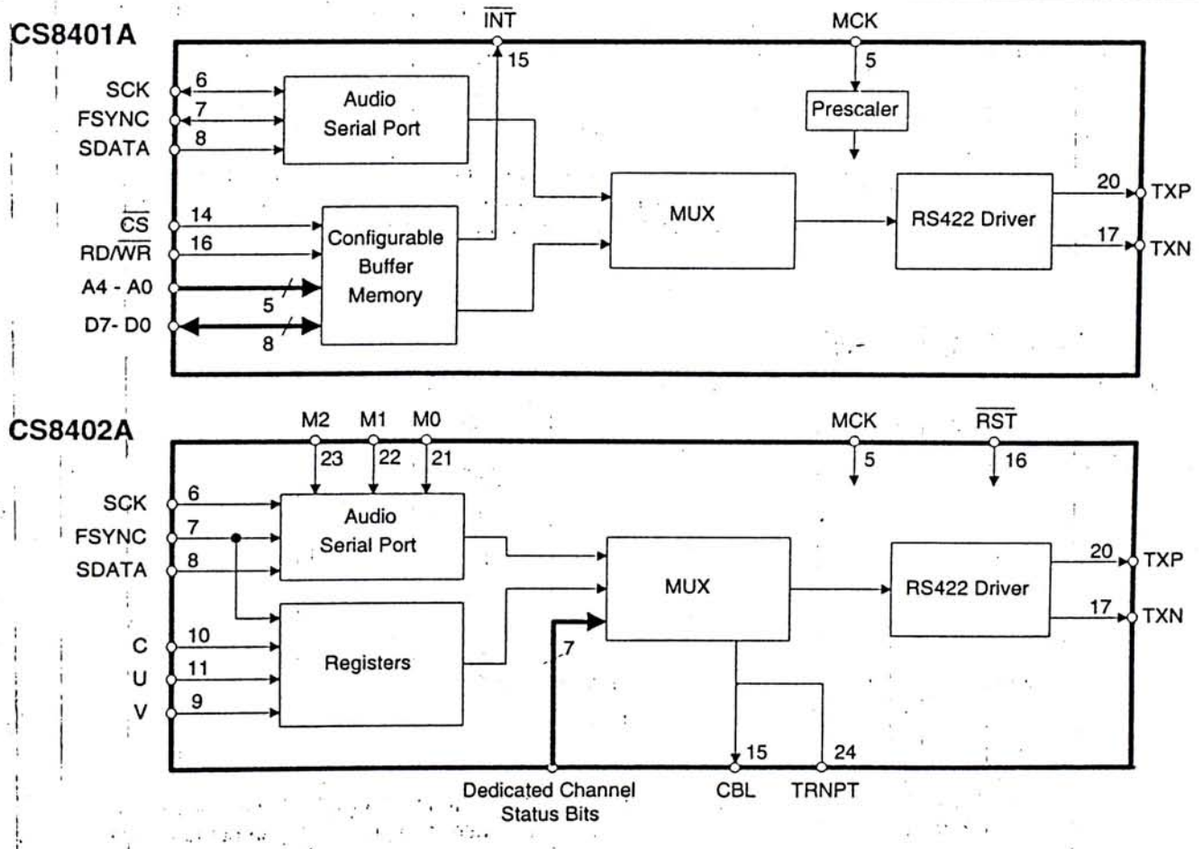


A Cirrus Logic Company

CS8403A CS8404A

96 kHz Digital Audio Transmitter

Features

- Sample rates up to 108 kHz
- Supports: AES/EBU, IEC 958, S/PDIF, & EIAJ CP-340 professional and consumer formats
- Generates CRC codes and parity bits
- On-Chip RS422 line driver
- Configurable buffer memory (CS8403A)
- Transparent mode allows direct connection of CS8404A and CS8414 or CS8403A and CS8413
- Pin compatible with CS8401A and CS8402A

Description

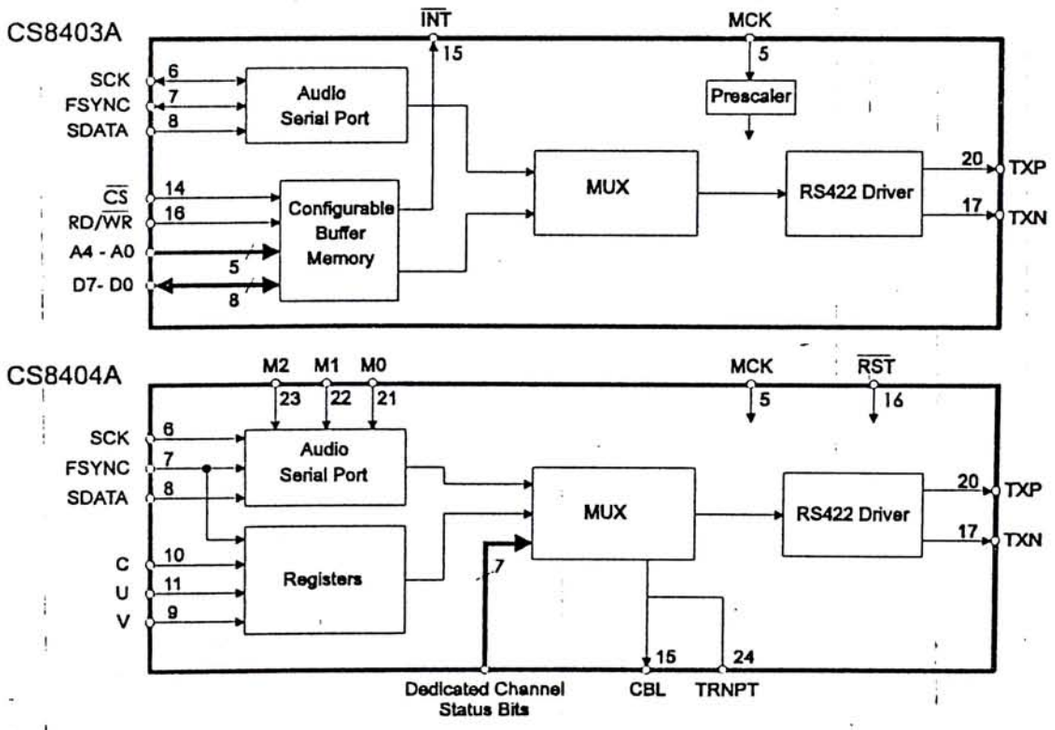
The CS8403A and CS8404A are digital audio transmitters which support 96 kHz sample rate operation. The devices encode and transmit audio data according to the AES/EBU, IEC958, S/PDIF, & EIAJ CP-340 interface standards. The CS8403A and CS8404A accept audio and digital data, which is then multiplexed, encoded and driven onto a cable. The audio serial port is double buffered and capable of supporting a wide variety of formats.

The CS8403A has a configurable internal buffer memory, loaded via a parallel port, which may be used to buffer channel status, auxiliary data, and/or user data.

The CS8404A multiplexes the channel, user, and validity data directly from serial input pins with dedicated input pins for the most important channel status bits.

ORDERING INFO

CS8403A-CS, 0 to 70 °C, 24-pin Plastic SOIC
CS8404A-CS, 0 to 70 °C, 24-pin Plastic SOIC



Preliminary Product Information

This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, Texas 78760
(512) 445 7222 FAX: (512) 445 7581
http://www.crystal.com

YAMAHA LSI

YM3437C

Digital Audio Interface Transmitter (DIT2)

■ OUTLINE

The YM3437C (DIT2) is a serial digital audio transmitter LSI. DIT2 can convert ④ different kinds of serial digital audio data into EIAJ CP-340 or AES/EBU digital audio interface format. It has capabilities of outputting with the 24-bit output and also setting the channel status, user data, etc.

■ FEATURES

- Operation synchronous with the external clock signals inputted through the MCLK terminal.
- Useable for either 24-bit output by using the auxiliary bit of the digital audio interface signal or 20-bit output.
- All of the validity flag, channel status and user data can be set as a control code.
  Synchronous mode; All bits of the validity flag, channel status and user data can be set synchronous with the audio data.
  Asynchronous mode; The first 32 bits of each of the channel status and user data can be set independently from the audio data timing.
- The output data can be muted according to the MUTE signal from outside.
- 5V power supply, Si-gate CMOS, 16-pin DIP and 16-pin SOP.

YAMAHA CORPORATION

YM3437C CATALOG
CATALOG No. : LSI-2134372
1992. 02

Clock Recovery and Data Retiming Phase-Locked Loop

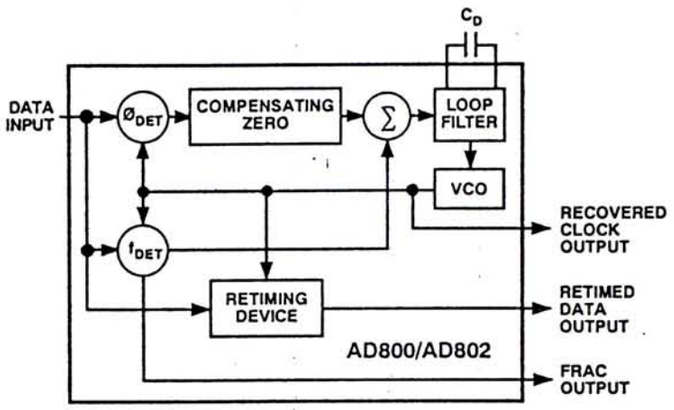
AD800/AD802*

FEATURES

Standard Products
- 44.736 Mbps—DS-3
- 51.84 Mbps—STS-1
- 155.52 Mbps—STS-3 or STM-1

Accepts NRZ Data, No Preamble Required
Recovered Clock and Retimed Data Outputs
Phase-Locked Loop Type Clock Recovery—No Crystal Required
Random Jitter: 20° Peak-to-Peak
Pattern Jitter: Virtually Eliminated
10KH ECL Compatible
Single Supply Operation: −5.2 V or +5 V
Wide Operating Temperature Range: −40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD800 and AD802 employ a second order phase-locked loop architecture to perform clock recovery and data retiming on Non-Return to Zero, NRZ, data. This architecture is capable of supporting data rates between 20 Mbps and 160 Mbps. The products described here have been defined to work with standard telecommunications bit rates. 45 Mbps DS-3 and 52 Mbps STS-1 are supported by the AD800-45 and AD800-52 respectively. 155 Mbps STS-3 or STM-1 are supported by the AD802-155.

Unlike other PLL-based clock recovery circuits, these devices do not require a preamble or an external VCXO to lock onto input data. The circuit acquires frequency and phase lock using two control loops. The frequency acquisition control loop initially acquires the clock frequency of the input data. The phase-lock loop then acquires the phase of the input data, and ensures that the phase of the output signals track changes in the phase of the input data. The loop damping of the circuit is dependent on the value of a user selected capacitor; this defines jitter peaking performance and impacts acquisition time. The devices exhibit 0.08 dB jitter peaking, and acquire lock on random or scrambled data within 4×10^5 bit periods when using a damping factor of 5.

During the process of acquisition the frequency detector provides a Frequency Acquisition (FRAC) signal which indicates that the device has not yet locked onto the input data. This signal is a series of pulses which occur at the points of cycle slip between the input data and the synthesized clock signal. Once the circuit has acquired frequency lock no pulses occur at the FRAC output.

The inclusion of a precisely trimmed VCO in the device eliminates the need for external components for setting center frequency, and the need for trimming of those components. The VCO provides a clock output within ±20% of the device center frequency in the absence of input data.

The AD800 and AD802 exhibit virtually no pattern jitter, due to the performance of the patented phase detector. Total loop jitter is 20° peak-to-peak. Jitter bandwidth is dictated by mask programmable fractional loop bandwidth. The AD800, used for data rates < 90 Mbps, has been designed with a nominal loop bandwidth of 0.1% of the center frequency. The AD802, used for data rates in excess of 90 Mbps, has a loop bandwidth of 0.08% of center frequency.

All of the devices operate with a single +5 V or −5.2 V supply.

*Protected by U.S. Patent No. 5,027,085.

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703

SamplePort Stereo Asynchronous Sample Rate Converters

AD1890/AD1891

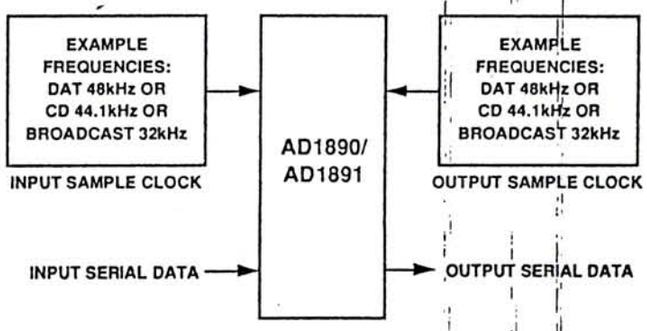
FEATURES

- Automatically Sense Sample Frequencies—No Programming Required
- Tolerant of Sample Clock Jitter
- Smooth Transition When Sample Clock Frequencies Cross
- Accommodate Dynamically Changing Asynchronous Sample Clocks
- 8 kHz to 56 kHz Sample Clock Frequency Range
- 1:2 to 2:1 Ratio Between Sample Clocks
- −106 dB THD+N at 1 kHz (AD1890)
- 120 dB Dynamic Range (AD1890)
- Optimal Clock Tracking Control
  - −Short/Long Group Delay Modes
  - −Slow/Fast Settling Modes
- Linear Phase in All Modes
- Equivalent of 4 Million 22-Bit FIR Filter Coefficients Stored On-Chip
- Automatic Output Mute
- Flexible Four Wire Serial Interfaces
- Low Power

APPLICATIONS

- Digital Mixing Consoles and Digital Audio Workstations
- CD-R, DAT, DCC and MD Recorders
- Multitrack Digital Audio and Video Tape Recorders
- Studio to Transmitter Links
- Digital Audio Signal Routers/Switches
- Digital Audio Broadcast Equipment
- High Quality D/A Converters
- Digital Tape Recorder Varispeed Applications
- Computer Communication and Multimedia Systems

SYSTEM DIAGRAM



PRODUCT OVERVIEW

The AD1890 and AD1891 SamplePorts™ are fully digital, stereo Asynchronous Sample Rate Converters (ASRCs) that solve sample rate interfacing and compatibility problems in digital audio equipment. Conceptually, these converters interpolate the input data up to a very high internal sample rate with a time resolution of 300 ps, then decimate down to the desired output sample rate. The AD1890 is intended for 18- and 20-bit professional applications, and the AD1891 is intended for 16-bit lower cost applications where large dynamic sample-rate changes are not encountered. These devices are asynchronous because the frequency and phase relationships between the input and output sample clocks (both are inputs to the AD1890/AD1891 ASRCs) are arbitrary and need not be related by a simple integer ratio. There is no need to explicitly select or program the input and output sample clock frequencies, as the AD1890/AD1891 automatically sense the relationship between the two clocks. The input and output sample clock frequencies can nominally range from 8 kHz to 56 kHz, and the ratio between them can vary from 1:2 to 2:1.

The AD1890/AD1891 use multirate digital signal processing techniques to construct an output sample stream from the input sample stream. The input word width is 4 to 20 bits for the AD1890 or 4 to 16 bits for the AD1891. Shorter input words are automatically zero-filled in the LSBs. The output word width for both devices is 24 bits. The user can receive as many of the output bits as desired. Internal arithmetic is performed with 22-bit coefficients and 27-bit accumulation. The digital samples are processed with unity gain.

The input and output control signals allow for considerable flexibility for interfacing to a variety of DSP chips, AES/EBU receivers and transmitters and for I²S compatible devices. Input and output data can be independently justified to the left/right clock edge, or delayed by one bit clock from the left/right clock edge. Input and output data can also be independently justified to the word clock rising edge or delayed by one bit clock from the word clock rising edge. The bit clocks can also be independently configured for rising edge active or falling edge active operation.

The AD1890/AD1891 SamplePort™ ASRCs have on-chip digital coefficients that correspond to a highly oversampled 0 kHz to 20 kHz low-pass filter with a flat passband, a very narrow transition band, and a high degree of stopband attenuation. A subset of these filter coefficients are dynamically chosen on the basis of the filtered instantaneous ratio between the input sample clock ($\overline{LR}$_I) and the output sample clock ($\overline{LR}$_O), and these coefficients are used in an FIR convolver to perform the sample rate conversion. Refer to the "Theory of Operation" section of this data sheet for a more thorough functional description. The low-pass filter has been designed so that full 20 kHz bandwidth is maintained when the input and output sample clock frequencies are as low as 44.1 kHz. If the output sample rate drops below the input sample rate, the bandwidth of the input signal is

(continued on Page 4)

REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703

OVERVIEW

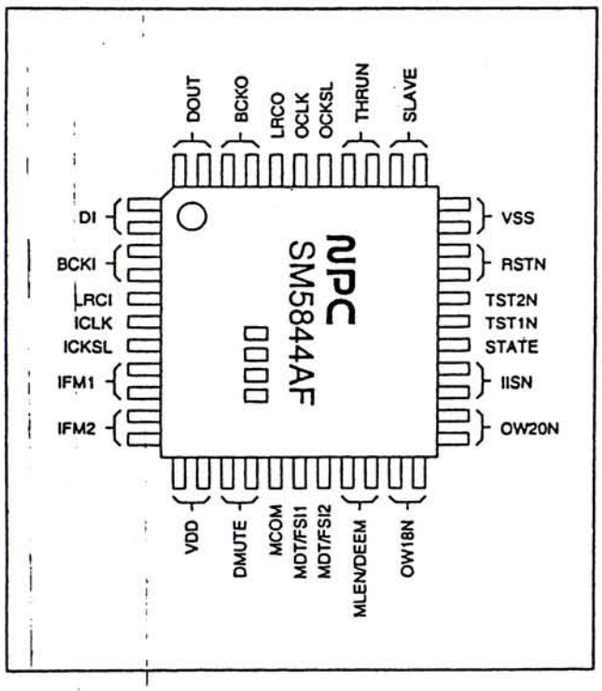
The SM5844AF is a digital audio signal, asynchronous sample rate converter LSI. It reads 16 or 20-bit word length input data, and writes 16, 18, or 20-bit word length output data. It also features a built-in digital deemphasis filter and digital attenuator.

The SM5844AF operates from a 5 V supply, and is available in 44-pin QFPs.

APPLICATIONS

- Digital audio equipment, sample rate conversion (audiovisual amplifiers, CD-R, DAT, MD and 8 mm VTRs)
- Commercial recording/editing equipment, sample rate conversion
- Input data jitter elimination

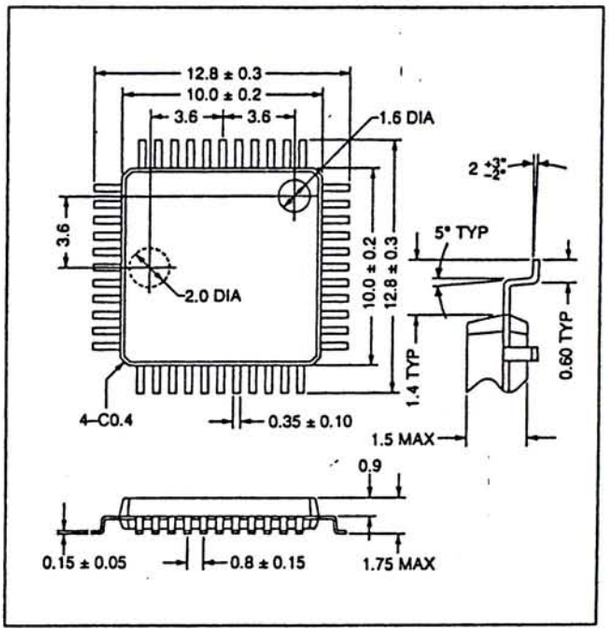
PINOUT



PACKAGE DIMENSIONS

Unit: mm

44-pin QFP



FEATURES

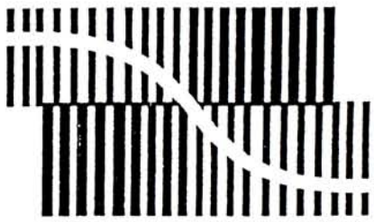
Functions

- Left/right-channel processing (stereo)
- Input sample rate (fsi) ranges
  - 24 to 48 kHz (256fsi mode)
  - 27 to 55 kHz (384fsi mode)
- Output sample rate (fso) range
  - 20 to 100 kHz
- Sample rate conversion ratio (fso/fsi)
  - 0.5 to 2.0 times
- Asynchronous input and output timing (clock inputs)
- System clock inputs (input and output clocks independent)
  - 256fsi or 384fsi input system clock
  - 256fso or 384fso output system clock
- Deemphasis filter
  - IIR-type filter
  - 44.1, 48 or 32 kHz
- Digital attenuator
  - 11-bit data for 1025 levels
  - Smooth, incremental attenuation change
  - +12 dB gain shift function

General Digital Input (GDIN) TDA1373H

FEATURES

- Four operating modes:
  - Sample Rate Conversion (SRC) mode
  - AD/DA mode
  - SLAVE-VCO mode
  - SLAVE-VCXO mode
- Full digital sample rate conversion over a wide range of input sample rates
- Fast and automatic detection and locking to the input sample rate with continuous tracking
- Digital Phase-Locked Loop (PLL) with adaptive bandwidth which removes jitter on the digital audio input
- Audio outputs (soft) muted during loop acquisition
- Full linear phase processing based on all-FIR filtering
- Integrated full digital IEC 958 demodulator for digital input signals (AES/EBU or SPDIF format) with intelligent error handling
- Extended input sample frequency range
- IEC 958 Channel Status (CS) and User Channel (UC) outputs
- On-chip CS and/or UC demodulation and buffering (consumer and professional format)
- Dedicated subcode processing for Compact Disc (CD)
- Final output quantization to 16, 18 or 20 bits with optional in-audio-band noise shaping
- Bitstream input and output for coupling with 1-bit analog-to-digital conversion (ADC) and digital-to-analog conversion (DAC)
- I^2S and Japanese serial input formats supported for SRC and DAC functions
- I^2S and Japanese serial output formats supported for SRC and ADC functions
- I^2S and Japanese 4× oversampled serial output available for SRC and ADC functions
- 8-bit digital gain/attenuation control
- Switchable Digital Signal Processor (DSP)-interface (I^2S input and output) for additional audio processing
- Additional clock outputs available at 768, 384, 256 and $128f_{so}$
- 3-line serial microcontroller interface, compatible with the Philips CD I.C. protocol (HCL)

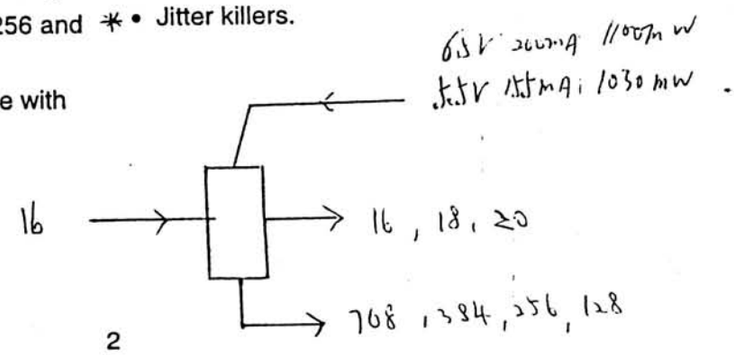


BITSTREAM CONVERSION

- 5 V power supply
- 0.7 µm double metal Complementary Metal Oxide Semiconductor (CMOS)
- SRC THD + N:
  - –113 dB over the 0 to 20 kHz band (1 kHz, 20 bits input and output) (see Fig.3)
  - –95 dB over the 0 to 20 kHz band (1 kHz, 16 bits input and output)
- Pass band ripple smaller than ±0.004 dB for up-sampling and down-sampling filters
- Stop band suppression:
  - selectable between 70 dB and 50 dB for 64× up-sampling filters
  - 80 dB for 128× down-sampling filters
- Microcontroller operated and stand-alone mode.

APPLICATIONS

- Professional audio equipment for:
  - mixing
  - recording
  - editing
  - broadcasting
- CD-Recordable (CD-R)
- Digital Speaker Systems (DSS)
- Digital Compact Cassette recorders (DCC)
- Digital Audio Tape (DAT) and MD recorders
- Digital amplifiers
- Jitter killers.



ANALOG CHARACTERISTICS (T_A = 25°C; VA+, VD+ = +5V; Full Scale Input Sine wave, 1 kHz; Word Clock = 44.1 kHz (PLL in use); Measurement Bandwidth is 20 Hz to 20 kHz; Local components as shown in "Recommended Connection Diagram"; SPI mode, Format 0, unless otherwise specified.)

Parameter		Symbol	Min	Typ	Max	Units
Analog Input Characteristics - Minimum gain setting (0 dB); unless otherwise specified.						
ADC Resolution	Stereo Audio channels Mono channel		16 16	- -	20 20	Bits Bits
Total Harmonic Distortion		THD		0.003	-	%
Dynamic Range	(A weighted):		TBD	95	-	dB
Total Harmonic Distortion + Noise		THD+N	-	-88	TBD	dB
Interchannel Isolation			-	90	-	dB
Interchannel Gain Mismatch			-	.1	-	dB
Programmable Input Gain			0	-	9	dB
Gain Step			2.7	3	3.3	dB
Offset Error (with high pass filter)			-	-	0	LSB
Full Scale Input Voltage (Single Ended):			TBD	2.82	TBD	V_{pp}
Gain Drift			-	200	-	ppm/°C
Input Resistance	(Note 1)		10	-	-	kΩ
Input Capacitance			-	-	15	pF
CMOUT Output Voltage			-	2.1	-	V
A/D Decimation Filter Characteristics						
Passband	(Note 4)		0.02	-	20.0	kHz
Passband Ripple			-	-	±0.01	dB
Stopband	(Note 4)		27.56	-	5617.2	kHz
Stopband Attenuation	(Note 2)		80	-	-	dB
Group Delay (Fs = Output Sample Rate)	(Note 3)	t_{gd}	-	15/Fs	-	s
Group Delay Variation vs. Frequency		Δ t_{gd}	-	-	0	µs
High Pass Filter Characteristics						
Frquency Response:	-3 dB -0.13 dB (Note 4)		- -	3.4 20	- -	Hz Hz
Phase Deviation	@ 20 Hz (Note 4)		-	10	-	Degree
Passband Ripple			-	-	0	dB

Notes:
1. Input resistance is for the input selected. Non-selected inputs have a very high (>1MΩ) input resistance. The input resistance will vary with gain value selected, but will always be greater than the min. value specified.
2. The analog modulator samples the input at 5.6448 MHz for an output sample rate of 44.1 kHz. There is no rejection of input signals which are multiples of the sampling frequency (n x 5.6448 MHz ±20.0 kHz where n = 0,1,2,3...).
3. Group delay for Fs = 44.1kHz, t_{gd} = 44.1kHz = 340µs
4. Filter characteristics scale with output sample rate.

CRYSTAL
A Cirrus Logic Company

CS4224/6

Surround Sound Codec

Features

- Stereo 20-bit A/D Converters
- Six 20-bit D/A Converters (CS4226)
  Four 20-bit DA Converters (CS4224)
- S/PDIF Receiver
  - AC-3 Auto-detection Capability
- >110 dB DAC Signal-to-Noise Ratio
- Mono 20-bit A/D Converter
- Programmable Input Gain & Output Attenuation
- On-chip Anti-aliasing and Output Smoothing Filters
- De-emphasis for 32kHz, 44.1kHz, 48kHz

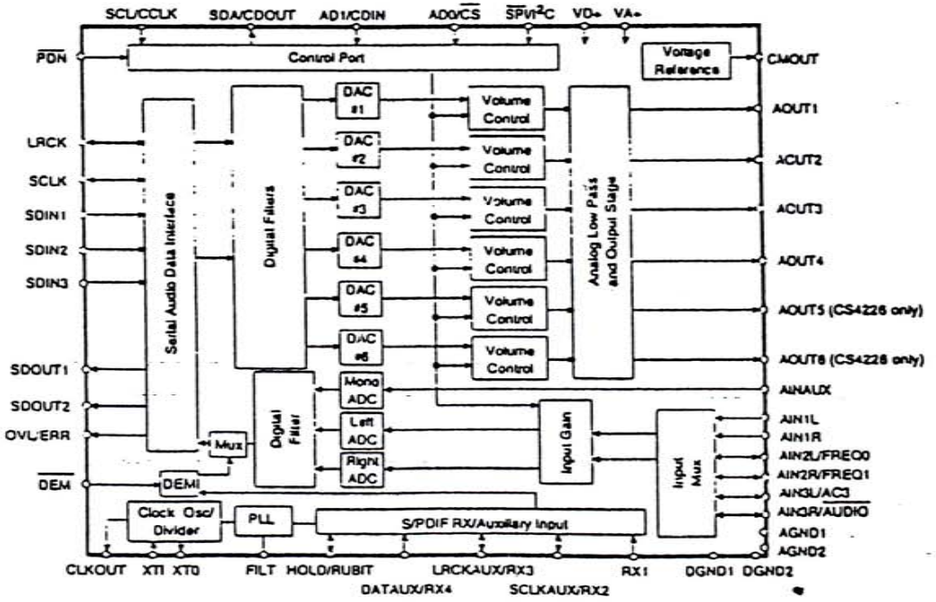
Description

The CS4226 is a single-chip codec providing stereo analog-to-digital and six (four in the CS4224) digital-to-analog converters using delta-sigma conversion techniques. This +5V device also contains volume control independently selectable for each of the six D/A channels. An S/PDIF receiver is included as a digital input channel. Applications include Dolby Pro-logic, THX, and AC-3 home theater systems, DSP based car audio systems, and other multi-channel applications.

The CS4224/6 is packaged in a 44-pin plastic TQFP.

ORDERING INFORMATION:

CS4224-KQ	TQFP, -10 °C to +70 °C
CS4224-BQ	TQFP, -40 °C to +85 °C
CS4226-KQ	TQFP, -10 °C to +70 °C
CS4226-BQ	TQFP, -40 °C to +85 °C
CDB4224	Evaluation Board
CDB4226	Evaluation Board



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

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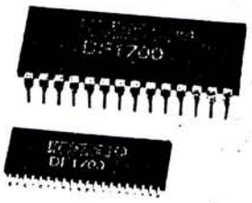


DF1700

Dual Channel, 8x Oversampling DIGITAL FILTER

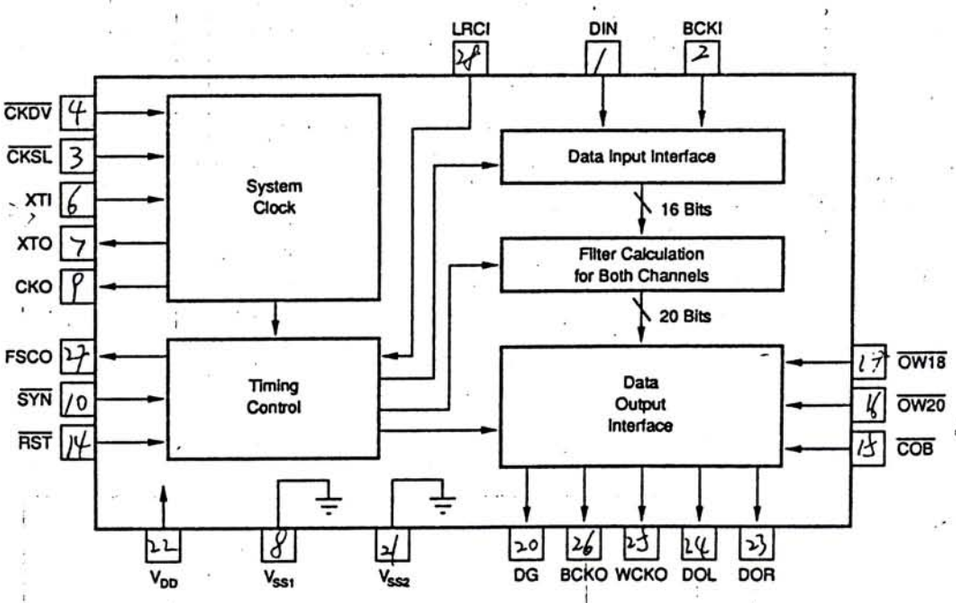
FEATURES

- DUAL CHANNEL DIGITAL INTERPOLATION FILTERS
- ACCEPTS 16-BIT INPUT DATA
- USER-SELECTABLE FOR 16-, 18-, OR 20-BIT OUTPUT DATA
- SERIAL OUTPUT IS COMPATIBLE WITH PCM1700 AND PCM63 DACs
- PASSBAND RIPPLE < 0.00005dB
- STOPBAND ATTENUATION > 110dB
- SINGLE +5V POWER SUPPLY FOR LOW POWER DISSIPATION OF 250mW Max
- PLASTIC 28-PIN DIP AND 40-PIN SOIC PACKAGES

DESCRIPTION

The DF1700 is a high performance, 8x oversampling CMOS digital filter. This filter accepts 16-bit input data and is user-selectable for 16-, 18-, or 20-bit output data. The 8x oversampling feature converts the input data frequency (fs) to an output data frequency of 8 x fs by digital interpolation. By providing 8x oversampled data to an audio DAC, lower order analog filters can be used at the DAC's output, thus reducing filter phase non-linearities. Oversampling with the DF1700 simultaneously improves the fidelity of the analog reconstruction and reduces analog filter complexity at the output of the DAC.

The DF1700 is available in a plastic 28-pin DIP and a 40-pin SOIC package, and is designed for compatibility with the Burr-Brown PCM1700 and PCM63 digital-to-analog converters.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1093

BURR-BROWN®

OVERVIEW

The SM5842AP is a Molybdenum-gate CMOS, two-channel, digital linear phase FIR filter IC for use in digital audio signal reproduction. The filter passband signal level is within ±0.00002 dB of the input signal, stopband attenuation exceeds 117 dB, and the phase response remains linear (zero group delay distortion).

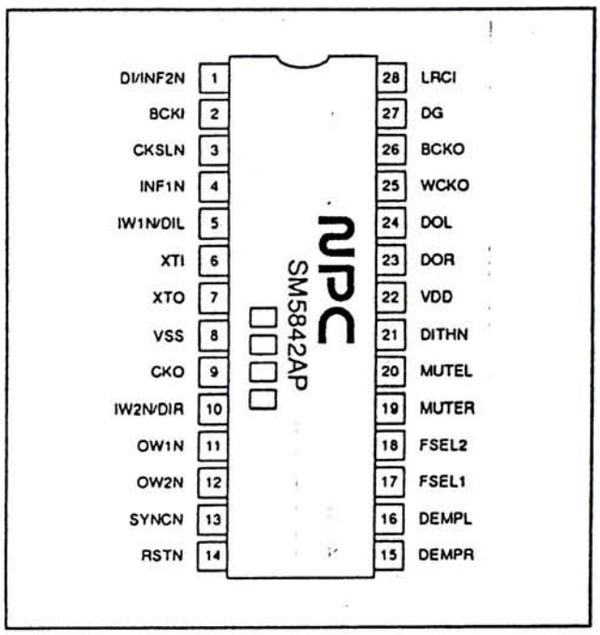
The SM5842AP incorporates 8-times oversampling, digital deemphasis and soft mute. The I/O interface allows 16-, 18-, 20- or 24-bit input data and 18-, 20-, 22- or 24-bit output data. The system clock can be 256fs or 384fs. At 384fs, fs can vary between 48 kHz and 48 kHz + 15%.

The SM5842AP operates from a 5 V supply and is available in 28-pin plastic DIPs.

FEATURES

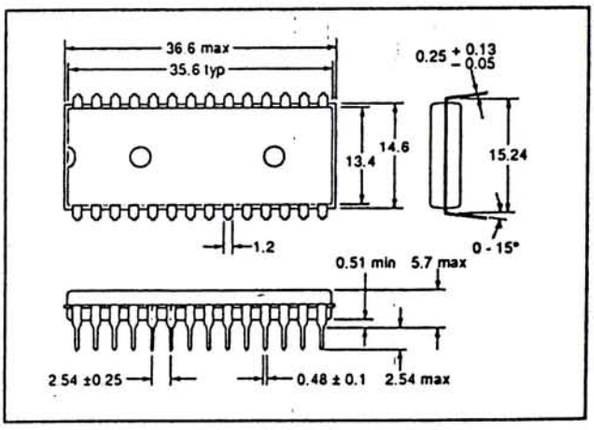
- 8-times oversampling
- Three-stage FIR filter configuration
- Two-channel independent ON/OFF digital deemphasis
- Selectable 44.1, 48 and 32 kHz input sampling rates
- 26 × 24-bit multiplier and 32-bit accumulator
- Two-channel independent ON/OFF soft mute
- Jitter-free/synchronous mode switching
- Round-off operation processing from dither (ON/OFF possible)
- 256fs or 384fs system clock selection
- f_{MAX} = 13 MHz with 256fs clock (fs = 50.7 kHz)
- f_{MAX} = 21.2 MHz with 384fs clock (fs = 55.2 kHz)
- Built-in quartz oscillator circuitry
- 5 V supply
- 28-pin plastic DIP

PINOUT



PACKAGE DIMENSIONS

Unit: mm



ULTRAANALOG, INC.
Advancing the Analog Art.

DAC D20400

Dual 20 Bit Audio DAC
8X – Oversampling

Features

- 20 Bit Resolution
- 2 Independent Channels
- 400 kHz Max. Update Rate Per Channel
- Fully Characterized For Audio Applications
- Includes Distortion Suppressors
- Guaranteed Maximum Specifications
- Unsurpassed T.H.D. + Noise Performance

Applications

- Upgrade 16 Bit Digital Audio Systems
- Digital Multi-channel Recorders
- Digital Audio Workstations
- Disk Based Recording
- Digital Audio Tape (DAT)
- Oversampled Audio Reconstruction
- Synthesizers

Description

The DAC D20400 includes two complete 20 Bit D/A Converters, a stable bipolar reference, a serial CMOS/TTL compatible digital interface and two distortion-suppressing output deglitcher amplifiers. The DAC D20400 converts at rates up to 400 kHz, thereby accommodating 8X oversampling applications. The product utilizes the finest available components including: a custom CMOS IC, custom thin-film resistor networks, low-noise operational amplifiers and a variety of discrete components.

The DAC D20400 achieves better initial linearity, superior long term stability and less sensitivity to resistor mismatch than other designs. Perhaps the most significant benefit of the proprietary UltraAnalog architecture is that no transitions of the more significant bits (MSBs) occur for near-zero signals. The proprietary architecture combines digital data enhancement techniques with an over-ranging discrete DAC for the 8 MSBs and a monolithic 12 bit DAC for the 12 less significant bits (LSBs). The additional resolution of the over-ranging DAC allows conversions to occur away from the major carry of the ladder network, while preventing an output over-range condition. This improves the integrity of conversions for small signals, thereby ensuring faithful audio signal reconstruction. The result is a typical **small-signal performance (THD + N) of 112 dB** over the 20 to 20 kHz band, that is guaranteed by design and will not deteriorate with time or temperature changes.

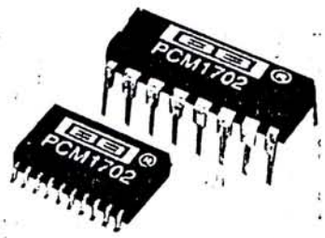
Another feature of the design architecture is that both D/A Converters share the same precision resistor ladder network that determines the weight of the 6 MSBs and also share the bipolar reference. By sharing these circuits, both D/A Converters will track each other over time and temperature and will behave nearly identically.

The large-signal performance of the product is limited by initial calibration and long term stability of the MSB ladder network. Consequently, the DAC D20400 uses premium quality thin-film resistor networks. Once installed in the product, the networks are fine-trimmed with stable metal film resistors. To perform the fine trimming, each DAC D20400 is exercised with a computerized calibration system that makes approximately 100,000 measurements and calculations to determine the optimum trim resistor values. Next, a test operator installs discrete metal film resistors into the DAC to complete the calibration. Although this procedure is more time consuming than laser trimming, the algorithm corrects for every conceivable error that affects large-signal linearity. Once factory calibration is complete, the user need not make any external adjustments.

Digital interface connections to the product are through the **universal serial interface.** The interface accepts Offset Binary, 2's Complement, Complementary Offset Binary and Complementary 2's Complement coding schemes. Input data words from 16 to 32 bits may be applied, which allows easy interfacing to existing systems. Further, data words for left and right channels may be applied simultaneously or multiplexed. An application note guides the user in selecting the appropriate interface configuration for the application. The interface is compatible with other serial input DACs, digital filter ICs and DSP processor ICs.

Finally, each DAC D20400 is 100% tested for critical parameters and guaranteed to meet its specifications. The overall result of these design innovations and specialized manufacturing techniques is the world's first Dual 20 Bit 8X Oversampling Audio DAC Subsystem.

BURR-BROWN®



PCM1702P
PCM1702U

**ADVANCED INFORMATION
SUBJECT TO CHANGE**

BiCMOS Advanced Sign Magnitude 20-Bit DIGITAL-TO-ANALOG CONVERTER

FEATURES

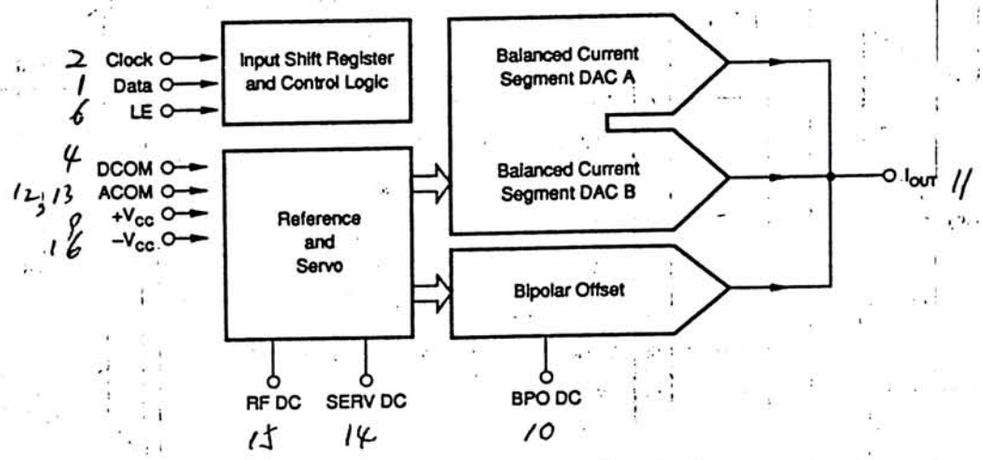
- ULTRA LOW –96dB max THD + N (No External Adjustment Required)
- NEAR-IDEAL LOW LEVEL OPERATION
- GLITCH-FREE OUTPUT
- 120dB SNR TYP (A-Weight Method)
- INDUSTRY STD SERIAL INPUT FORMAT
- FAST (200ns) CURRENT OUTPUT (±1.2mA)
- CAPABLE OF 16X OVERSAMPLING
- COMPLETE WITH REFERENCE
- LOW POWER (150mW typ)

DESCRIPTION

The PCM1702 is a precision 20-bit digital-to-analog converter with ultra-low distortion (–96dB typ with a full scale output). Incorporated into the PCM1702 is an advanced sign magnitude architecture that eliminates unwanted glitches and other nonlinearities around bipolar zero. The PCM1702 also features a very low noise (120dB typ SNR: A-weighted method) and fast settling current output (200ns typ, 1.2mA step) which is capable of 16X oversampling rates.

Applications include very low distortion frequency synthesis and high-end consumer and professional digital audio applications.

$48k]^{-1} = 20.8\mu s \div 104 = 200ns$



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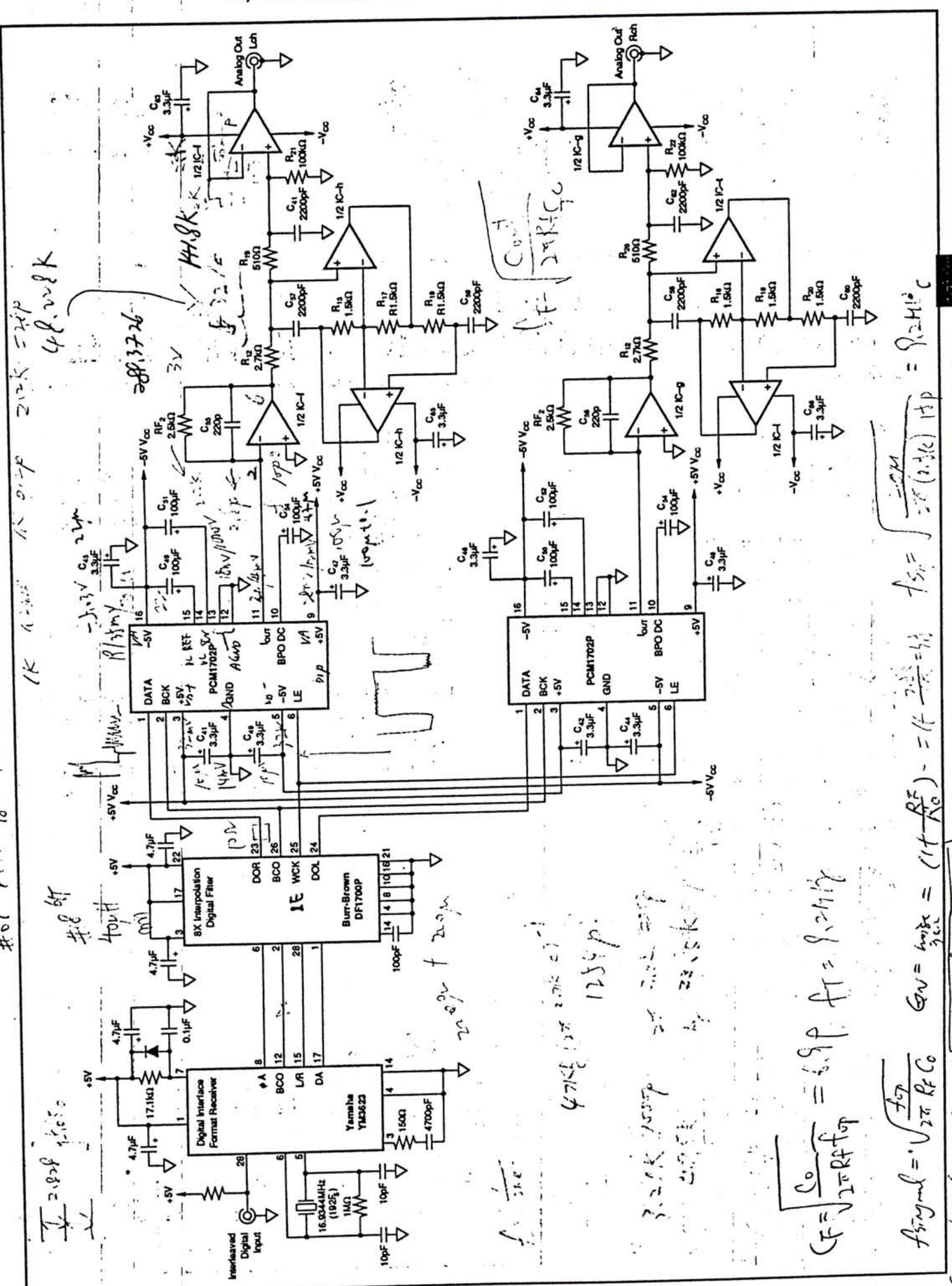


FIGURE 4. Typical Application for Stereo Audio 8X Oversampling system.

AKM

= Preliminary = **AK4321**

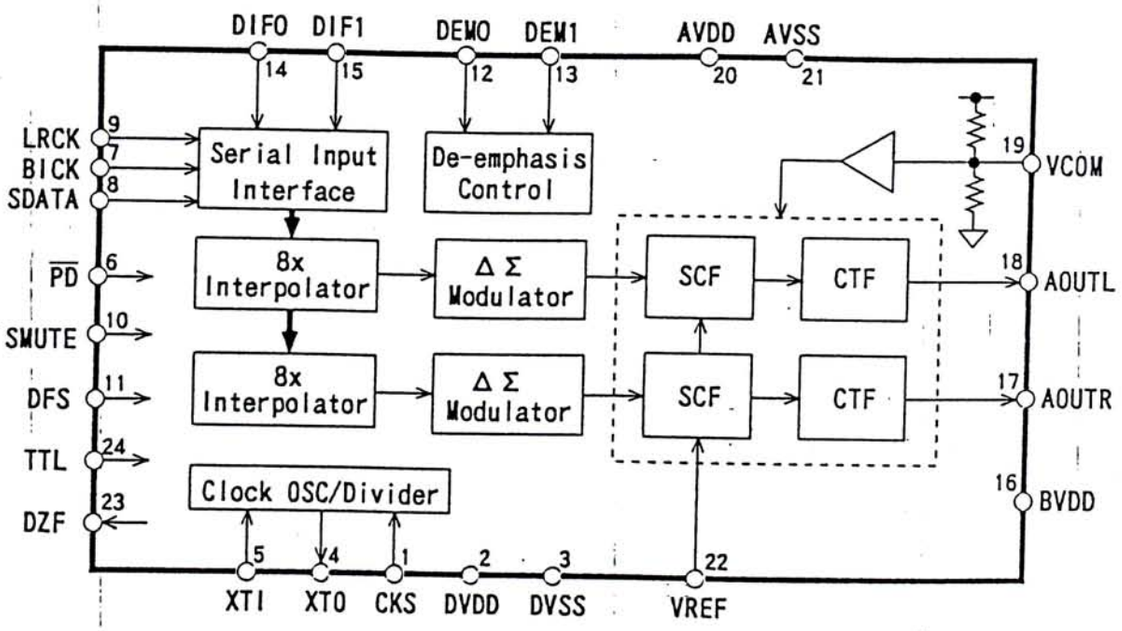
96kHz Sampling 20Bit Δ Σ DAC

General Description

The AK4321 is a high performance 1bit stereo DAC for the 96kHz sampling mode of DAT,DVD including a 20bit digital filter. A 1bit DAC can achieve monotonicity and low distortion with no adjustment and is superior to traditional R-2R ladder based DACs. In the AK4321, the analog outputs are filtered in the analog domain by a combination of switched-capacitor filter(SCF) with high tolerance to clock jitter and continuous-time filter(CTF). Therefore, no external filters are generally required. The AK4321 can operate at the power supply from 2.7V to 5.5V and the digital I/F can also correspond to both TTL and CMOS levels.

Features

- ☐ High Performance Stereo 1bit DAC
- ☐ Sampling Rate up to 96kHz
- ☐ On chip Perfect Filtering
  - 20Bit 8 times FIR Interpolator
  - 2nd order SCF
  - 2nd order CTF
  - Total Response: ± 0.5dB at 40kHz
- ☐ On chip Buffer with Single End Output
- ☐ Digital de-emphasis for 32, 44.1, 48kHz sampling
- ☐ Soft Mute
- ☐ High Tolerance to Clock Jitter
- ☐ THD+N: -90dB
- ☐ Dynamic Range, S/N: 100dB
- ☐ Power Supply: Normal Speed(2.7V ~ 5.5V)
  Double Speed(3.0V ~ 5.5V)
- ☐ Small Package: 24pin VSOP



NPC
NIPPON PRECISION CIRCUITS LTD.

CMOS LSI ΣDECO SM5864AP

Digital Audio D/A Converter

OVERVIEW

The ΣDECO SM5864AP D/A converter is a high-speed converter for digital audio systems fabricated using NPC's molybdenum-gate CMOS process. A selectable operating frequency and balanced outputs allow the ΣDECO SM5864AP to be adapted to a wide range of applications.

The ΣDECO SM5864AP is designed to be used with a digital eight-times oversampling filter and has two serial inputs for left- and right-channel data. The serial input data format consists of 20-bit words in 2s complement, with the most significant bit first.

The ΣDECO SM5864AP linearly interpolates the input signal at a high multiple of the original sampling frequency and then requantizes the resulting signal. A fourth-order noise shaper is used to remove most of the quantizing noise before the signal is output as a pulsewidth-modulated (PWM) waveform. Quasi-symmetrical PWM outputs allow the use of low system clock frequencies.

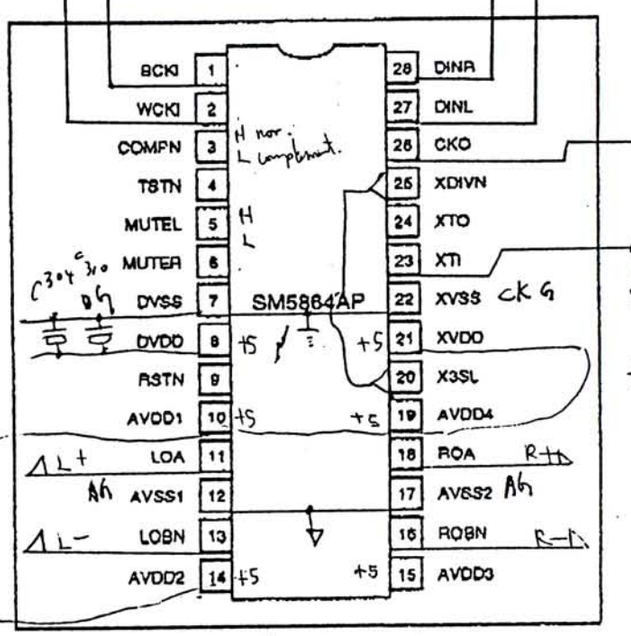
The ΣDECO SM5864AP has a complementary output mode that produces a single low-distortion, high-linearity output channel.

The ΣDECO SM5864AP operates from a single 5 V supply and is available in 28-pin plastic DIPs.

FEATURES

- Two-channel D/A converter
- Designed for use with a digital eight-times oversampling filter.
- Quasi-symmetrical PWM outputs
- High-accuracy pulsewidth-modulated output
- 384fs, 768fs, 512fs or 1024fs selectable system clock frequencies
- On-chip crystal oscillator circuit
- Fourth-order, 32fs noise shaper
- TTL-compatible inputs and outputs
- Molybdenum-gate CMOS process
- Single 5 V supply
- 28-pin plastic DIPs

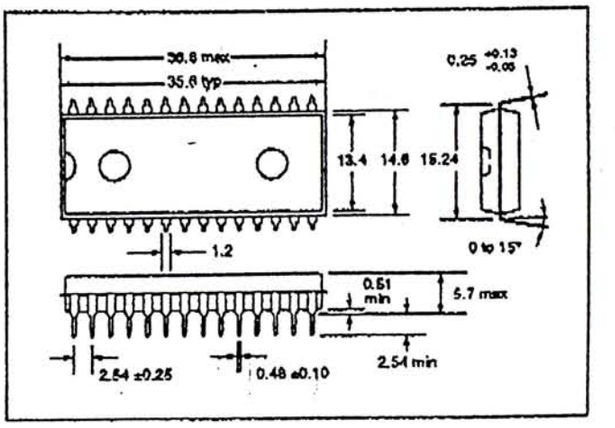
PINOUT



PACKAGE DIMENSIONS

Unit: mm

Plastic DIP28



SN54HC164, SN74HC164
8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- AND-Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Direct Clear
- Package Options Include Ceramic Chip Carriers and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These 8-bit shift registers feature AND-gated serial inputs and an asynchronous Clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of the clock input.

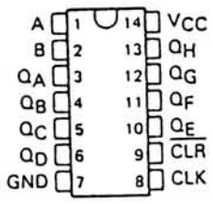
The SN54HC164 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC164 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

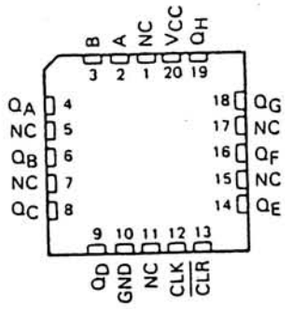
INPUTS				OUTPUTS		
$\overline{CLR}$	CLK	A	B	Q_A	Q_B . . . Q_H	
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

H = high level (steady state). L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one-bit shift.

SN54HC164 . . . J PACKAGE
SN74HC164 . . . N PACKAGE
(TOP VIEW)

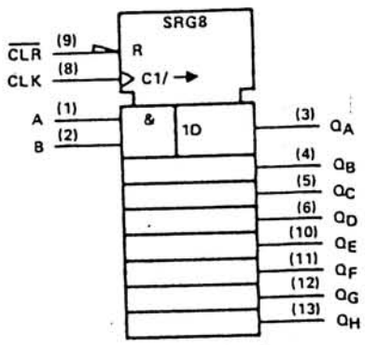


SN54HC164 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for J and N packages.

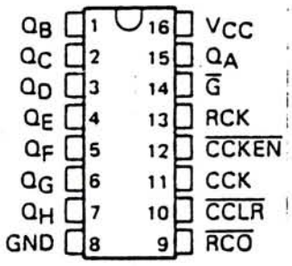
2 HCMOS Devices

SN54HC590A, SN74HC590A
8-BIT BINARY COUNTERS WITH 3-STATE OUTPUT REGISTERS

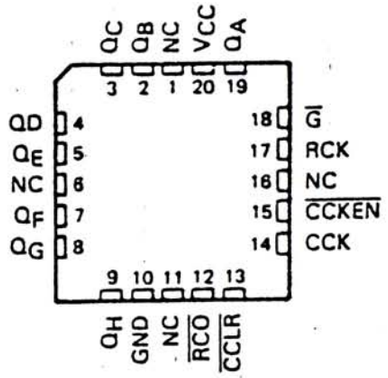
D2684, DECEMBER 1982—REVISED SEPTEMBER 1987

- 8-Bit Counter with Register
- High-Current 3-State Parallel Register Outputs Can Drive Up to 15 LSTTL Loads
- Counter has Direct Clear
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54HC590A . . . J PACKAGE
SN74HC590A . . . DW OR N PACKAGE
(TOP VIEW)



SN54HC590A . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

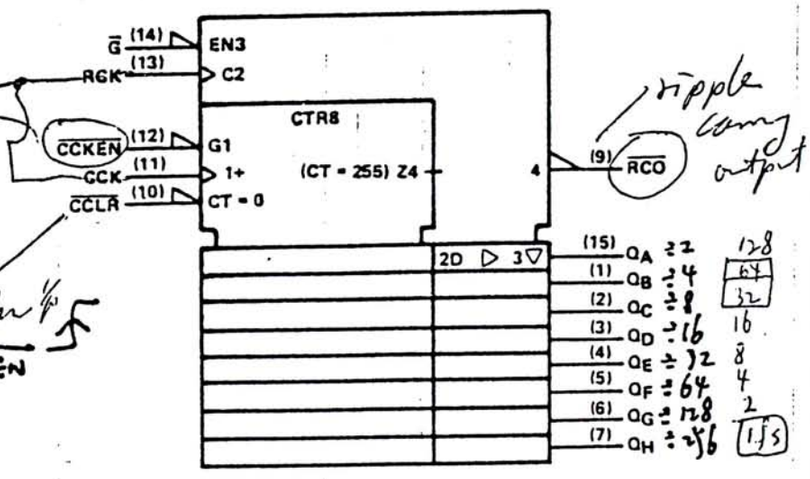
description

These devices each contain an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register. The binary counter features a direct clear input $\overline{CCLR}$ and a count enable input $\overline{CCKEN}$. For cascading a ripple carry output RCO is provided. Expansion is easily accomplished for two stages by connecting $\overline{RCO}$ of the first stage to $\overline{CCKEN}$ of the second stage. Cascading for larger count chains can be accomplished by connecting $\overline{RCO}$ of each stage to CCK of the following stage.

Both the counter and register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the counter state will always be one count ahead of the register. Internal circuitry prevents clocking from the clock enable.

The SN54HC590A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HC590A is characterized for operation from −40°C to 85°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, J, and N packages.

74AC/ACT11074

Dual D-Type Flip-Flop w/Set and Reset; Positive-Edge Trigger

Product Specification

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: SSI**

DESCRIPTION

The 74AC/ACT11074 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11074 provides two D-type flip-flops with independent Data, Clock, Set and Reset inputs, and complementary Q and $\overline{Q}$ outputs.

Set ($\overline{S}_n$) and Reset ($\overline{R}_n$) are asynchronous active-Low inputs and operate independently of the Clock input. Information on the Data (D) input is transferred to the Q output on the Low-to-High transition of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. The D inputs must be stable one set-up time prior to the Low-to-High clock transition for predictable operation.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay CP_n to Q_n or $\overline{Q}_n$	C_L = 50pF	5.2	5.9	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	f = 1MHz; C_L = 50pF	30	30	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF	150	125	MHz

Note:

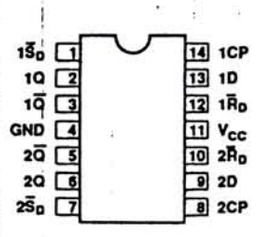
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

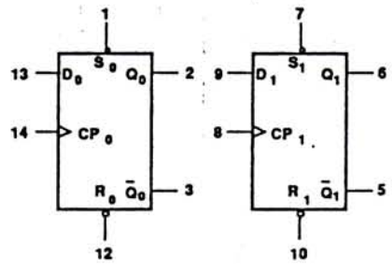
PACKAGES	TEMPERATURE RANGE	ORDER CODE
14-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11074N 74ACT11074N
14-pin plastic SO (150mil-wide)	-40°C to +85°C	74AC11074D 74ACT11074D

PIN CONFIGURATION

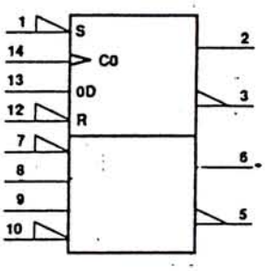
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



DATA SHEET

NEC

OPTIC LINK

PLT1101, PLR1101

PLT1101 : LIGHT TRANSMISSION MODULE
PLR1101 : LIGHT RECEIVING MODULE

PLT1101, a light transmission module, having a built-in GaAlAs high output red LED and an LED driving IC; PLR1101, a light receiving module, having a built-in light receiving IC where a photodiode and a signal processing circuit are integrated into one chip; and a photo connector attached plastic optical fiber constitute a light transmission link (PLT1101, PLR1101).

FEATURES

- Excellent tolerance for external noise owing to the monolithic light receiving IC.
- Direct drive by TTL signal is possible. (Non adjust)
- High speed transmission. (DC ~ 6 Mb/s, NRZ)
- The photo connector can be quickly attached and detached. (snap-in type)
- Low supply current
  Light transmission module PLT1101: I_{CC} = 15 mA TYP.
  Light receiving module PLR1101: I_{CC} = 25 mA TYP.

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

APPLICATIONS

- Signal transmission between measuring and control equipment.
- Multiplex transmission system of computer.
- Signal transmission system of automobile.
- Signal transmission system requiring interception of electromagnetic hindrance.

ocument No. LC-2260A
(O.D. No. LC-7650A)
ate Published February 1993 M
rinted in Japan

DATA SHEET

NEC

OPTIC LINK
PLT101, PLT102, PLT104
PLR101, PLR102

PLT101, PLT102, PLT104 : TRANSMITTER MODULE
PLR101, PLR102 : RECEIVER MODULE

— NEPOC SERIES —

DESCRIPTION

Transmitter modules (PLT101, PLT102, PLT104) incorporate a 660 nm LED and a LED driver. Receiver modules (PLR101, PLR102) incorporate an integrated photo detector and wide bandwidth dc amplifier.

The combinations of PLT101, PLT102, PLT104 and PLR101, PLR102 with plastic fiber optic cable (1 mm core) have guaranteed performance over –20 to 70 degrees centigrade from DC to 6 Mb/s (NRZ) up to 5 meters.

FEATURES

- Small Package
- Snap-in Connector
- TTL Compatible Output Level
- DC to 6 Mb/s (NRZ) Data Rate
- Single +5 V Power Supply
- Low Power Dissipation
- Snap-in type (PLT104)

APPLICATIONS

- Local Area Networks
- Computer to Peripheral Links
- Digital Audio Interface
- Factory Data Highways

QUALITY GRADE

Standard

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Document No. LC-2277A
(O.D. No. LC-7662A)
Date Published December 1992 M
Printed in Japan

ANALOG DEVICES

Ultrafast Comparators

AD96685/AD96687

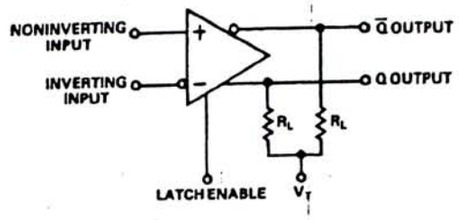
FEATURES

Fast: 2.5 ns Propagation Delay
Low Power: 118 mW per Comparator
Packages: DIP, TO-100, SOIC, PLCC
Power Supplies: +5 V, –5.2 V
Logic Compatibility: ECL
MIL-STD-883 Versions Available
50 ps Delay Dispersion

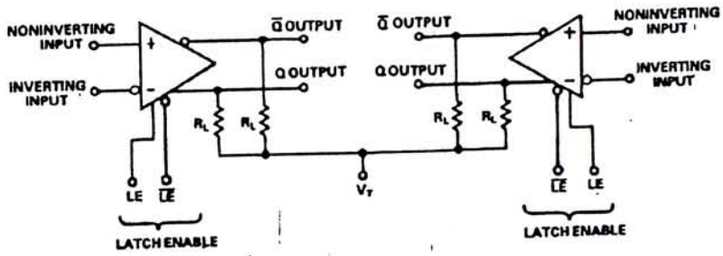
APPLICATIONS

High Speed Triggers
High Speed Line Receivers
Threshold Detectors
Window Comparators
Peak Detectors

AD96685 FUNCTIONAL BLOCK DIAGRAM



AD96687 FUNCTIONAL BLOCK DIAGRAM



THE OUTPUTS ARE OPEN EMITTERS, REQUIRING EXTERNAL PULL-DOWN RESISTORS. THESE RESISTORS MAY BE IN THE RANGE OF 50Ω – 200Ω CONNECTED TO –2.0V, OR 200Ω – 2000Ω

GENERAL DESCRIPTION

The AD96685 and AD96687 are ultrafast voltage comparators. The AD96685 is a single comparator with 2.5 ns propagation delay; the AD96687 is an equally fast dual comparator. Both devices feature 50 ps propagation delay dispersion which is a particularly important characteristic of high speed comparators. It is a measure of the difference in propagation delay under differing overdrive conditions.

A fast, high precision differential input stage permits consistent propagation delay with a wide variety of signals in the common-mode range from –2.5 V to +5 V. Outputs are complementary digital signals fully compatible with ECL 10 K and 10 KH logic families. The outputs provide sufficient drive current to directly drive transmission lines terminated in 50 Ω to –2 V. A level sensitive latch input is included which permits tracking, track-hold, or sample-hold modes of operation.

The AD96685 and AD96687 are available in both industrial, –25°C to +85°C, and military temperature ranges. Industrial range devices are available in 16-pin DIP, SOIC, and 20-lead PLCC; additionally, the AD96685 is available in a 10-pin, TO-100 metal can.

REV. C

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703

ANALOG DEVICES

Ultrafast Comparators

AD96685/AD96687

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Low Power: 118mW per Comparator
Packages: DIP, TO-100, SOIC, PLCC
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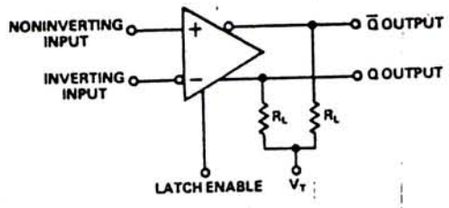
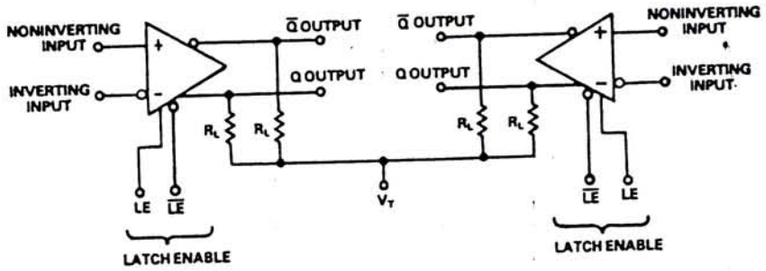
AD96685 FUNCTIONAL BLOCK DIAGRAM



AD96687 FUNCTIONAL BLOCK DIAGRAM



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The AD96685 and AD96687 are available in both industrial, −25°C to +85°C, and military temperature ranges. Industrial range devices are available in 16-pin DIP, SOIC, and 20-lead PLCC; additionally, the AD96685 is available in a 10-pin, TO-100 metal can. Both devices are available qualified to MIL-STD-883, Class B in 16-pin ceramic DIP and 20-lead ceramic LCC; the TO-100 version of the AD96685 is also mil-qualified.

19-0200; Rev. 1; 11/94

MAXIM

Calibrated, Low-Drift, +4.096V/+5V/+10V Precision Voltage References

677

General Description

The MAX676/MAX677/MAX678 precision +4.096V, +5V, and +10V voltage references feature a factory-programmed on-chip ROM that calibrates each reference at specific temperatures, and reduces the temperature drift to less than 1ppm/°C over temperature—the lowest in the industry.

The MAX676/MAX677/MAX678 have excellent line and load regulation: 30ppm/V and 3ppm/mA, respectively. Load regulation specifications are guaranteed for source currents up to 5mA and sink currents up to 500µA. The 4.096V MAX676 operates from a supply voltage as low as 4.75V, making it an ideal reference for single 5V, high resolution ADCs.

Applications

High Resolution 16-Bit ADCs and DACs

Precision Test and Measurement Systems

Precision, Calibrated Voltage-Reference Standard

High-Accuracy Transducers

Features

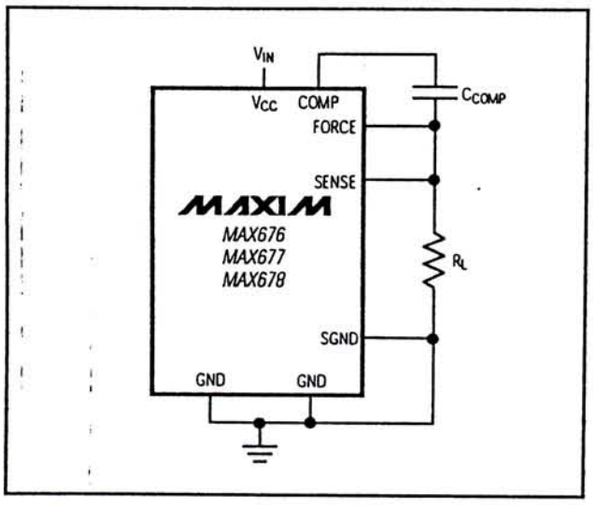
- **Lowest Temperature Drift:**
  1ppm/°C Max Over -40°C to +85°C
  1.5ppm/°C Max Over -55°C to +125°C
- **0.02% Initial Accuracy**
- **3ppm/mA Max Load Regulation**
- **30ppm/V Max Line Regulation**
- **4.096V Reference Operates from 5V ±5% Supply**
- **Available in Surface-Mount Package**

Ordering Information

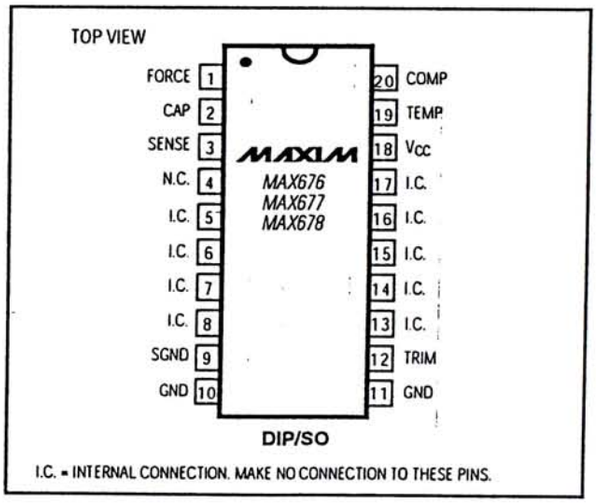
PART	TEMP. RANGE	PIN-PACKAGE	MAX DRIFT (ppm/°C)
MAX676ACPP	0 °C to +70 °C	20 Plastic DIP	1.0
MAX676BCPP	0 °C to +70 °C	20 Plastic DIP	2.0
MAX676ACWP	0 °C to +70 °C	20 Wide SO	1.0
MAX676BCWP	0 °C to +70 °C	20 Wide SO	2.0
MAX676ACJP	0 °C to +70 °C	20 CERDIP	1.0
MAX676AEPP	-40 °C to +85 °C	20 Plastic DIP	1.0
MAX676BEPP	-40 °C to +85 °C	20 Plastic DIP	2.0
MAX676AEWP	-40 °C to +85 °C	20 Wide SO	1.0
MAX676BEWP	-40 °C to +85 °C	20 Wide SO	2.0
MAX676AEJP	-40 °C to +85 °C	20 CERDIP	1.0
MAX676AMJP	-55 °C to +125 °C	20 CERDIP	1.5
MAX676BMJP	-55 °C to +125 °C	20 CERDIP	3.0

Ordering Information continued on last page.

Typical Operating Circuit



Pin Configuration



I.C. = INTERNAL CONNECTION. MAKE NO CONNECTION TO THESE PINS.