Hall mobility enhancement caused by annealing of $Si_{0.2}Ge_{0.8}/Si_{0.7}Ge_{0.3}/Si(001)$ *p*-type modulation-doped heterostructures

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The effect of post-growth furnace thermal annealing (FTA) on the Hall mobility and sheet carrier density measured at 9–300 K in the $Si_{0.2}Ge_{0.8}/Si_{0.7}Ge_{0.3}/Si(001)$ *p*-type modulation-doped heterostructures was studied. FTA treatments in the temperature range of 600–900 °C for 30 min were performed on similar heterostructures but with two $Si_{0.2}Ge_{0.8}$ channel thicknesses. The annealing at 600 °C is seen to have a negligible effect on the Hall mobility as well as on the sheet carrier density. Increases in the annealing temperature resulted in pronounced successive increases of the mobility. For both samples the maximum Hall mobility was observed after FTA at 750 °C. Further increases of the annealing temperature resulted in a decrease in mobility. The sheet carrier density showed the opposite behavior with an increase in annealing temperature. The mechanism causing this behavior is discussed. Structural characterization of as-grown and annealed samples was done by cross-sectional transmission electron microscopy. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1478779]

The growth of $Si_{1-x}Ge_x$ epilayers with high Ge contents ($x>0.5$) on a Si(001) substrate by molecular beam epitaxy (MBE) is of great interest both for device applications and for fundamental research.[1,2] The main problem in growing a $Si_{1-x}Ge_x$ alloy on a Si(001) substrate is lattice mismatch, which increases from 0% to 4.2% as x is varied from 0 to 1. The larger x becomes, the thinner the $Si_{1-x}Ge_x$ channel has to be grown in order to prevent the appearance of roughness and misfit dislocations from relaxation of strain. One possible way in which to obtain Ge compositions $x>0.5$, while retaining strain in the $Si_{1-x}Ge_x$ layer, is to use a relaxed $Si_{1-y}Ge_y$ substrate with a bulk lattice constant. This allows strained Si, Ge or $Si_{1-x}Ge_x$ to be grown on an underlying Si(001) wafer. This kind of substrate is termed a virtual substrate (VS) and the whole structure is called a metamorphic heterostructure. In this letter we report the effect of post-growth furnace thermal annealing (FTA) on the Hall mobility and sheet carrier density, measured in the range of 9–300 K, in $Si_{0.2}Ge_{0.8}/Si_{0.7}Ge_{0.3}/Si(001)$ *p*-type modulation-doped (MOD) heterostructures with two $Si_{0.2}Ge_{0.8}$ channel thicknesses. This is an extremely interesting approach because the FTA temperature range of 600–900 °C is widely used during the fabrication of Si and SiGe based metal–oxide–semiconductor field effect transistor (MOSFET) devices.

The $Si_{0.2}Ge_{0.8}/Si_{0.7}Ge_{0.3}/Si(001)$ *p*-type MOD heterostructures were grown on a Si(001) substrate by solid-source molecular beam epitaxy (SS-MBE) in a commercial VG Semicon V90S UHV system. The substrates were rotated during growth to ensure temperature and growth rate uniformity across the wafer. When growing high Ge content $Si_{1-x}Ge_x$ epilayers by SS-MBE it is advantageous to use low growth temperatures to kinetically suppress surface segregation, which smears the Ge profile, and also to suppress surface diffusion that can produce roughness on the surface and relief of strain energy. The $Si_{0.2}Ge_{0.8}$ channel was grown at $T_g=300$ °C on a quite thin (850 nm thick) virtual substrate involving a low-temperature ($T_g=390$ °C) Si buffer.[3,4] The top layers of the VS were relaxed with respect to the lattice constant of the $Si_{0.7}Ge_{0.3}$ bulk alloy. The active layers of a MOD heterostructure were similar in each sample and consisted of an undoped channel for mobile carriers (in this case holes), a 7 nm thick undoped spacer layer that separates the ionized dopants from the channel and a 10 nm thick boron doping layer with a doping level of 2×10^{18} cm^{-3}. The heterointerface is located between the channel and the spacer and it separates the two regions energetically. The $Si_{0.2}Ge_{0.8}$ channel thickness in sample A is 10 nm and in sample B is 14 nm. Annealing was performed after growth at temperatures of 600, 700, 750, 800 and 900 °C for 30 min in flowing N_2 ambient.

In order to determine the structural integrity, interface quality and layers thickness cross-sectional transmission electron microscopy (XTEM) analysis was done on as-grown and after FTA samples. XTEM images of the surface region of sample A as-grown and after FTA at 750 °C are presented in Fig. 1. The $Si_{0.2}Ge_{0.8}$ channel is clearly visible as a stripe of dark contrast between $Si_{0.7}Ge_{0.3}$ layers [Fig. 1(a)]. This region is dislocation free. Relatively short- and long-range $Si_{0.2}Ge_{0.8}$ channel roughness was observed. The long-range roughness of the bottom and top $Si_{0.2}Ge_{0.8}$ channel interfaces is characterized by an average height of $\Delta=24$ nm in the growth direction and the correlation length of $\Lambda=360$ nm in the plane is mainly caused by nonoptimum growth conditions of the $Si_{0.7}Ge_{0.3}$ VS. The short-range roughness of the top $Si_{0.2}Ge_{0.8}$ channel interface characterized by $\Delta=2$ nm and $\Lambda=48$ nm is mainly caused by nonoptimum growth temperatures of the $Si_{0.2}Ge_{0.8}$ channel. The average thickness of the $Si_{0.2}Ge_{0.8}$ channel is around 11 nm.

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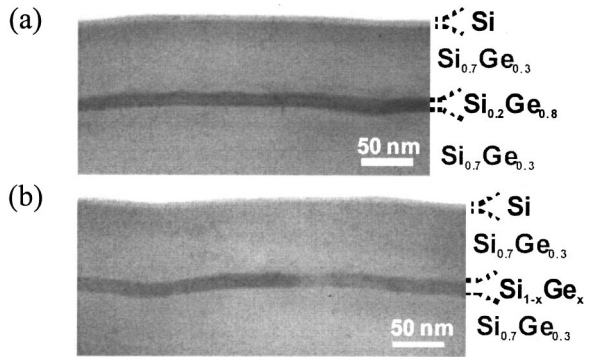

FIG. 1. XTEM images of the $Si_{0.2}Ge_{0.8}$ channel region for as-grown Sample A (a) and after FTA at 750 °C for 30 min (b).

After FTA at 750 °C for 30 min significant changes were observed in the $Si_{0.2}Ge_{0.8}$ channel region, as shown in Fig. 1(b). Broadening of the $Si_{0.2}Ge_{0.8}$ channel was observed, accompanied by smearing of the bottom and top $Si_{0.2}Ge_{0.8}/Si_{0.7}Ge_{0.3}$ interfaces. A reduction in the short-range roughness of the $Si_{0.2}Ge_{0.8}/Si_{0.7}Ge_{0.3}$ top interface was also observed [Fig. 1(b)]. The average thickness of the $Si_{0.2}Ge_{0.8}$ channel increased to 13 nm. The broadening of the $Si_{0.2}Ge_{0.8}$ channel was due to Ge diffusion during thermal annealing from the region with high Ge concentration (the $Si_{0.2}Ge_{0.8}$ channel) to the region with low Ge concentration (the $Si_{0.7}Ge_{0.3}$ layers). Consequently the Ge composition in the $Si_{0.2}Ge_{0.8}$ channel after FTA at 750 °C for 30 min decreased.

The Hall mobilities and sheet carrier densities of the as-grown and annealed samples were obtained by a combination of resistivity and Hall effect measurements in the temperature range of 9–300 K. The data were obtained in the dark beginning at low temperature. Samples were fabricated in mesa-etched Greek cross geometry for van der Pauw measurements. Ohmic contacts were formed by evaporating Al at the corners of the $4\times4\ mm^2$ samples and alloying them at 420 °C for 20 min in flowing N_2 ambient.

The 9–300 K temperature dependences of the Hall mobility and sheet carrier density for samples A as-grown and after FTA at 600, 700, 750, 800 and 900 °C for 30 min are presented in Fig. 2. The Hall mobility of two-dimensional hole gas (2DHG) (at the sheet carrier density) that formed in the $Si_{0.2}Ge_{0.8}$ channel of the as-grown sample measured at 9 K is 624 $cm^2\,V^{-1}\,s^{-1}$ ($1.37\times10^{12}\ cm^{-2}$). The Hall mobility (at the sheet carrier density) for the as-grown sample measured at 293 K is 170 $cm^2\,V^{-1}\,s^{-1}$ ($2.6\times10^{12}\ cm^{-2}$). The annealing at 600 °C is seen to have a negligible effect on the Hall mobility as well on the sheet carrier density. Increasing the annealing temperature results in pronounced successive increases of Hall mobility. The highest Hall mobility at 9 and 293 K was observed after annealing at 750 °C for 30 min. The values are 1680 ($1.27\times10^{12}\ cm^{-2}$) and 512 $cm^2\,V^{-1}\,s^{-1}$ ($2.11\times10^{12}\ cm^{-2}$) at 9 and 293 K, respectively. A further increase in the annealing temperature up to 900 °C results in a decrease of Hall mobility. For the sheet carrier density opposite behavior was observed.

The Hall mobility of 2DHG (at the sheet carrier density) that formed in the $Si_{0.2}Ge_{0.8}$ channel of as-grown sample B measured at 9 K is 297 $cm^2\,V^{-1}\,s^{-1}$ ($1.4\times10^{12}\ cm^{-2}$). The Hall mobility (at the sheet carrier density) for the as-grown sample B measured at 293 K is 98 $cm^2\,V^{-1}\,s^{-1}$ ($3.28\times10^{12}\ cm^{-2}$). The lower values of Hall mobility observed in sample B might be explained by the critical thickness of the 14 nm $Si_{0.2}Ge_{0.8}$ channel that was exceeded and consequently by a stronger influence of the $Si_{0.2}Ge_{0.8}$-channel/$Si_{0.7}Ge_{0.3}$-spacer interface roughness scattering on hole mobility due to a partially relaxed $Si_{0.2}Ge_{0.8}$ channel. A similar FTA effect on Hall mobility and sheet carrier density was observed for sample B. The highest Hall mobilities at 9 and 293 K were observed after annealing at 750 °C for 30 min. The values are 938 ($9.86\times10^{11}\ cm^{-2}$) and 153 $cm^2\,V^{-1}\,s^{-1}$ ($3.11\times10^{12}\ cm^{-2}$) at 9 and 293 K, respectively.

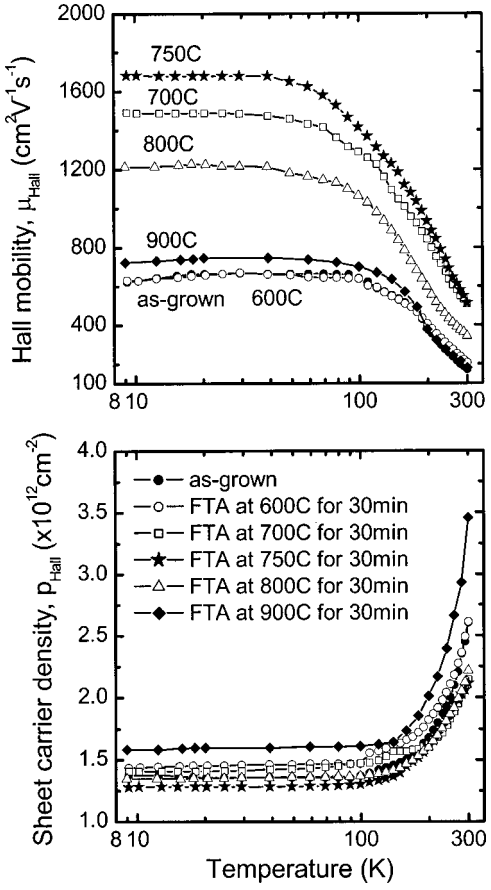

FIG. 2. Temperature dependence of the Hall mobility and sheet carrier density for as-grown sample A and after FTA at 600, 700, 750, 800 and 900 °C for 30 min.

Similar FTA effects on the Hall mobility and sheet carrier density measured at 9 and 293 K (Fig. 3) were observed in both samples. Annealing at 600 °C is seen to have a negligible effect on the Hall mobility as well as on sheet carrier density. Increasing the annealing temperature results in pronounced successive increases of the mobility. For both samples the maximum Hall mobility was observed after FTA at 750 °C. A further increase of the annealing temperature results in a decrease of the mobility. The sheet carrier density displayed opposite behavior with an increase in annealing temperature.

A tentative explanation for the above mentioned results is as follows. The decrease in the sheet carrier density was found to be consistent with the decrease in hole transfer from the B doped region to the $Si_{0.2}Ge_{0.8}$ channel due to Ge diffusion in the buffer/channel/spacer region during FTA, which

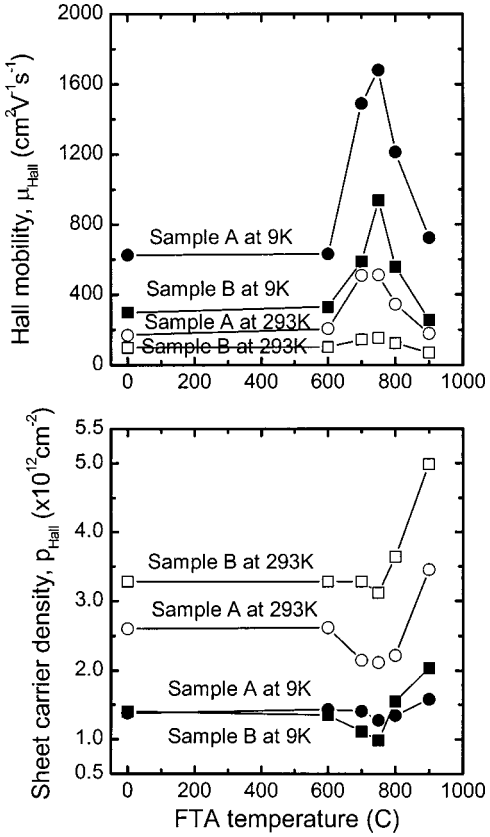

FIG. 3. FTA effect on the Hall mobility and sheet carrier density measured at 9 and 293 K for samples A and B.

resulted in a decrease in Ge concentration in the channel and as consequence the valence band offset decreased. This was confirmed by numerical solution of a one-dimensional (1D) Poisson–Schrödinger simulation. As the $Si_{0.7}Ge_{0.3}$ spacer width is decreased, due to B diffusion from the B doped $Si_{0.7}Ge_{0.3}$ layer and Ge diffusion from the $Si_{0.2}Ge_{0.8}$ channel (due to higher Ge content in the channel) carrier transfer from the B doped region increased. Consequently the sheet carrier density increased. The observed decrease in sheet carrier density with an increase of the FTA temperature (Fig. 3) corresponds to a case where the effect of a reduction of the valence band offset is dominant. The minimum in the sheet carrier density as a function of the FTA temperature corresponds to a case where the effect of the reduced $Si_{0.7}Ge_{0.3}$ spacer width becomes balanced by the effect of the reduction in the valence band offset. Finally, increases in the sheet carrier density with further increases of the FTA temperature correspond to a case where the effect of reduced $Si_{0.7}Ge_{0.3}$ spacer width becomes more important than the reduction in valence band offset.

The low Hall mobility observed in as-grown samples might be explained by the effect of short-range interface roughness scattering due to nonoptimum growth conditions, remote and background impurity scattering, and point defects that appear at low growth temperature because of reduced surface adatom mobility.[5] As was mentioned earlier annealing causes Ge diffusion in the buffer/channel/spacer region, resulting in a decrease in Ge concentration in the channel and consequently an increase in width of the $Si_{1-x}Ge_x$ channel ($x<0.8$). In addition, the point defects are annihilated during annealing. The observed increase of Hall mobility after FTA (Fig. 3) can be attributed to the reduction of interface roughness scattering due to smearing of the channel/spacer interface and broadening of the $Si_{1-x}Ge_x$ channel width L due to Ge diffusion because $\mu_{IR} \propto L^6$.[6,7] The mobility will increase until the effects of remote impurity scattering and alloy scattering begin to dominate. The mobility might be reduced due to a decrease in spacer thickness L_s because $\mu_{IR} \propto L_s^3$ (Refs. 6 and 7) and a decrease in the Ge composition x in the $Si_{1-x}Ge_x$ channel ($\mu_{AL} \propto [L/x(1-x)]$) (Refs. 6 and 7).

In summary, a strong FTA effect on the Hall mobility and sheet carrier density measured in the range of 9–300 K was observed in $Si_{0.2}Ge_{0.8}/Si_{0.7}Ge_{0.3}/Si(001)$ *p*-type MOD heterostructures. Pronounced increases of Hall mobility occurred after FTA at 700 and 750 °C with a maximum at 750 °C followed by decreases of the mobility after FTA at 800 and 900 °C. The sheet carrier density showed opposite behavior with an increase in the annealing temperature. In comparison with annealing experiments performed on SiGe MOD heterostructures with *p*-type Ge strained channels,[8] where the Hall mobility decreases even after annealing at 600 °C for 30 min, the heterostructures with $Si_{0.2}Ge_{0.8}$ channels show better thermal stability that make them more compatible for fabrication of SiGe MODFET and MOSFET devices using existing Si MOSFET technology.

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