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## Technique for producing highly planar Si/Si<sub>0.64</sub>Ge<sub>0.36</sub>/Si metal–oxide–semiconductor field effect transistor channels

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Si/Si<sub>0.64</sub>Ge<sub>0.36</sub>/Si heterostructures have been grown at low temperature (450 °C) to avoid the strain-induced roughening observed for growth temperatures of 550 °C and above. The electrical properties of these structures are poor, and thought to be associated with grown-in point defects as indicated in positron annihilation spectroscopy. However, after an *in situ* annealing procedure (800 °C for 30 min) the electrical properties dramatically improve, giving an optimum 4 K mobility of 2500 cm<sup>2</sup>V<sup>-1</sup>s<sup>-1</sup> for a sheet density of 6.2×10<sup>11</sup> cm<sup>-2</sup>. The low temperature growth yields highly planar interfaces, which are maintained after anneal as evidenced from transmission electron microscopy. This and secondary ion mass spectroscopy measurements demonstrate that the metastably strained alloy layer can endure the *in situ* anneal procedure necessary for enhanced electrical properties. Further studies have shown that the layers can also withstand a 120 min thermal oxidation at 800 °C, commensurate with metal–oxide–semiconductor device fabrication.

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Biaxial compressive strain in SiGe alloy layers splits the light and heavy hole subbands reducing the effective mass and suppressing carrier scattering, making possible enhanced mobilities in the two dimensional hole gas (2DHG) compared to those at the Si/SiO<sub>2</sub> interface. This, and the compatibility of the SiGe material system with silicon, offers the exciting prospect of an enhanced-performance, complementary metal–oxide–semiconductor (CMOS) technology.<sup>1</sup> To exploit the advantages of SiGe, the ability to grow highly planar SiGe layers is necessary to facilitate very large scale integrated (VLSI) processing and maximize performance gain. For high Ge concentrations such planar growth becomes increasingly difficult as strain driven “macroroughening” occurs, on a 100 nm lateral length at typical growth temperatures of 550 °C<sup>2</sup>—a phenomenon common to all growth techniques. Furthermore, it is necessary to thermally oxidize a Si cap layer to leave a Si spacer between the oxide and the SiGe channel. This must be very thin (~2 nm) to maximize transconductance and to suppress conduction in a second inferior mobility channel at the Si/SiO<sub>2</sub> interface. Growth at low temperatures has been reported to kinetically limit Si/SiGe/Si (001) surface roughening.<sup>3,4</sup> However, such low temperature growth perturbs crystallinity and consequently produces layers of low electrical quality.<sup>5</sup> High quality epitaxial material may be achieved by growing the chan-

nel at a low temperature and then annealing out atomic imperfections.<sup>6</sup> This growth strategy should be compatible with device manufacture, which requires appreciable thermal budgets for activation of dopant implants and oxidation.

In this letter we present a two-stage growth process for  $x=0.36$  pseudomorphic Si<sub>1-x</sub>Ge<sub>x</sub> layers. The process consists first of a low temperature deposition (450 °C) of both the SiGe channel (to suppress the macroroughening) and the Si capping layer. An *in situ* annealing stage is then performed under ultrahigh vacuum. The Si capping layer gives the metastably strained channel improved thermal stability during annealing.<sup>7</sup> For remote-doped structures the B doping supply layer is deposited after completion of the *in situ* anneal. We show that vacuum annealing leads to a dramatic increase in the 4 K carrier mobilities, compared to the as-grown sample, without degrading the structural integrity. We also report on thermal oxidation of undoped samples and show that the Si cap layer can be oxidized to give a very thin and uniform Si spacer layer between the SiO<sub>2</sub> and the SiGe channel.

The Si<sub>0.64</sub>Ge<sub>0.36</sub> strained layers were grown on *n*<sup>-</sup>Si (001) substrates at a growth rate 0.1 nm/s by solid source molecular beam epitaxy (MBE), in a V G V90S system. Prior to growth the wafers were chemically cleaned in a modified RCA etch, followed by a 90s 5% HF dip to hydrogen terminate the surface. The last cleaning stage consisted of an *in situ* 860 °C flash off to remove any residual native

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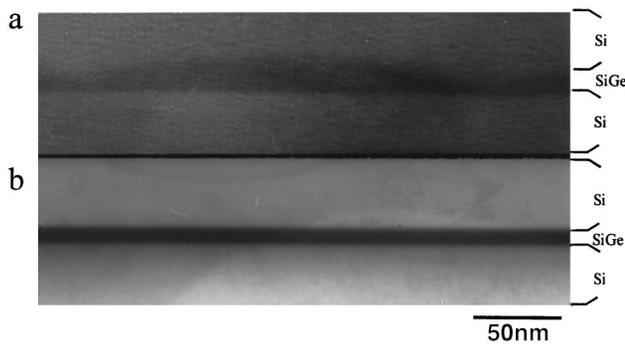


FIG. 1. (a) XTEM of Si/Si<sub>0.7</sub>Ge<sub>0.3</sub>/Si structure grown at 705 °C showing strain-induced local thinning of the SiGe ( $\Delta = 5$  nm  $\Lambda = 70$  nm). (b) XTEM micrograph of a Si/Si<sub>0.64</sub>Ge<sub>0.36</sub>/Si channel grown at 450 °C and annealed at 800 °C. The layer thickness was uniform with no discernible surface roughening.

oxide, followed by growth of a 250 nm high quality Si buffer. The temperature was reduced to 450 °C during this process before growing the Si<sub>0.64</sub>Ge<sub>0.36</sub> channel and 25 nm thick Si cap layer. Growth was then interrupted for the *in situ* 30 min anneal at temperatures  $T_a$  in the range 450–800 °C. Finally, in remote doped structures a 50 nm Si-B ( $2 \times 10^{18}$  cm<sup>-3</sup>) doping supply layer was grown at 600 °C. The doping layer was deposited after the annealing to minimize any temperature dependent B diffusion into the SiGe channel. All the samples had the same nominal structure but differed in the anneal temperature.

Specimens were structurally characterized by cross sectional and plan view transmission electron microscopy (TEM) and high resolution secondary ion mass spectroscopy (HRSIMS) using 500 and 250 eV O<sub>2</sub><sup>+</sup> sources at normal incidence. Positron annihilation spectroscopy (PAS) was also used to examine open-volume defects such as vacancies.<sup>8</sup> High resolution x-ray diffraction (HRXD) was used to determine the Ge concentration and strain condition. The 2DHG carrier concentration and mobilities were established by van der Pauw Hall measurements in the temperature range 4–300 K, on samples prepared using a standard photolithographic method.<sup>9</sup> Thermal oxidation was carried out at 800 °C for 2 h on undoped samples in a dry oxidation furnace in order to establish the resilience of the SiGe channel to the oxidation process.

Cross sectional TEM (XTEM) measurements on two SiGe alloy layers, one grown at a growth temperature of 705 °C, and the other grown at 450 °C and then annealed at 800 °C for 30 min, are shown in Figs. 1(a) and 1(b). The channel grown at 705 °C shows dramatic macroroughening, with a peak to peak amplitude  $\Delta = 5$  nm and lateral correlation length  $\Lambda = 70$  nm over the entire alloy surface. This is typical of compressively strained Si<sub>0.64</sub>Ge<sub>0.36</sub> grown at temperatures  $>550$  °C. The channel grown at low temperature was planar, with no observed dislocations. HRSIMS analysis of the as-grown samples (without annealing) revealed smearing of both the top (normal) and bottom (inverted) SiGe/Si interfaces, as expected for growth at 450 °C.<sup>10</sup> However, the Ge profile was found not to broaden significantly with anneal temperature, within the SIMS resolution limit, indicating that the Ge diffusion was minimal (Fig. 2). PAS on the as-grown (without anneal) sample showed significant positron trapping

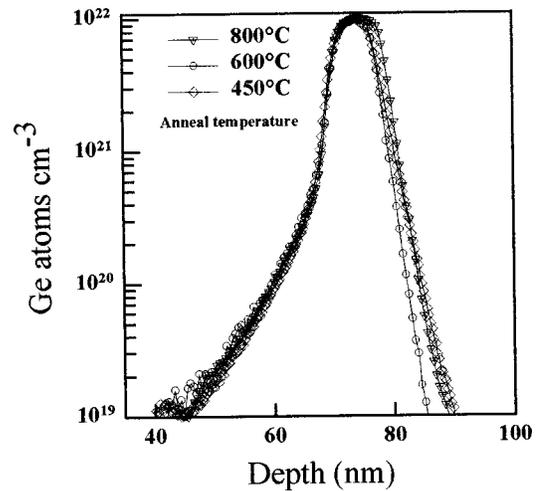


FIG. 2. Normalized Ge SIMS profiles for samples annealed in the temperature range 450–800 °C obtained using a 500 eV O<sub>2</sub><sup>+</sup> source at normal incidence.

at a depth equal to that of the Si<sub>epi</sub>/Si<sub>bulk</sub> interface. The defects appeared to consist of vacancy complexes, indicated by the decrease in the  $S$  parameter measured at the Si<sub>epi</sub>/Si<sub>bulk</sub> interface. However, no positron trapping was observed at defects in the samples annealed at 600 °C and above, indicating vacancy concentrations below the sensitivity limit ( $7 \times 10^{15}$  cm<sup>-3</sup>). HRXD confirmed the Ge fraction to be 36% and that the channel remained fully strained after annealing at temperatures of 750 °C.

The electrical properties of SiGe channels grown at low temperature were investigated by Hall measurements. The as-grown sample showed strong carrier freeze-out with a mobility of 20 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> at 30 K, indicative of poor material quality, although XTEM did not reveal any extended defects

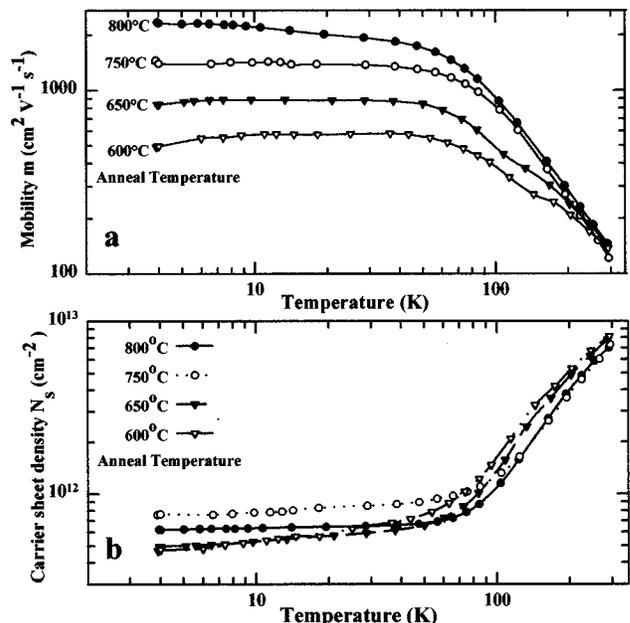


FIG. 3. (a) Carrier mobilities of samples subjected to annealing temperatures in the range 600–800 °C following growth at 450 °C. The as-grown sample showed strong carrier freeze-out compared to a mobility of 2500 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> with a carrier sheet density of  $6.2 \times 10^{11}$  cm<sup>-2</sup> for the sample annealed at 800 °C. (b) Carrier sheet density variations with anneal temperature.

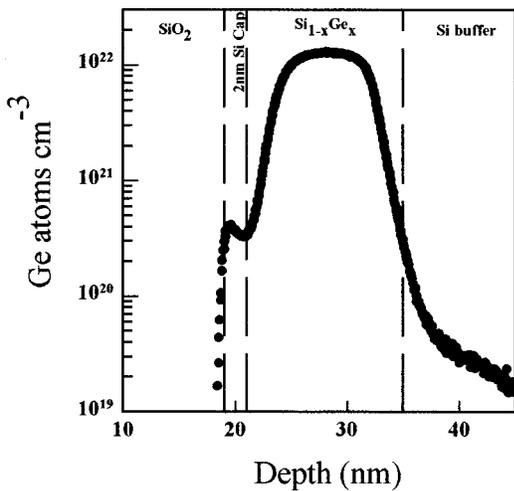


FIG. 4. Ge SIMS revealing the Ge pileup at the SiO<sub>2</sub>/Si interface, obtained using a 250 eV O<sub>2</sub><sup>+</sup> source at normal incidence.

(i.e.,  $<10^5$  cm<sup>-2</sup>, the detection limit of the technique). Figure 3(a) shows the temperature dependence of the Hall mobility obtained for samples annealed in the range 600–800 °C. The 4 K mobility increases dramatically with anneal temperature up to 2500 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> with a carrier sheet density of  $6.4 \times 10^{11}$  cm<sup>-2</sup> for  $T_a = 800$  °C. Figure 3(b) shows small carrier sheet density variations with anneal temperature and is being further investigated. Hall and strip analysis have been used to eliminate the effects of parallel conduction in the doping supply layer and yields room temperature transport characteristics  $\sim 3 \times$  greater than that obtained in a Si  $\mu$ MOS control. This is the subject of a future publication.

An oxidation study was carried out to investigate the stability of the channel under a low thermal budget CMOS process. SIMS revealed a Ge “pileup” ( $\sim 0.5\%$ ) at the SiO<sub>2</sub>/Si interface (see Fig. 4). It can be seen from Fig. 2 that Ge is present in the Si capping layer, seen as a shoulder in the SIMS leading edge. The Si is preferentially oxidized and the excess Ge accumulates behind the advancing SiO<sub>2</sub>/Si interface. In Fig. 5 it can be seen that the SiGe layer remains planar and that no dislocations are formed during the oxidation process. Crucially, a highly planar thin spacer layer has been produced with a thickness of  $\sim 2$  nm. The XTEM also shows the Ge pileup as a thin dark line at the SiO<sub>2</sub>/Si interface. The presence of 0.5% Ge in the Si cap will result in a reduction of  $\sim 1\%$  in the confining potential, which will not be determined for device applications and low frequency

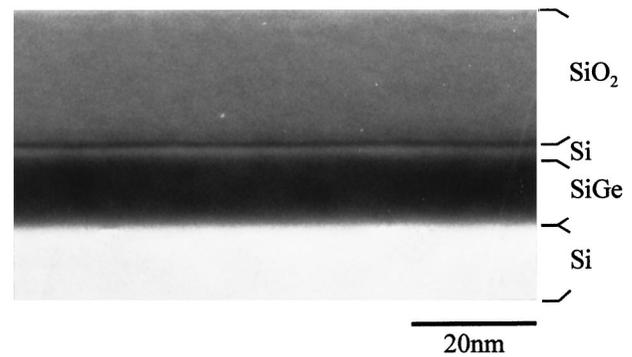


FIG. 5. XTEM of Si/Si<sub>0.64</sub>Ge<sub>0.36</sub>/Si channel grown at 450 °C and subsequently annealed at 800 °C for 2 h during the growth of the 30 nm of oxide. This shows a reduced cap thickness of 2 nm and that the interfaces remain planar during oxidation with no evidence of strain relaxation.

capacitance–voltage ( $C-V$ ) measurements indicate that an inversion layer can be created in the SiGe channel.

In summary, high Ge content ( $x=0.36$ ) heterostructures grown at low temperature, then annealed at temperatures up to 800 °C, have been found to have abrupt and planar interfaces. The enhancement of transport characteristics with annealing is attributed to a reduction in the grown-in defects from the SiGe channel. Oxidation studies revealed that the layers can withstand a thermal budget typical of that likely to be required in deep submicron device fabrication. Also, the SiO<sub>2</sub>/Si interface can be placed very close to the SiGe channel, thereby maximizing hole confinement in the SiGe, and device performance. This is only possible due to the suppression of the macroroughening of the alloy layer.

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