CALIFORNIA STATE UNIVERSITY NORTHRIDGE

Three Stage Low Noise Amplifier at 6GHz Frequency

A graduate project submitted in partial fulfillment of the requirements

For the degree of Masters of Science

in Electrical Engineering

By

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THREE STAGE LOW NOISE AMPLIFIER AT 6GHZ FREQUENCY

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Low Noise Amplifiers are the main components at the receiving end of nearly every communication system. The primary purpose of an LNA is to amplify the input signal while adding minimum noise as little as possible.

This project consist of a 6 GHz three stage Low noise amplifier. NEC and CAS are used to create and simulate the design. Microwave office is used to design and simulate the final configuration. The LNA is designed to produce a 35dB gain and an overall noise figure of 2dB at 6GHz frequency. However, the actual design provides an overall gain of 50dB and a noise figure of 1.04dB. The LNA designed meets and exceeds our design requirements. Advancements in the technology and the end user requirement has also influenced in pushing these limits to a new level.

This project gives a good base and hands on experience with the industrial standard tools. It also provides an overview of types of amplifiers, detailed design steps and types of matching techniques.

1. INTRODUCTION

Signal amplification is one of the most important radio frequency and microwave circuit functions. The introduction to radar in World War II provided the significance of microwave signals. Early microwave amplifiers were vacuum tube devices such as klystrons, travelling wave tube amplifiers and magnetrons, etc. Now all these are being dominated by solid state amplifiers except for the use of high power applications. Solid state devices are being classified into two types: 1) two terminal negative resistance diode devices 2) transistors. Nowadays we are using three terminal device transistors since it can control and amplify in an efficient manner. Solid state transistors are again being grouped into two types: bipolar and unipolar.

Many different types of amplifiers are available today and perform different functions. These include high-gain amplifiers, (HGA), maximum-gain amplifiers (MGA) which is a special case of HGA, low-noise amplifiers (LNA), and minimum-noise amplifiers (MNA) which is a special case of LNA. These general class of amplifiers have the same general design procedure and techniques and are usually narrow-band amplifiers. A low-noise amplifier is a specific type of amplifier that tries to maximize the amount of the gain while also reducing the amount of noise. Low noise amplifiers have many practical uses in automotive navigation, cellphones with GPS, wireless communications, and personal navigation devices.

LNA is a circuit that amplifies a signal while blocking noise. Like most circuit designs, LNA requires a tradeoff between the amount of gain and the amount of noise. In order to design any type of amplifier, we first need to take into account some of the features and

parameters such as biasing the transistor, operating point of the device, stability, gain and noise figure.

A RF transreciever typically includes a low noise amplifier, mixer, filter, power amplifier. LNA is the most important building block in the RF receiver. The LNA amplifies the weak signals from the antenna and duplex filter without adding too much noise to the overall system. Since it is the first stage in the receive path, its noise figure influences significantly to the system performance. Aside from providing gain, LNA should also have high linearity. To meet RF front end requirement, the LNA should have enough gain to amplify the received signals with little distortion, add low inherent noise, and match the input and output ports with unconditional stability. The effect of noise from subsequent stages of the receiver chain is reduced by the gain of the LNA, while the noise of the LNA itself is injected directly into the received signal. Thus, it is necessary for an LNA to boost the desired signal power while adding as little noise and distortion as possible, so that the retrieval of this signal is possible in the later stages in the system.

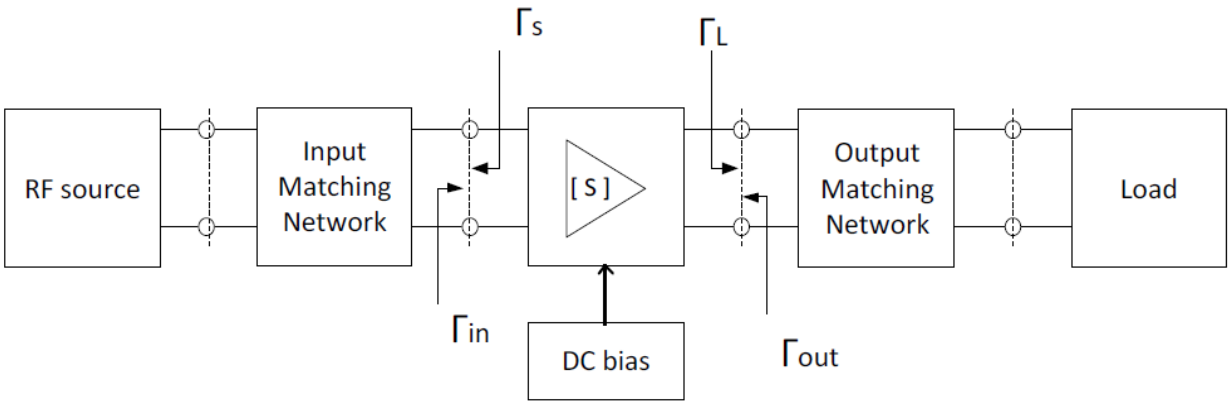


Figure 2.1: Block Diagram of a General Transistor Amplifier

For low noise, the amplifier needs to have a high amplification in its first stage. Therefore JFETs and HEMTs are often used. They are driven in a high-current regime,

which is not energy-efficient, but reduces the relative amount of shot noise. Input and output matching circuits for narrow-band circuits enhance the gain.

1.1 Design Goal

The following summarizes our design goal:

Parameter	Design Goal
Frequency(GHz)	6
Gain(dB)	35
Noise figure(dB)	< 2

2. AMPLIFIER THEORY

2.1 Noise

Noise figure is a measurement of noise performance in the circuit. In a microwave amplifier, even when there is no input signal, a small output voltage can be measured. We refer to this small output power as amplifier noise power. The total noise output power is composed of the amplified noise input power plus the noise output power produced by the amplifier.

The noise input power can be modeled by a noisy resistor that produces thermal noise. This noise is produced by the random fluctuations of the electrons due to thermal agitation. The rms value of the noise voltage V_n, produced by the noisy resistor R_n over a bandwidth, B is given by:

$$V_n = \sqrt{4kTBR_n} \tag{2.1}$$

Where k is Boltzmann's constant (i.e., k = 1.374×10^{-23}J/K) and T is the resistor noise temperature. The above equation shows that the thermal noise power depends on the bandwidth and not on a given center frequency. Such a distribution of noise is called white noise. The maximum available noise power from R_n is given by:

$$P_n = kTB \tag{2.2}$$

The noise figure describes quantitatively the performance of a noisy amplifier. The noise figure of an amplifier is defined as the ratio of the total available noise power at the

output of the amplifier to the available noise power at the output due to thermal noise from R_n.

The noise figure can be expressed in the following form:

$$F=\frac{P_{No}}{P_{Ni}\,G_A} \tag{2.3}$$

Where P_{No} is the total available noise power at the output of the amplifier, P_{Ni} = kTB is the available noise power due to R_n in a bandwidth B, and G_A is the available power gain. Since G_A can be expressed in the form of:

$$G_A = \frac{P_{So}}{P_{Si}} \tag{2.4}$$

Where P_{So} is the available signal power at the output and Ps_i is the available signal power at the input, then the equation (2.3) can be written as:

$$F = \frac{\frac{P_{Si}}{P_{Ni}}}{\frac{P_{Si}}{P_{No}}} \tag{2.5}$$

In other words, F can also be defined as the ratio of the available signal-to-noise power ratio at the input to the available signal-to-noise power ratio at the output. A minimum noise figure is obtained by properly selecting the source reflection coefficient of the amplifier.

The noise figure of a multistage amplifier can be given as follows:

$$F_{tot} = F1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots$$

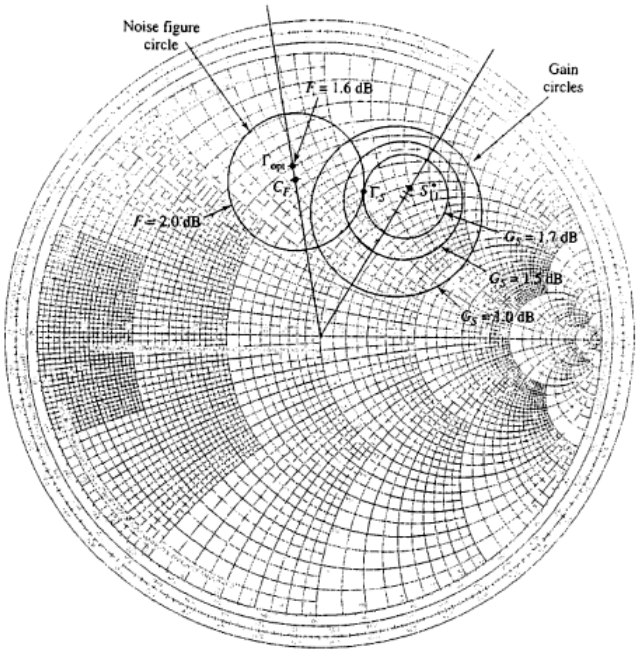


Figure 2.2: Example for Noise Figure and Gain Circles

2.2 Stability Factor

The stability of an amplifier or its resistance to oscillate is very important consideration in a design. These can be determined using S-parameters, matching networks, and the terminations. After selecting the desired transistor, it is necessary to check its stability. The transistor should be made unconditionally stable if it is either unstable or conditionally stable, before designing the amplifier. The necessary and sufficient conditions for unconditional stability are

$$K > 1 \text{ and } |\Delta| < 1$$

Where

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$

and

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|}$$

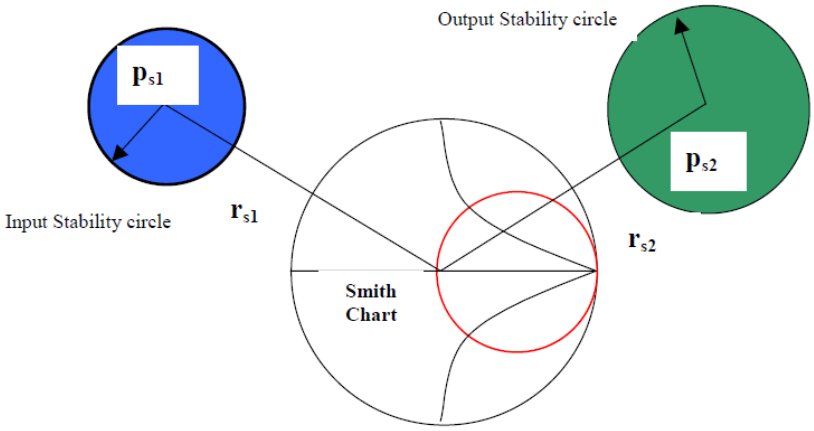


Figure 2.3: Example for Stability Circles

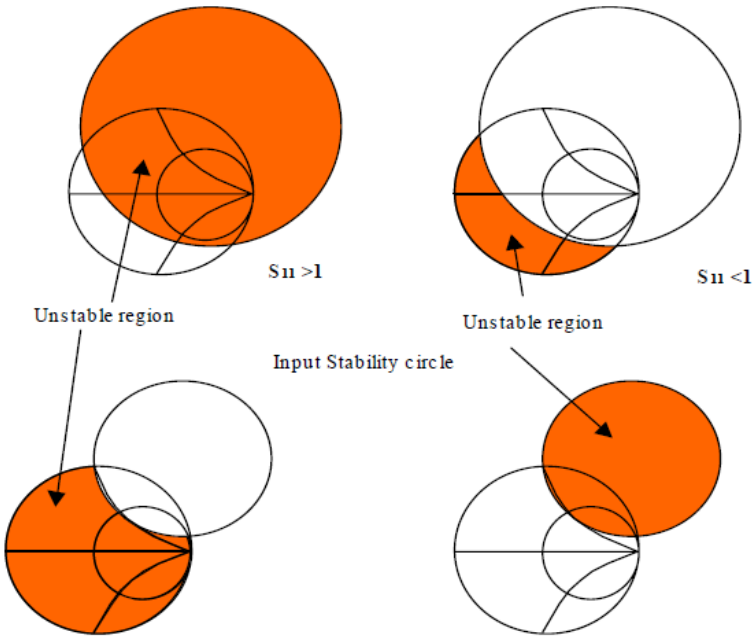


Figure 2.4: Areas of Instability

2.3 Gain (S- parameter)

S-parameters are valuable for characterizing a transistor and using the data to predict the performance and design of an amplifier circuit. The values of S-parameters depend on the properties of the transistor. With proper selection of Γ_S and Γ_L, it is possible to achieve maximum gain. Maximum power transfer from the input matching section to the transistor will occur when the following condition is satisfied:

$$\Gamma_S = \Gamma_{in}^{*}.$$

Where * is used to denote complex conjugation. The maximum power transfer from the transistor to the output matching section will occur if $\Gamma_L = \Gamma_{out}^{*}$. If these two conditions are satisfied, the resulting gain is given by:

$$G_{TU\max} = G_{S\max}\ G_0\ G_{L\max} = \frac{1}{(1-\left|S_{11}\right|^2)}\ \left|S_{21}\right|^2\ \frac{1}{\left|(1-\left|S_{22}\right|^2)\right|}$$

Where

$$\Gamma_S = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_L}$$

$$\Gamma_L = S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1-S_{11}\Gamma_s}$$

S_{12} is often small enough to be ignored and the equations above become as simple as

$$\Gamma_S = S_{11}^{*}$$

$$\Gamma_L = S_{22}^{*}$$

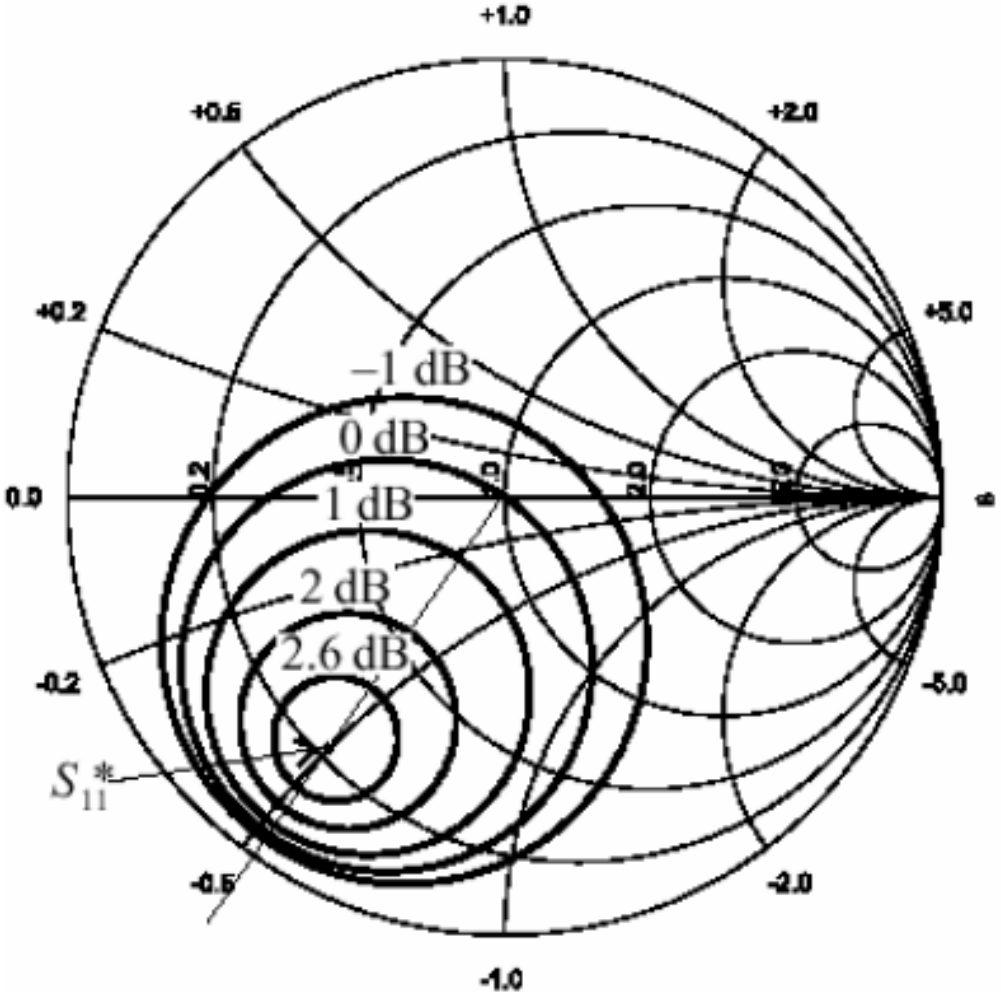


Figure 2.5: Example for Input Matching Network Gain Circles

3. DESIGN THEORY

3.1 RF/MW Circuit Design

As stated earlier, low noise amplifiers are more concerned with the amount of distortion at the output rather than the absolute gain. The LNA operates in Class A, usually at 15-20 % of its maximum useful current. Class A has a bias point roughly at the center of the maximum current and voltage characteristic of the transistor. The ideal LNA achieves a low noise figure, substantial gain, and stability over its entire useful frequency range. Its primary purpose in RF receiver architectures is to amplify extremely weak signals at very low-power levels without adding noise (distortion), therefore maintaining the desired Signal-to-Noise Ratio (SNR), where

$$SNR_{dB} = 10 \log \frac{P_{sig}}{P_{noise}}$$

The procedure for effective LNA design can be described as follows:

3.1.1 Select Proper Device

The transistor should exhibit high gain, have a low noise figure, and offer high IP3 (third order intercept point) performance at the lowest possible current consumption. The designer should first look at the main design parameters as: Noise, Gain, and IP3, and decide what Vce and Ic levels will produce optimal performance.

3.1.2 DC Bias Network Design

The DC Q-point of an amplifier must be chosen approximately in the midrange of current-voltage (I_D- V_{DS} for FET) characteristics for class A amplifiers. One of the popular arrangements for biasing a FET is shown below.

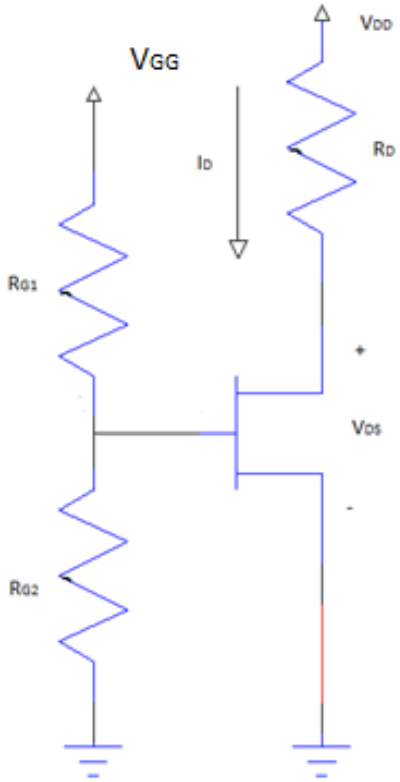


Figure 3.1 DC Biasing Circuit

The following equations are used to plot the load line:

$$V_{DD}=V_{DSQ} + R_D I_{DQ} \quad \text{(KVL)} \tag{1}$$

$$I_{DQ} = V_{DD} / R_D - V_{DSQ} / R_D \tag{2}$$

$$V_{GSQ} = (R_2 / R_1 + R_2) V_{GG} \tag{3}$$

Let V_{DD} =3V and V_{GG} = -3V. From the datasheet for V_{GSQ} = -0.4 V, we obtain I_{DQ} = 10mA, and V_{DSQ} = 2V at the Q- point. Substituting the values in equation (2) we get:

$$R_D = (V_{DD} - V_{DSQ}) / I_{DQ}$$

$$R_D = (3 - 2) / 10$$

$$R_D = 100 \text{ ohms}$$

Substituting the values of V_{GG} and V_{GSQ} in equation (3) we get:

$$-0.4 = (R_2 / R_1 + R_2) (-3)$$

$$\frac{R1}{R2} = \frac{2.6}{0.4} = 6.5$$

Assuming R_2= 100 Kohms, then R_1= 65 Kohms.

To begin the design of an amplifier a suitable quiescent point must be selected. The Q-point should be located in a linear region of the transistor drain voltage versus current curves. The Q-point affects the performance of the amplifier.

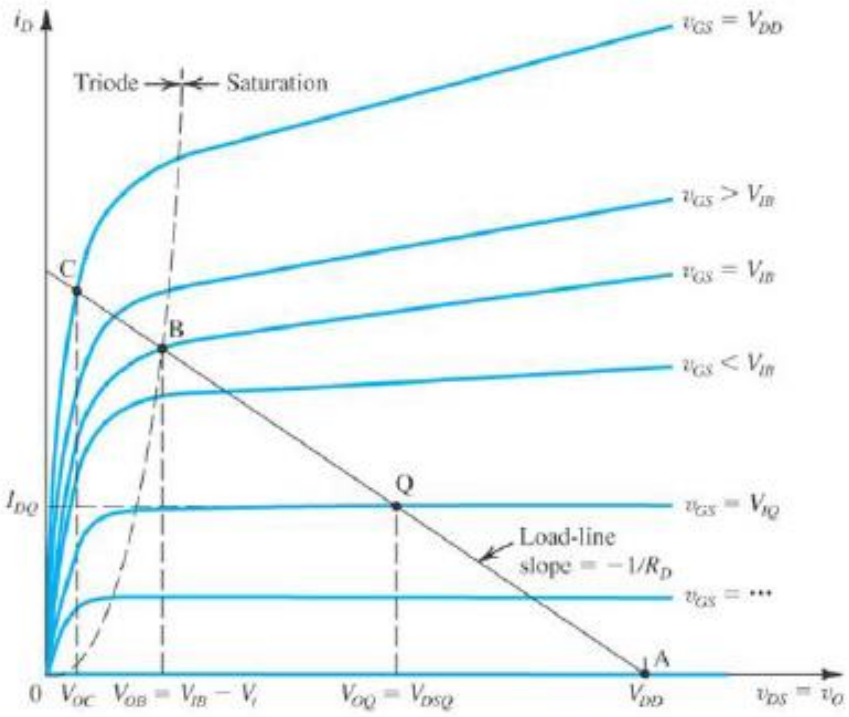


Figure 3.2: DC load line, Q point

3.1.3 Device Characterization

Measure the S-parameters of the transistors at the appropriate Q-point.

3.1.4 Stability Condition

There are two possible types:

a) *Unconditional Stability*: $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$ for all passive source and load impedances ($|\Gamma_S| < 1$ and $|\Gamma_L| < 1$).

b) *Conditional Stability*: $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$ for a limited range of passive source and load impedances.

The K-factor is a quick way to check the stability for the given biasing conditions. A sweep of the K-factor over frequency should be performed to ensure unconditional stability outside band of operation. There are five primary methods for circuit stabilization:

- Resistive loading of the input. This method is almost never used due to noise degradation of the LNA.
- Output resistive loading. This is the preferred method of stabilization, but should be used carefully because it effects lower gain, lower P1dB point and IP3.
- RLC feedback. This method is employed from collector-to-base to lower gain at lower frequencies adding stability.
- Filter matching. Usually used at the transistor output, this method is used for eliminating gain at high frequencies, far above the frequency of operation. Short circuit quarter-wave transformers used as notch filters or capacitors with same resonant frequency as frequency of oscillation can be employed to stabilize LNA.
- Emitter-feedback inductor. A small inductor can make the circuit more stable at higher frequencies, but if the source inductance is increased, the K-factor drops below 1.

In addition to these methods for stabilization, the LNA should be checked for stability far beyond the band of interest by verifying both small-signal and large-

signal stability. Stability circles should be verified on Smith Chart to check legitimacy of chosen Z_{in} and Z_{out}.

3.1.5 Input and Output Matching Network

When designing the input matching circuit we calculate the allocated gain values for both input(Gs) matching network and output (Gl) matching network, and the transistor gain (Go) Then, plot the input and output gain circles along with the noise figure circles on the same smith chart, we will choose the gain circles along with the noise figure circles on the same smith chart. We will choose the gain circle intercepting points with the desired noise figure circle. Use ΓS which lies on the constant gain circle between the intercept points and inside the constant noise figure circle to design the input matching networks. Similarly, plot the output gain circle and choose ΓL on the circle to design the output matching network.

3.1.6 Layout

Design the circuit schematic and physical design with matching networks using software tools (e.g. HFSS, Microwave Office, ADS).

3.1.7 Fabrication & Testing

Fabricate circuit on PCB using photolithography, solder devices on PCB, attach connectors, and test using vector network analyzer (VNA).

3.1.8 Post-process Tuning and Redesign

Apply minor adjustments to components and redesign amplifier if necessary.

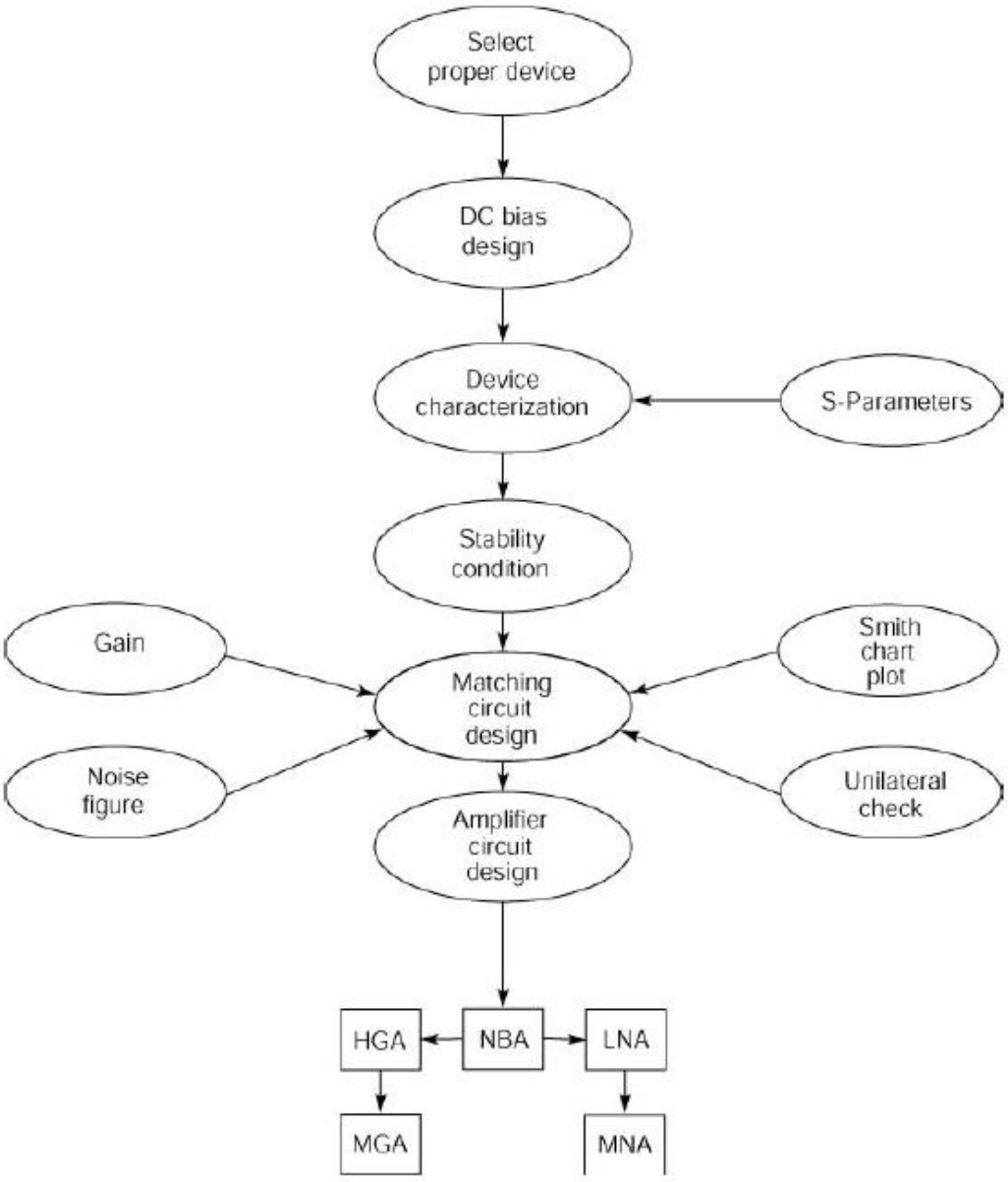


Figure 3.3 Summary of Design Steps

3.2 Matching Network Design

Normally this type of designs have a tradeoff between gain and noise figure, our goal is to get the maximum gain with the least amount of noise possible. We have to calculate allocated gain for input matching networks (G_S), output matching network (G_L) and also the transistor gain (G_O) while we design the input matching circuit.

The input and output values obtained are used to plot the smith chart along with the noise circles. The input matching networks are designed with the Γ_S values on constant gain circle between intercept points and constant noise figure circle. Same way we use the Γ_L on the constant gain circle to plot the output gain circle and design the output matching network.

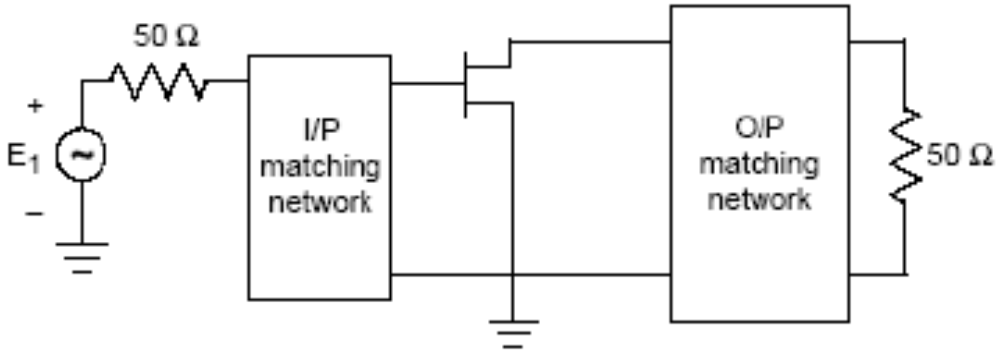


Figure 3.4: Example Circuit for Matching Network

3.3 Multistage LNA Design

Stability of transistor based amplifiers depends on the stability of each stage and also the stability of the entire network. Generally amplifier designed with transistors compose of N- number of stages in which every stage has its specific function. In our project we designed a three stage amplifier, the figure below shows an N-stage design.

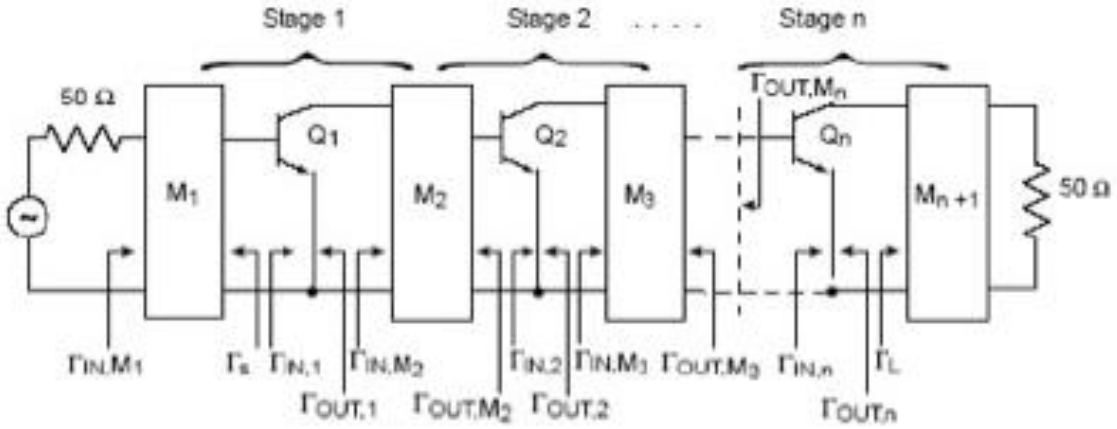


Figure 3.5: Multistage Amplifier Design

4. AMPLIFIER DESIGN USING MICROWAVE OFFICE SOFTWARE

4.1 DESING OF SINGLE STAGE LNA USING LUMPED ELEMENTS

This chapter will provide the design of a three stage low noise amplifier with a gain of 35dB and a noise figure less than 2dB at an operating frequency of 6 GHz. We will follow the process stated above to design the required LNA. Microwave Office from Advanced Wave Research (AWR) is used to simulate the amplifier prior to fabrication.

4.1.1 Selecting a Transistor

Initial step is to find an appropriate transistor that meets the requirements of the specifications. We have selected a NE32684A ultra low noise pseudomorphic HJ FET for our design. The F_{min} at 0.37 dB is giving us a total of 1.1 dB for the three stages and is under the desired 2dB. Small signal gain is 18.9 dB > (35/3) =11.6 dB, therefore the gain of the transistor is greater than the desired gain of the LNA. The Q point of the transistor is already set to V_{ds} =2V and I_{ds}=10mA.

The scattering parameters can be referred from the datasheet while the s2p file has to be uploaded into the software. Below is the AWR model of NE32684A.

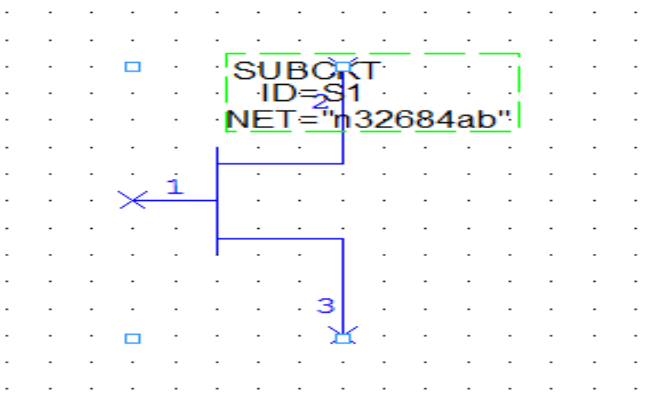


Figure 4.1 AWR Model of NE32684A

The S- parameters from the microwave office are being displayed below.

1.0	.986	-18.9	6.298	161.0	.014	77.6	.476	-11.5
1.5	.969	-27.7	6.248	152.4	.020	75.0	.469	-17.0
2.0	.948	-36.2	6.108	143.6	.026	72.2	.467	-22.0
2.5	.925	-44.3	5.955	135.3	.033	67.7	.454	-26.9
3.0	.894	-52.3	5.792	127.1	.038	62.0	.449	-31.2
3.5	.865	-60.0	5.567	119.6	.043	60.4	.439	-35.4
4.0	.833	-67.8	5.404	112.1	.049	55.8	.436	-40.4
4.5	.798	-75.0	5.216	104.8	.053	52.7	.427	-44.7
5.0	.766	-82.1	5.063	97.6	.058	49.4	.413	-49.2
5.5	.735	-89.1	4.872	90.9	.062	46.0	.406	-54.0
6.0	.703	-95.8	4.713	84.3	.067	44.1	.394	-58.3
6.5	.677	-102.5	4.542	77.7	.071	41.3	.389	-63.2
7.0	.653	-108.9	4.385	71.3	.074	38.3	.382	-67.4
7.5	.630	-114.0	4.245	66.3	.078	36.8	.377	-70.3
8.0	.607	-119.6	4.112	59.8	.082	33.8	.374	-74.9
8.5	.588	-125.3	3.983	54.3	.086	31.2	.373	-79.0
9.0	.569	-130.6	3.861	48.6	.090	28.3	.375	-83.3
9.5	.545	-136.2	3.775	43.0	.093	25.8	.377	-86.6
10.0	.529	-141.4	3.686	37.5	.097	23.4	.378	-90.8
10.5	.508	-147.3	3.591	32.0	.101	21.1	.378	-94.6
11.0	.487	-153.2	3.517	26.0	.107	18.4	.374	-99.4
11.5	.470	-159.7	3.446	20.5	.111	14.8	.370	-103.4
12.0	.454	-166.0	3.376	14.8	.114	11.8	.365	-108.0
12.5	.439	-172.6	3.312	9.6	.117	9.8	.360	-112.4
13.0	.428	-179.3	3.262	4.1	.121	6.3	.354	-116.8
13.5	.416	173.9	3.214	-1.3	.124	2.7	.350	-121.4
14.0	.407	167.9	3.165	-5.9	.130	0.6	.341	-125.5
14.5	.396	160.9	3.125	-11.7	.133	-2.3	.342	-130.5
15.0	.387	154.5	3.081	-17.3	.138	-5.4	.345	-136.6

Figure 4.2 Scattering Parameters From s2p File

Since we are operating at 6GHz frequency the S- parameters at that particular frequency are

$$[S] = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} 0.703\angle -95.8° & 0.067\angle 44.1° \\ 4.71\angle 84.3° & 0.394\angle -58.3° \end{bmatrix}$$

Since the S- parameters determine the stability of the transistor we will calculate the stability parameters which are K, Δ.

$$\Delta = S_{11}S_{22} - S_{12}S_{21} = (0.37\angle -98.18°) < 1$$

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} = 0.77 < 1$$

Since K< 1, $\Delta < 1$, the transistor is said to be conditionally stable. So we have to draw the input and output stability cirlces to find the stable region of operation. Stability circles were plotted using the S-parameters downloaded. The unstable regions are inside the blue circles, shown below. This suggests almost the entire Smith Chart is stable.

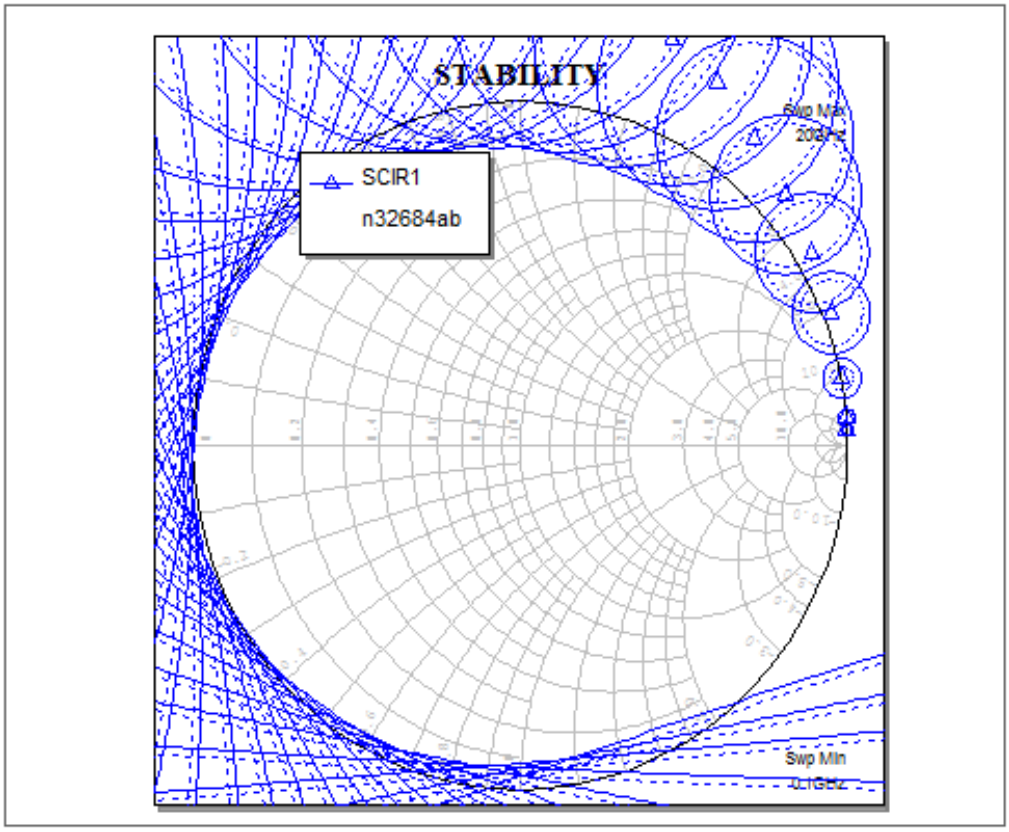


Figure 4.3 Stability Circles for NE32684A Transistor

4.1.2 Input Stability Circles

The center of the input stability circle is found by

$$c_S = \frac{S_{11} - \Delta^* S_{22}}{|S_{11}|^2 - |\Delta|^2} = 1.77 \angle 114.29^0$$

The radius of input stability circle is

$$r_S = \frac{|S_{12} S_{21}|}{\left||S_{11}|^2 - |\Delta|^2\right|} = 0.88$$

We tried drawing the input stability circle manually and using the microwave office software. A snap of the input and output stability circles in AWR is given below in figure 4.4.

4.1.3 Output Stability Circles

To determine the output stability circles we use $|S_{11}|$ if $|S_{11}|$<1 then the stability circle containing the center of the smith chart will be the stable region. Since from the below figure we can see that the output stability circle does not include the center of the smith chart, so the stable region is within the smith chart which does not include the output stability circle.

$$c_L = \frac{S_{22}^* - \Delta^* S_{11}}{|S_{22}|^2 - |\Delta|^2} = 21.40 \angle 99.7^0$$

$$r_L = \frac{|S_{12} S_{21}|}{\left||S_{22}|^2 - |\Delta|^2\right|} = 20.76$$

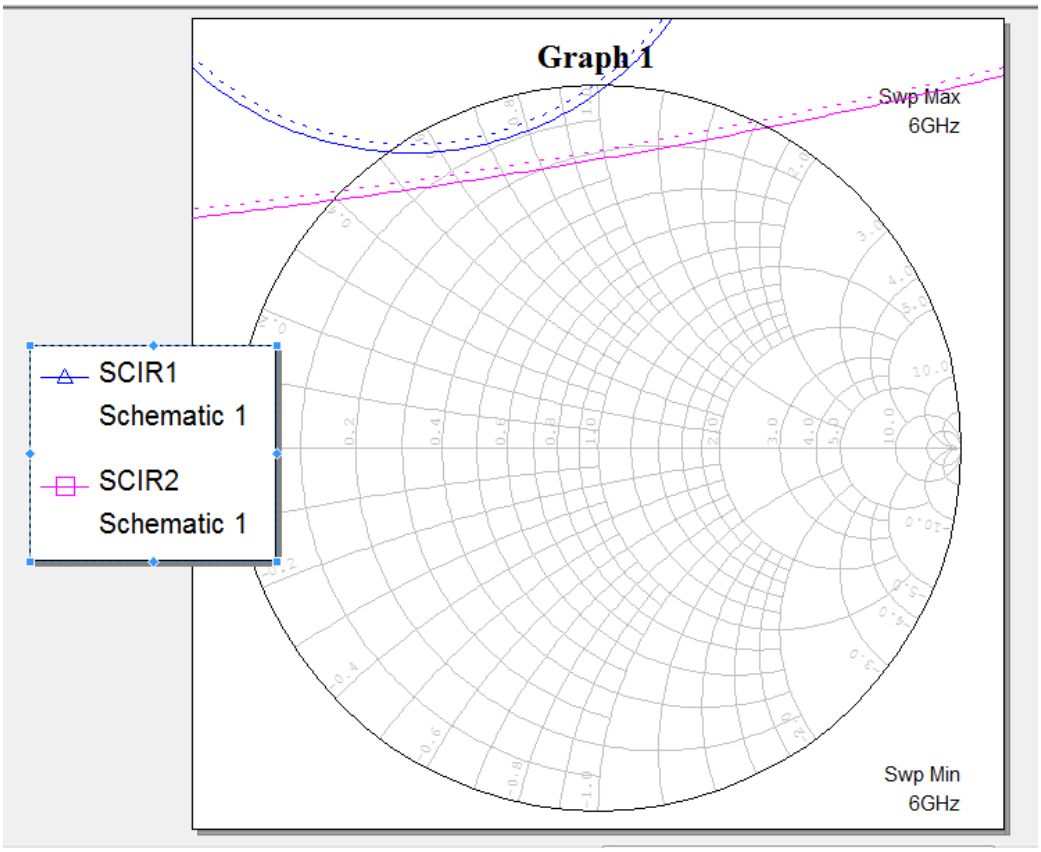


Figure 4.4 Input and Output Stability Circles

Since the stable regions are being determined, now we have to check if the transistor will be unilateral or bilateral case. The unilateral figure of merit of transistor is

$$U=\frac{|S_{11}||S_{12}||S_{21}||S_{22}|}{(1-|S_{11}|^2)(1-|S_{22}|^2)} \quad =0.204$$

The maximum transistor gain is given by

$$G_{TU\max} = G_{S\max}\ G_0\ G_{L\max} = \frac{1}{(1-|S_{11}|^2)}\ |S_{21}|^2\ \frac{1}{(1-|S_{22}|^2)}$$

Where

$$G_{S\max} = \frac{1}{(1-\left|S_{11}\right|^2)}$$

$$= \frac{1}{1-0.7^2}$$

$$= \ 2.9\text{dB}$$

$$G_0 = \left|S_{21}\right|^2 = 13.46\text{dB}$$

$$G_{L\max} = \frac{1}{\left|(1-\left|S_{22}\right|^2)\right|}$$

$$= \frac{1}{1-0.39^2} = 0.73\text{dB}$$

$$G_{TU\max} = G_{S\max}\ G_0\ G_{L\max}\ = (13.46+0.73+2.9)\ \text{dB}$$

$$G_{TU\max} = 17.11\text{dB}$$

The error in the transducer gain caused by the unilateral assumption is given by,

$$\frac{1}{(1+U)^2} < \frac{G_T}{G_{TU\max}} < \frac{1}{(1-U)^2}$$

$$\text{-1.61dB} < \frac{G_T}{G_{TU\max}} < 1.98\text{dB}$$

4.1.4 Noise Figure Circles

The 1dB noise figure circle is plotted with the noise figure parameter (N) calculated as:

$$N = \frac{F - F_{min}}{\frac{4R_N}{Z_0}} \left|1 + \Gamma_{opt}\right|^2$$

$$N = \frac{1.25 - 1.08}{4(0.21)} |1 + 0.62\angle 91°|^2$$

$$N = 0.272$$

We then calculate the center and radius of the 1 dB noise figure circle:

$$C_F = \frac{\Gamma_{opt}}{N + 1}$$

$$= \frac{0.62\angle 91°}{0.272 + 1}$$

$$C_F = 0.488\angle 91°$$

$$R_F = \frac{\sqrt{N\left(N + 1 - \left|\Gamma_{opt}\right|^2\right)}}{N + 1}$$

$$= \frac{\sqrt{0.272(0.272 + 1 - 0.62^2)}}{0.272 + 1}$$

$$R_F = 0.38$$

4.1.5 Gain Circles

While designing a transistor for a specific gain, the goal is to design an input and output matching network so that we get the required gain. So we assume Gs= 2dB, now we need to draw the 2 dB gain circle by selecting:

$$G_S = 2dB = 1.58$$

$$g_S = G_S / G_{S\max} = 1.58/\ 1.94 = 0.81$$

The center and radius of the 2dB gain circle are calculated using the formulas below:

$$C_S = \frac{g_S {S_{11}}^*}{1-(1-g_S)|S_{11}|^2} = 0.62\angle 95.8°$$

$$R_S = \frac{\sqrt{1-g_S}(1-|S_{11}|^2)}{1-(1-g_S)|S_{11}|^2} = 0.245$$

The transducer gain circle is considered to be 0dB so the g_L is calculated to be as

$$G_L = 0dB = 1$$

$$g_L = G_L / G_{L\max} = 1/\ 1.18 = 0.84$$

The center and radius of the 0dB gain circle are calculated using the formulas below:

$$C_L = \frac{g_l {S_{22}}^*}{1-(1-g_l)|S_{22}|^2} = 0.34\angle 58.8°$$

$$R_L = \frac{\sqrt{1-g_l}(1-|S_{22}|^2)}{1-(1-g_l)|S_{22}|^2} = 0.34$$

The input matching network is designed by choosing any point located both on the 2dB gain circle and inside the 1dB noise figure circle. The reflection coefficient at the source is selected farthest away from the input stability circle. In the same way the reflection coefficient at the load value is selected at any point located on the 0dB gain circle. The smith chart plot is presented below where the Γ_S and Γ_L values are chosen inside the noise figure circle and on the gain circle.

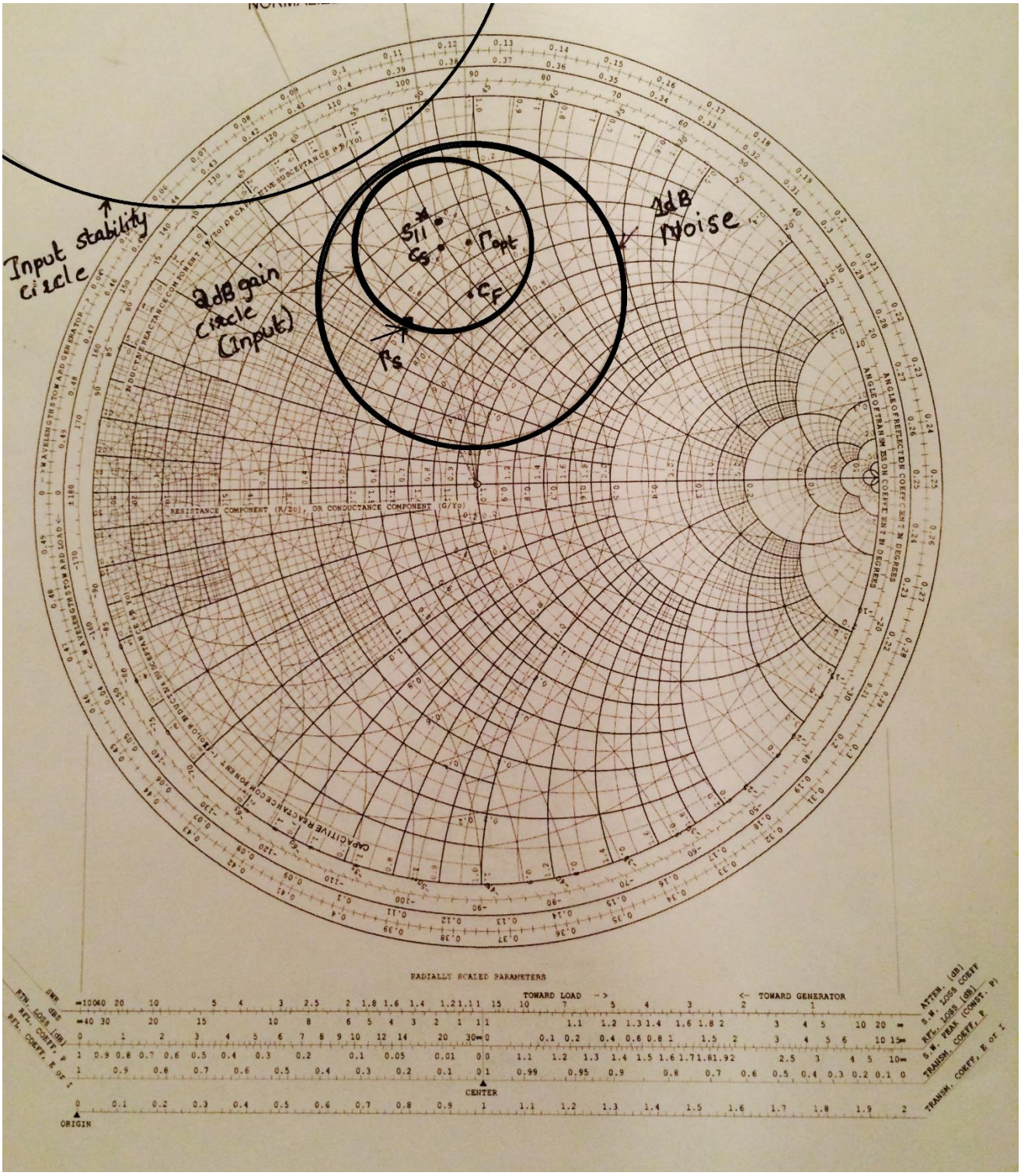


Figure 4.5 Reflection Coefficient at Source

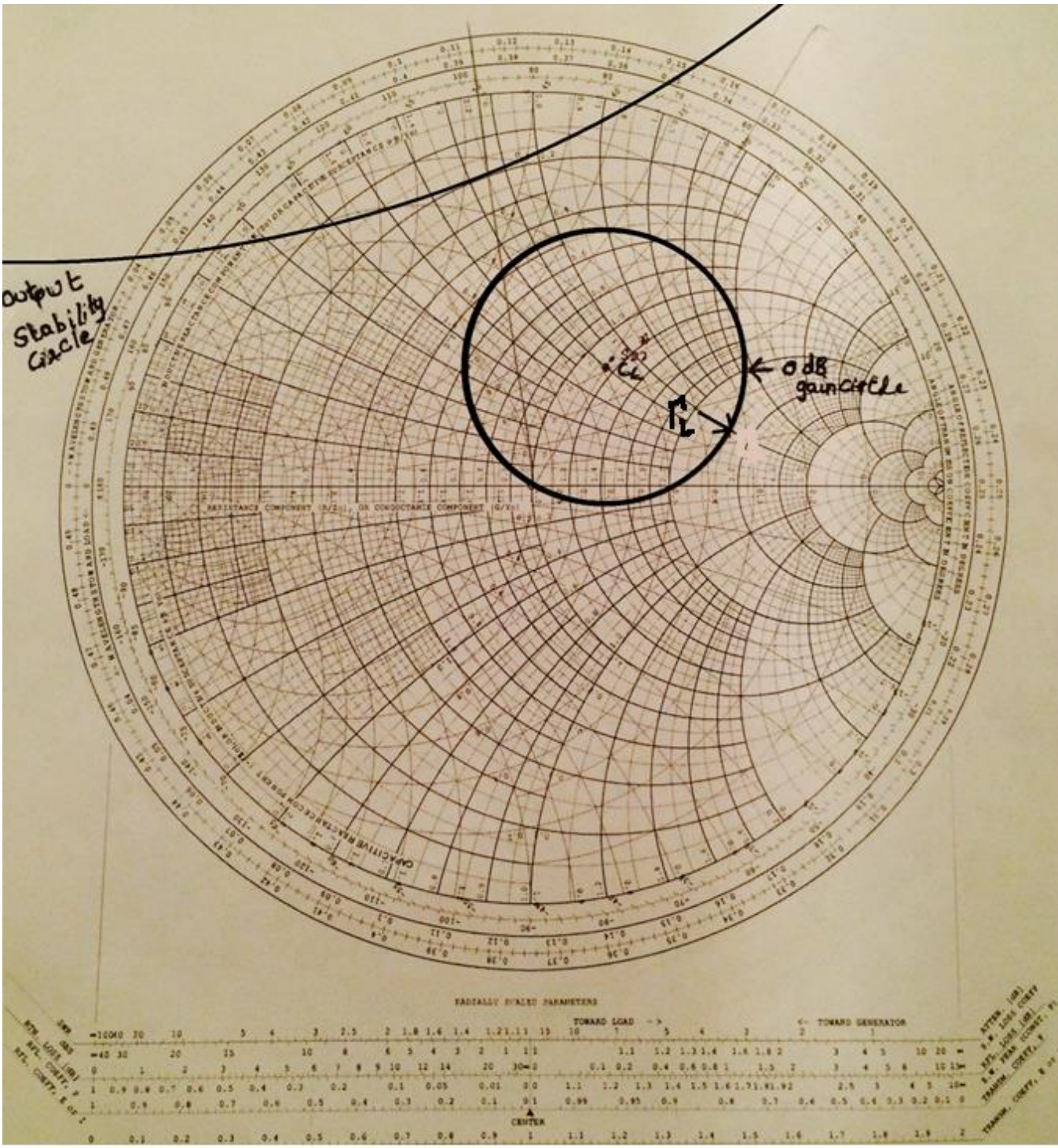


Figure 4.6: Reflection Coefficient at Load

4.1.6 Input matching network

Input matching network can be designed by moving from the center of the smith chart to the Γ_S value. From the Smith Chart above, the optimum solution is Γ_S = 0.46∠114.5°, yielding G_S = 2 dB and F = 1 dB.

The element values for the input matching network:

Shunt c:

$$jb_p = \frac{j\omega c}{(Y_0)}$$

$$0.55j = \frac{jx2\Pi x\ 6x10^9 xc}{(0.02)}$$

C= 0.53 pF

Series L

$$jx_s = \frac{j\omega L}{(Z_0)}$$

$$0.42j + 0.2j = \frac{j\ x\ 2\Pi\ x\ 6\ x\ 10^9\ x\ L}{(50)}$$

L=1.35nH

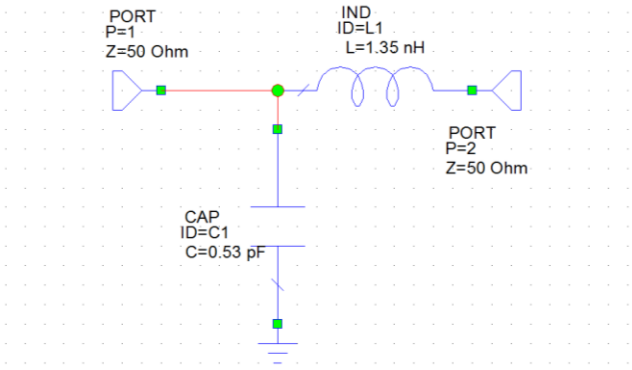


Figure 4.7 Input Matching Network

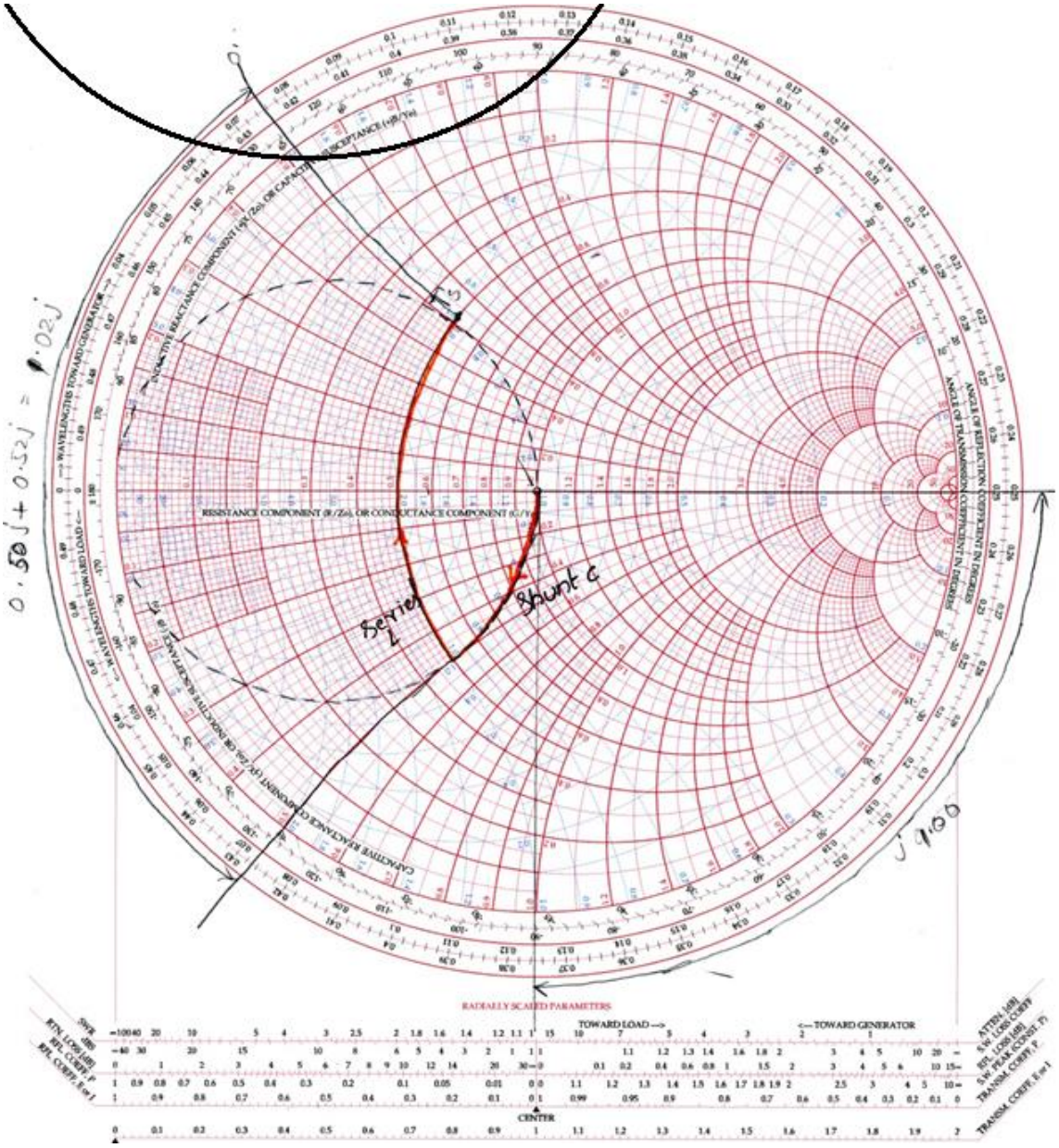


Figure 4.8 Smith Chart for Input Matching Network

4.1.7 Output Matching Network

Output matching network can be designed my moving from the center of the smith chart to the selected Γ_L value. The elements values for the output matching network are

Series C:

$$jx_s = \frac{-j}{(Z_0 \omega C)}$$

C= -0.37 pF

Shunt L:

$$jb_p = \frac{-j}{(\omega L Y_0)}$$

L= -2.21nH

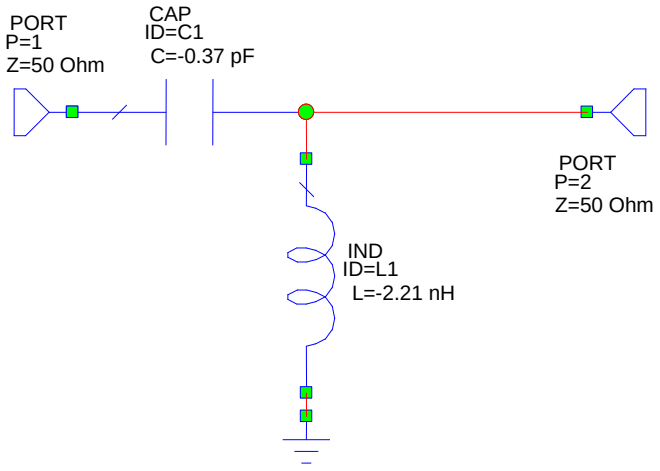


Figure 4.9 Output Matching Network

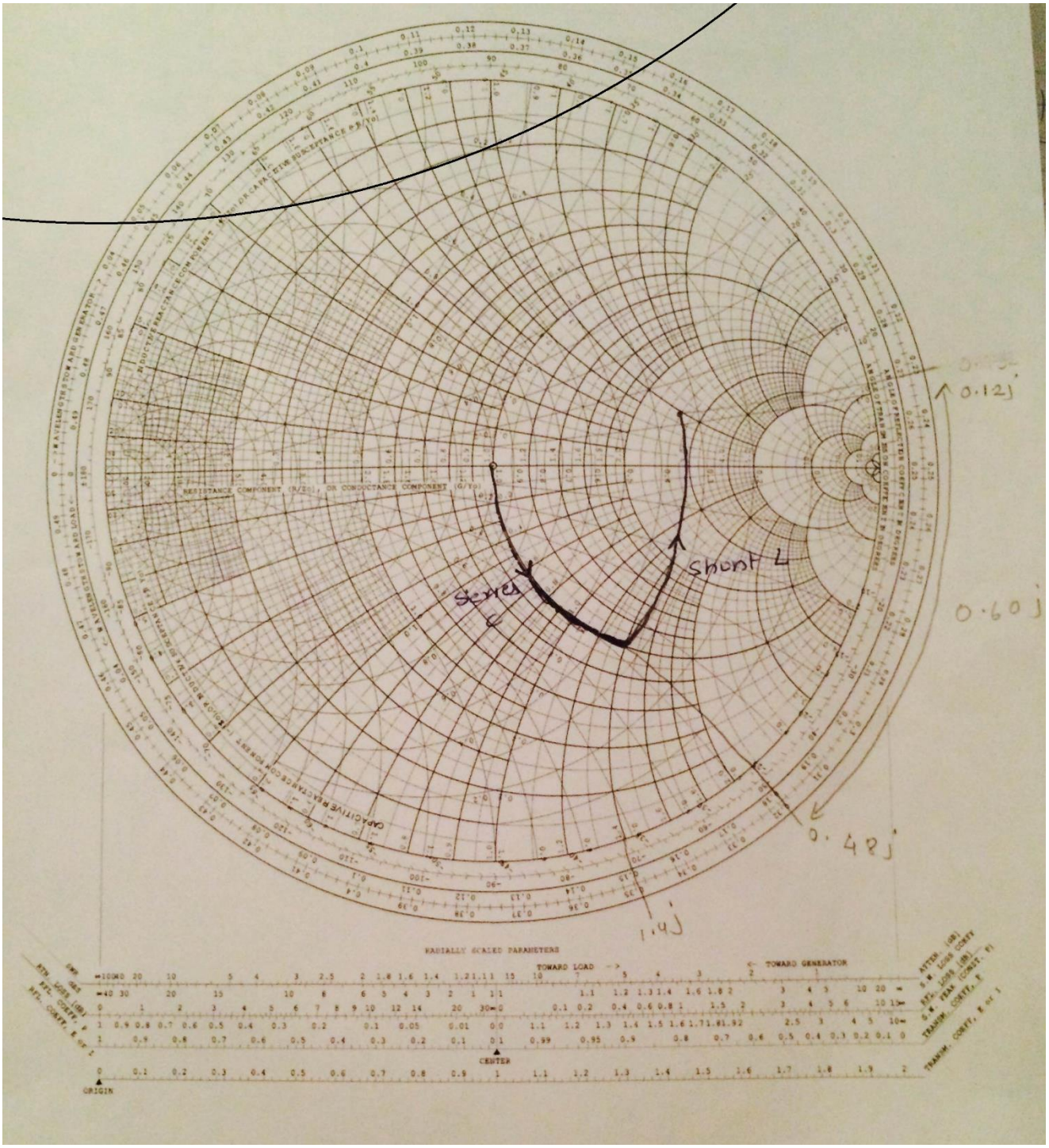


Figure 4.10 Smith Chart for Output Matching Network

The final design of the single stage LNA is given in figure 4.10. Looking at the results the noise figure comes out to be 0.59 dB for a single stage with gain of 17.9 dB. The values are much better after designing the matching network

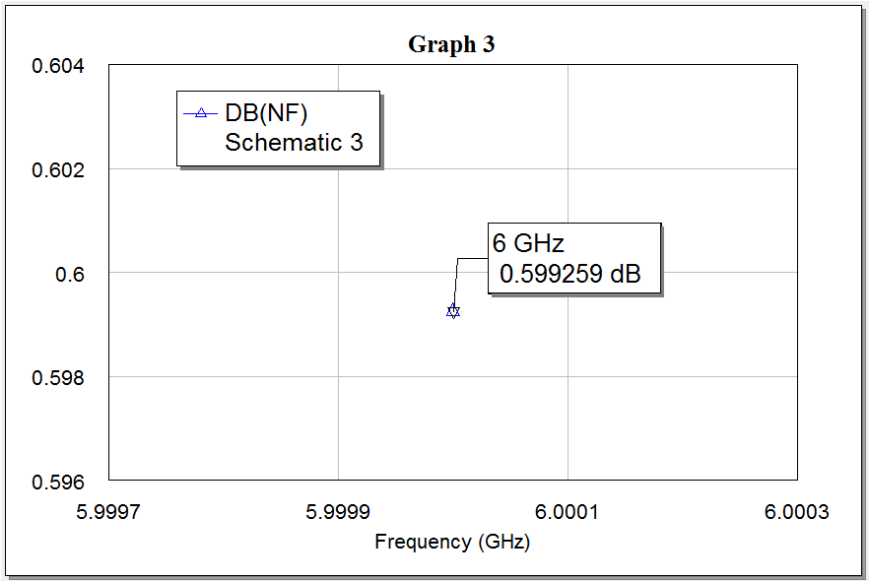


Figure 4.11 Noise Figure for Single Stage

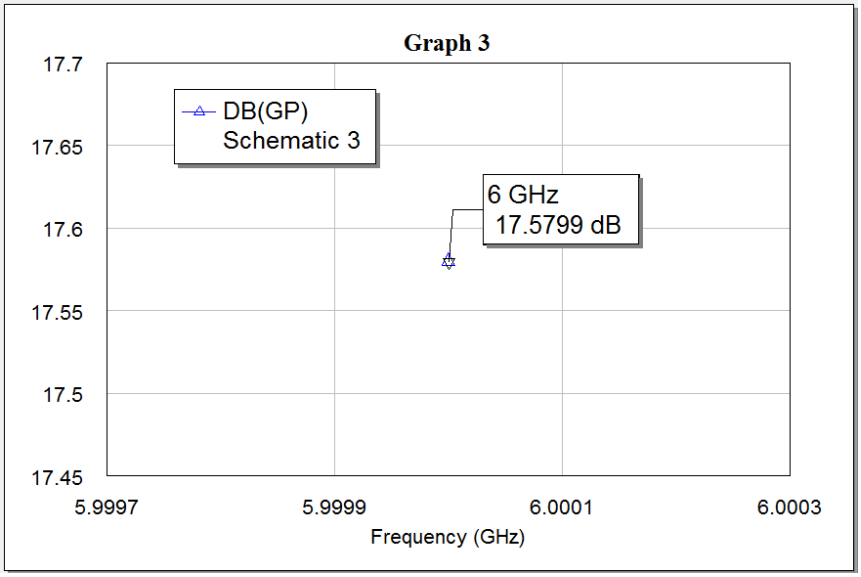


Figure 4.12 Power Gain for the Single Stage LNA

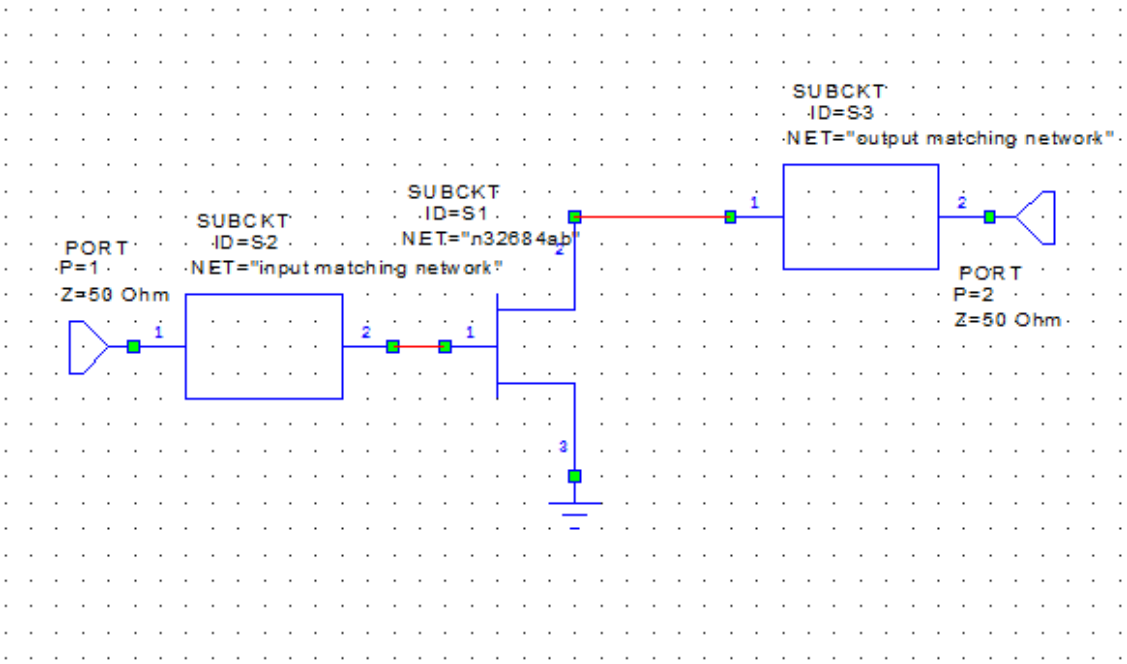


Figure 4.13 Single Stage LNA Schematic with Subcircuits

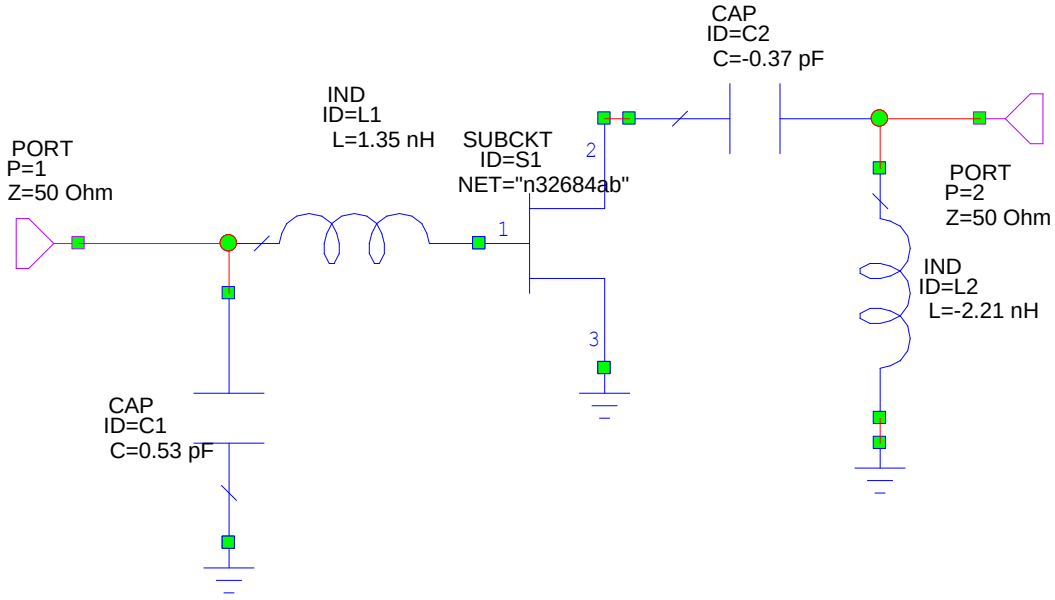


Figure 4.14 Schematic of Single Stage LNA Using Lumped Elements

4.2 Multistage LNA

The noise figure of the cascaded amplifier is given by:

$$F_{tot} = F1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots$$

F1= Noise figure of first stage, F2= noise figure of second stage, F3= noise figure of the third stage. Since all the transistors are same we have noise figure F1=F2=F3= 1dB = 1.25 and G=G1=G2= 11.66dB= 14.45

$$F_{tot} = 1.25 + \frac{1.25 - 1}{14.45} + \frac{1.25 - 1}{14.45\ x\ 14.45}$$

=1.04dB

For a cascade design identical stages can be combined together without any changes in the matching network. Figure 4.12 shows the full schematic. The main benefit of using cascade method is that it's less time consuming than designing a different matching network.

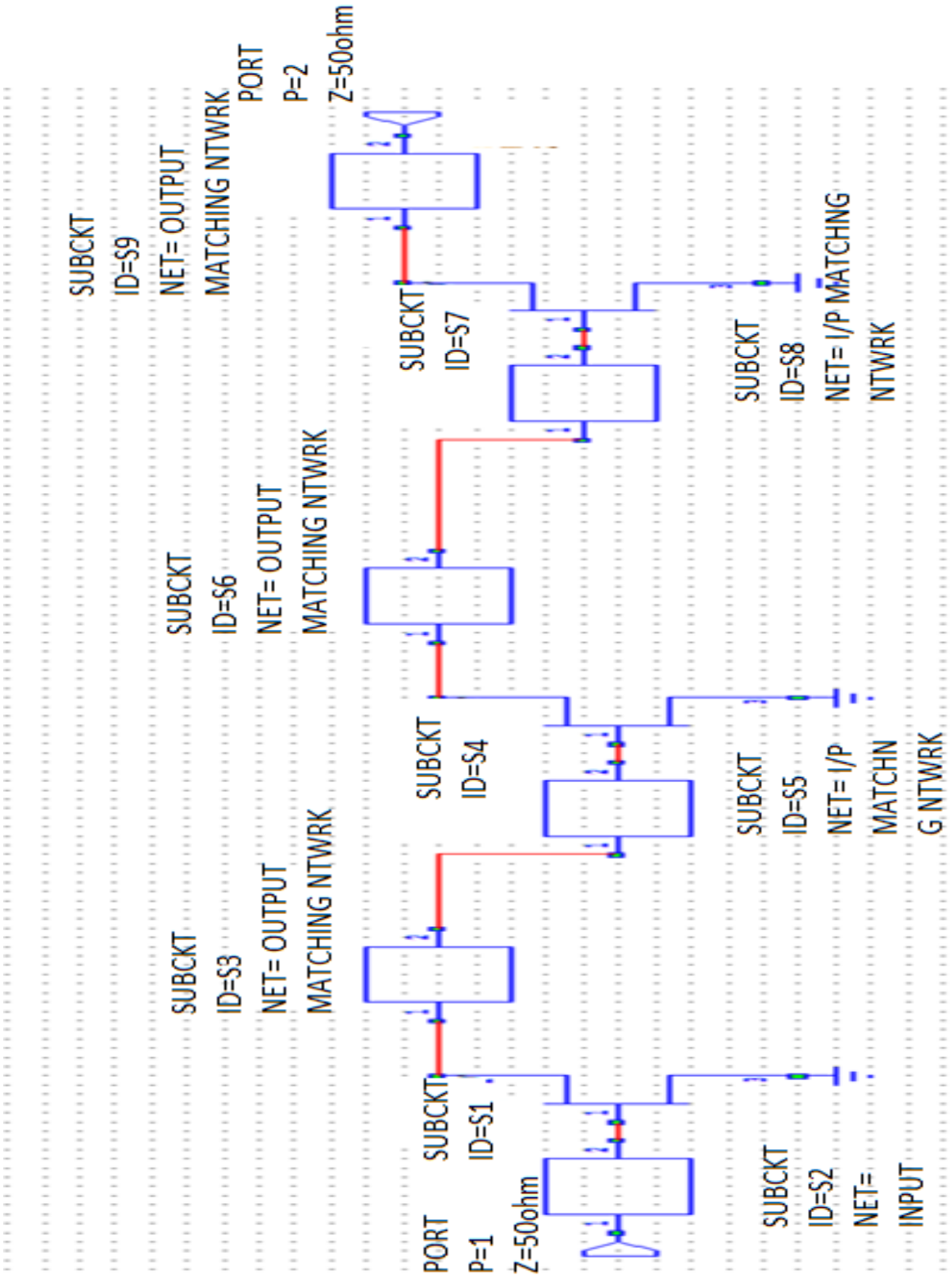


Figure 4.15 Cascaded LNA

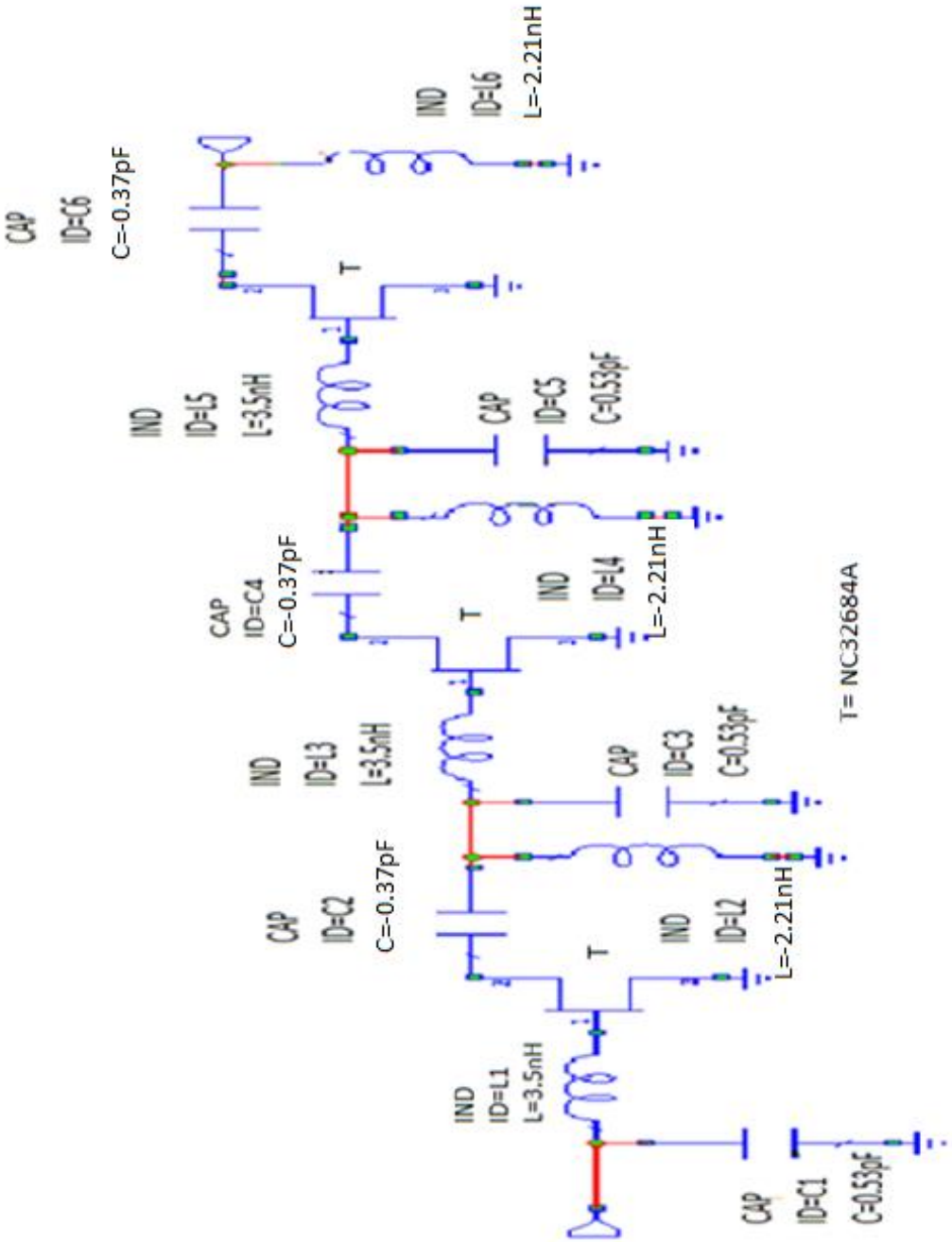


Figure 4.16 Cascade LNA using Lumped Elements

The above figure shows the cascaded LNA at 6GHz using lumped elements. The graphs are being plotted for the transducer power gain, noise figure and power gain of a three stage low noise amplifier.

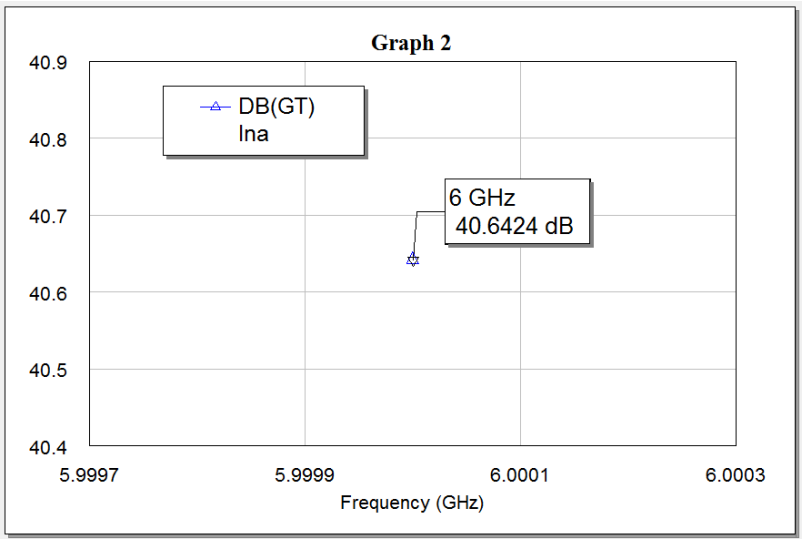


Figure 4.17 Transducer Power Gain for Three Stage LNA

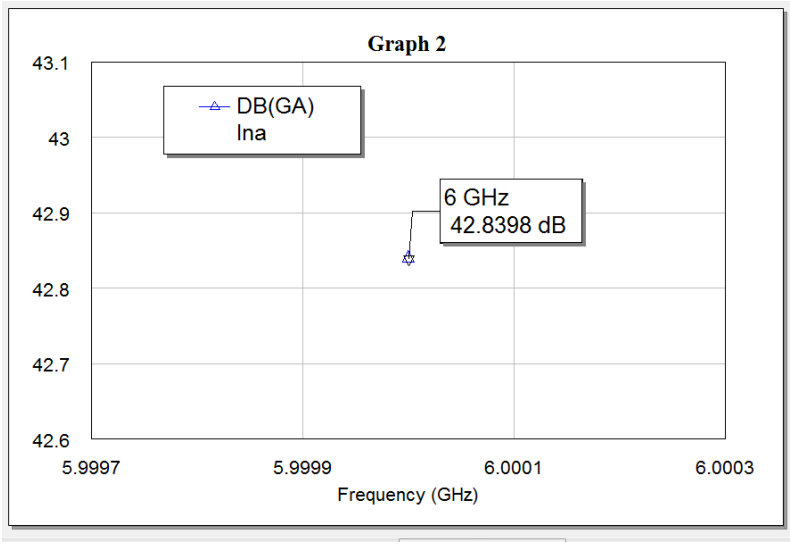


Figure 4.18 Available Gain for a Three Stage LNA

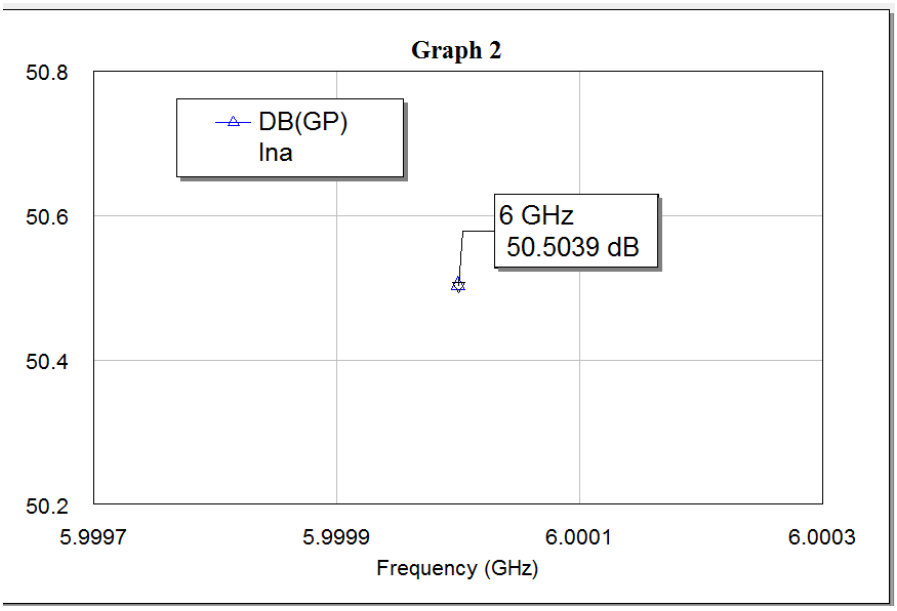


Figure 4.19 Power Gain at 6Ghz

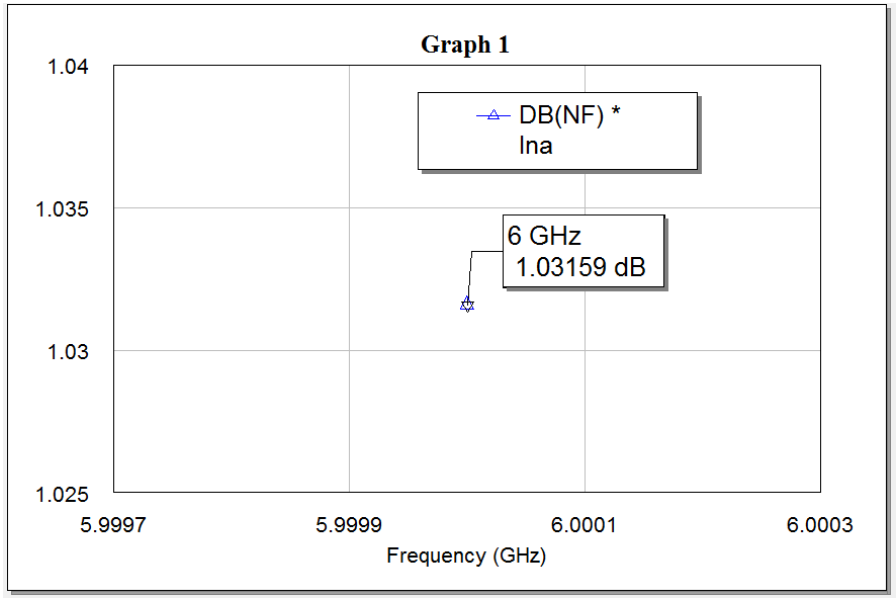


Figure 4.20 Noise Figure in dB for Three Stage LNA at 6GHz

5. CONCLUSION

A low noise amplifier was designed, built, and tested. A NE32684A ultra low noise pseudomorphic HJ FET for our design which exhibits a minimum noise figure of 0.35dB at 6GHz frequency. At a 6GHz frequency the low noise amplifier exhibits low noise, moderately high gain, and good input and output return loss.

The three stage low noise amplifier was designed using cascading technique. A low noise amplifier is designed to operate in a linear region due to small signal input. In our case linearity is not tested because of the unavailability of a nonlinear transistor. But it is believed that the combination of small signal and linear components would produce an output, which is linear to the input.

In this 3- stage low noise amplifier we have achieved a power gain of 57.4 dB and a noise figure of 1.04dB. These values meet and exceed our design requirements. AWR microwave office made the design process very simple and its collaboration with semiconductor companies provided accurate results.

PARAMETER	DESIGN GOAL	Hand Calculations	MATLAB RESULTS	AWR RESULTS
Frequency(GHz)	6	6	6	6
Noise figure(dB)	< 2	1.04	1.037	1.031
Gain(dB)	35	50.32	50.57	50.5

References

1. Matthew M. Radmanesh. RF & Microwave Design Essentials. Bloomington, Indiana: Authorhouse, 2007.

2. David M. Pozar. Microwave Engineering, Fourth Edition. Hoboken, New Jersey: John Wiley & Sons, Inc., 2012.

3. I. J. Bahl, Fundamentals of RF and Microwave Transistor Amplifiers. Wiley, 2009.

4. M. M. Radmanesh, Advanced RF & Microwave Circuit Design: The Ultimate Guide to Superior Design. AuthorHouse, 2009.

5. Iulian Rosu. "LNA Design." YO3DAC - VA3IUL. Iulian Rosu. RF Technical Articles. Retrieved 20 October 2014. http://www.qsl.net/va3iul/"

6. Michael V. Aust,et.al. "Wideband Dual-Gate HEMT Low Noise Amplifier for Front-End Receiver Electronics." IEEE Compound Semiconductor Integrated Circuit Symposium, Nov. 2006, p. 89-92.

7. G. Gonzalez, Microwave Transistor Amplifiers: Analysis and Design, New Jersey: Prentice Hall, 1997.

8. I. Bahl and P. Bhartia, Microwave Solid-State Circuit Design, New York: Wiley Interscience, 1988.

APPENDIX 1

MATLAB CODE

```
S11_mag=0.703;

S12_mag=0.067;

S21_mag=4.713;

S22_mag=0.394;

%Input S-parameters
S11=-0.071-0.699i
S12=0.048+0.046i
S21=0.468+4.689i
S22=0.207-0.335i
s22=0.207+0.335i % conjugate of s22
s11=-0.071+0.669i % conjugate of s11


Z0=50;%characteristic impedance

%1) Check stability.
d=(S11*S22)-(S12*S21)%delta
K=(1-((abs(S11)).^2)-((abs(S22)).^2+(abs(d)).^2))./(2*abs(S12)*abs(S21))%K

% input stability cirles
ds=abs(S11)^2-abs(d)^2
rs=abs((S21*S12)/ds)
cs= (conj(S11-(d*s22)))/ds

% output stability circles
dl=abs(S22)^2-abs(d)^2
rl=abs((S21*S12)/dl)
cl= (conj(S22-(d*s11)))/dl
%2) Find gains.
%Unilateral Case- maximum gain:

G0=abs(S21).^2
Gs_max=1./(1-((abs(S11)).^2))
```

```
Gl_max=1./(1-((abs(S22)).^2))

G0_dB=10*log10(G0)
Gs_max_dB=10*log10(Gs_max)
Gl_max_dB=10*log10(Gl_max)

GTU_max_dB=G0_dB+Gs_max_dB+Gl_max_dB

%3) Plot gain circles.
%input gain circles
Gs_dB=2;
Gs=10.^(Gs_dB./10)
Gl_dB=0;
Gl=10.^(Gl_dB./10)

gs=Gs./Gs_max;
Cgs_mag=(gs*S11_mag)./(1-(S11_mag).^2*(1-gs));
Cgs_deg=-S11_deg;
Cgs=[Cgs_mag  Cgs_deg]%center coordinate
Rgs=((1-gs).^0.5*(1-S11_mag.^2))/(1-(S11_mag).^2*(1-gs))%radius

%output gain circles
gl=Gl./Gl_max;
Cgl_mag=(gl*S22_mag)./(1-(S22_mag).^2*(1-gl));
Cgl_deg=-S22_deg;
Cgl=[Cgl_mag  Cgl_deg]%center coordinate
Rgl=((1-gl).^0.5*(1-S22_mag.^2))/(1-(S22_mag).^2*(1-gl))%radius

%Unilateral Figure of Merit
%If S12/=0, try the unilateral figure of merit
U=(S12_mag*S21_mag*S11_mag*S22_mag)./((1-(S11_mag).^2)*(1-(S22_mag).^2))

%lower boundary condition
Ul=1./(1+U).^2;
Ul_dB=10*log10(Ul)
%upper boundary condition
Uu=1./(1-U).^2;
Uu_dB=10*log10(Uu)
```

APPENDIX 2

NEC

ULTRA LOW NOISE PSEUDOMORPHIC HJ FET

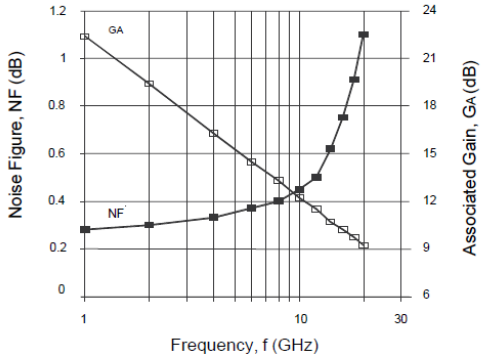
NE32684A

NOT RECOMMENDED FOR NEW DESIGN

FEATURES

- **VERY LOW NOISE FIGURE:**
  0.5 dB typical at 12 GHz
- **HIGH ASSOCIATED GAIN:**
  11.5 dB Typical at 12 GHz
- **L_G = 0.20 µm, W_G = 200 µm**
- **LOW COST METAL CERAMIC PACKAGE**
- **TAPE & REEL PACKAGING OPTION AVAILABLE**

NOISE FIGURE & ASSOCIATED GAIN vs. FREQUENCY
V_{DS} = 2 V, I_{DS} = 10 mA



DESCRIPTION

The NE32684A is a pseudomorphic Hetero-Junction FET that uses the junction between Si-doped AlGaAs and undoped InGaAs to create very high mobility electrons. The device features mushroom shaped TiAl gates for decreased gate resistance and improved power handling capabilities. The mushroom gate also results in lower noise figure and high associated gain. This device is housed in an epoxy-sealed, metal/ceramic package and is intended for high volume consumer and industrial applications.

NEC's stringent quality assurance and test procedures assure the highest reliability and performance.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

PART NUMBER PACKAGE OUTLINE			NE32684A 84AS		
SYMBOLS	**PARAMETERS AND CONDITIONS**	**UNITS**	**MIN**	**TYP**	**MAX**
NF^1	Optimum Noise Figure, V_{DS} = 2 V, I_{DS} = 10 mA, f = 12 GHz	dB		0.5	0.6
G_A^1	Associated Gain, V_{DS} = 2 V, I_{DS} = 10 mA, f = 12 GHz	dB	10.0	11.5	
P_{1dB}	Output Power at 1 dB Gain Compression Point, f = 12 GHz V_{DS} = 2 V, I_{DS} = 10 mA V_{DS} = 2 V, I_{DS} = 20 mA	 dBm dBm		 8.5 10.75	
G_{1dB}	Gain at P_{1dB}, f = 12 GHz, V_{DS} = 2 V, I_{DS} = 10 mA V_{DS} = 2 V, I_{DS} = 20 mA	dB dB		11.0 11.5	
I_{DSS}	Saturated Drain Current, V_{DS} = 2 V, V_{GS} = 0 V	mA	15	40	70
V_P	Pinch-off Voltage, V_{DS} = 2 V, I_{DS} = 100 µA	V	-2.0	-0.8	-0.2
g_m	Transconductance, V_{DS} = 2 V, I_D = 10 mA	mS	45	60	
I_{GSO}	Gate to Source Leakage Current, V_{GS} = -3 V	µA		0.5	10.0
$R_{TH(CH-A)}$	Thermal Resistance (Channel to Ambient)	°C/W		750	
$R_{TH(CH-C)}$	Thermal Resistance (Channel to Case)	°C/W			350

Note:
1. Typical values of noise figures and associated gain are those obtained when 50% of the devices from a large number of lots were individually measured in a circuit with the input individually tuned to obtain the minimum value. Maximum values are criteria established on the production line as a "go-no-go" screening tuned for the "generic" type but not for each specimen.

ABSOLUTE MAXIMUM RATINGS[1] (T_A = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{DS}	Drain to Source Voltage	V	4.0
V_{GS}	Gate to Source Voltage	V	-3.0
I_{DS}	Drain Current	mA	I_{DSS}
I_{GRF}	Gate Current	µA	200
T_{CH}	Channel Temperature	°C	150
T_{STG}	Storage Temperature	°C	-65 to +150
P_T	Total Power Dissipation	mW	165

Note:
1. Operation in excess of any one of these parameters may result in permanent damage.

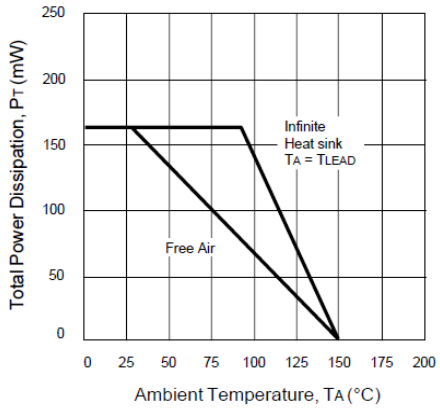
TYPICAL NOISE PARAMETERS (T_A = 25°C)

FREQ. (GHz)	NF_{OPT} (dB)	G_A (dB)	Γ_{OPT} MAG	Γ_{OPT} ANG	Rn/50
1	0.28	22.4	.90	17	0.45
2	0.30	19.4	.85	32	0.37
4	0.33	16.3	.72	64	0.27
6	0.37	14.5	.62	91	0.21
8	0.40	13.3	.54	116	0.15
10	0.45	12.2	.48	138	0.10
12	0.50	11.5	.42	164	0.07
14	0.62	10.7	.38	-169	0.07
16	0.75	10.2	.34	-139	0.08
18	0.91	9.7	.34	-101	0.09
20[1]	1.10	9.2	.38	-77	0.10

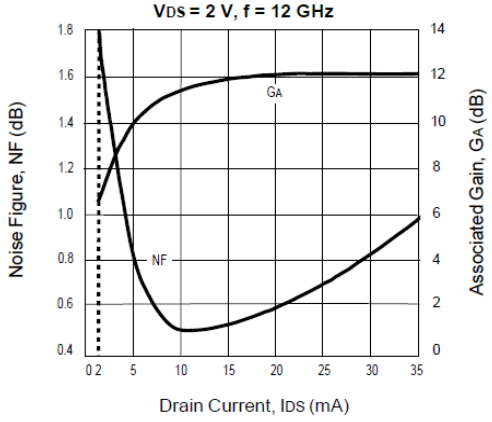
Note:
1. Data at 20 GHz is extrapolated, not measured.

TYPICAL PERFORMANCE CURVES (T_A = 25°C)

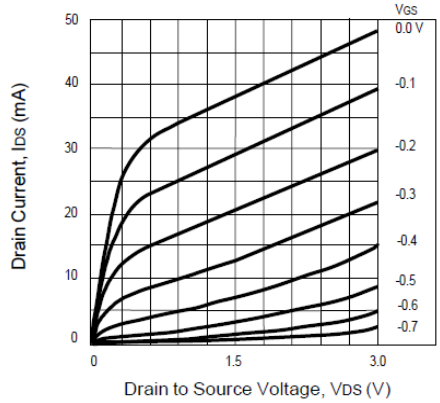
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



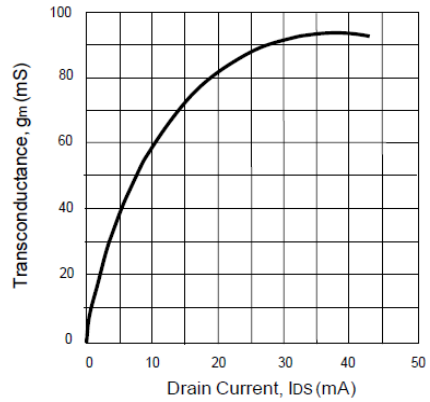
NOISE FIGURE AND ASSOCIATED GAIN vs. DRAIN CURRENT V_{DS} = 2 V, f = 12 GHz



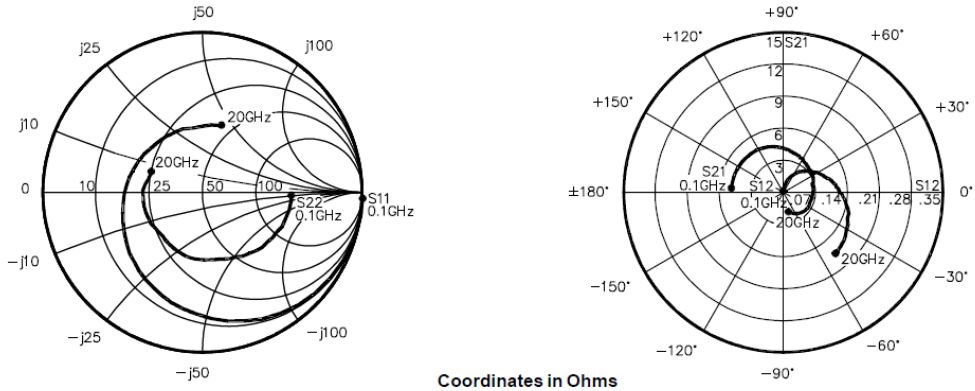
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



TRANSCONDUCTANCE vs. DRAIN CURRENT



TYPICAL COMMON SOURCE SCATTERING PARAMETERS (TA = 25°C)



Coordinates in Ohms
Frequency in GHz
(V_{DS} = 2 V, I_{DS} = 10 mA)

NE32684A
V_{DS} = 2 V, I_{DS} = 10 mA

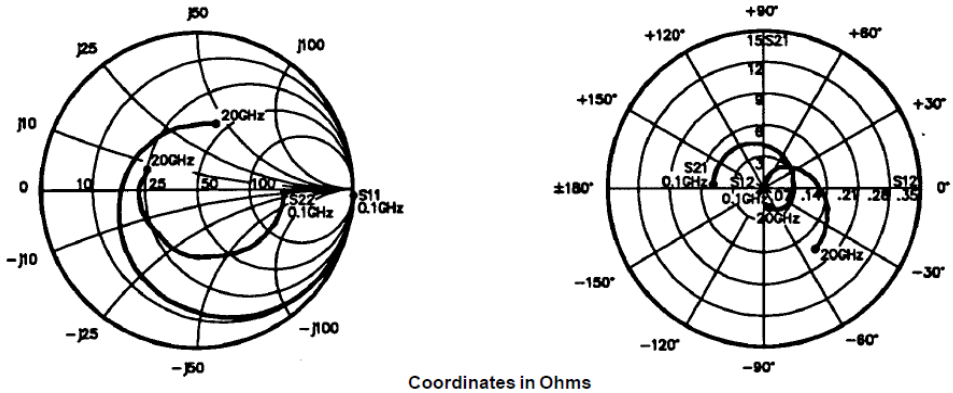
FREQUENCY	S11		S21		S12		S22		K	S21	MAG[1]
GHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG		(dB)	(dB)
0.1	0.999	-2.0	4.879	178.4	0.002	88.8	0.555	-1.9	0.06	13.8	33.9
0.2	0.999	-3.6	4.872	176.7	0.003	88.1	0.554	-2.8	0.04	13.7	32.1
0.5	0.999	-9.0	4.859	171.5	0.008	85.9	0.556	-6.0	0.01	13.7	27.8
1.0	0.991	-17.6	4.796	162.2	0.015	77.7	0.552	-12.0	0.13	13.6	25.0
2.0	0.960	-33.9	4.750	146.0	0.029	70.4	0.541	-23.1	0.24	13.5	22.1
3.0	0.922	-49.4	4.618	130.4	0.042	60.0	0.520	-33.0	0.36	13.3	20.4
4.0	0.873	-64.5	4.370	115.8	0.054	52.4	0.505	-42.8	0.45	12.8	19.1
5.0	0.816	-79.0	4.179	101.5	0.062	45.2	0.478	-52.5	0.57	12.4	18.3
6.0	0.758	-92.9	3.962	87.9	0.070	38.9	0.454	-62.2	0.68	12.0	17.5
7.0	0.712	-106.0	3.720	74.7	0.077	32.5	0.437	-71.8	0.76	11.4	16.8
8.0	0.667	-117.2	3.527	63.3	0.084	27.9	0.425	-79.7	0.83	10.9	16.2
9.0	0.629	-128.8	3.348	51.3	0.090	22.7	0.421	-88.7	0.88	10.5	15.7
10.0	0.592	-140.1	3.218	39.9	0.095	18.5	0.418	-96.8	0.92	10.1	15.3
11.0	0.549	-152.4	3.104	28.3	0.103	13.5	0.410	-105.2	0.96	9.8	14.8
12.0	0.513	-165.5	2.994	17.1	0.110	8.1	0.396	-114.2	0.99	9.5	14.3
13.0	0.487	-179.2	2.901	5.8	0.115	3.4	0.382	-123.2	1.02	9.2	13.1
14.0	0.464	168.1	2.825	-4.5	0.121	-1.2	0.368	-132.4	1.03	9.0	12.5
15.0	0.443	154.0	2.763	-16.3	0.130	-7.7	0.369	-143.0	1.01	8.8	12.6
16.0	0.423	139.4	2.707	-27.6	0.138	-13.9	0.373	-154.5	0.99	8.6	12.9
17.0	0.415	123.9	2.638	-40.1	0.144	-22.2	0.374	-166.2	0.98	8.4	12.6
18.0	0.414	107.4	2.614	-52.5	0.152	-30.1	0.371	-176.5	0.95	8.3	12.3
19.0	0.413	89.2	2.581	-65.4	0.161	-38.6	0.360	171.9	0.93	8.2	12.0
20.0	0.432	74.1	2.528	-78.0	0.167	-49.2	0.341	158.7	0.91	8.1	11.8

Note:
1. Gain Calculations:

$$MAG = \frac{|S_{21}|}{|S_{12}|}\left(K \pm \sqrt{K^2 - 1}\right)$$. When $K \le 1$, MAG is undefined and MSG values are used. $MSG = \frac{|S_{21}|}{|S_{12}|}$, $K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2\,|S_{12}S_{21}|}$, $\Delta = S_{11}S_{22} - S_{21}S_{12}$

MAG = Maximum Available Gain
MSG = Maximum Stable Gain

TYPICAL COMMON SOURCE SCATTERING PARAMETERS (TA = 25°C)



Coordinates in Ohms
Frequency in GHz
(V_{DS} = 2 V, I_D = 20 mA)

NE32684A
V_{DS} = 2 V, I_D = 20 mA

FREQUENCY	S11		S21		S12		S22		K	S21	MAG[1]
GHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG		(dB)	(dB)
0.1	0.999	-2.3	6.403	178.0	0.002	88.9	0.480	-2.0	0.06	16.1	35.0
0.2	0.999	-4.0	6.366	176.1	0.003	88.6	0.480	-2.9	0.04	16.1	33.3
0.5	0.998	-9.6	6.384	170.6	0.007	87.6	0.480	-5.9	0.03	16.1	29.6
1.0	0.986	-18.9	6.298	161.0	0.014	77.6	0.476	-11.5	0.17	16.0	26.5
2.0	0.948	-36.2	6.108	143.6	0.026	72.2	0.467	-22.0	0.30	15.7	23.7
3.0	0.894	-52.3	5.792	127.1	0.038	62.0	0.449	-31.2	0.46	15.3	21.8
4.0	0.833	-67.8	5.404	112.1	0.049	55.8	0.436	-40.4	0.56	14.6	20.4
5.0	0.766	-82.1	5.063	97.6	0.058	49.4	0.413	-49.2	0.68	14.1	19.4
6.0	0.703	-95.8	4.713	84.3	0.067	44.1	0.394	-58.3	0.77	13.5	18.5
7.0	0.653	-108.6	4.385	71.3	0.074	38.3	0.382	-67.4	0.85	12.8	17.7
8.0	0.607	-119.6	4.112	59.8	0.082	33.8	0.374	-74.9	0.90	12.3	17.0
9.0	0.569	-130.6	3.861	48.6	0.090	28.3	0.375	-83.3	0.93	11.7	16.3
10.0	0.529	-141.4	3.686	37.5	0.097	23.4	0.378	-90.8	0.96	11.3	15.8
11.0	0.487	-153.2	3.517	26.0	0.107	18.4	0.374	-99.4	0.98	10.9	15.2
12.0	0.554	-166.0	3.376	14.8	0.114	11.8	0.365	-108.0	1.00	10.7	14.4
13.0	0.428	-179.3	3.262	4.1	0.121	6.3	0.354	-116.8	1.01	10.3	13.6
14.0	0.407	167.8	3.165	-5.9	0.130	0.6	0.341	-125.5	1.01	10.0	13.3
15.0	0.387	154.5	3.081	-17.3	0.138	-5.4	0.345	-136.6	0.99	9.8	13.5
16.0	0.368	139.9	3.007	-27.9	0.146	-13.5	0.352	-148.4	0.97	9.6	13.1
17.0	0.359	124.4	2.934	-40.2	0.154	-21.6	0.353	-160.0	0.96	9.3	12.8
18.0	0.358	107.6	2.910	-52.3	0.160	-30.1	0.349	-170.6	0.94	9.3	12.6
19.0	0.361	89.4	2.865	-65.4	0.169	-39.1	0.337	177.9	0.92	9.1	12.3
20.0	0.379	73.7	2.812	-77.8	0.174	-49.0	0.319	165.2	0.91	9.0	12.1

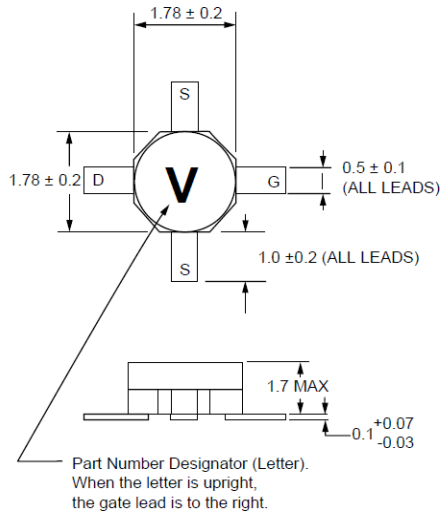
Note:
1. Gain Calculation:

$$MAG = \frac{|S21|}{|S12|}\left(K \pm \sqrt{K^2 - 1}\right)$$. When $K \le 1$, MAG is undefined and MSG values are used. $$MSG = \frac{|S21|}{|S12|}$$, $$K = \frac{1 + |\Delta|^2 - |S11|^2 - |S22|^2}{2\,|S12\,S21|}$$, $\Delta = S11\,S22 - S21\,S12$

MAG = Maximum Available Gain
MSG = Maximum Stable Gain

OUTLINE DIMENSIONS (Units in mm)

PACKAGE OUTLINE 84AS



ORDERING INFORMATION

PART NUMBER	AVAILABILITY	PACKAGE OUTLINE
NE32684AS	Bulk up to 1K	84AS
NE32684A-T1	1K/Reel	84AS

Note:
Long leaded (1.7 mm min.) 84A package available upon request in bulk quantitites up to 1000 pcs. To order specify NE32684A-SL.